CUSTOMER APPROVAL SHEET

Company Name	
MODEL	**A070VW04 V4**
CUSTOMER APPROVED	Title : Name :

☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver. 0.0)**

☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver. 0.0)**

☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMP1LE (Spec. Ver. 0.0)**

☐ **CUSTOMER REMARK :**

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P/N : 97.07A13.432

Comment :

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Product Specification

7.0" COLOR TFT-LCD MODULE

Model Name： A070VW04 V4

Planned Lifetime:	From 2009/Jul. To 2010/Jul.
Phase-out Control:	From 2010/Jan. To 2010/Jul.
EOL Schedule:	2010/Jul.

< ◆ >Preliminary Specification

< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0	2009/06/03		Draft.

Contents

A. General Description

A070VW04 is a amorphous transmissive type TFT (Thin Film Transistor) LCD (Liquid Crystal Display). This model is composed of TFT-LCD, drive IC, FPC (flexible printed circuit), and backlight unit.The timing controller is embedded, so it is easily to design for consumer product.

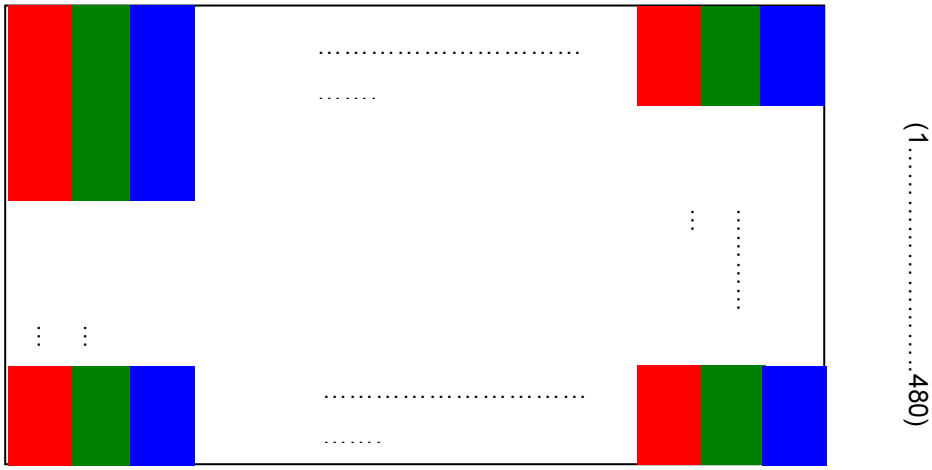
B. Features

- 7-inch display size
- WVGA resolution and stripe dot arrangement
- Built in timing controller
- LED backlight
- Standby mode supported
- Up/Down, Left/Right reversion selection
- SYNC + DE Mode
- Parallel 18/24bits interface support
- 16.7M color supported
- Wide viewing angle
- RoHS compliant green design

C. General Information

NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	800RGB(H)×480(V)	
2	Active Area	mm	152.40(H)×91.44(V)	
3	Screen Size	inch	7.0(Diagonal)	
4	Pixel Pitch	mm	0.1905(H)×0.1905(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	16.7M Colors	Note 2
7	Overall Dimension	mm	164(H) × 103(V) × 5.1(T)	Note 3
8	Weight	g	153.5 +/- 10%	
9	Panel surface treatment	--	Anti-Glare	
10	Display Mode	--	Normally White	

Note 1: Below figure shows dot stripe arrangement.



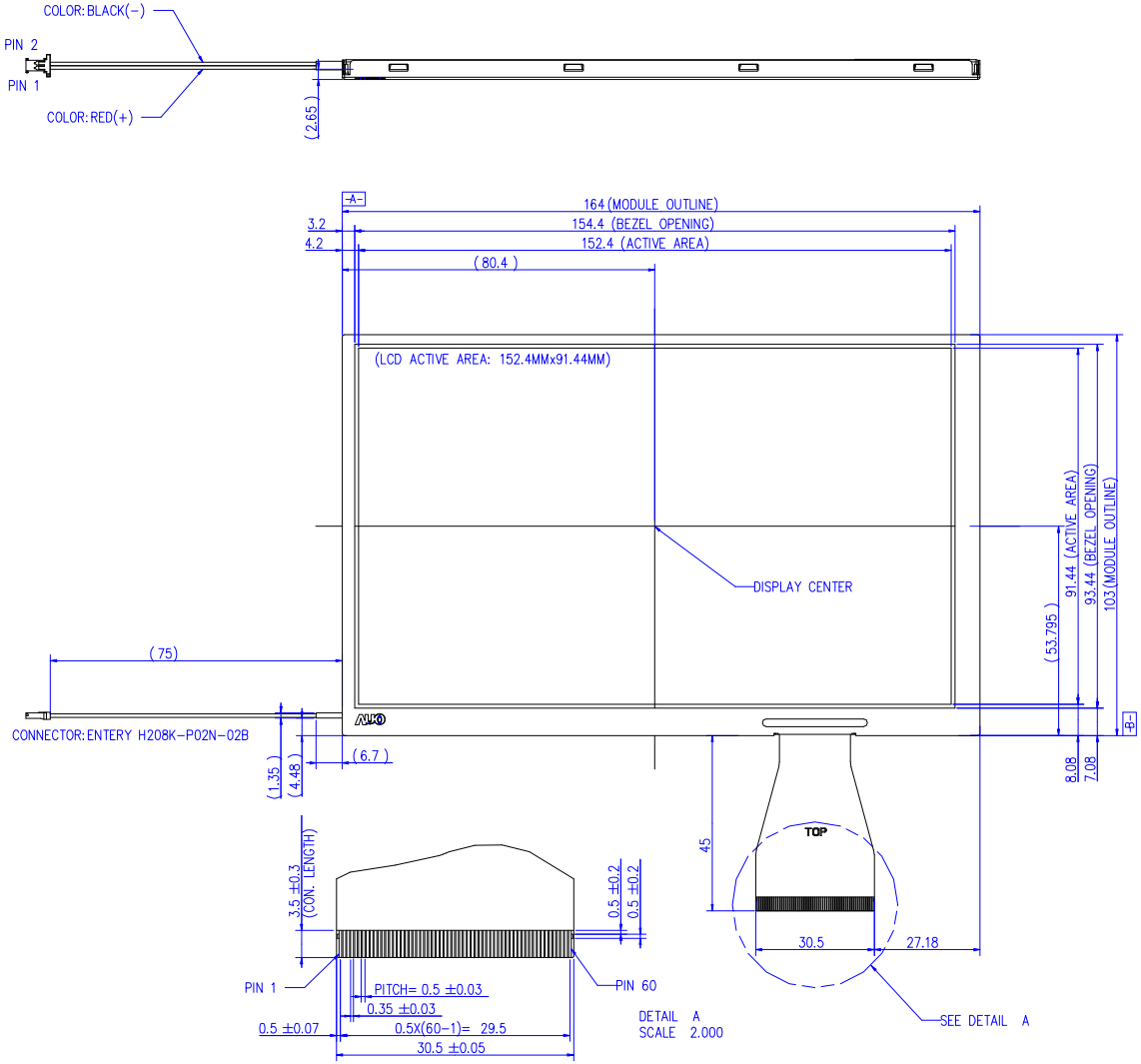
(1 2 3……2398 2399 2400)

Note 2: The full color display depends on 24-bit data signal (pin 4~27).

Note 3: Not include blacklight cable and FPC. Refer next page to get further information.

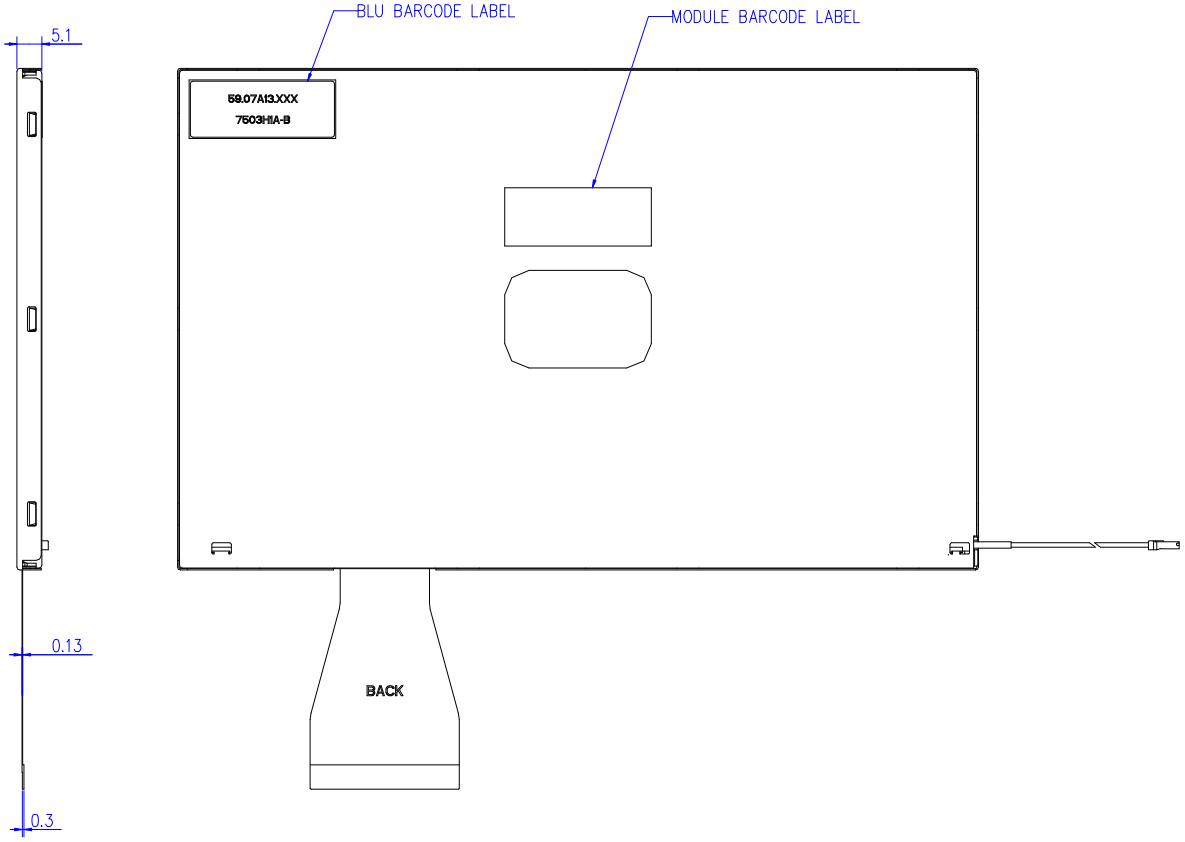
D. Outline Dimension

1. TFT-LCD Module – Front View



2. TFT-LCD Module – Rear View

NOTES:
1. GENERAL TOLERANCE IS ±0.3.
2. THE BENDING RADIUS OF FPC SHOULD BE LARGER THAN 0.6.
3. UNIT: MM



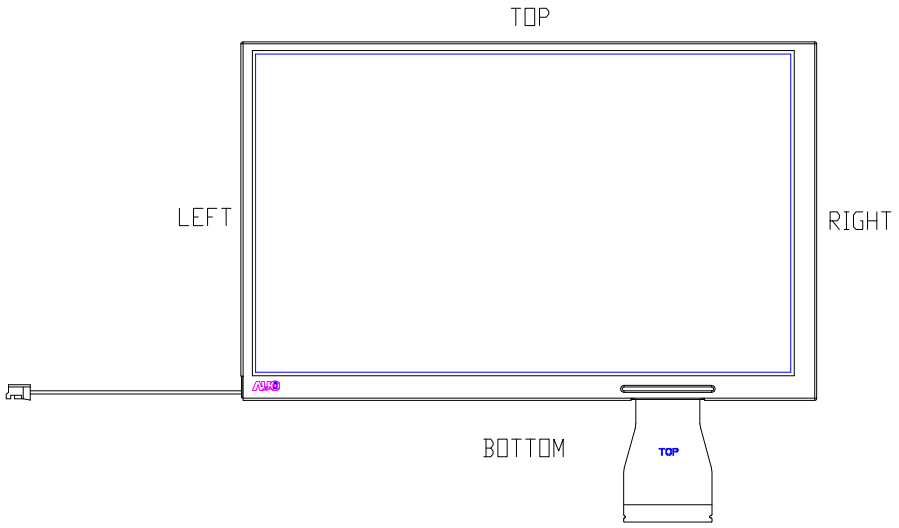
E. Electrical Specifications

1. FPC Pin Assignment (HRS FH28-60S-0.5SH)

Pin no	Symbol	I/O	Description
1	AGND2	P	Analog Ground
2	AVDD2	P	Analog Power
3	VDD	P	Digital Power
4	R0	I	Data input (LSB)
5	R1	I	Data input
6	R2	I	Data input
7	R3	I	Data input
8	R4	I	Data input
9	R5	I	Data input
10	R6	I	Data input
11	R7	I	Data input (MSB)
12	G0	I	Data input (LSB)
13	G1	I	Data input
14	G2	I	Data input
15	G3	I	Data input
16	G4	I	Data input
17	G5	I	Data input
18	G6	I	Data input
19	G7	I	Data input (MSB)
20	B0	I	Data input (LSB)
21	B1	I	Data input
22	B2	I	Data input
23	B3	I	Data input
24	B4	I	Data input
25	B5	I	Data input
26	B6	I	Data input
27	B7	I	Data input (MSB)
28	DCLK	I	Clock input
29	DE	I	Data enable signal
30	HSYNC	I	Horizontal sync input. Negative polarity
31	VSYNC	I	Vertical sync input. Negative polarity
32	SCL	I	Serial communication clock input
33	SDA	I	Serial communication data input
34	CSB	I	Serial communication chip select

35	NC	--	Not connect (Please leave it open)
36	VDD	P	Digital Power
37	NC	--	Not connect (Please leave it open)
38	GND	P	Digital ground
39	AGND1	P	Analog ground
40	AVDD1	P	Analog Power
41	VCOMin	I	For external VCOM DC input (Optional)
42	NC	-	Not connect
43	NC	-	Not connect
44	VCOM	O	connect a capacitor
45	V10	P	Gamma correction voltage reference
46	V9	P	Gamma correction voltage reference
47	V8	P	Gamma correction voltage reference
48	V7	P	Gamma correction voltage reference
49	V6	P	Gamma correction voltage reference
50	V5	P	Gamma correction voltage reference
51	V4	P	Gamma correction voltage reference
52	V3	P	Gamma correction voltage reference
53	V2	P	Gamma correction voltage reference
54	V1	P	Gamma correction voltage reference
55	NC	-	Not connect
56	VGH	P	Positive power for TFT
57	GVCC	P	Digital Power
58	VGL	P	Negative power for TFT
59	GGND	P	Digital Ground
60	CAP	C	Connected to a capacitor

I: Input pin; P: Power pin; G: Ground pin; C: capacitor pin



2 . Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	VDD	GND=0	-0.5	5	V	Note 1
	AVDD 1 AVDD 2	AGND1=0 AGND2=0	-0.5	15	V	Note 1
	VGH	GGND = 0	-0.3	40	V	Note 1
	VGL		-20	0.3	V	Note 1
	VGH-VGL		--	40	V	Note 1
Input Signal Voltage	V_I		-0.3	VDD+0.3	V	Note 1
Operating temperature	Topa	--	0	60	□	Ambient Temperature
Storage temperature	Tstg	--	-10	70	□	Ambient Temperature

Note 1: Functional operation should be restricted under normal ambient temperature.

F. Electrical Characteristics

The following items are measured under stable condition and suggested application circuit.

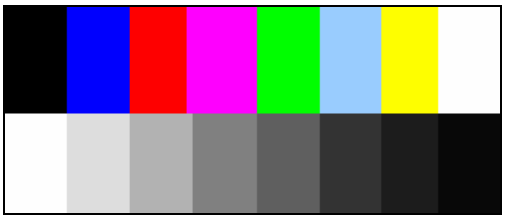
1. TFT- LCD Typical Operation Condition (AGND1 = AGND2 = GND = GGND = 0V)

ITEM		Symbol	MIN.	TYP.	MAX.	UNIT	Remark
Power supply		VDD	3.1	3.3	3.6	V	Note3
		I_{VDD}	--	15	20	mA	Pin3 + Pin36
		AVDD 1 AVDD 2	10.5	11	11.5	V	Note3
		I_{AVDD}	--	10	20	mA	Pin2 + Pin40
		GVCC	3.1	3.3	3.6	V	Note3
		I_{GVCC}	--	0.08	0.15	mA	Pin57
		VGH	17.5	18	18.5	V	Note3
		I_{VGH}	--	0.35	0.5	mA	Pin56
		VGL	-7.5	-7	-6.5	V	Note3
		I_{VGL}	--	0.35	0.5	mA	Pin58
Input Signal	H Level	V_{IH}	0.7VDD	-	VDD	V	
	L Level	V_{IL}	GND	-	0.3VDD	V	
Input Reference Voltage		V1 ~ V5	AVDD/2	-	AVDD – 1	V	
		V6 ~ V10	1	-	AVDD/2	V	
VCOMin		V_{CDC}	3.3	3.6	3.9	V	Note 1

Note1: Above every operation range is based on stable operation from suggested application circuit.

Note2: Based on recommended Gamma 2.2 voltage.

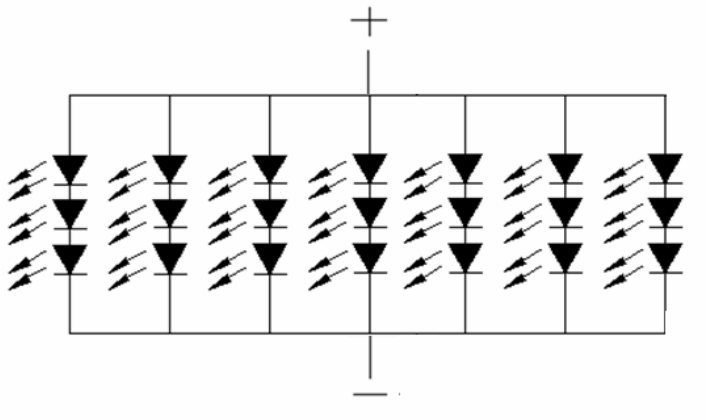
Note3: Typical current test pattern



2. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED lightbar Current	I_L	--	175	--	mA	--
BL Power Consumption	P_{BL}	1.548	1.758	1.968	W	--
LED Life Time	L_L	10,000	--	--	Hr	Note 2, 3

Note 1: The LED driving condition is defined for LED module (21 LED). The voltage range will be 8.85 to 11.25 V based on suggested driving current set as 175mA



Note 2: Define "LED Lifetime": brightness is decreased to 50% of the initial value. LED Lifetime is restricted under normal condition, ambient temperature = 25℃ and LED lightbar current = 175mA.

Note 3: If it uses larger LED lightbar voltage more than 175mA, it maybe decreases the LED lifetime.

3. AC Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	Remark
Clock High time	T_{WCL}	8	-	-	ns	
Clock Low time	T_{WCH}	8	-	-	ns	
Clock rising time	T_{RCLK}	-	-	1	ns	
Clock falling time	T_{ACK}	-	-	1	ns	
Hsync setup time	T_{HSU}	5			ns	
Hsync hold time	T_{HHD}	10			ns	
Vsync setup time	T_{VSU}	0			ns	
Vsync hold time	T_{VHD}	2			ns	
Data setup time	T_{DSU}	5			ns	
Data hold time	T_{DHD}	10			ns	
Data enable set-up time	T_{ESU}	4			ns	
Data enable hold time	T_{EHD}	2			ns	

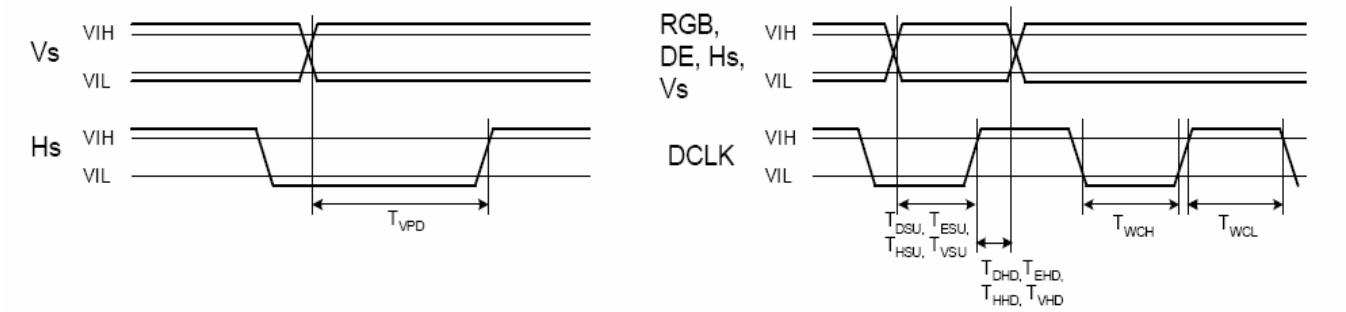


Figure 1 : Input timing details

4. RGB Parallel Input Timing

a. Horizontal Timing

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX	UNIT
DCLK frequency	F_{DCLK}		25	33	40	MHz
DCLK period	T_{DCLK}		25	30.3	40	ns
Hsync Period (= T_{HD} + T_{HBL})	T_H		986	1056	1183	DCLK
Active Area	T_{HD}		-	800	-	DCLK
Horizontal blanking (= T_{HF} + T_{HE})	T_{HBL}		186	256	383	DCLK
Hsync front porch	T_{HF}			40	-	DCLK
Delay from Hsync to 1st data input (= T_{HW} + T_{HB})	T_{HE}	Function of HDL[7..0] settings	146	216	343	DCLK
Hsync pulse width	T_{HW}		1	128	136	DCLK
Hsync back porch	T_{HB}		10	88	342	DCLK

b. Vertical Timing

PARAMETER	SYMBO	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vsync period (= T_{VD} + T_{VBL})	T_V		497	505	512	Th
Active lines	T_{VD}			480		Th
Vertical blanking (= T_{VF} + T_{VE})	T_{VBL}		17	25	32	Th
Vsync front porch	T_{VF}			1	-	Th
GD start pulse delay	T_{VE}	Function of VDL[3..0] settings	16	24	31	Th
Vsync pulse width	T_{VW}		1	3	16	Th
Hsync/ Vsync phase shift	T_{VPD}		2	320	-	DCLK

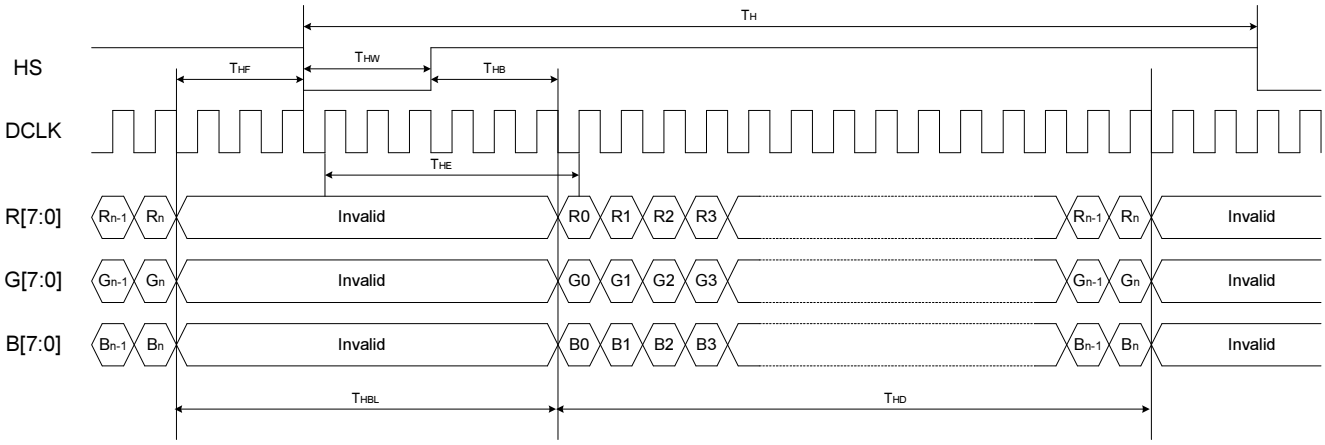


Figure 2 Horizontal input timing. (HV mode)

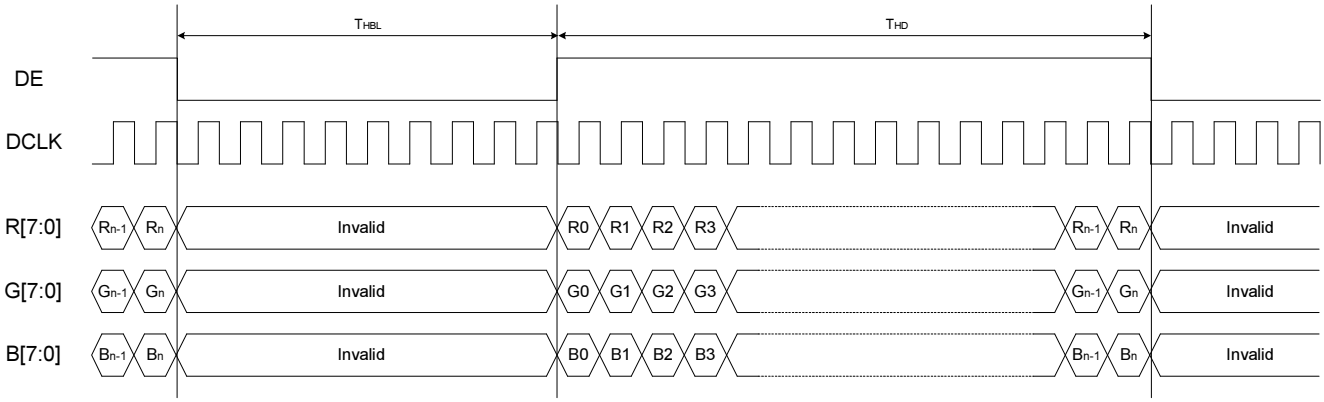


Figure 3: Horizontal input timing. (DE mode)

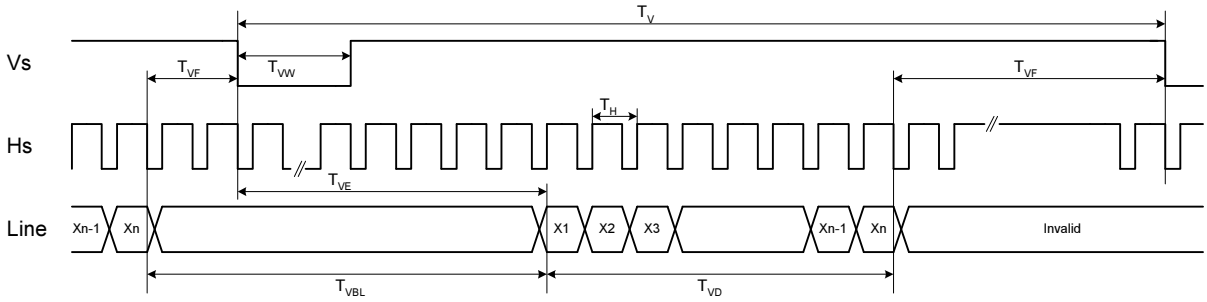


Figure 4: Vertical timing. (HV mode)

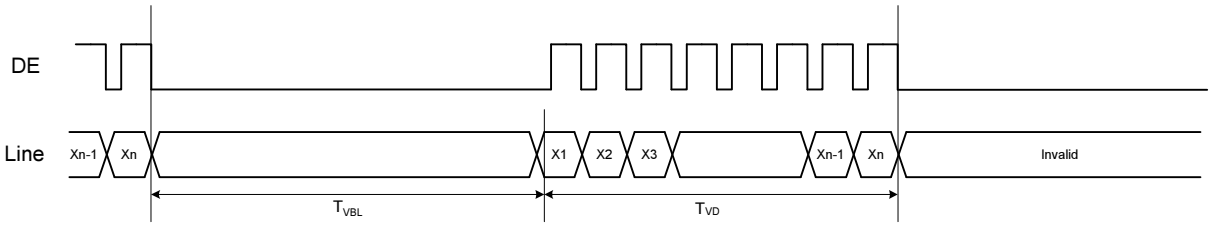


Figure 5: Vertical timing. (DE mode)

5. Serial Control Interface AC Characteristic

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial clock	T_{SCK}		320			ns
SCL pulse duty	T_{SCW}		40	50	60	%
Serial data setup time	T_{IST}		120			ns
Serial data hold time	T_{IHD}		120			ns
Serial clock high/low	T_{SSW}		120			ns
CSB setup time	T_{CST}		120			ns
CSB hold time	T_{CHD}		120			ns
Chip select distinguish	T_{CD}		1			us
Delay from CSB to VSYNC	T_{CV}		1			us

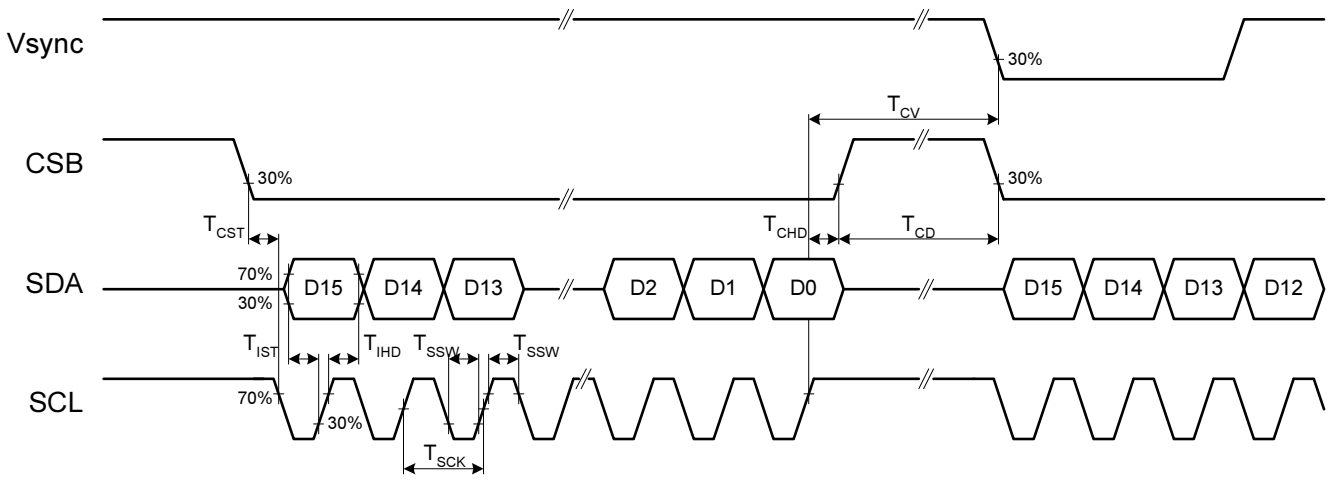


Figure 6 : AC serial interface write mode timing

6. Register Information

There is a total of 6 registers each containing several parameters. For a detailed description of the parameters refer to register table.The serial register has read/write function. D[15:12] are the register address, D[11] defines the read or write mode and D[10:0] are the data.

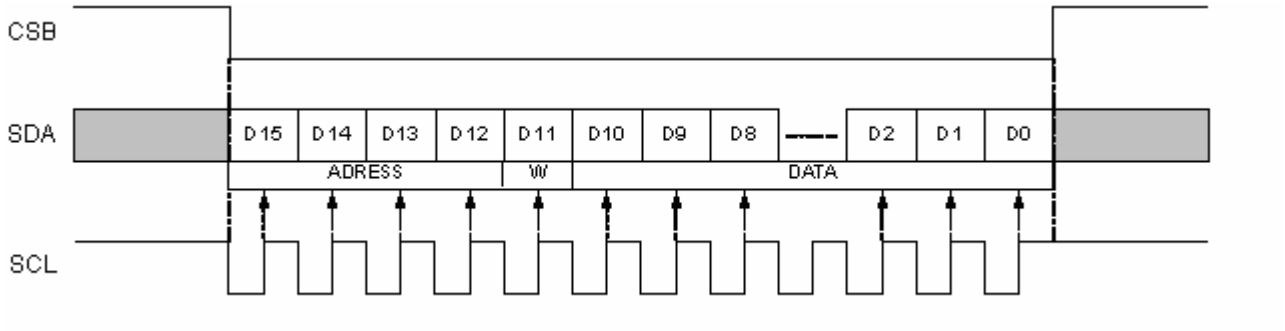


Figure 7: Serial interface write sequence

1. At power-on, the default values specified for each parameter are taken.
2. If less than 16-bit data are read during the CS low time period, the data is cancelled.
   a. The write operation is cancelled.
3. All items are set at the falling edge of the vertical sync, except R0[1:0].
4. When GRB is activated through the serial interface, all registers are cleared, except the GRB value.
5. The register setting values are valid when VDD already goes to high and after VSYNC starts.
6. It is suggested that VSYNC, HSYNC, DCLK always exists in the same time. But if HSYNC, DCLK stops, only VSYNC operating, the register setting is still valid.
7. If the chip goes to standby mode, the register value will still keep. MCU can wake up the chip only by changing standby mode value from low to high.
8. The register setting values are rewritten by the influence of static electricity, a noise, etc. to unsuitable value, incorrect operating may occur. It is suggested that the SPI interface will setup as frequently as possible.

7. Register Table (Default Value)

Reg No.	ADDRESS				W	DATA										
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	(01)		(01)		(1)	U/D (0)	SHL (1)	(0)	(0)	GRB (1)	STB (1)
R2	0	0	1	0	0	X	X	X	HDL(80h)							
R3	0	0	1	1	0	X	X	(0)	(0)	(0)	(0)	(0)	VDL(1000)			
R4	0	1	0	0	0	X	X	(1)	(0)	(00)		(1)	(1111)			
R6	0	1	1	0	0	X	0	EnGB12 (1)	EnGB11 (1)	EnGB10 (1)	(0)	(0)	EnGB5 (1)	EnGB4 (1)	EnGB3 (1)	(0)

X : Reserved, please set to “0”.

8. Register Description

R0 settings

Address	Bit	Description		Default
0000	[10..0]	Bits 10-9	AUO Internal Use	01
		Bits 8-7	AUO Internal Use	01
		Bit6	AUO Internal Use	1
		Bit5 (U/D)	Vertical shift direction selection.	0
		Bit4 (SHL)	Horizontal shift direction selection.	1
		Bit3	AUO Internal Use	1
		Bit2	AUO Internal Use	0
		Bit1 (GRB)	Global reset.	1
		Bit0 (STB)	Standby mode setting.	1

Bit5	U/D function
0	Scan down; First line=Gn→ Gn-1 →…→ G2 → Last line=G1. **(default)**
1	Scan up; First line=G1 → G2 → … → Gn-1 → Last line=Gn.

Bit4	SHL function
0	Shift left; First data=Y600 → Y601 → …→ Y2 → Last data=Y1.
1	Shift right: First data=Y1→ Y2 → …→ Y600 → Last data=Y600. **(default)**

Bit1	GRB function
0	The controller is reset. Reset all registers to default value.
1	Normal operation. **(default)**

Bit0	STB function
0	T-CON, source driver and DC-DC converters are off, and all outputs are High-Z.
1	Normal operation. (**default)**

R2 settings

Address	Bit	Description		Default
0010	[7..0]	Bit7-0 (HDL)	Horizontal start pulse adjustment function	80h

Bit7-0	HDL function.
00h	$T_{HE} = T_{HEtyp} – 128$ CLK period.
80h	$T_{HE} = T_{HEtyp}$. **(default)**
FFh	$T_{HE} = T_{HEtyp} + 127$ CLK period.

R3 settings

Address	Bit	Description		Default
0011	[8..0]	Bit8	AUO Internal Use	0
		Bit7	AUO Internal Use	0
		Bit6	AUO Internal Use	0
		Bit5	AUO Internal Use	0
		Bit4	AUO Internal Use	0
		Bit3-0 (VDL)	Vertical start pulse adjustment function	1000

Bit3-0	VDL function.
0000	$T_{VE} = T_{VEtyp} – 8$ Hs period.
0001	$T_{VE} = T_{VEtyp} – 7$ Hs period.
0010	$T_{VE} = T_{VEtyp} – 6$ Hs period.
0011	$T_{VE} = T_{VEtyp} – 5$ Hs period.
0100	$T_{VE} = T_{VEtyp} – 4$ Hs period.
0101	$T_{VE} = T_{VEtyp} – 3$ Hs period.
0110	$T_{VE} = T_{VEtyp} – 2$ Hs period.
0111	$T_{VE} = T_{VEtyp} – 1$ Hs period.
1000	$T_{VE} = T_{VEtyp}$. **(default)**
1001	$T_{VE} = T_{VEtyp} + 1$ Hs period.
1010	$T_{VE} = T_{VEtyp} + 2$ Hs period.
1011	$T_{VE} = T_{VEtyp} + 3$ Hs period.
1100	$T_{VE} = T_{VEtyp} + 4$ Hs period.
1101	$T_{VE} = T_{VEtyp} + 5$ Hs period.
1110	$T_{VE} = T_{VEtyp} + 6$ Hs period.

1111	$T_{VE} = T_{VEtyp} + 7$ Hs period.

R6 settings

Address	Bit	Description		Default
0110	[9..0]	Bit9	AUO Internal Use	0
		Bit8(EnGB12)	Gamma buffer Enable for V9	1
		Bit7(EnGB11)	Gamma buffer Enable for V8	1
		Bit6(EnGB10)	Gamma buffer Enable for V7	1
		Bit5	AUO Internal Use	0
		Bit4	AUO Internal Use	0
		Bit3(EnGB5)	Gamma buffer Enable for V4	1
		Bit2(EnGB4)	Gamma buffer Enable for V3	1
		Bit1(EnGB3)	Gamma buffer Enable for V2	1
		Bit0	AUO Internal Use	0

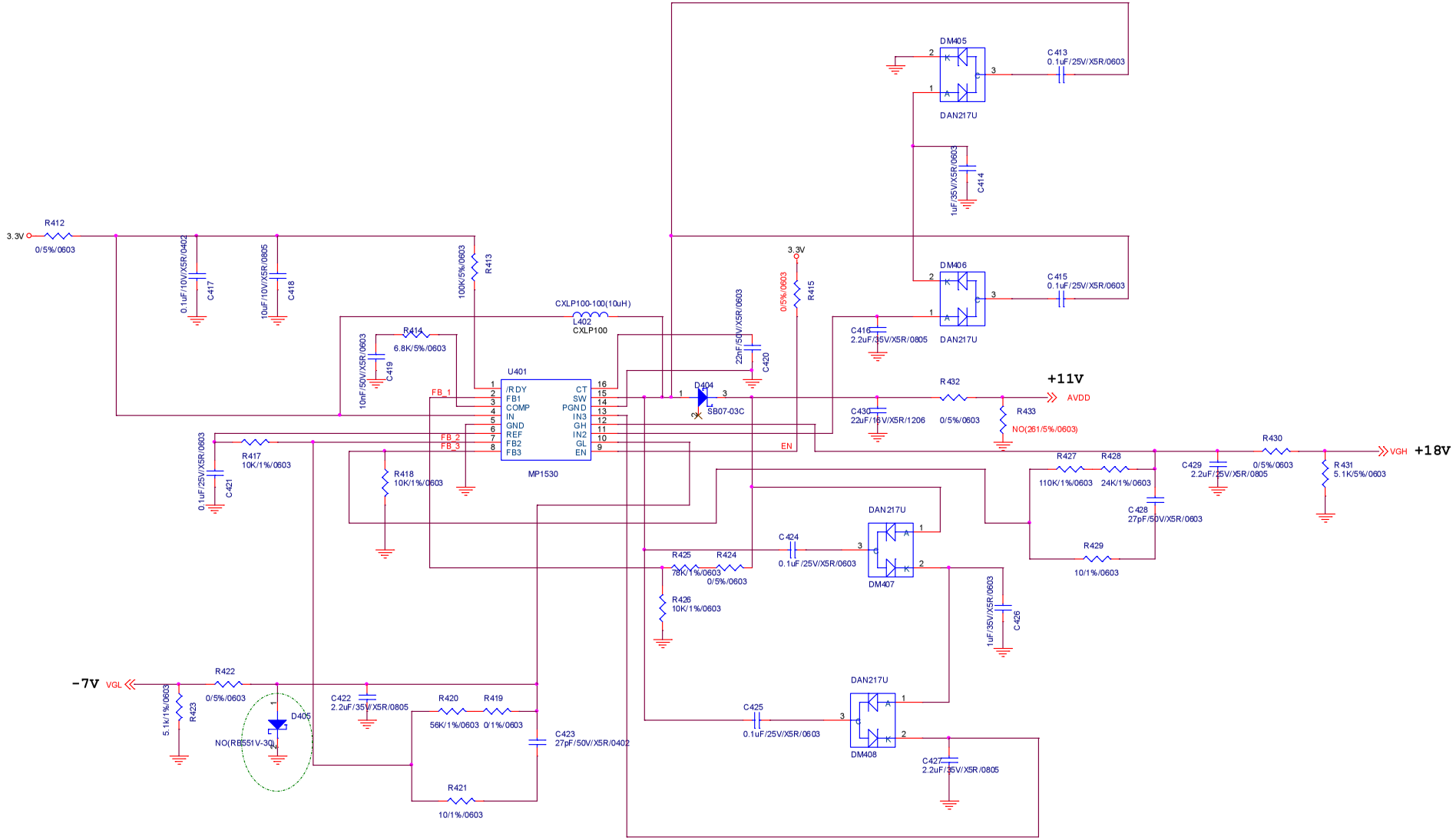
Bitx	EnGBx function
0	Gamma buffer for VX is disable (High Z).
1	Gamma buffer is enable. VX must be connected externally.

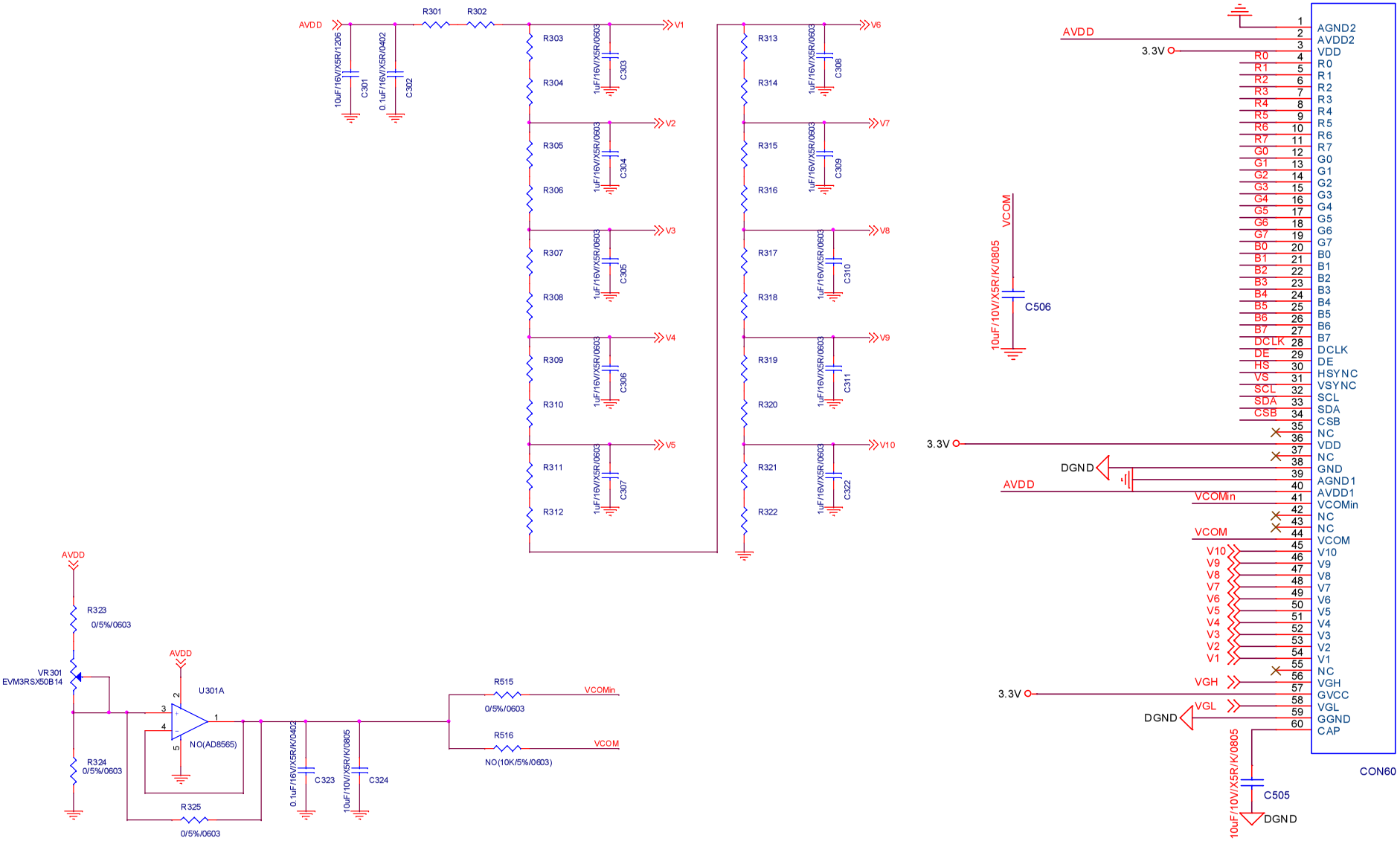
9. Recommended Power On Register Setting

Reg	ADDRESS				R/W	DATA										
No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	01		01		1	0	1	0	0	1	1
R2	0	0	1	0	0	0	0	0	80h							
R3	0	0	1	1	0	0	0	0	0	0	0	0	1000			
R4	0	1	0	0	0	0	0	1	1	00		1	1111			
R6	0	1	1	0	0	0	0	1	1	1	0	0	1	1	1	0

10. Application Circuit Example

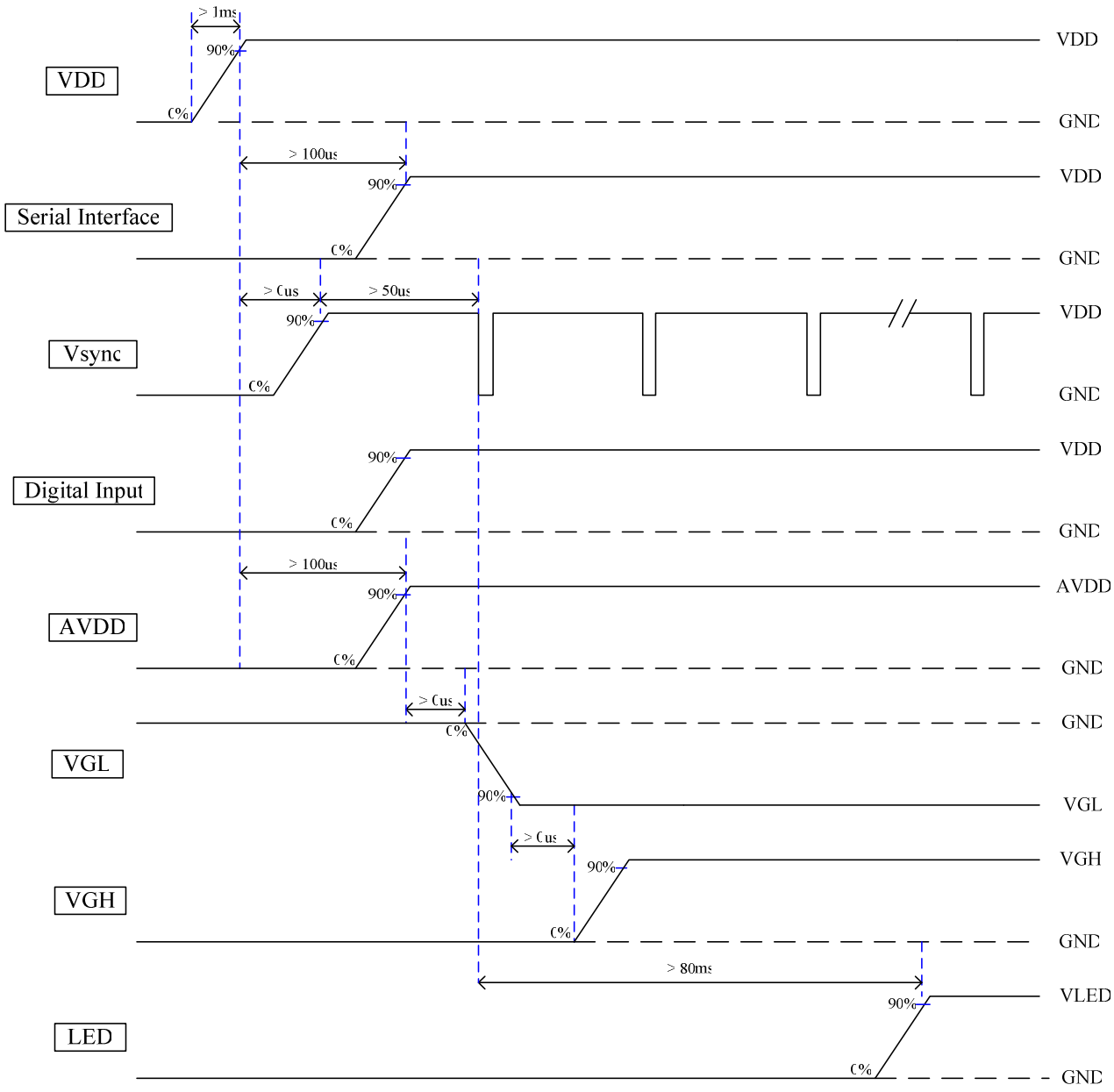
(Note: for reference only, not limited to this circuit)



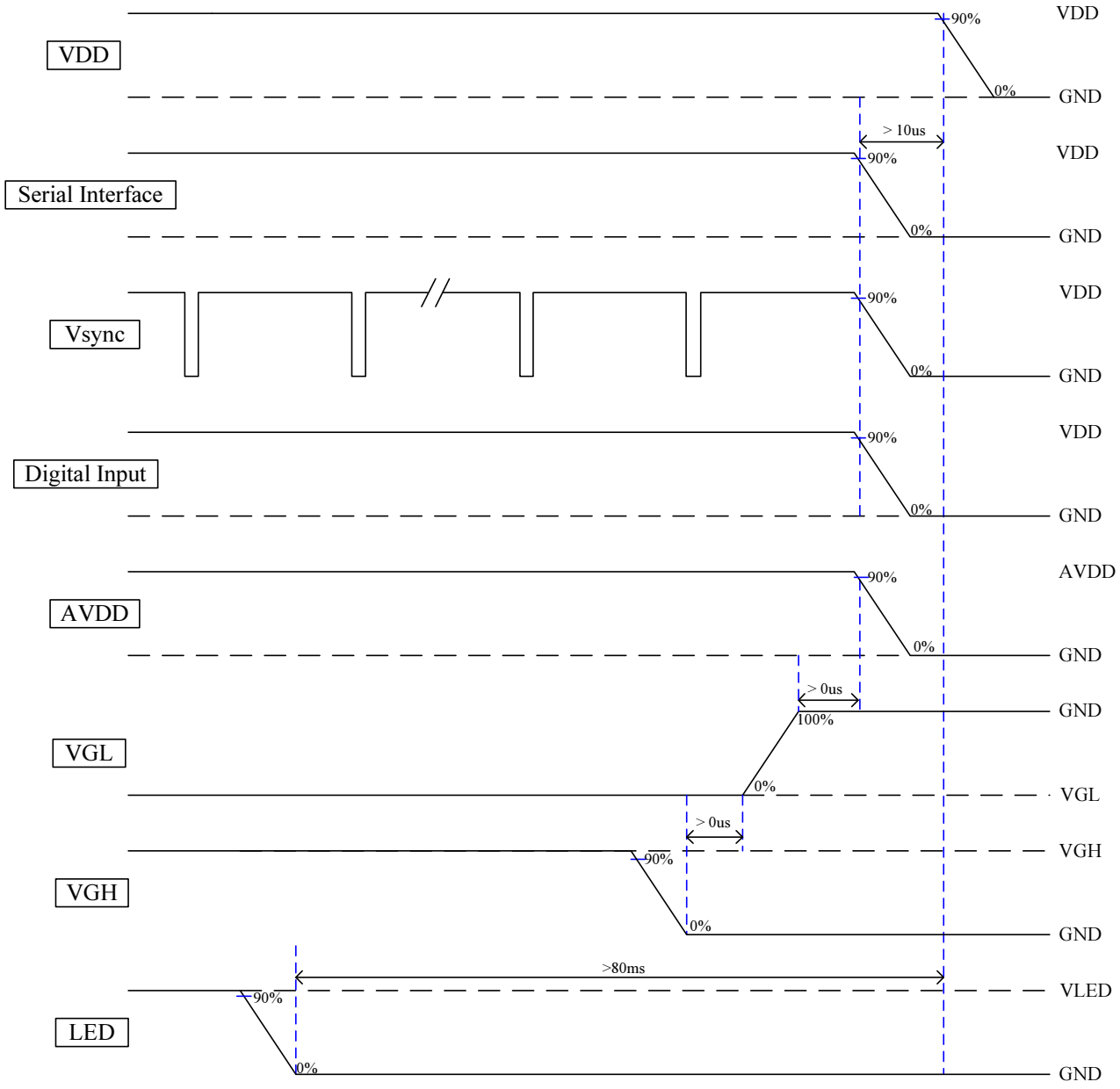


11. Recommended Power On/Off Sequence

Power On Sequence



Power Off Sequence

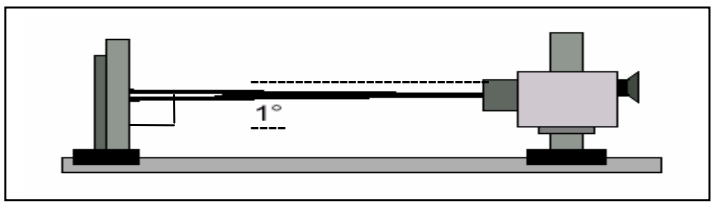


G. Optical specification (Note 1, 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise Fall		 Tr Tf	θ=0°	 -- --	 12 18	 20 30	 ms ms	Note 3
Contrast ratio		CR	At optimized viewing angle	200	300	--		Note 4
Viewing Angle	Top		CR≧10	30	50		deg.	Note 5
	Bottom			50	65			
	Left			50	65			
	Right			50	65			
Brightness		Y_L	θ=0°	230	250	--	cd/m²	Note 6
Chromaticity	White	X	θ=0°	0.26	0.31	0.36		
		Y	θ=0°	0.28	0.33	0.38		
	Red	X	θ=0°	0.53	0.58	0.63		
		Y	θ=0°	0.30	0.35	0.40		
	Green	X	θ=0°	0.27	0.32	0.37		
		Y	θ=0°	0.54	0.59	0.64		
	Blue	X	θ=0°	0.10	0.15	0.20		
		Y	θ=0°	0.02	0.07	0.12		
Uniformity		ΔY_L	%	70	75	--	%	Note 7

Note 1:Ambient temperature =25℃, and LED lightbar current I_L = 175mA. To be measured in the dark room.

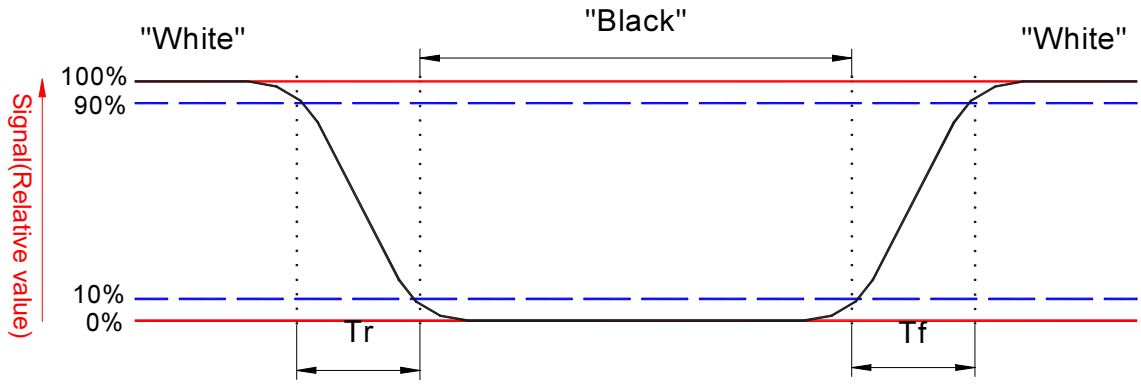
Note 2:To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-7, after 15 minutes operation.



Note 3. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

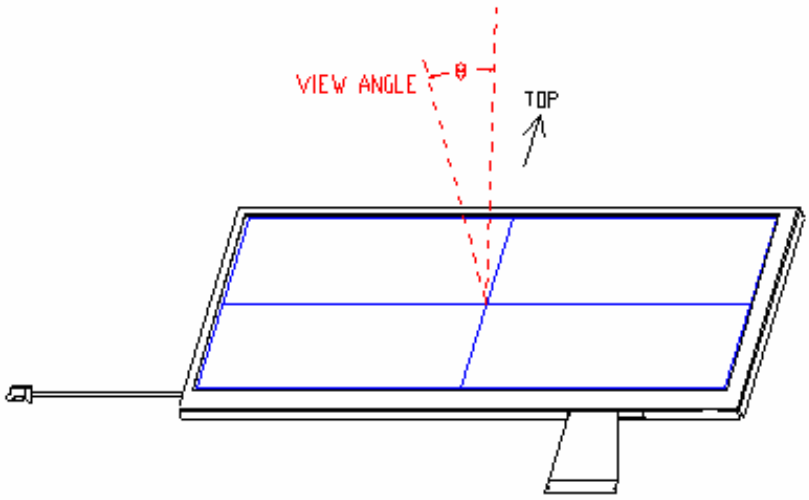


Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

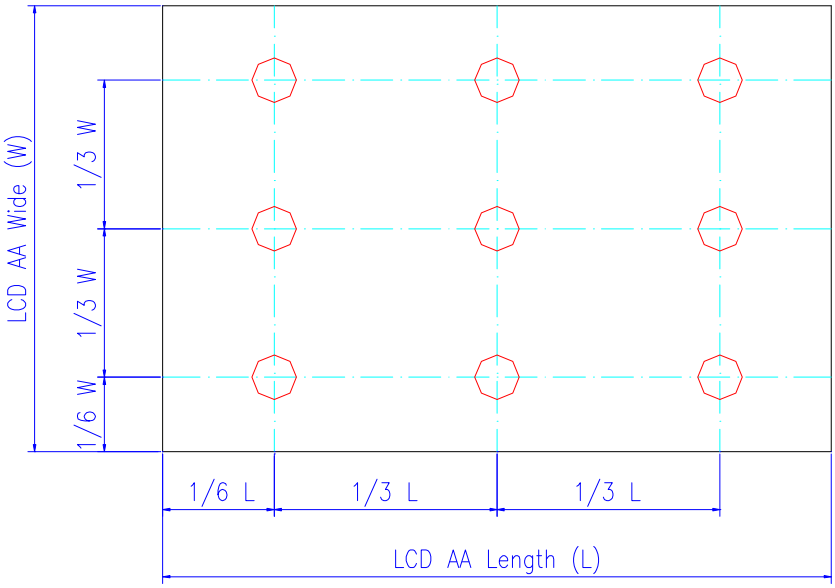
$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 5. Definition of viewing angle, θ, Refer to figure as below.



Note 6. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 7: Luminance Uniformity of these 9 points is defined as below:

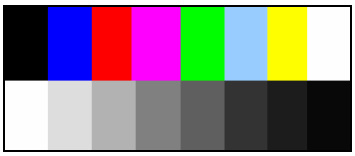
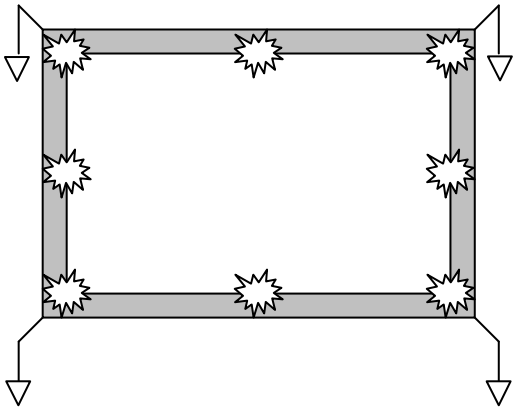


H. Reliability test items(Note 2)

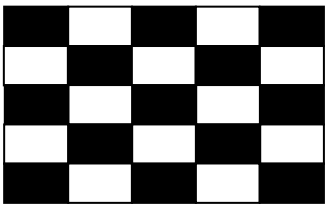
No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 70□ 240Hrs	
2	Low Temperature Storage	Ta= -10□ 240Hrs	
3	High Ttemperature Operation	Ta= 60□ 240Hrs	
4	Low Temperature Operation	Ta= 0□ 240Hrs	
5	High Temperature & High Humidity	Ta= 50□. 80% RH 240Hrs	Operation
6	Heat Shock	-10□~60□, 50 cycle, 2Hrs/cycle	Non-operation
7	Electrostatic Discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Image Sticking	25□, 20hrs	Note 5
9	Vibration	Frequency range : 10Hz~55Hz Stoke : 1.5mm Sweep : 10Hz~55Hz~10Hz 2 hours for each direction of X,Y,Z Total 6 hours	Non-operation JIS C7021, A-10 condition A : 15 minutes
10	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
11	Vibration (With Carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
12	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	
13	Pressure	5kg, 5sec	Note 6

Note1: Ta: Ambient Temperature.

Note2: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

Test Condition		Note
Pattern		
Procedure And Set-up	Contact Discharge：330Ω, 150pF, 1sec, 8 point, 25times/point Air Discharge：330Ω, 150pF, 1sec, 8 point, 25times/point 	
Criteria	B – Some performance degradation allowed. No data lost. Self-recoverable hardware failure.	
Others	1. Gun to Panel Distance 2. No SPI command, keep default register settings.	

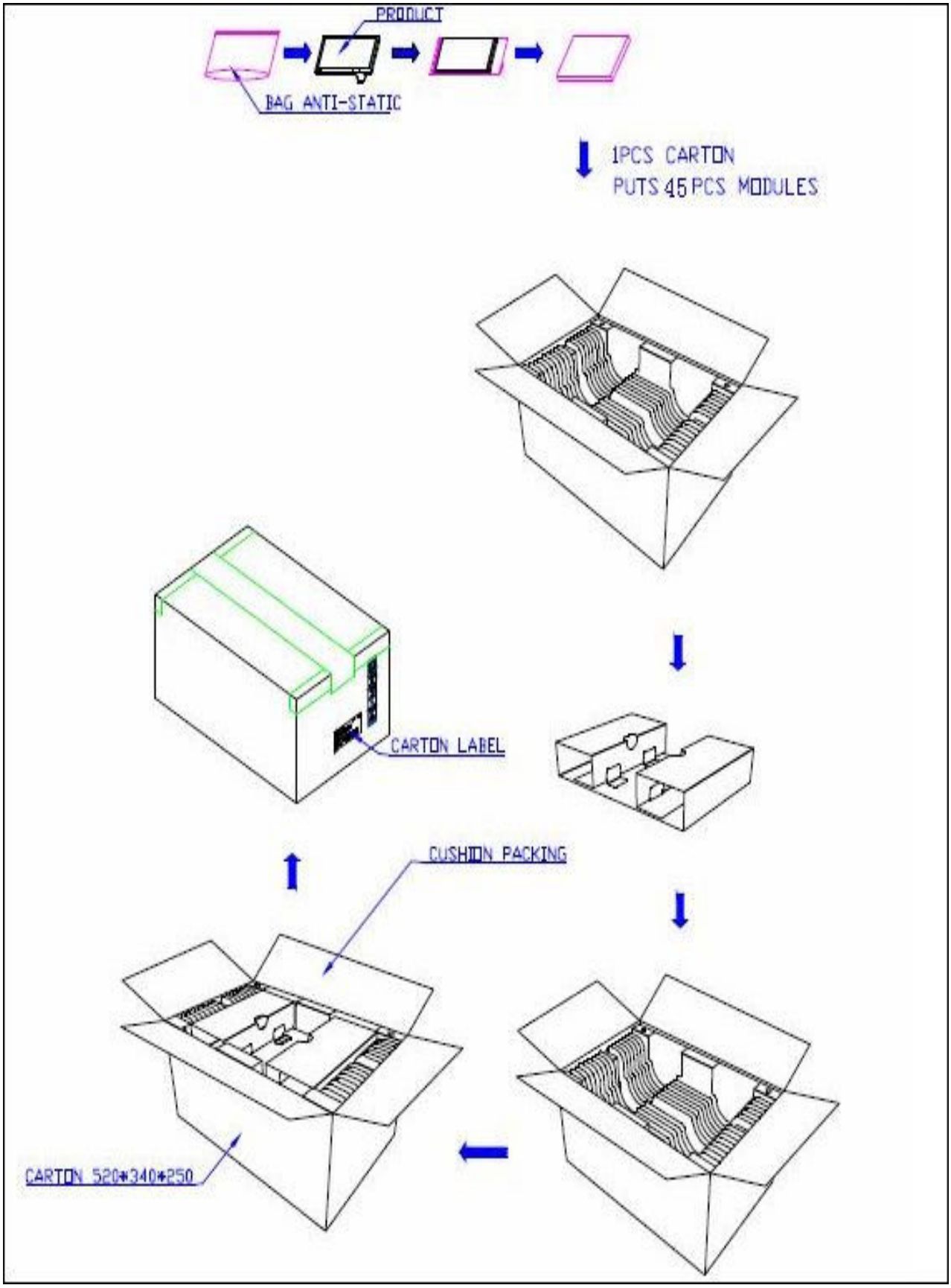
Note 5: Operate with 5 x 5 chess board pattern as figure and light on 24 hrs. Then modify to 32 degree gray pattern. After 20 minutes, the mura is less than JND 2.5



Note 6: The panel is tested as figure. The jig is ϕ 10 mm made by Cu with rubber and the loading speed is 3mm/min on position A~E. After the condition, no glass crack will be found and panel function check is OK.(no guarantee LC mura、LC bubble)

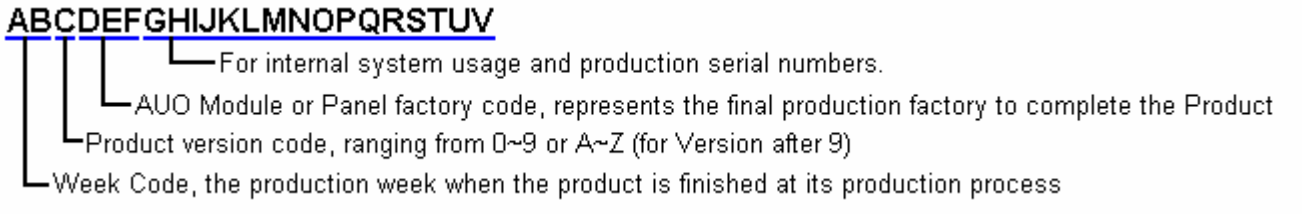
I. Packing and Making

1. Packing Form



2. Module/Panel Label Information

The module/panel (collectively called as the "Product") will be attached with a label of Shipping Number which represents the identification of the Product at a specific location. Refer to the Product outline drawing for detailed location and size of the label. The label is composed of a 22-digit serial number and printed with code 128 with the following definition:



Example:

501M06ZL06123456781Z05:

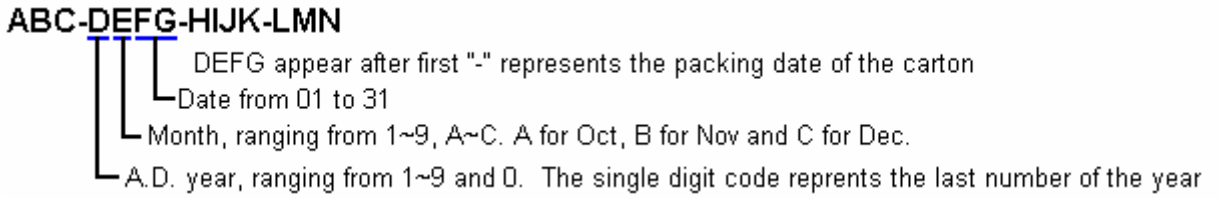
Product Manufacturing Week Code: WK50

Product Version: Version 1

Product Manufactuing Factory: M06

3. Carton Label Information

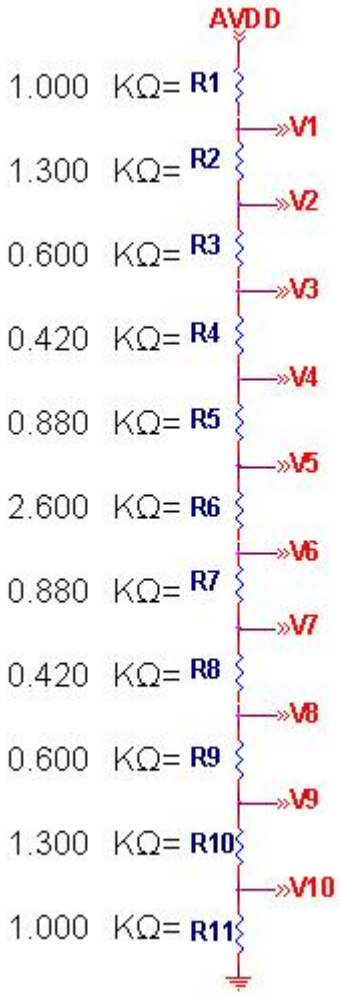
The packing carton will be attached with a carton label where packing Q'ty, AUO Model Name, AUO Part Number, Customer Part Number (Optional) and a series of Carton Number in 13 or 14 digits are printed. The Carton Number is apparing in the following format:



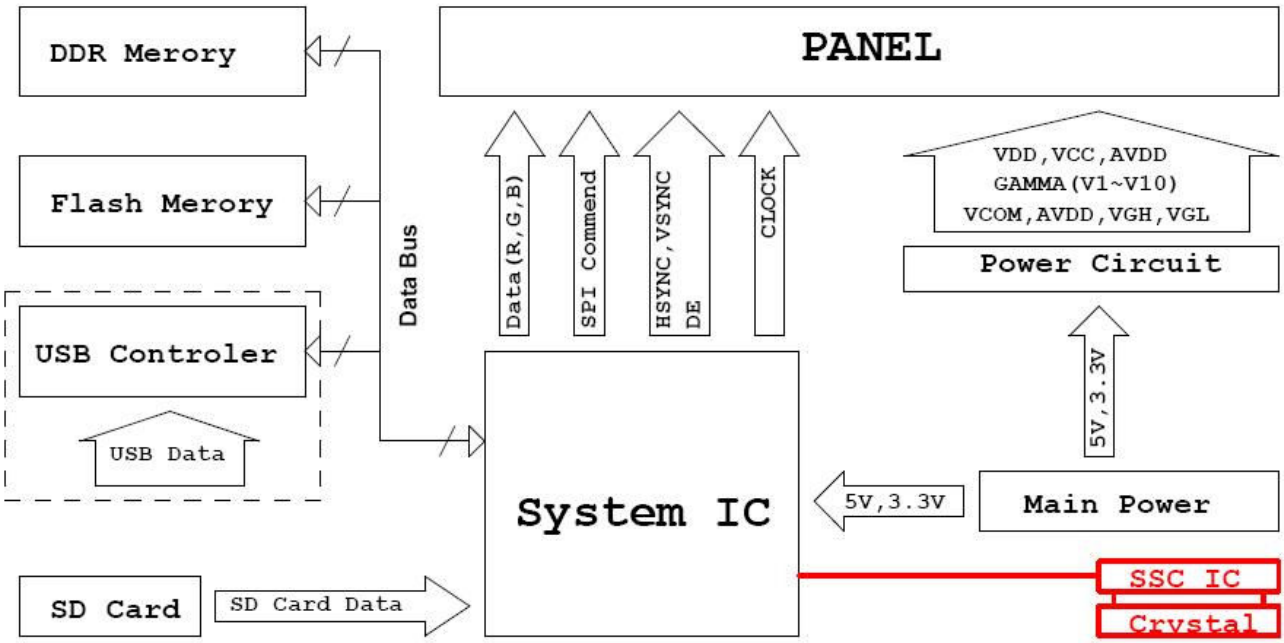
Refer to the drawing of packing format for the location and size of the carton label.

J. Recommend Gamma Voltage & Resistor (Gamma 2.2)

Gamma 2.2		
	AVDD	11
00H	**V1**	10
10H	**V2**	8.7
20H	**V3**	8.1
30H	**V4**	7.68
3FH	**V5**	6.8
3FH	**V6**	4.2
30H	**V7**	3.32
20H	**V8**	2.9
10H	**V9**	2.3
00H	**V10**	1



K. Suggestion- System block



According to there are some risks of EMI issue.
Please refer to this function block before design.
If add SSC (Spread Spectrum Clocking) IC on the clock of system may cause USB abnormal work. Please add USB controller to control USB data.

L. Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with TFT display module.
15. Static electricity will damage the module, please do not touch the module without any grounded device.
16. Do not disassemble and reassemble the module by self.
17. Be careful do not touch the rear side directly.
18. No strong vibration or shock. It will cause module broken.
19. Storage the modules in suitable environment with regular packing.
20. Be careful of injury from a broken display module.
21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.