Doc. Version	0.8
Total Page	22
Date	2008/03/06

Product Specification

7.0” COLOR TFT-LCD MODULE

MODEL NAME: C070VW03 V0

< >Preliminary Specification
< □ >Final Specification

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Note: The content of this specification is subject to change

Record of Revision

Version	Revise Date	Page	Description
0.0	23 Mar,2007	--	Preliminary specification
0.1	26 Apr,2007	8	LED current , from150 change to 125mA
	26 Apr,2007	16,17	Update Drawing
0.2	2 May,2007	5	Outline dimension changed to 167x92.9x5.45mm
		5	AG Haze changed to 25%
		8	Storage temp. changed to 95° C
		15	High Temp. Storage changed to 95° C
		16,17	Update Drawing – add LED wire length and position
0.3		16	Update Drawing – Frame width revised to 2.7mm.
0.4		5	Note 2, change to 18 bit data signal input
		6~8	2.1Pin assignment updates – precise wording and explanation
		9	3.1 “Power Voltage”,AVDD, V-COM,, typical values change to TBD.
		9	3.1 “Power Voltage”, VGL typical value changes to -10V
		10	3.2 Current consumption change to TBD
		10	3.4 AC Timing Condition, Clk frequency,”typical value” change to 33, “Max value” change to 40
		18~19	Mechanical Drawing update
		22	8.2 Power “on/off” sequence update
0.5		18~19	Mechanical Drawing update (Add FPC thickness…)
0.6		9	2.2 LED Maximum Ratings
		9	3.1 Typical operating condtion
		10	3.2 Current Consumption
			3.3 LED Backlight driving condition
		20	7 Packing Form
		21	8.1 Gamma Circuit

0.7		10	LED_Absolute Maximum Rating
		11	LED_Back Light Driving Condition
		10	AVDD, V-COM value updates
		18/19	2D drawing updates
		21	Gamma Circuit updates
0.8		15	Optical Specification, If current updates
		18/19	Drawing Updates
		20	Packing Form : 40pcs in one carton

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General Description

The AUO Color amorphous silicon Thin Film Transistor LCD module is an active matrix Liquid Crystal Display produced by making the most of AUO's expertise in Flat Panel Display technologies having a 17:9 aspect ratio which the main application will cover navigation and entertainment systems of automotive industry.

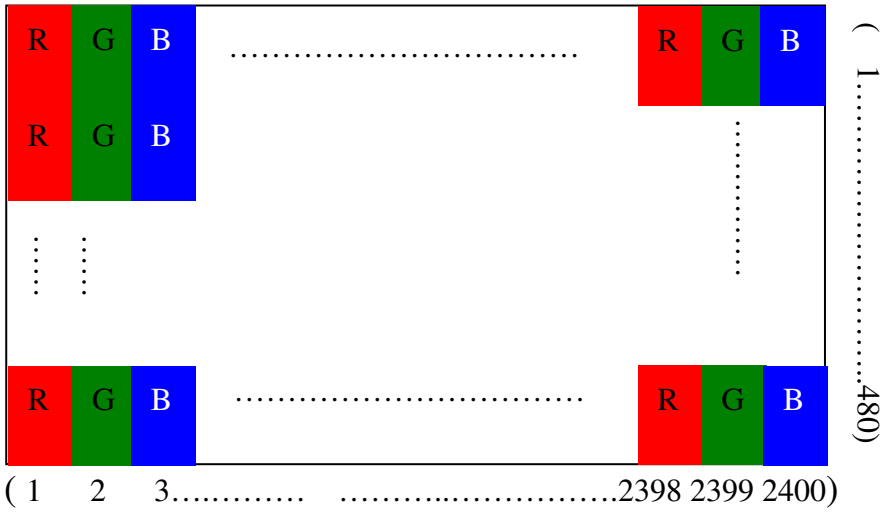
Features

- 17:9 aspect ratio suitable in wide-screen systems
- Higher resolution image composed of 384,000 pixel elements
- Wide viewing angle technology
- High contrast by Super Wide View technology
- Robust module design by using COG mounting technology
- TN-normally white mode
- High power LEDs backlight with Mercury-free solution

1. General Information

NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	800RGB(H)×480(V)	
2	Active Area	mm	157.20(H)×82.8(V)	
3	Screen Size	inch	6.95(Diagonal)	
4	Pixel Pitch	mm	0.0655xRGB(H)×0.1725(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	262K Colors	Note 2
7	Overall Dimension	mm	167.0(H) × 92.9(V) × 5.45(T)	
8	Weight	g	TBD	
9	Panel surface treatment	--	AG(25% haze)	
10	Display Mode	--	Normally White	
11	Backlight Unit	--	High Power LEDs	

Note 1: Below figure shows the dot stripe arrangement.



Note 2: The 262K color display depends on 18-bit data signal input.

2. Electrical Specifications

2.1 Pin Assignment

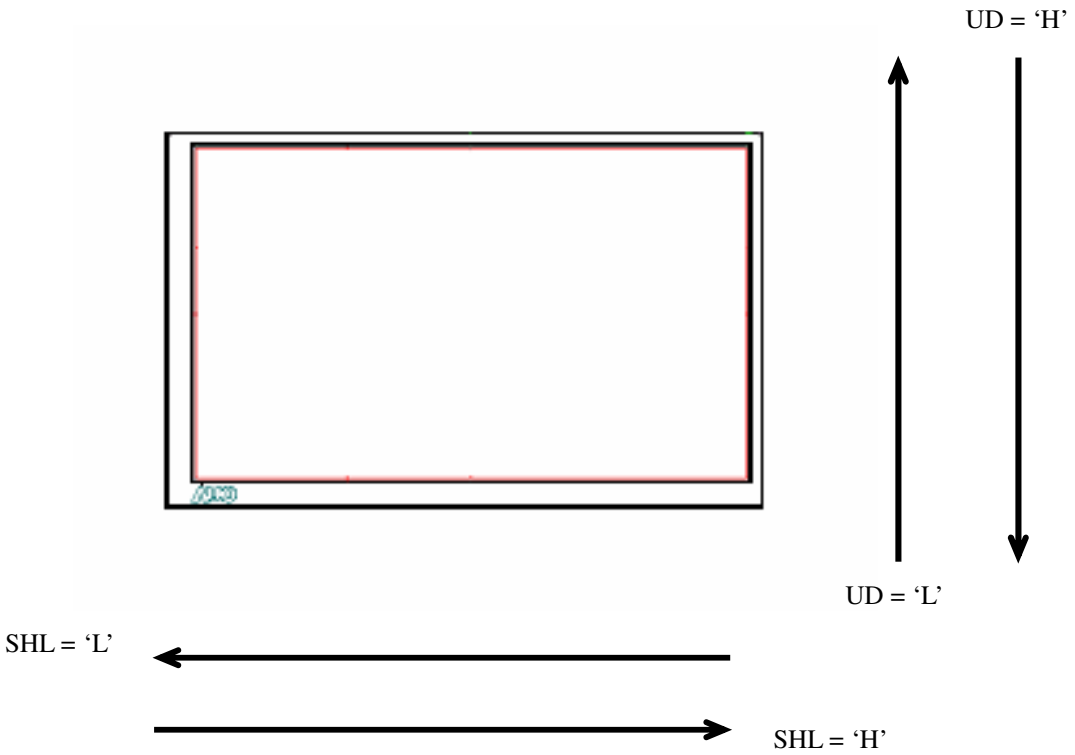
Connector type: FH12-50S-0.5SH or compatible

Pin No	Symbol	I/O	Function	Remark
1	GND	P	Digital Ground for gate drive	
2	VCC	P	Digital voltage for gate driver	
3	VGL	P	TFT low voltage	
4	VGH	P	TFT high voltage	
5	STVL	I/O	Start pulse signal input/output (Vertical)	Note 1
6	STVR	I/O	Start pulse signal input/output (Vertical)	Note 1
7	CKV	I	Shift clock input for gate driver	
8	U/D	I	Up or Down display control	Note 1
9	OEV	I	Output enable, active low. The gate driver outputs are disable when OEV = “H”.	
10	VCOM	I	Common electrode driving signal	
11	DIO1	I/O	Start pulse signal input/output (Horizontal)	Note 1
12	AVDD	P	Analog voltage for source driver	
13	AGND	P	Analog ground for source driver	
14	GND	P	Digital ground for source driver	
15	VCC (DVDD)	P	Digital voltage for source driver	
16	EDGSL	I	Select raising edge or raising/falling edge When EDGSL = "0", Latching source data onto the line latches at the rising edge When EDGSL = "1", Latching source data onto the line latches at the rising edge and falling edge	
17	CLK	I	Sampling and shifting clock pulse for source driver	
18	SHL(R/L)	I	Right or Left display control	Note 1
19	R0	I	Red data (LSB)	
20	R1	I	Red data	
21	R2	I	Red data	
22	R3	I	Red data	
23	R4	I	Red data	

24	R5	I	Red data (MSB)	
25	G0	I	Green Data (LSB)	
26	G1	I	Green Data	
27	G2	I	Green Data	
28	G3	I	Green Data	
29	G4	I	Green Data	
30	G5	I	Green Data (MSB)	
31	V1	I	Gamma Correction Reference Voltage	
32	V2	I	Gamma Correction Reference Voltage	
33	V3	I	Gamma Correction Reference Voltage	
34	V4	I	Gamma Correction Reference Voltage	
35	V5	I	Gamma Correction Reference Voltage	
36	V6	I	Gamma Correction Reference Voltage	
37	V7	I	Gamma Correction Reference Voltage	
38	V8	I	Gamma Correction Reference Voltage	
39	V9	I	Gamma Correction Reference Voltage	
40	V10	I	Gamma Correction Reference Voltage	
41	B0	I	Blue Data (LSB)	
42	B1	I	Blue Data	
43	B2	I	Blue Data	
44	B3	I	Blue Data	
45	B4	I	Blue Data	
46	B5	I	Blue Data (MSB)	
47	LD (OEH)	I	Latch and switch data to output	Note 2
48	REV	I	Control Whether RGB data are inverted or not When “REV” = 1 these data will be inverted. Ex. “00” ” 3F” , “07” ” 38” , and so on	
49	POL	I	Polarity selection	Note 3
50	DIO2	I/O	Start pulse signal input/output (Horizontal)	Note 1

I: Input pin; O: Output pin; I/O : Input or Output pin; P: Power

Note 1.



U/D	STVL	STVR	Direction
H	Output	Input	U → D
L	Input	Output	D → U

SHL	DIO1	DIO2	Direction
H	Input	Output	L → R
L	Output	Input	R → L

Note 2. LD

Latches the polarity of outputs and switches the new data to outputs.

1. At the rising edge, latches the "POL" signal to control the polarity of the outputs.

2. The pin also controls the switch of the line registers that switches the new incoming data to outputs.

Note 3. POL

"POL" value is latched at the rising edge of "LD" to control the polarity of the even or odd outputs.

"POL=1" represents that even outputs are of positive polarity with a voltage range from V1 to V5, and odd outputs are of negative polarity with a voltage range from V6 to V10. On the other hand, if LD gets low level "POL", even outputs are of negative polarity and odd outputs are of positive.

POL=1: Even outputs range from V1 ~ V5, and Odd outputs range from V6 ~ V10

POL=0: Even outputs range from V6 ~ V10, and Odd outputs range from V1 ~ V5

2.2 Absolute Maximum Ratings

Items	Symbol	Product Specification			Unit
		Min.	Typ.	Max.	
Power Voltage	Vcc	-0.3		5	V
	AVDD	-0.5		12	V
	VGH	-0.3		18	V
	VGL	-15		0.3	V
	VGH-VGL			33	V
Input Signal Voltage	Vi	-0.3		Vcc+0.3	V
	Vref(V1~V5)	0.4AVDD		AVDD+0.3	V
	Vref(V6~V10)	-0.3		0.6AVDD	V
	VCOM	4.0		4.4	V
Operating Temperature	Topa	-30		85	□
Storage Temperature	Tstg	-40		95	□
LED	Vf		18.6	21	V
	If		125	150	mA

3. Electrical Characteristics

3.1 Typical Operating Condition

Items	Symbol	Product Specification			Unit
		Min.	Typ.	Max.	
Power Voltage	VCC	3.0	3.3	3.6	V
	AVDD	9	9.9	10	V
	VGH	13.5	15.0	16.5	V
	VCOM	3.6	4.1	4.6	V
	VGL	-8	-7	-6	V
Input Reference Voltage	V1~V5	0.4AVDD	—	AVDD-0.1	V
	V6~V10	0.1	—	0.6AVDD	V
Input H/L level Voltage	VIH	0.8VCC	—	VCC	V
	VIL	0	—	0.2VCC	V

Note: All values should be measured under the condition of GND=AVss=0V

3.2 Current Consumption

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Current For Driver	IGH	VGH=(15V)		100	250	uA
	IGL	VGL=(-7V)		300	500	uA
	ICC	VCC=(3.3V)		5	15	mA
	IDD	AVDD=(9.8V)		30	36	mA

3.3 LED Backlight Driving Condition (Connector : JST-PHR-2)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Voltage	Vf			18.6	21	V
Current	If			125	150	mA
LED life time		Note 2	10,000	--	--	Hrs

Note 1: Panel surface temperature should be kept less than content of section 2.2. “Absolute maximum ratings"

Note 2: The ”LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃, If=125mA

3.4 AC Timing Condition

Characteristics (VCC=3.3V, AVDD=9.8V, AVSS=GND=0V, TA=25℃)

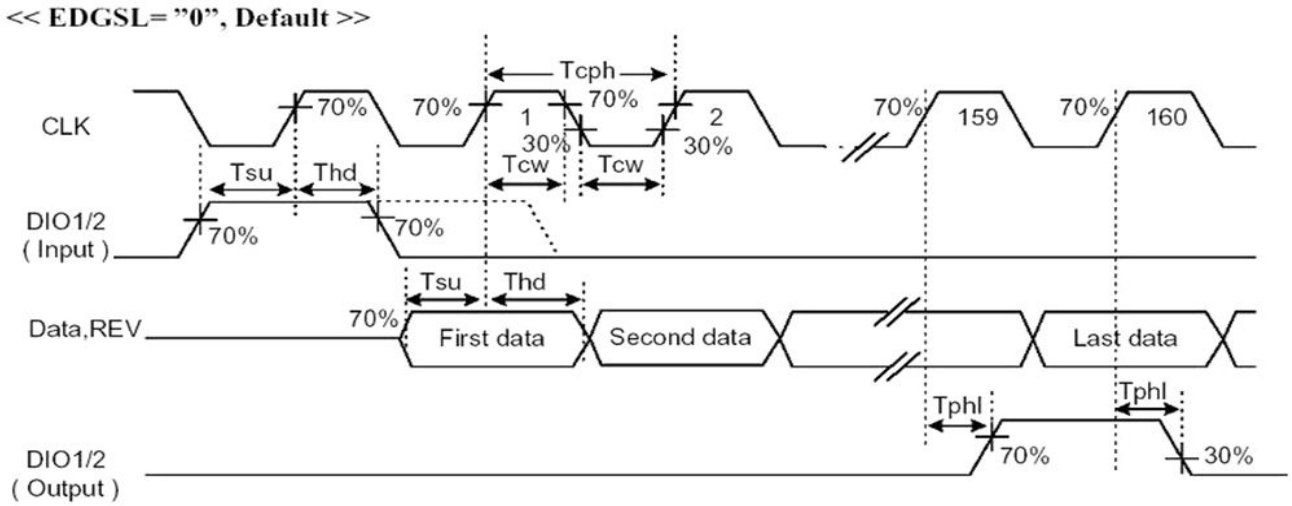
Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK frequency	Fclk		33	40	MHz
CLK pulse width	Tcw	8			ns
Data set-up time	Tsu	4			ns
Data hold time	Thd	2			ns
Propagation delay of DIO2/1	Tphl	6	10	15	ns
Time for the last data to LD	Tld	1			Tcw
Pulse width of LD	Twld	2			Tcw
Time for LD to DIO1/2	Tlds	5			Tcw
POL set-up time	Tpsu	6			ns
POL hold time	Tphd	6			ns
CKV pulse width	Tckv	16	28	40	Tcw
STV setup time	Tsuv	400			ns
STV hold time	Thdv	400			ns
Vertical display start	Tsv		3		TDH
Output stable time	Tst			15	us

Note: The panel is designed to prevent the current leakage for the best display performance. If shorter discharge time is desired when system power off, then extra discharge circuit may be required at customer's side.

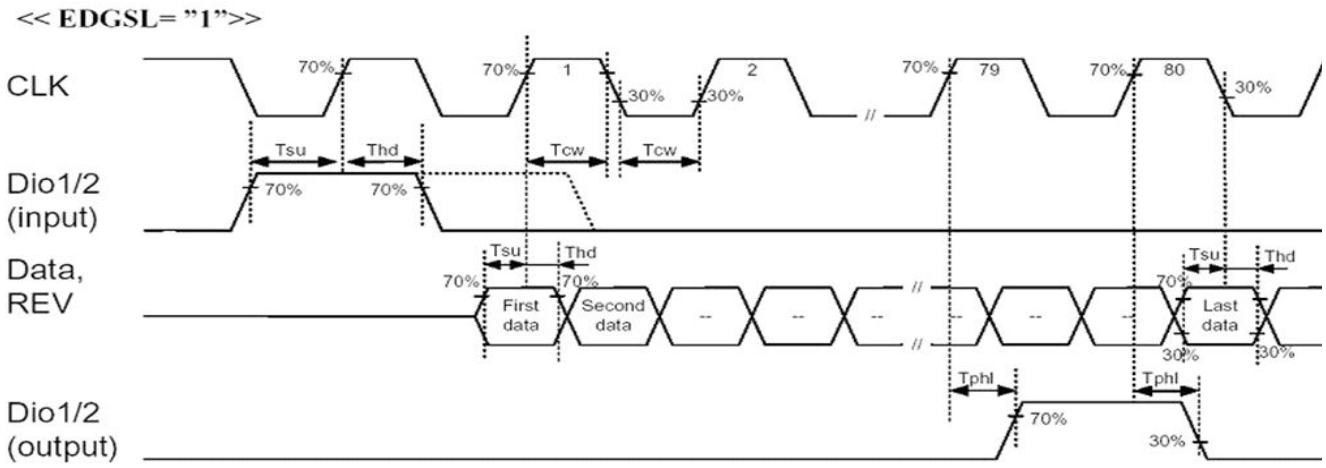
3.5 Timing Diagrams

Operation Mode 1

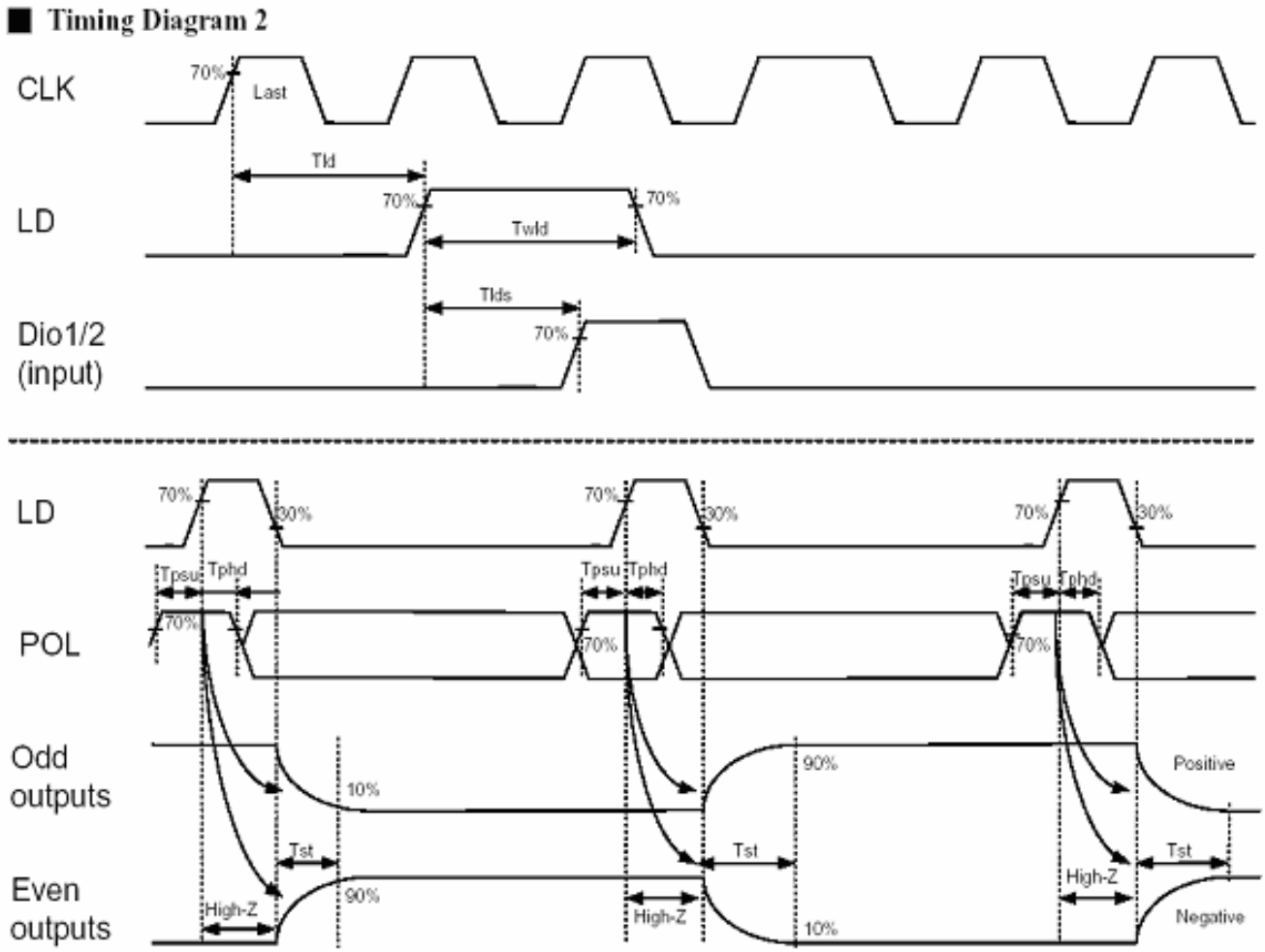
■ Timing Diagram 1 (CHNSL="1" , Default)



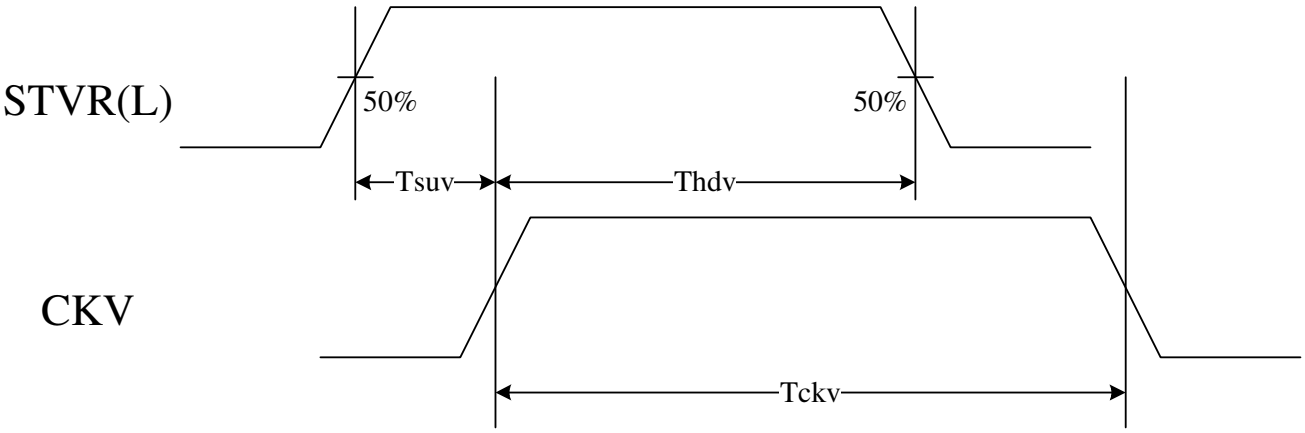
Operation Mode 2



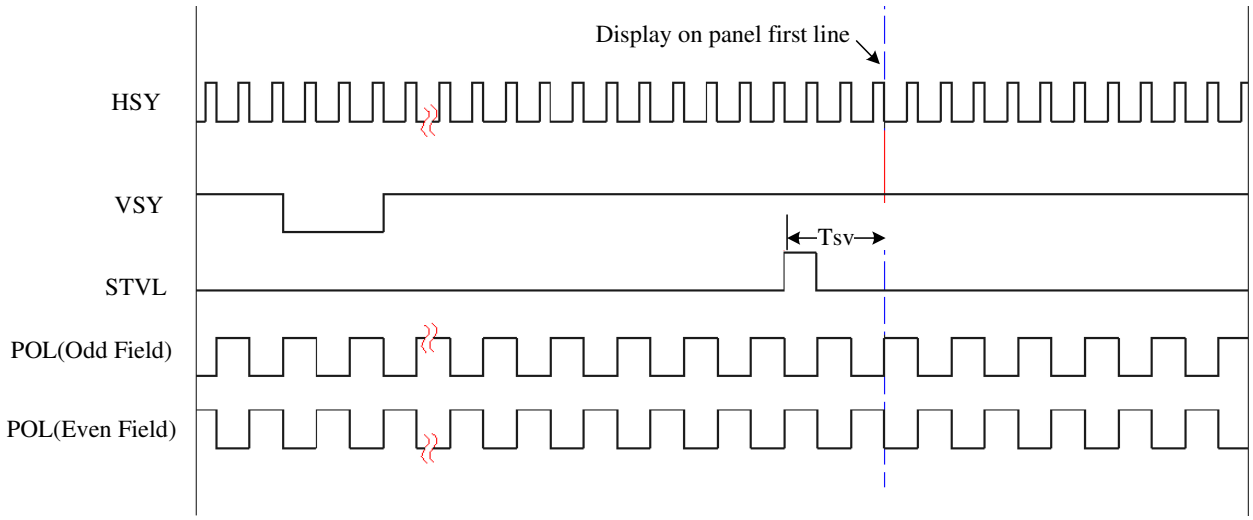
Horizontal timing



Vertical shift clock timing



Vertical timing (from up to down)



4. Optical Specifications

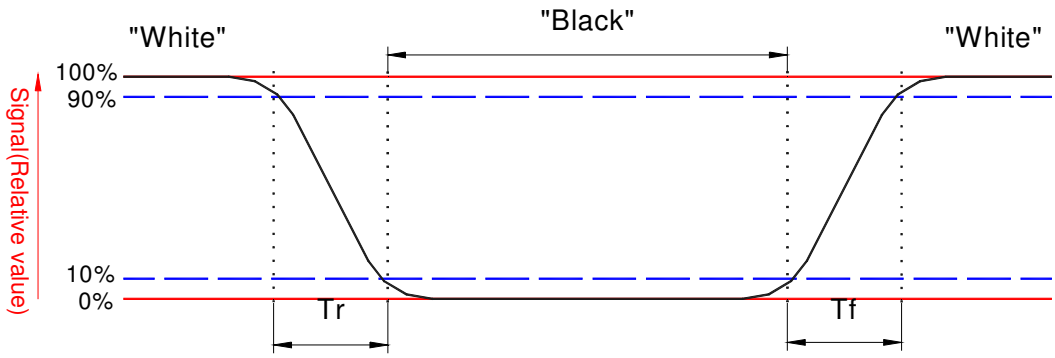
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise Fall	Tr Tf	θ=0°	- -	6 10	10 20	ms ms	Note 3,5
Contrast ratio		CR	At optimized Viewing angle	200	300	-	-	Note 4, 5
Viewing angle	Top Bottom Left Right		CR□10	30 50 50 50	40 60 60 60		deg.	Note 5
Viewing angle	Top Bottom Left Right		CR□5	40 60 60 60	50 70 70 70		deg.	Note 5
Brightness		Y_L	If= 125 mA,25□	450	500	-	nit	Note 6
White chromaticity		x	θ=0°	0.26	0.31	0.36		Note 6
		y	θ=0°	0.29	0.34	0.39		

Note 1 : Ambient temperature = 25℃, and LED current If = 125 mA. To be measured in the dark room.

Note 2 :To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5A, after 10 minutes operation.

Note 3: Definition of response time:

The response time is defined as the time interval between the 10% and 90% of amplitudes. The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time).



Note 4. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 5. White Vdata=V5 or V6

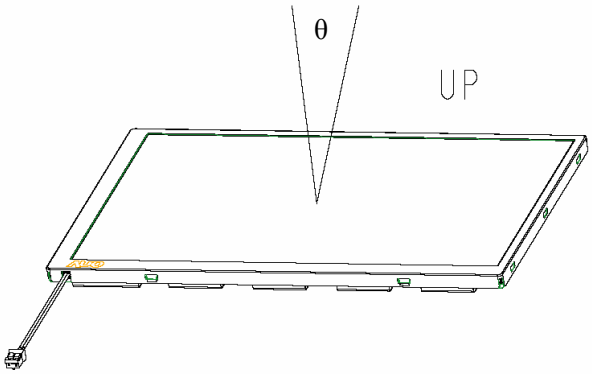
Black Vdata=V1 or V10

(For definition of V1, V5, V6 & V10, please refer to section 9.1)

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 6. Brightness and White Chromaticity are measured at the center area of the panel at white frame.

Note 7. For definition of viewing angle please refer to figure as below.



5. Reliability Test Items

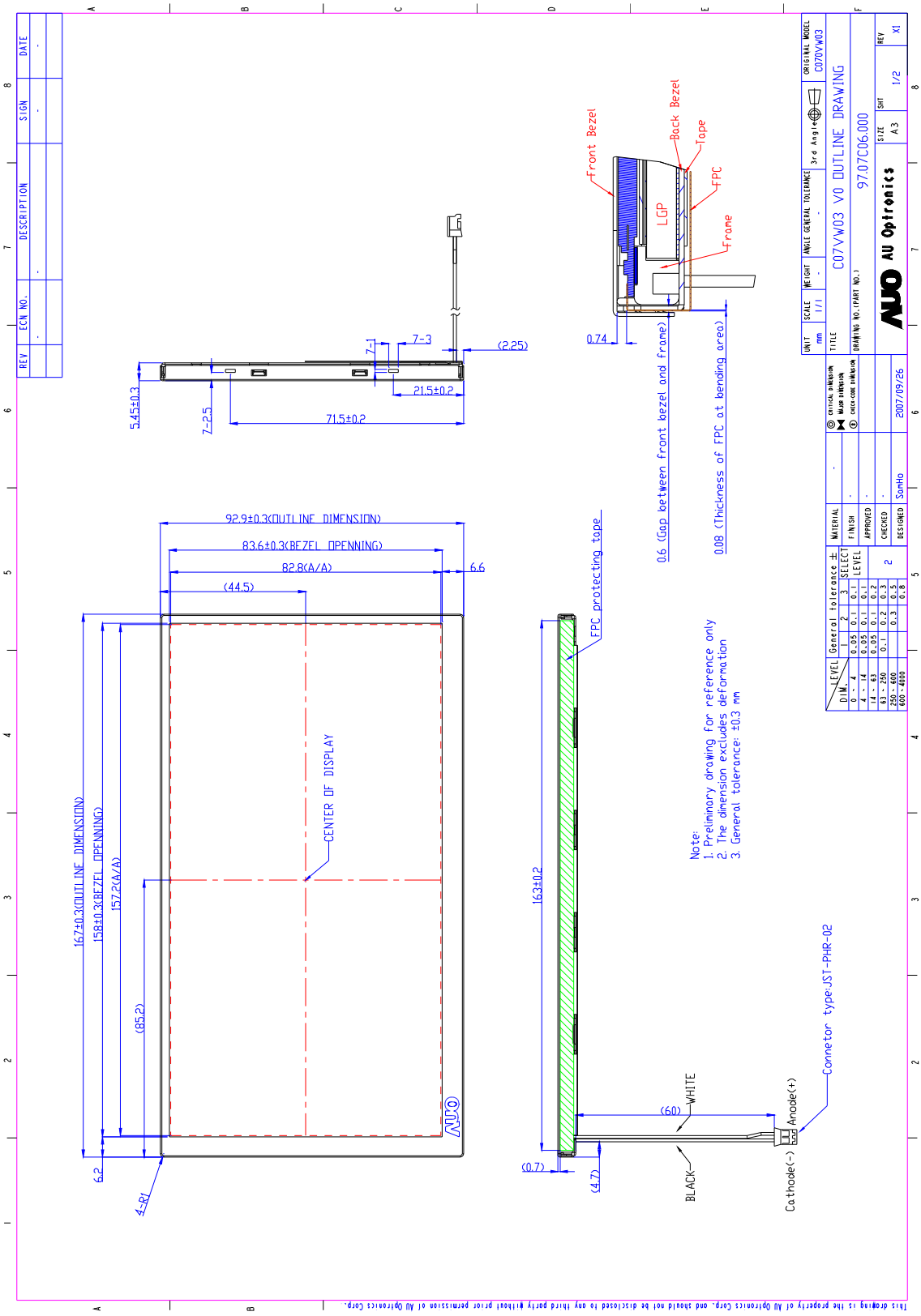
No.	Test items	Conditions		Remark
1	High temperature storage	Ta= 95□	240Hrs	
2	Low temperature storage	Ta= -40□	240Hrs	
3	High temperature	Ta= 85□	240Hrs	
4	Low temperature	Ta= -30□	240Hrs	
5	High temperature and	Ta= 60□, 90% RH	240Hrs	Operation
6	Heat shock	-30□~85□/100 cycles 1Hrs/cycle		Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal		Non-operation
8	Vibration	Frequency range	8~33.3Hz	JIS D1601,A10 Condition A
		Stoke	1.3mm	
		Sweep	2.9G, 33.3~400Hz	
		Cycle	15min.	
		2 hours for each direction of X, Z 4 hours for Y direction		
9	Mechanical shock	100G, 6ms, ±X,±Y,±Z 3 times for each direction		
10	Vibration (with carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz		IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces		

Note 1: Ta: Ambient temperature.

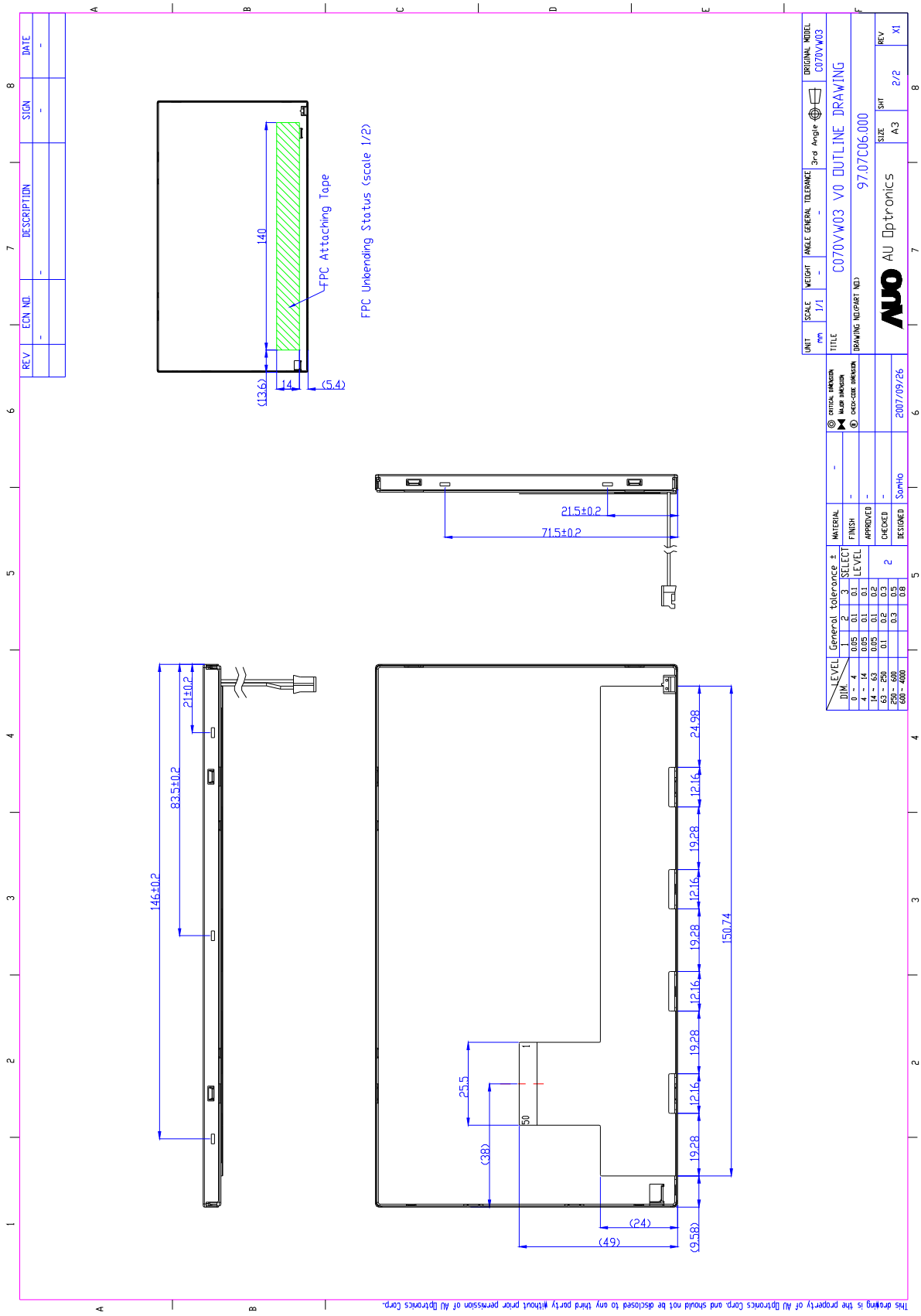
Note 2: In the standard conditions, there is not display function failure issue occurred. All the cosmetic specification is judged before the reliability stress.

6. Outline Dimension

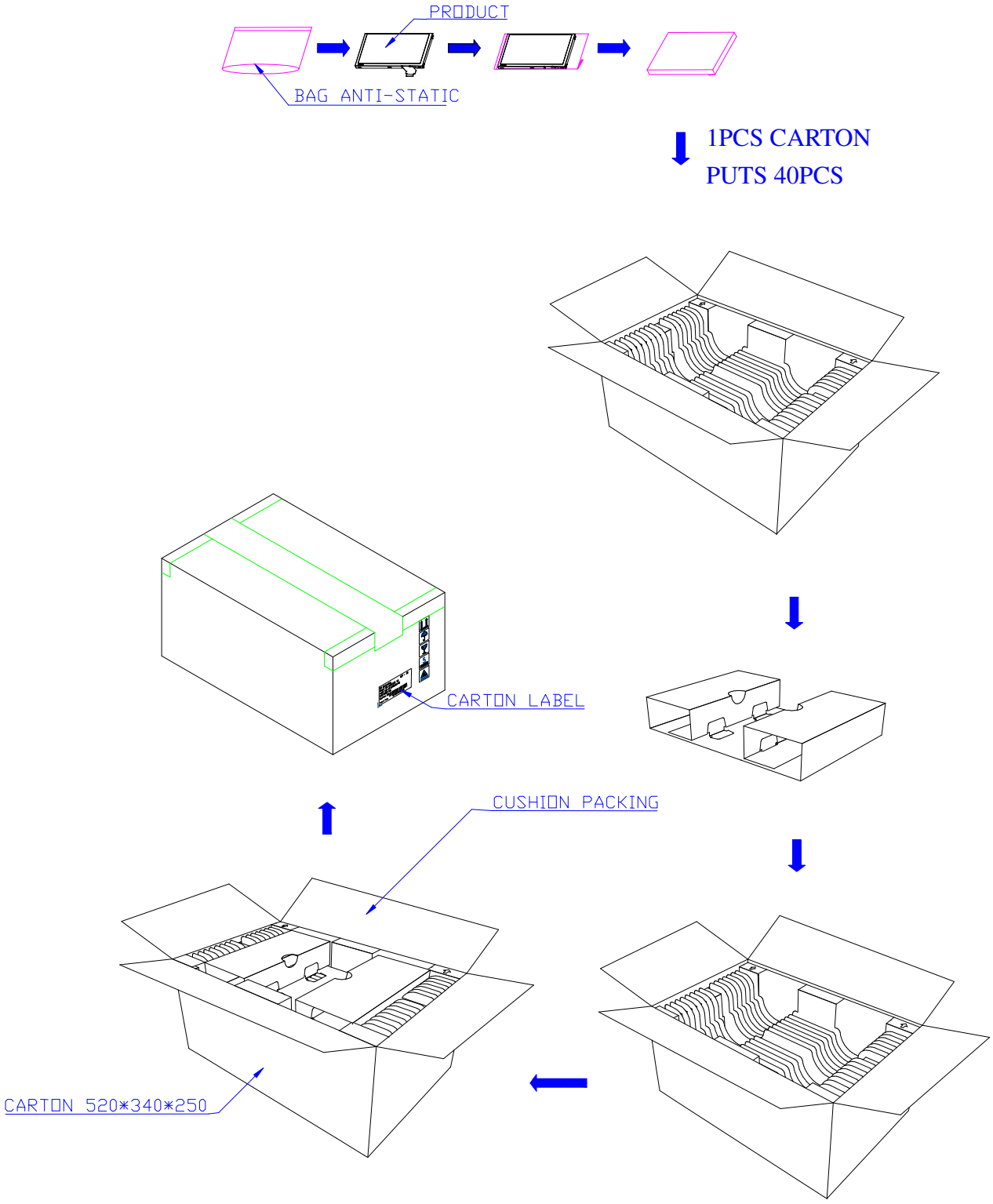
Front View



Rear View

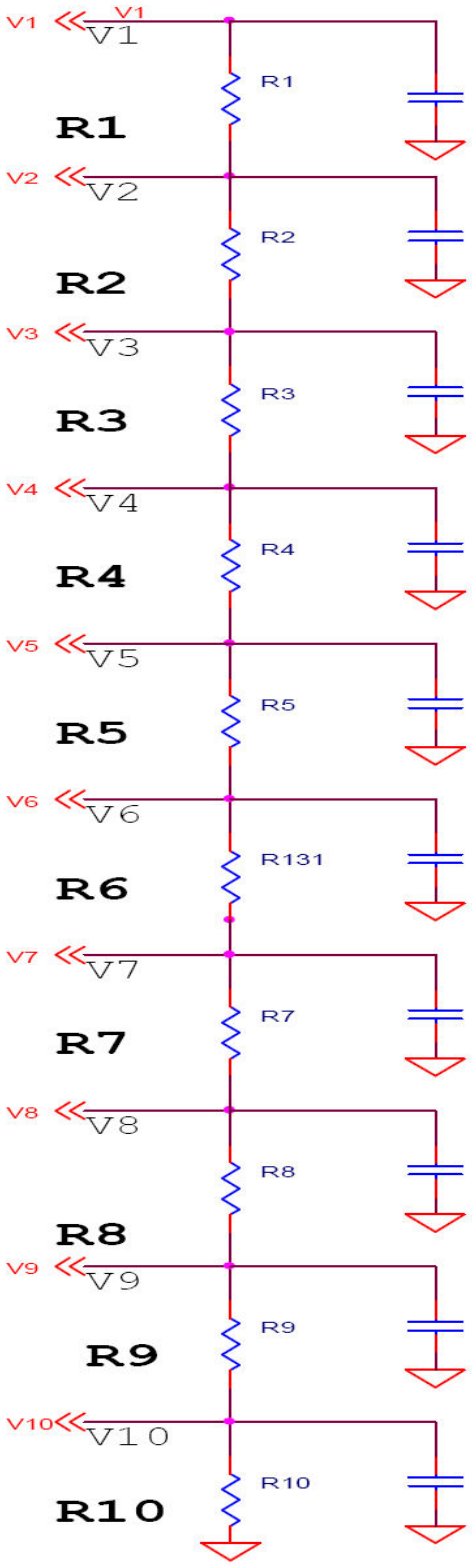

FPC Attaching Tape
FPC Unbending Status (scale 1/2)
140
(13.6)
14
(5.4)
21.5±0.2
71.5±0.2
146±0.2
83.5±0.2
21±0.2
24.98
12.16
19.28
150.74
25.5
(38)
(24)
(49)
(9.58)
C070VW03 V0 OUTLINE DRAWING
97.07C06.000
AU Optronics
2007/09/26
This drawing is the property of AU Optronics Corp. and should not be disclosed to any third party without prior permission of AU Optronics Corp.

7. Packing Form -

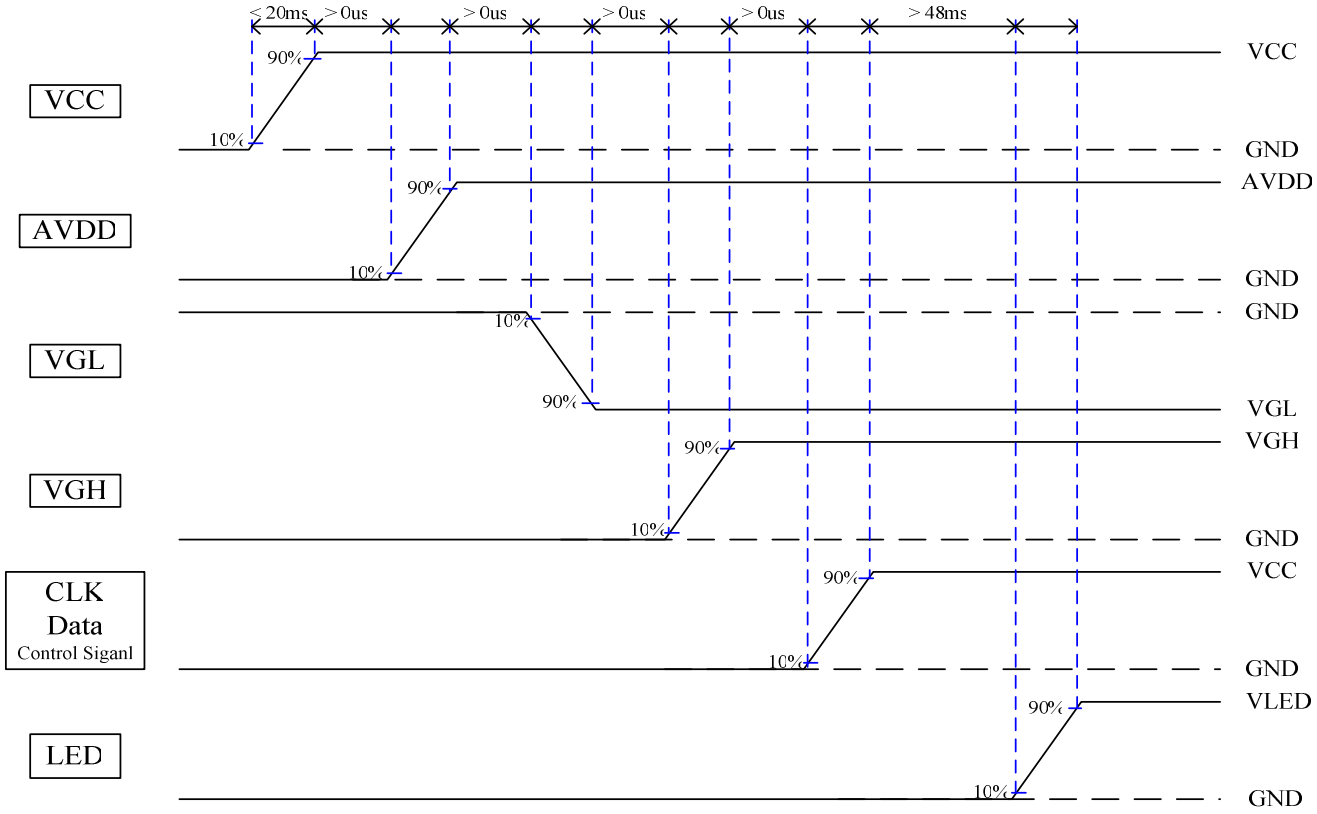
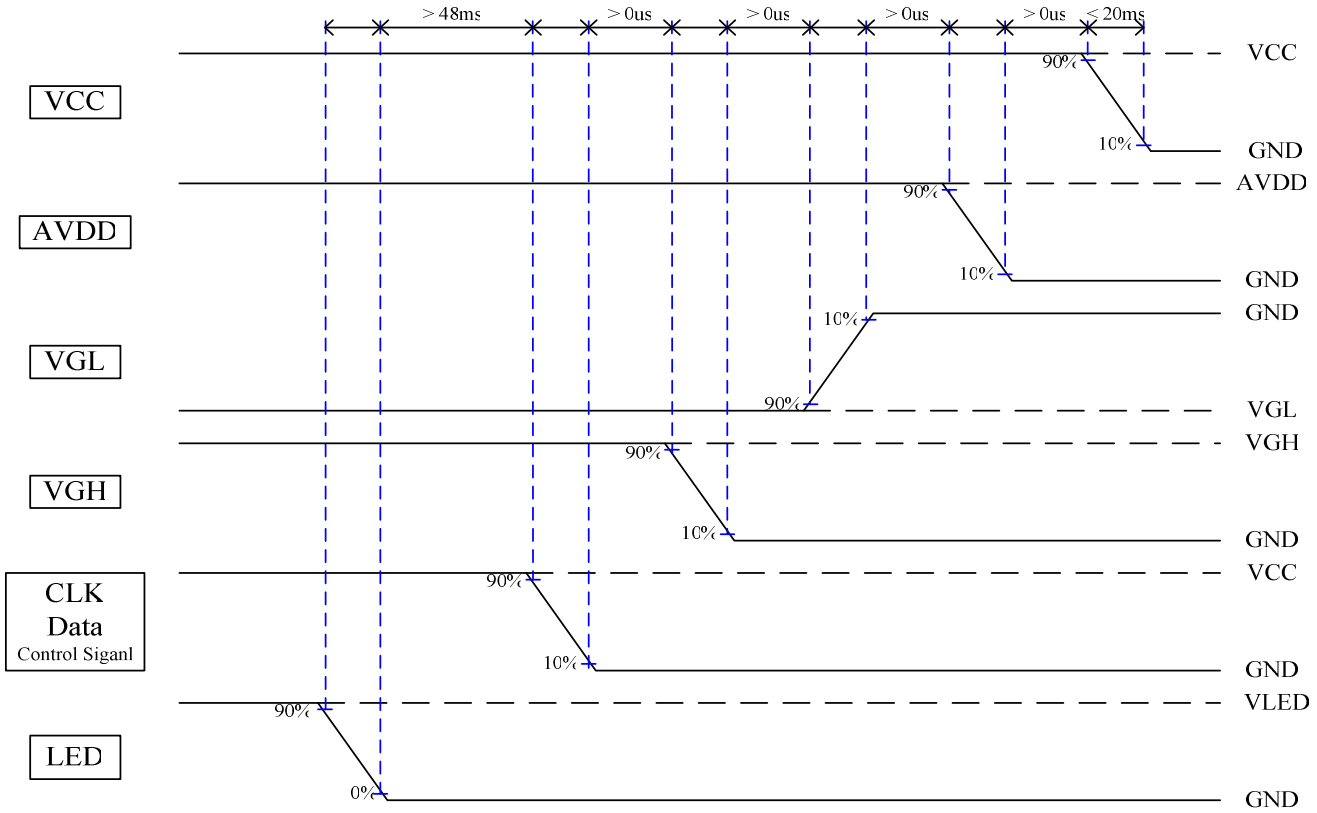


8. Application Notes – (For Reference only, could be modified after the product come out.)

8.1 Typical application circuit – Gamma Circuit



Gamma	Voltage(V)
V1	9.8
V2	8.22
V3	7.6
V4	7.2
V5	6.49
V6	3.87
V7	2.84
V8	2.36
V9	1.66
V10	0.17

R	Gamma2
R1	392
R2	162
R3	107
R4	178
R5	523
R6	289.2
R7	137
R8	189.2
R9	362.2
R10	36

8.2 Power On/Off sequence