TFT LCD Tentative Specification

MODEL NO.: N089L6 - L02

Customer : _____

Approved by : _____

Note :

- CONTENTS -

REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver. 0.0	Mar. 12, 2008	All	All	Tentative specification first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N089L6 - L02 is a 8.9" TFT Liquid Crystal Display module with LED Backlight unit and 40 pins LVDS interface. This module supports 1024 x 600 Wide-SVGA mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction. The converter module for Backlight is built in.

1.2 FEATURES

- Thin and High Brightness
- WSVGA (1024 x 600 pixels) resolution
- DE only mode
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 1 pixel/clock
- Build in LED Converter

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	195.072(H) x 113.4(V)	mm	(1)
Bezel Opening Area	198.27(H) x 116.6(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1024 x R.G.B. x 600	pixel	-
Pixel Pitch	0.1905(H) X 0.189(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), Glare Type	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	213.06	213.36	231.66	mm	(1)
	Vertical (V)	129.25	129.55	129.85	mm	
	Depth (D)	---	5.15	5.45	mm	
Weight		---	185	200	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

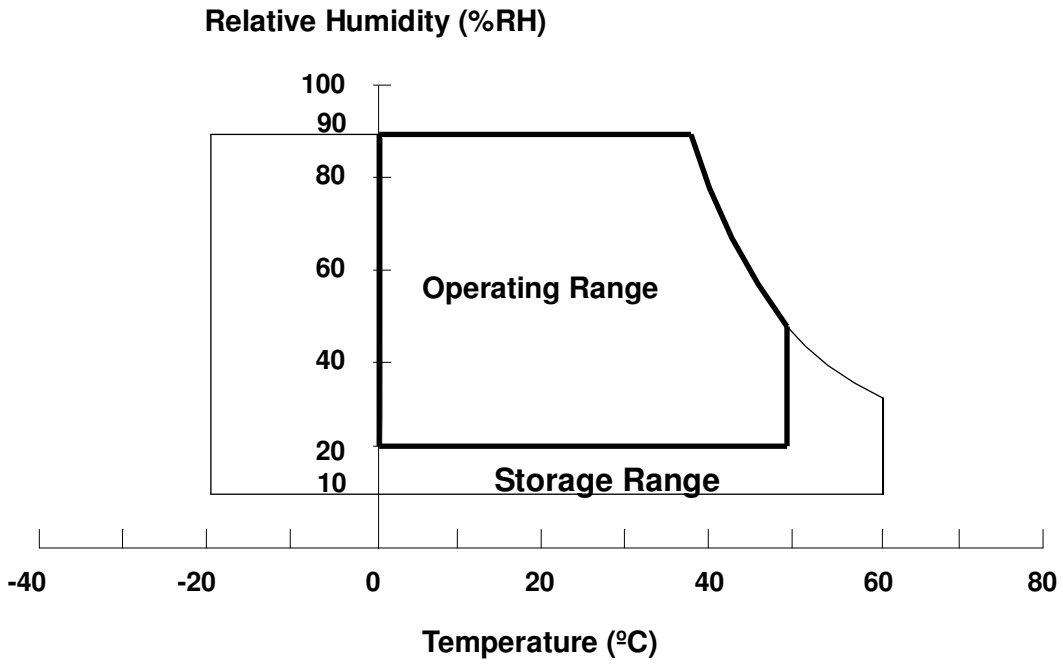
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	220/2	G/ms	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.5	G	(4), (5)

Note (1) (a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The temperature of panel display surface area should be 0 ºC Min. and 60 ºC Max.

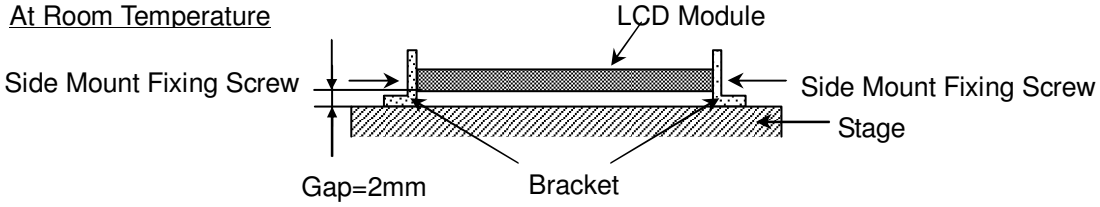


Note (3) 1 time for ± X, ± Y, ± Z. for Condition (220G / 2ms) is half Sine Wave,.

Note (4) 10 ~ 500 Hz, 30 min/cycle,1cycles for each X, Y, Z axis.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	V_{CC}+0.3	V	
LED Converter Enable	ENA	0	5	V	
LED BLU Brightness Control	ADJ	0	5	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

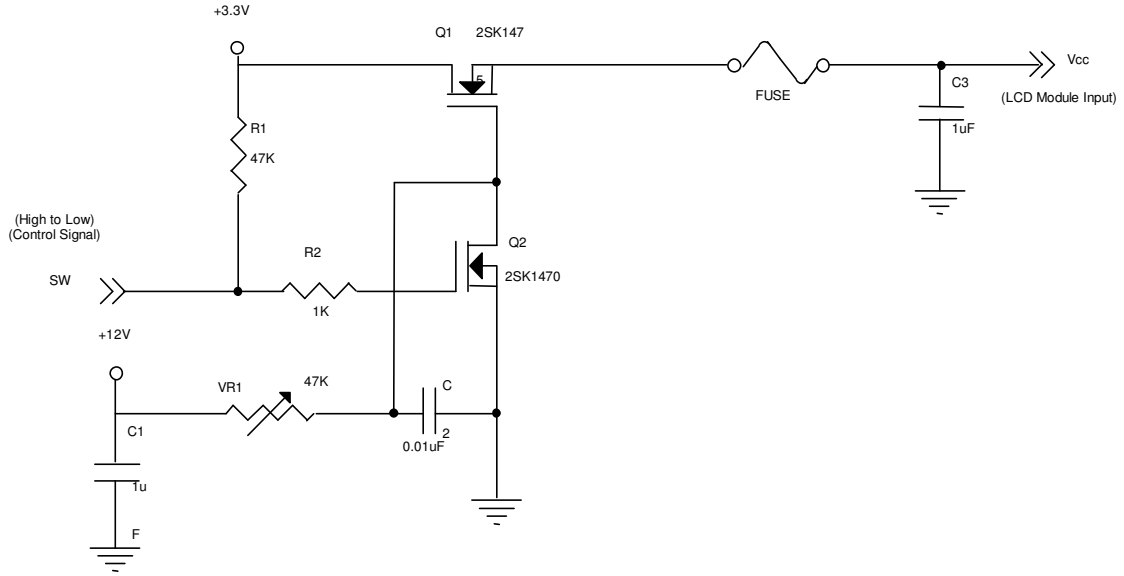
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCC	3.0	3.3	3.6	V	-
Ripple Voltage		V_{RP}	-		100	mV	-
Rush Current		I_{RUSH}	-	1.2	1.5	A	(2)
Initial Stage Current		I_{IS}			1.0	A	(2)
Power Supply Current	White	Lcc	-	(162)	TBD	mA	(3)a
	Black		-	(212)	TBD	mA	(3)b
LVDS Differential Input High Threshold		$V_{TH(LVDS)}$			+100	mV	(5), V_{CM}=1.2V
LVDS Differential Input Low Threshold		$V_{TL(LVDS)}$	-100			mV	(5) V_{CM}=1.2V
LVDS Common Mode Voltage		V_{CM}	1.125		1.375	V	(5)
LVDS Differential Input Voltage		$\|V_{ID}\|$	100		600	mV	(5)
Terminating Resistor		R_T	-	100	-	Ohm	-
Power per EBL WG		P_{EBL}	-	TBD		W	(4)
LED Power Supply		VLED	4.5	5	5.5	V	
LED Power Current	VLED=5V		TBD	(446)	TBD	mA	
Enable Signal Turn-on Level Threshold		VIH_{ENA}	(1.4)			V	
Enable Signal Turn-off Level Threshold		VIL_{ENA}			(0.5)	V	
Brightness Control Signal High Level Threshold		VIH_{ADJ}	(1.4)			V	
Brightness Control Signal Low Level Threshold		VIL_{ADJ}			(0.5)	V	
LED BLU Brightness Control Signal Frequency		F_{ADJ}	TBD	200	TBD	Hz	

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

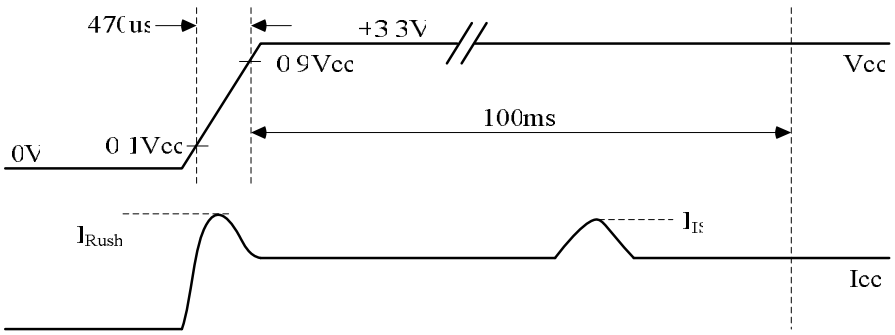
Note (2) I_{RUSH}: the maximum current when VCC is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.

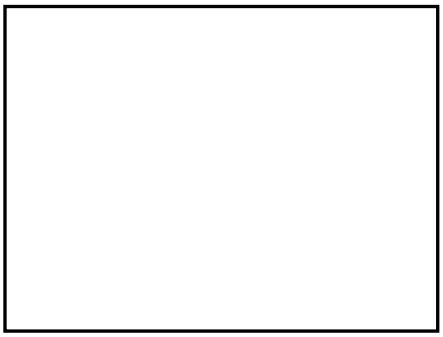


Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern



Active Area

b. Black Pattern

Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.

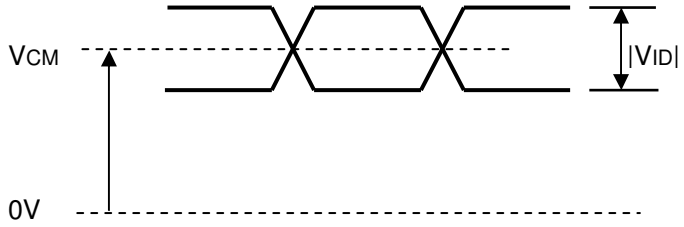
(a) Vcc = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz,

(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

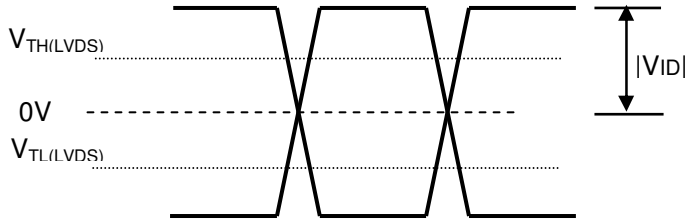
(c) Luminance: 60 nits.

Note (5) The parameters of LVDS signals are defined as the following figures.

Single Ended



Differential



3.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

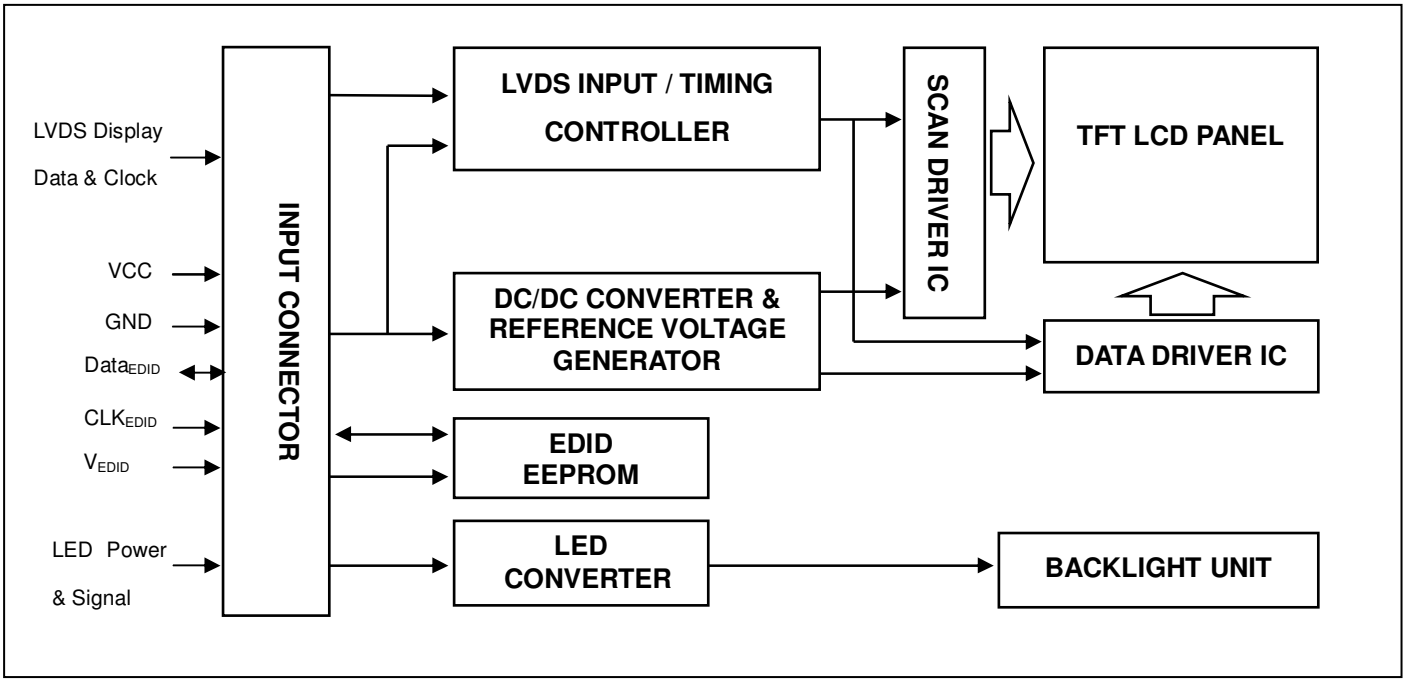
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Life Time	L_{BL}	12000	-	-	Hrs	(1)

Note (1) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 °C and I = 20 mA(Per EA) until one of the following events occurs:

When the brightness becomes ≦ 50% of its original value.

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

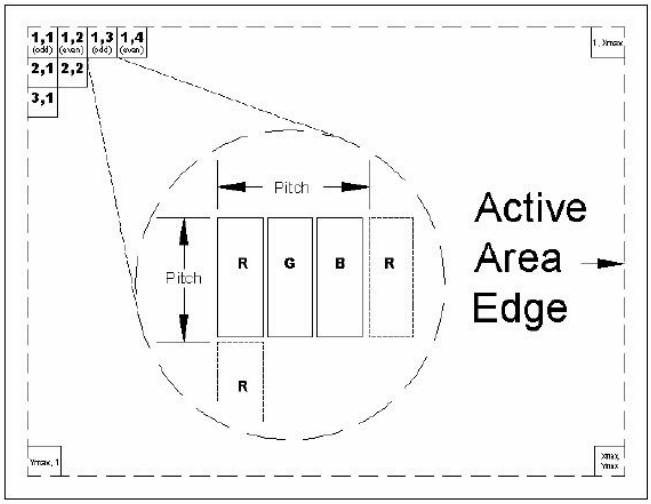
Pin	Symbol	Description	Polarity	Remark
1	GND	Ground		
2	VCC	Power Supply (+3.3V typ.)		
3	VCC	Power Supply (+3.3V typ.)		
4	V_{EDID}	EDID power (+3.3V typ.)		
5	NC	No Connection (Reserved for CMO test)		
6	CLK_{EDID}	EDID clock		
7	$DATA_{EDID}$	EDID data		
8	Rxin0-	LVDS Differential Data Input	Negative	R0~R5,G0
9	Rxin0+	LVDS Differential Data Input	Positive	
10	GND	Ground		
11	Rxin1-	LVDS Differential Data Input	Negative	G1~G5,B0,B1
12	Rxin1+	LVDS Differential Data Input	Positive	
13	GND	Ground		
14	Rxin2-	LVDS Differential Data Input	Negative	B2~B5,DE,Hsync,Vsync
15	Rxin2+	LVDS Differential Data Input	Positive	
16	GND	Ground		
17	CLK-	LVDS Clock Data Input	Negative	LVDS Level Clock
18	CLK+	LVDS Clock Data Input	Positive	
19	GND	Ground		
20	NC	No Connection		
21	NC	No Connection		
22	GND	Ground		
23	NC	No Connection		
24	NC	No Connection		
25	GND	Ground		
26	NC	No Connection		
27	NC	No Connection		
28	GND	Ground		
29	VLED	LED Converter Input Power		
30	VLED	LED Converter Input Power		
31	LED_GND	LED Ground		
32	LED_GND	LED Ground		
33	LED_GND	LED Ground		
34	NC	No Connection		
35	NC	No Connection		
36	NC	No Connection		
37	NC	No Connection		
38	ADJ	LED BLU Brightness Control (PWM)		(3)
39	ENA	LED Converter Enable		
40	NC	No Connection		

Note (1) Connector Part No.: I-PEX 20347-340E-12 or equivalent

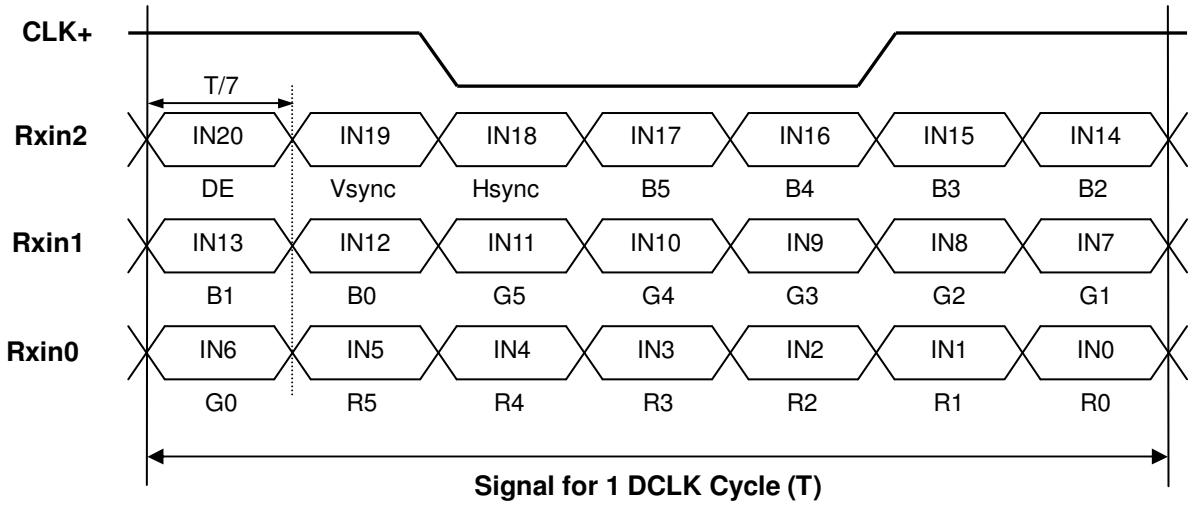
Note (2) User's connector Part No: I-PEX 20345-040T-31 or equivalent

Note (3) BLU brightness is proportion to the duty of ADJ signal.

Note (4) The first pixel is odd as shown in the following figure.



5.2 TIMING DIAGRAM OF LVDS INPUT SIGNAL



5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.5 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	TBD	TBD
1	1	Header	TBD	TBD
2	2	Header	TBD	TBD
3	3	Header	TBD	TBD
4	4	Header	TBD	TBD
5	5	Header	TBD	TBD
6	6	Header	TBD	TBD
7	7	Header	TBD	TBD
8	8	EISA ID manufacturer name (“CMO”)	TBD	TBD
9	9	EISA ID manufacturer name (Compressed ASCII)	TBD	TBD
10	0A	ID product code (N089L6-L02)	TBD	TBD
11	0B	ID product code (hex LSB first; N089L6-L02)	TBD	TBD
12	0C	ID S/N (fixed “0”)	TBD	TBD
13	0D	ID S/N (fixed “0”)	TBD	TBD
14	0E	ID S/N (fixed “0”)	TBD	TBD
15	0F	ID S/N (fixed “0”)	TBD	TBD
16	10	Week of manufacture (fixed week code)	TBD	TBD
17	11	Year of manufacture (fixed year code)	TBD	TBD
18	12	EDID structure version # (“1”)	TBD	TBD
19	13	EDID revision # (“3”)	TBD	TBD
20	14	Video I/P definition (“digital”)	TBD	TBD
21	15	Max H image size (“19.392cm”)	TBD	TBD
22	16	Max V image size (“11.53cm”)	TBD	TBD
23	17	Display Gamma (Gamma = ”2.2”)	TBD	TBD
24	18	Feature support (“Active off, RGB Color”)	TBD	TBD
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	TBD	TBD
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	TBD	TBD
27	1B	Rx=TBD	TBD	TBD
28	1C	Ry=TBD	TBD	TBD
29	1D	Gx=TBD	TBD	TBD
30	1E	Gy=TBD	TBD	TBD
31	1F	Bx=TBD	TBD	TBD
32	20	By=TBD	TBD	TBD
33	21	Wx=TBD	TBD	TBD
34	22	Wy=TBD	TBD	TBD
35	23	Established timings 1	TBD	TBD
36	24	Established timings 2	TBD	TBD
37	25	Manufacturer’s reserved timings	TBD	TBD
38	26	Standard timing ID # 1	TBD	TBD
39	27	Standard timing ID # 1	TBD	TBD
40	28	Standard timing ID # 2	TBD	TBD
41	29	Standard timing ID # 2	TBD	TBD

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
42	2A	Standard timing ID # 3	TBD	TBD
43	2B	Standard timing ID # 3	TBD	TBD
44	2C	Standard timing ID # 4	TBD	TBD
45	2D	Standard timing ID # 4	TBD	TBD
46	2E	Standard timing ID # 5	TBD	TBD
47	2F	Standard timing ID # 5	TBD	TBD
48	30	Standard timing ID # 6	TBD	TBD
49	31	Standard timing ID # 6	TBD	TBD
50	32	Standard timing ID # 7	TBD	TBD
51	33	Standard timing ID # 7	TBD	TBD
52	34	Standard timing ID # 8	TBD	TBD
53	35	Standard timing ID # 8	TBD	TBD
54	36	Detailed timing description # 1 Pixel clock (“45MHz”, According to VESA CVT Rev1.1)	TBD	TBD
55	37	# 1 Pixel clock (hex LSB first)	TBD	TBD
56	38	# 1 H active (“1024”)	TBD	TBD
57	39	# 1 H blank (“176”)	TBD	TBD
58	3A	# 1 H active : H blank (“1024 : 176”)	TBD	TBD
59	3B	# 1 V active (”600”)	TBD	TBD
60	3C	# 1 V blank (”25”)	TBD	TBD
61	3D	# 1 V active : V blank (”600 :25”)	TBD	TBD
62	3E	# 1 H sync offset (”48”)	TBD	TBD
63	3F	# 1 H sync pulse width ("32”)	TBD	TBD
64	40	# 1 V sync offset : V sync pulse width (”3 : 6”)	TBD	TBD
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width (”48: 32 : 3 : 6”)	TBD	TBD
66	42	# 1 H image size (”193 mm”)	TBD	TBD
67	43	# 1 V image size (”115 mm”)	TBD	TBD
68	44	# 1 H image size : V image size (”193 : 115”)	TBD	TBD
69	45	# 1 H boarder (”0”)	TBD	TBD
70	46	# 1 V boarder (”0”)	TBD	TBD
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	TBD	TBD
72	48	Detailed timing description # 2	TBD	TBD
73	49	# 2 Flag	TBD	TBD
74	4A	# 2 Reserved	TBD	TBD
75	4B	# 2 FE (hex) defines ASCII string (Model Name “N089L6-L02”, ASCII)	TBD	TBD
76	4C	# 2 Flag	TBD	TBD
77	4D	# 2 1st character of name (“N”)	TBD	TBD
78	4E	# 2 2nd character of name (“0”)	TBD	TBD
79	4F	# 2 3rd character of name (“8”)	TBD	TBD
80	50	# 2 4th character of name (“9”)	TBD	TBD
81	51	# 2 5th character of name (“L”)	TBD	TBD
82	52	# 2 6th character of name (“6”)	TBD	TBD
83	53	# 2 7th character of name (“-”)	TBD	TBD
84	54	# 2 8th character of name (“L”)	TBD	TBD

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
85	55	# 2 9th character of name (“0”)	TBD	TBD
86	56	# 2 9th character of name (“2”)	TBD	TBD
87	57	# 2 New line character indicates end of ASCII string	TBD	TBD
88	58	# 2 Padding with “Blank” character	TBD	TBD
89	59	# 2 Padding with “Blank” character	TBD	TBD
90	5A	Detailed timing description # 3	TBD	TBD
91	5B	# 3 Flag	TBD	TBD
92	5C	# 3 Reserved	TBD	TBD
93	5D	# 3 FE (hex) defines ASCII string (Vendor “CMO”, ASCII)	TBD	TBD
94	5E	# 3 Flag	TBD	TBD
95	5F	# 3 1st character of string (“C”)	TBD	TBD
96	60	# 3 2nd character of string (“M”)	TBD	TBD
97	61	# 3 3rd character of string (“O”)	TBD	TBD
98	62	# 3 New line character indicates end of ASCII string	TBD	TBD
99	63	# 3 Padding with “Blank” character	TBD	TBD
100	64	# 3 Padding with “Blank” character	TBD	TBD
101	65	# 3 Padding with “Blank” character	TBD	TBD
102	66	# 3 Padding with “Blank” character	TBD	TBD
103	67	# 3 Padding with “Blank” character	TBD	TBD
104	68	# 3 Padding with “Blank” character	TBD	TBD
105	69	# 3 Padding with “Blank” character	TBD	TBD
106	6A	# 3 Padding with “Blank” character	TBD	TBD
107	6B	# 3 Padding with “Blank” character	TBD	TBD
108	6C	Detailed timing description # 4	TBD	TBD
109	6D	# 4 Flag	TBD	TBD
110	6E	# 4 Reserved	TBD	TBD
111	6F	# 4 FE (hex) defines ASCII string (Model Name“N089L6-L02”, ASCII)	TBD	TBD
112	70	# 4 Flag	TBD	TBD
113	71	# 4 1st character of name (“N”)	TBD	TBD
114	72	# 4 2nd character of name (“0”)	TBD	TBD
115	73	# 4 3rd character of name (“8”)	TBD	TBD
116	74	# 4 4th character of name (“9”)	TBD	TBD
117	75	# 4 5th character of name (“L”)	TBD	TBD
118	76	# 4 6th character of name (“6”)	TBD	TBD
119	77	# 4 7th character of name (“-”)	TBD	TBD
120	78	# 4 8th character of name (“L”)	TBD	TBD
121	79	# 4 9th character of name (“0”)	TBD	TBD
122	7A	# 4 9th character of name (“2”)	TBD	TBD
123	7B	# 4 New line character indicates end of ASCII string	TBD	TBD
124	7C	# 4 Padding with “Blank” character	TBD	TBD
125	7D	# 4 Padding with “Blank” character	TBD	TBD
126	7E	Extension flag	TBD	TBD
127	7F	Checksum	TBD	TBD

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

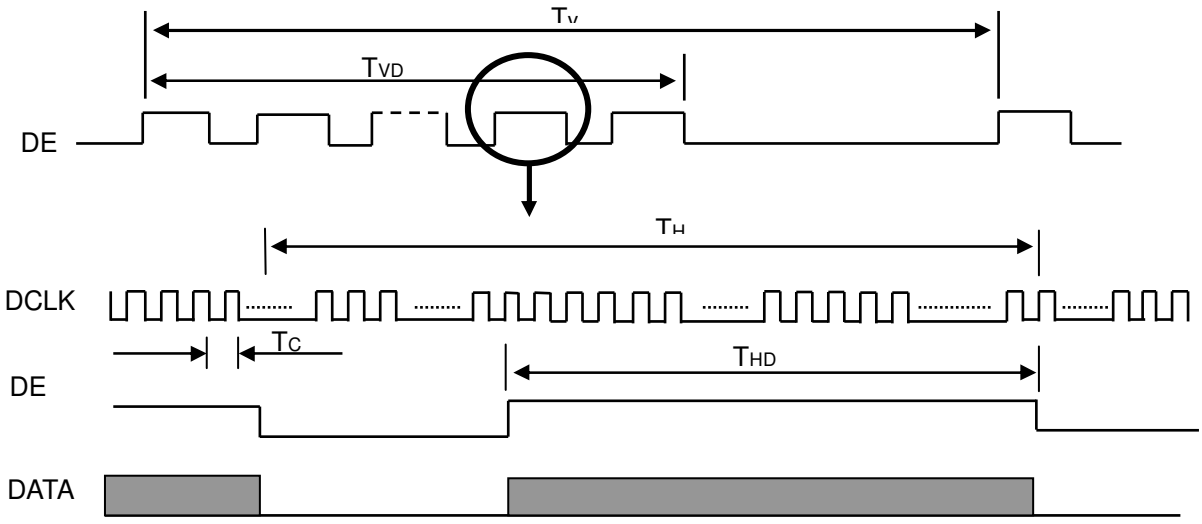
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	TBD	(45)	TBD	MHz	-
DE	Vertical Total Time	TV	TBD	(625)	TBD	TH	-
	Vertical Active Display Period	TVD	TBD	600	TBD	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	(25)	TV-TVD	TH	
	Horizontal Total Time	TH	TBD	(1200)	TBD	Tc	(2)
	Horizontal Active Display Period	THD	TBD	1024	TBD	Tc	(2)
	Horizontal Active Blanking Period	THB	TH-THD	(176)	TH-THD	Tc	(2)

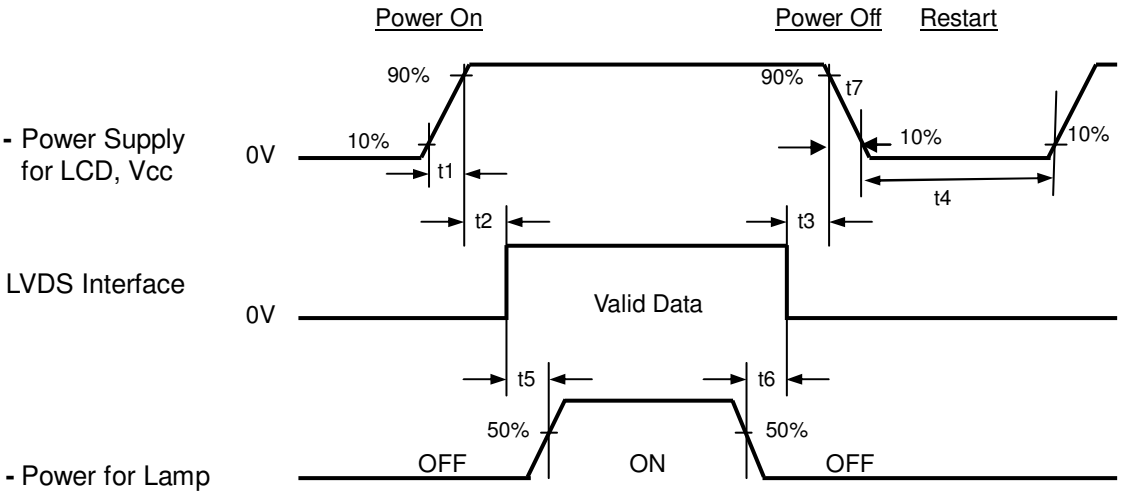
Note (1) Because this module is operated by DE only mode, Hsync and Vsync are ignored.

(2) 1 channel LVDS input.

INPUT SIGNAL TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE



Timing Specifications:

0.5 < t1 ≦ 10 ms

0 < t2 ≦ 50 ms

0 < t3 ≦ 50 ms

t4 ≧ 500 ms

t5 ≧ 200 ms

t6 ≧ 200 ms

Note (1) Please follow the power on/off sequence described above. Otherwise, the LCD module might be damaged.

Note (2) Please avoid floating state of interface signal at invalid period. When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time is better to follow 5≦t7≦300 ms.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

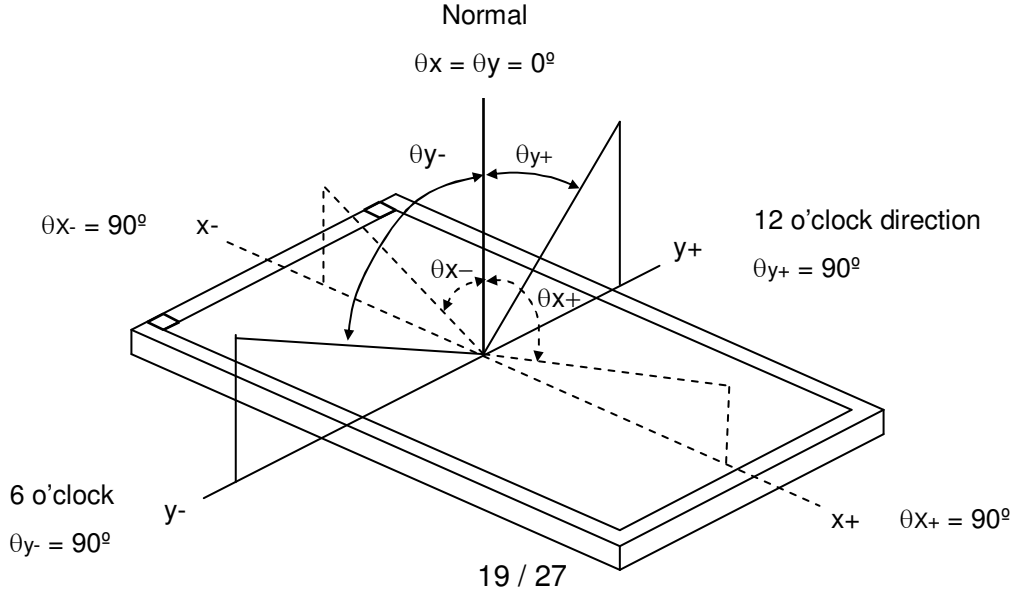
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I_L	6.0	mA
Inverter Driving Frequency	F_L	61	KHz
Inverter	Sumida-H05-4915		

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (5).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	200	300	-	-	(2), (5)
Response Time		T_R		-	3	5	ms	(3)
		T_F		-	7	11	ms	
Average Luminance of White		L_{5p}		150	200	-	cd/m^2	(4), (5)
Luminance Non-Uniformity		δW_{5p}		-	-	1.4		(5), (6)
Color Chromaticity	Red	Rx		TYP -0.05	TBD	TYP +0.05	-	(1), (5)
		Ry			TBD		-	
	Green	Gx			TBD		-	
		Gy			TBD		-	
	Blue	Bx			TBD		-	
		By			TBD		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	40	45	-	Deg.	
		θ_x-		40	45	-		
	Vertical	θ_Y+		15	20	-		
		θ_Y-		40	45	-		

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

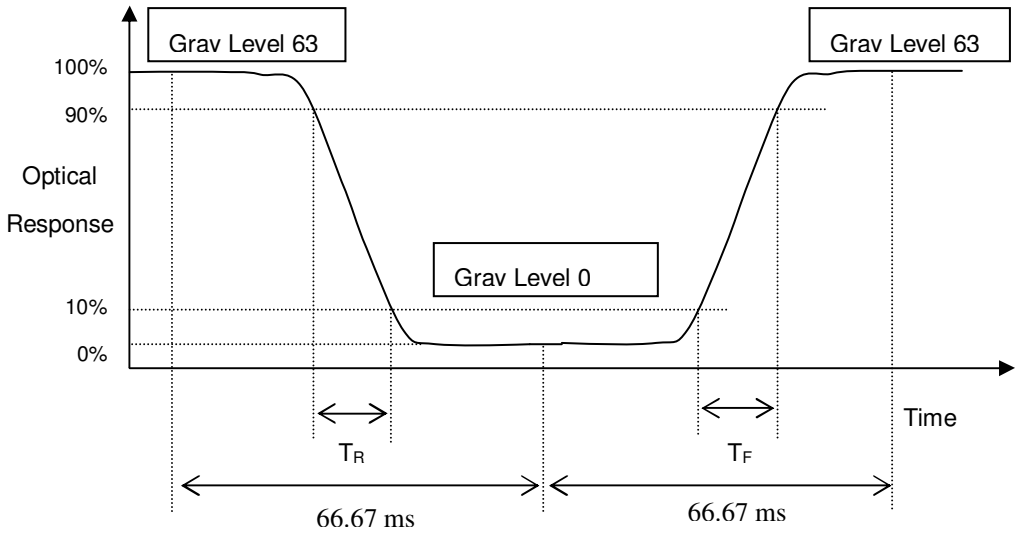
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

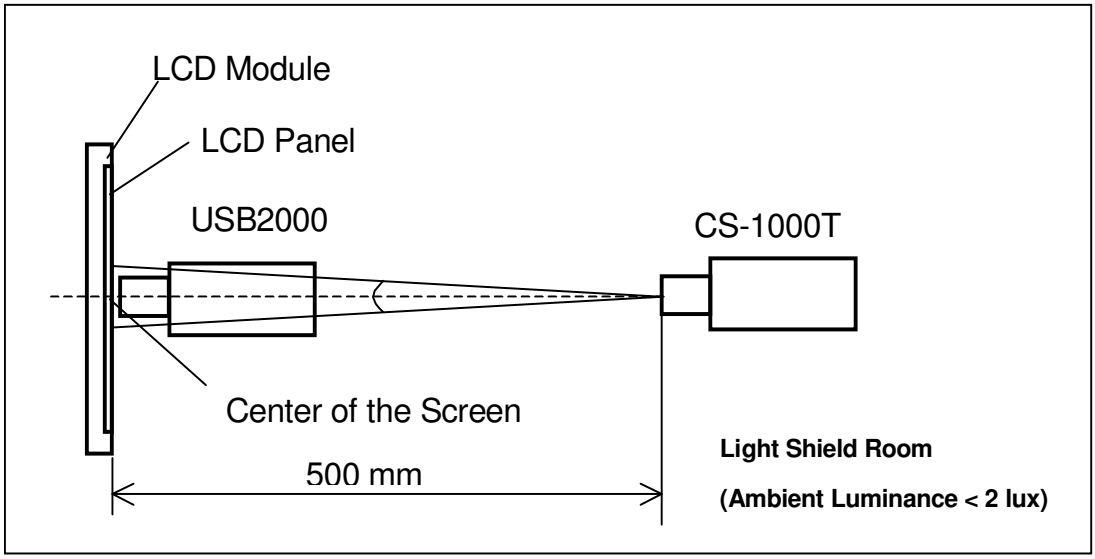
Measure the luminance of gray level 63 at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

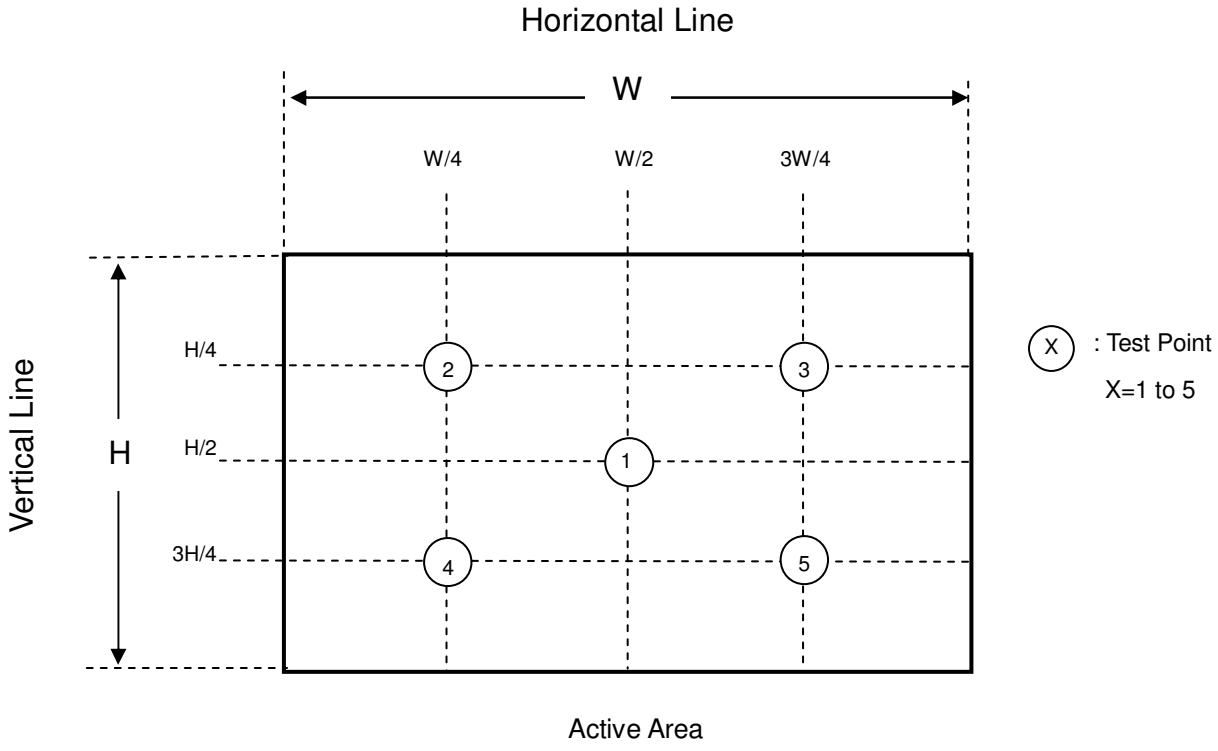
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

δW = { Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. PRECAUTIONS

8.1 SYSTEM MATCHING PRECAUTIONS

(1) Refer to the drawing.

(2) To avoid wireless noise interference, please keep the antenna away from LCD control board.

8.2 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the lamp wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.3 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

8.4 OPERATION PRECAUTIONS

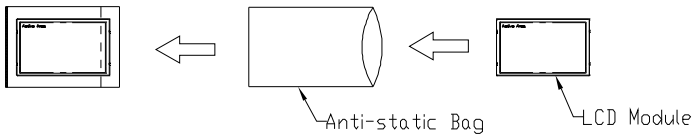
(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

9. PACKING

9.1 CARTON



Box Dimensions: 575(L)*380(W)*300(H) mm
Weight: Approx. 11.63kg (50 module .per. 1 box)

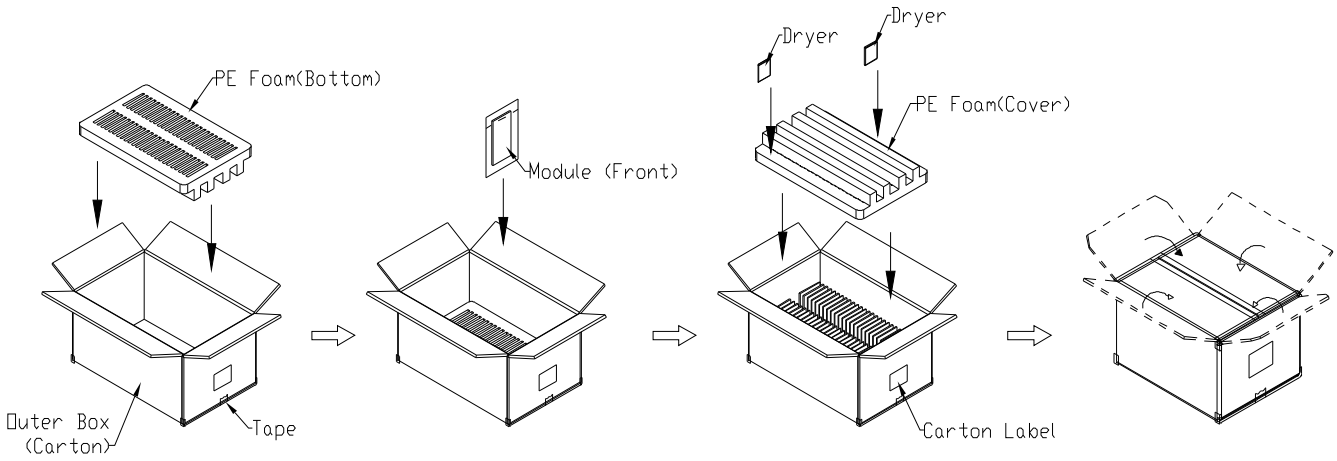


Figure. 9-1 Packing method

9.2 PALLET

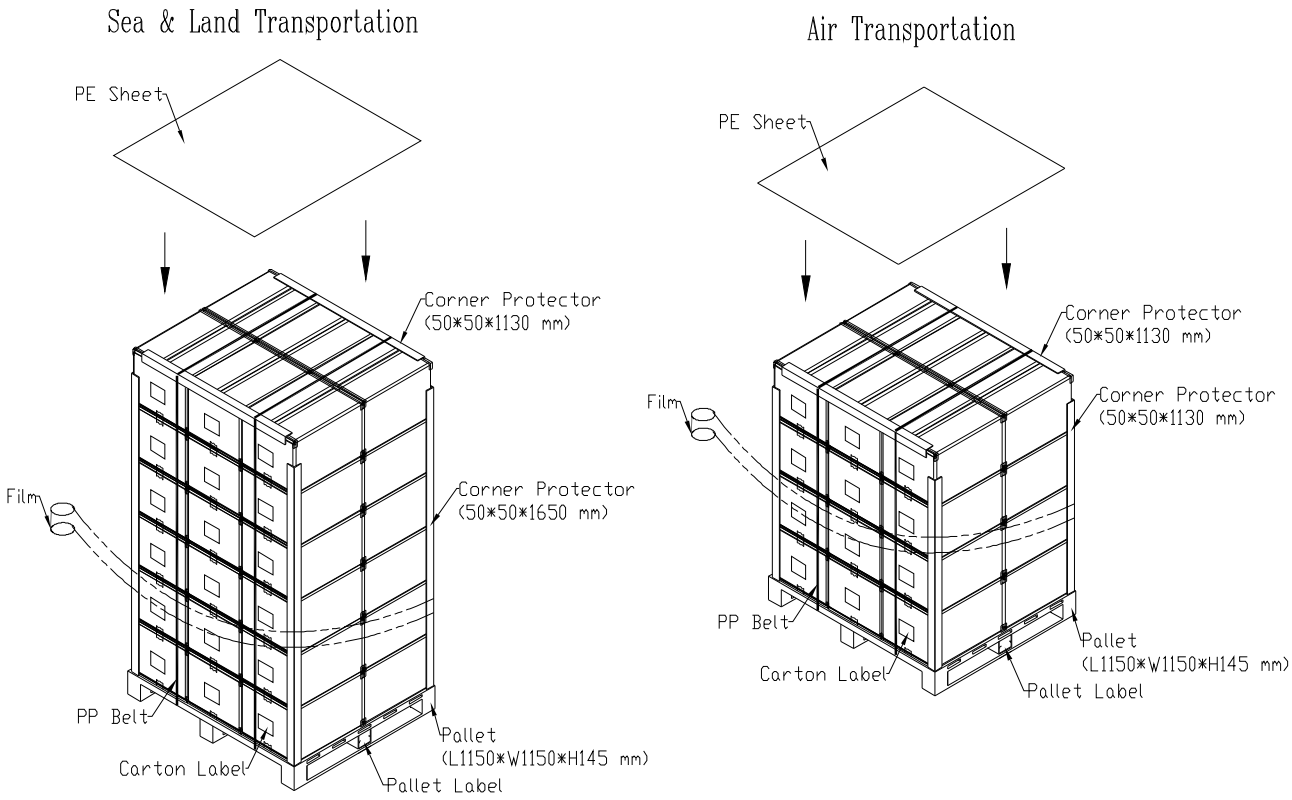
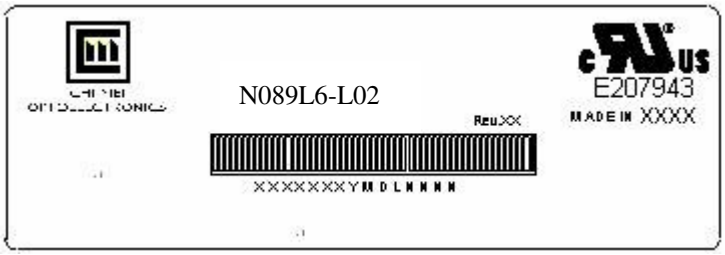


Figure. 9-2 Packing method

10. DEFINITION OF LABELS

10.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: N089L6 - L02

(b) Revision: Rev. XX, for example: A1, …, C1, C2 …etc.

(c) Serial ID: X X X X Y M D X N N N N

- Serial No.
- CMO Internal Use
- Year, Month, Date
- CMO Internal Use
- Revision
- CMO Internal Use

(d) Production Location: MADE IN XXXX. XXXX stands for production location.

(e)UL logo: LEOO especially stands for panel manufactured by CMO NingBo satisfying UL requirement. The panel without LEOO mark stands for manufactured by CMO Taiwan satisfying UL requirement.

Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

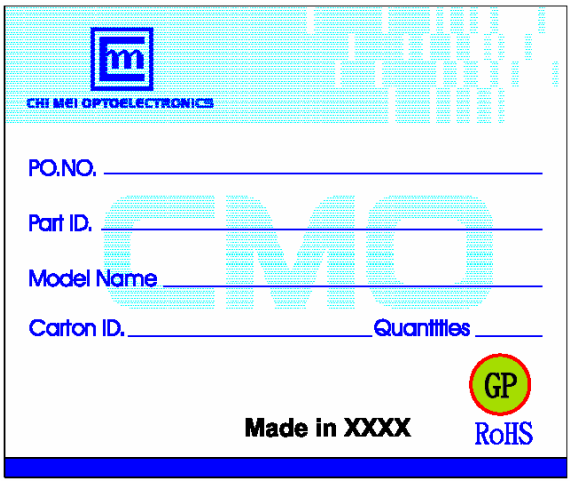
Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

10.2 CMO CARTON LABEL



(a) Production location: Made In XXXX. XXXX stands for production location.