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EPSON
EPSON AMERICA, INC.
OEM Products Division

SPECIFICATIONS

REF
DATE
PAGE OF
REV.

To Gordon Frye
From Pat Stanton

E G 7 5 0 0 B - L S
(BLUE & WHITE) - N S -1 -2

AND

E G 7 5 0 0 D - L S
(BLACK & WHITE) - N S -1 -2

LCD MODULE FOR 320 X 200 DOTS

Post-it® Fax Note 7671	Date 6.25.98	# of pages ▶ 26
To Pat	From Renee Osborne	
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1. DESCRIPTION

The Epson EG7500*-LS Displays are 320 X 200 graphic modules with fluorescent backlights and 6:00 o'clock viewing angles. The EG7500B is a negative blue super-twist display with white pixels. The EG7500D is a film-compensated super-twist (FTN),display with a negative black background and white pixels.

The Displays utilize chip-on-flex drivers for minimum overall size, weight and cost. These Displays are recommended for P.O.S. terminals, medical equipment, and any application where a small CRT might be used.

1.1 FEATURES

1) Large-scale CMOS drivers, bonded to flexible circuits.

2) Dot addressable, 320 X 200 graphics module.

3) Four bit parallel, data transfer mode.

4) Negative type displays with super-twist fluid.

5) EG7500D has a film, color-compensation layer.

6) Transmissive operating mode.

7) Removable, cold cathode fluorescent back-light assembly.

8) 1/200 duty multiplexed drive scheme

9) Colors:

	EG7500B	EG7500D
Background.....	Blue	Black
Display Dots.....	White	White

10) Viewing Angle: 6:00 o'clock (standard)
12:00 o'clock (optional)
(P/N = EG7500*-NS)

11) INVERTER OMITTED (-1 OR -2) (3 TINNED WIRES)

2. MECHANICAL SPECIFICATIONS

Item	Specifications
Dot matrix	320 x 200 DOTS
Overall dimensions (L x W x D)	164.0 x 143.0 x 25.0 (without mounting TABS)
Viewing area (L x W)	128.0 x 110.0
Active area (L x W)	121.5[illegible] x 103.98
Dot pitch (L x W)	0.38 x 0.52
Dot size (L x W)	0.34 x 0.48
Weight	Approx 500 (g)

Unit : mm

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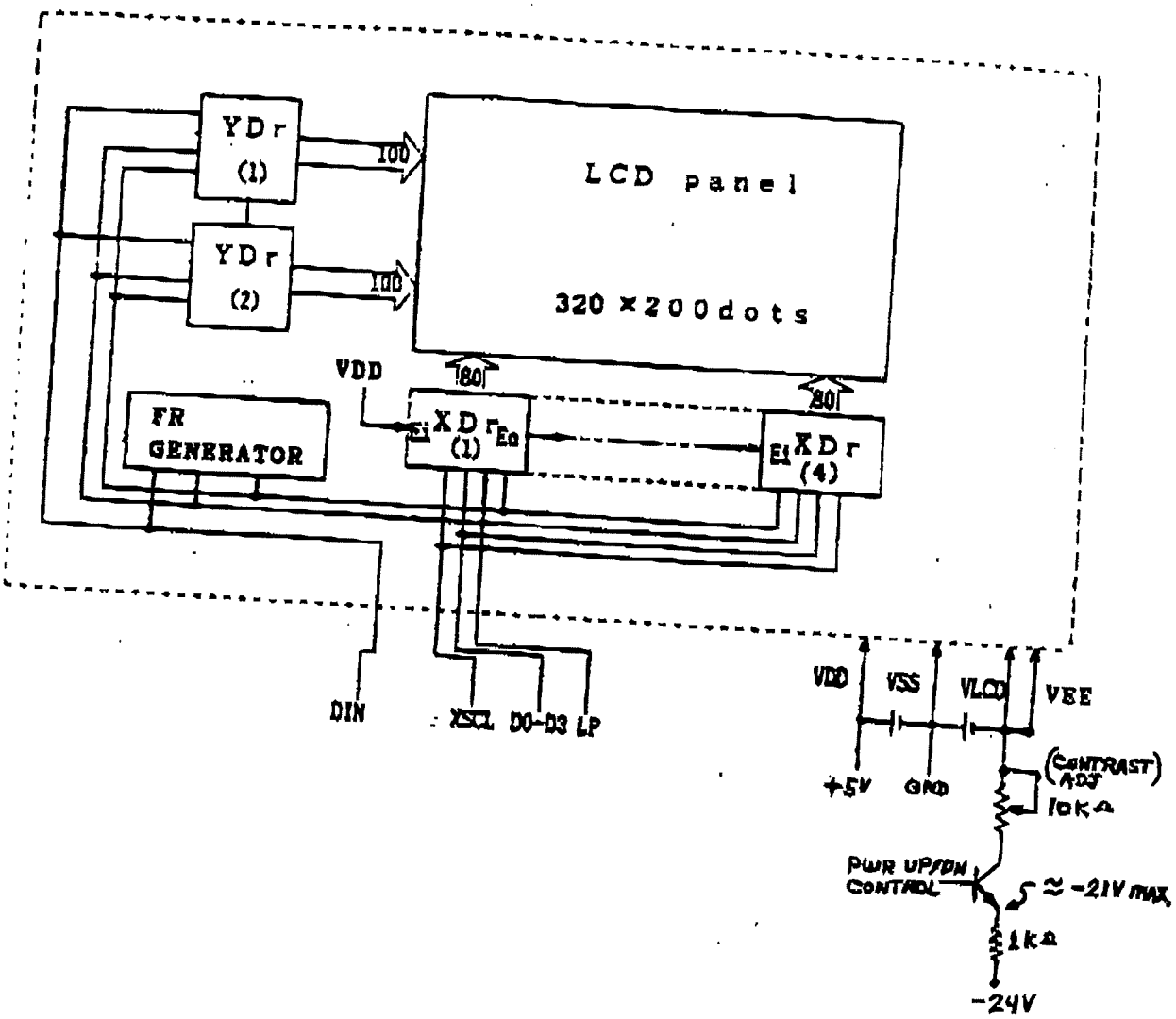
3. BLOCK DIAGRAM



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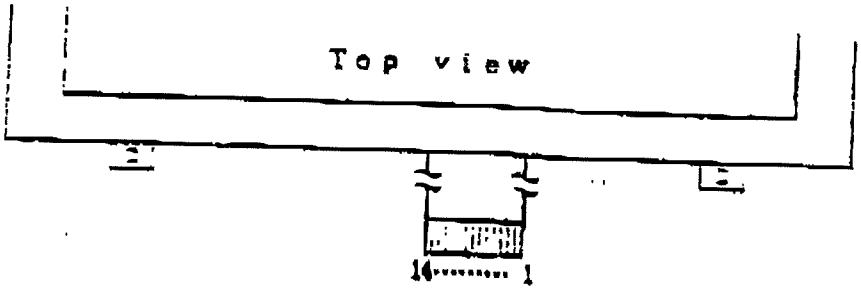
4. I/O TERMINALS

4.1 Terminal Configuration



4.2 Terminal Functions

NO.	SYMBOL	NAME	FUNCTION
1	VDD	POWER SUPPLY	+5V ±5%
2	VSS	GND	0V
3	VEE	POWER SUPPLY	−20V TO −22V (ABSOLUTE MAX = −23V)
4	VLCD	CONTRAST VOLTAGE FOR LCD PANEL	−14V TO −22V
5	NC	NO CONNECTION	
6	LP	LATCH PULSE	DATA LATCH SIGNAL
7	NC	NO CONNECTION	
8	NC	NO CONNECTION	
9	DIN	SYNCHRONIZING PULSE	ROW SCAN START-UP PULSE
10	XSCL	X SHIFT CLOCK	DATA SHIFT CLOCK
11 – 14	D0 ~ D3	DATA	DISPLAY DATA INPUT

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5. DATA INPUT FORMAT

(320 x 200 dots)

5.1. Display Dot Map

Column → / Row ↓	1 D	2 D	3 D	4 D	5 D	6 D		318 D	319 D	320 D
1 D	1.1	1.2	1.3	1.4	1.5	1.6		1.318	1.319	1.320
2 D	2.1	2.2	2.3	2.4	2.5	2.6		2.318	2.319	2.320
3 D	3.1	3.2	3.3	3.4	3.5	3.6		3.318	3.319	3.320
⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮
198 D	198.1	198.2	198.3	198.4	198.5	198.6		198.318	198.319	198.320
199 D	199.1	199.2	199.3	199.4	199.5	199.6		199.318	199.319	199.320
200 D	200.1	200.2	200.3	200.4	200.5	200.6		200.318	200.319	200.320

The previous display dot map shows the entry order of data in terms of dots on the LCD.
Display data is sequentially entered in D0~D3 on a 4 bits basis, from left to right, beginning with location "1.1".
This display from 1.1 ~ 1.4, 1.5 ~ 1.8, ... to 1.320 on a 4 dots (bits) basis.
This completes input of data on the first line (row no.1) followed by entry on the second line, the third line ....

5.2 Correspondence of Data Input Terminals to Dot Numbers in a Row

Data Input Terminal	Dots (Row) on Display
D0	dot 4, dot 8 ..... dot 316, dot 320
D1	dot 3, dot 7 ..... dot 315, dot 319
D2	dot 2, dot 6 ..... dot 314, dot 318
D3	dot 1, dot 5 ..... dot 313, dot 317

Input data D0~D3 correspond to display dots as shown above. The first input data corresponds to dot 4~1, and the last input data to dot 317~320.

5.3 Data Input Method

This module uses 'Chip Enable Transmission System" to reduce its power consumption. Data is inputted directly into LCD drivers (chips) on a chip basis. If the n-th chip in enable state becomes full of data, the Enable is transmitted by automaticaly to (n+1)th chip.

Supplying a total of 200 lines with data (one line consisting of 320 dots, equivalent to 4 chips) causes the viewing area of display to become full of data.

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6. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Standard Value	Unit
Supply voltage	VDD	0 ~ +7	V
	* VEE	VDD-VEE= 28 MAX	
	* VLCD	VDD-VLCD=28 Max	
Input voltage	VIN	VSS≦VIN≦VDD	V
Operating temperature	Top	0 ~ +50 Without Back light	°C
Storage temperature	Tst	-20 ~ +60	

* $V_{EE_{MAX}}$ and $V_{LCD_{MAX}} = (V_{DD} - 28)$

IF V_{DD}= +5V ; THEN $V_{LCD_{MAX}}$ = −23V

IF. V_{DD} = +6V; THEN $V_{LCD_{MAX}}$ = −22V

[DISPLAY DAMAGE CAN OCCUR IF THESE ABSOLUTE RATINGS ARE EXCEEDED.]

7. ELECTRICAL CHARACTERISTICS

7.1 DC Characteristics

Ta=5~40°C
VDD=5V±5%, VSS=0V

Parameter	Symbol	Standard value			Unit	Condition
		Min	Typ	Max		
Supply voltage (Logic)	VDD	4.75	5	5.25	V	VDD
Supply voltage (LCD)	VEE		-	VDD-28	V	VEE
LCD control voltage	VLCD	VDD-20	-	VDD-25	V	VLCD
"High" input voltage	VIH	0.8VDD	-	VDD	V	
"Low" input voltage	VIL	0	-	0.2VDD	V	
"High" input leakage current	IIH	-	-	20	uA	LP, DIN XSCL D0~D3
"Low" input leakage current	IIL	-	-	-20	uA	
Input capacitance	CI	-	-	220	pF	
Supply current (Logic)	IDD	-	5.5	13.5	mA	VDD .VDD = 5V * .fF = 75Hz
Supply current (LCD)	IEE	-	3.0	8.0	mA	VEE .VDD = 5V * .fF = 75Hz
Power consumption	PC	-	78.5	203.5	mW	.VDD = 5V * .fF = 75Hz

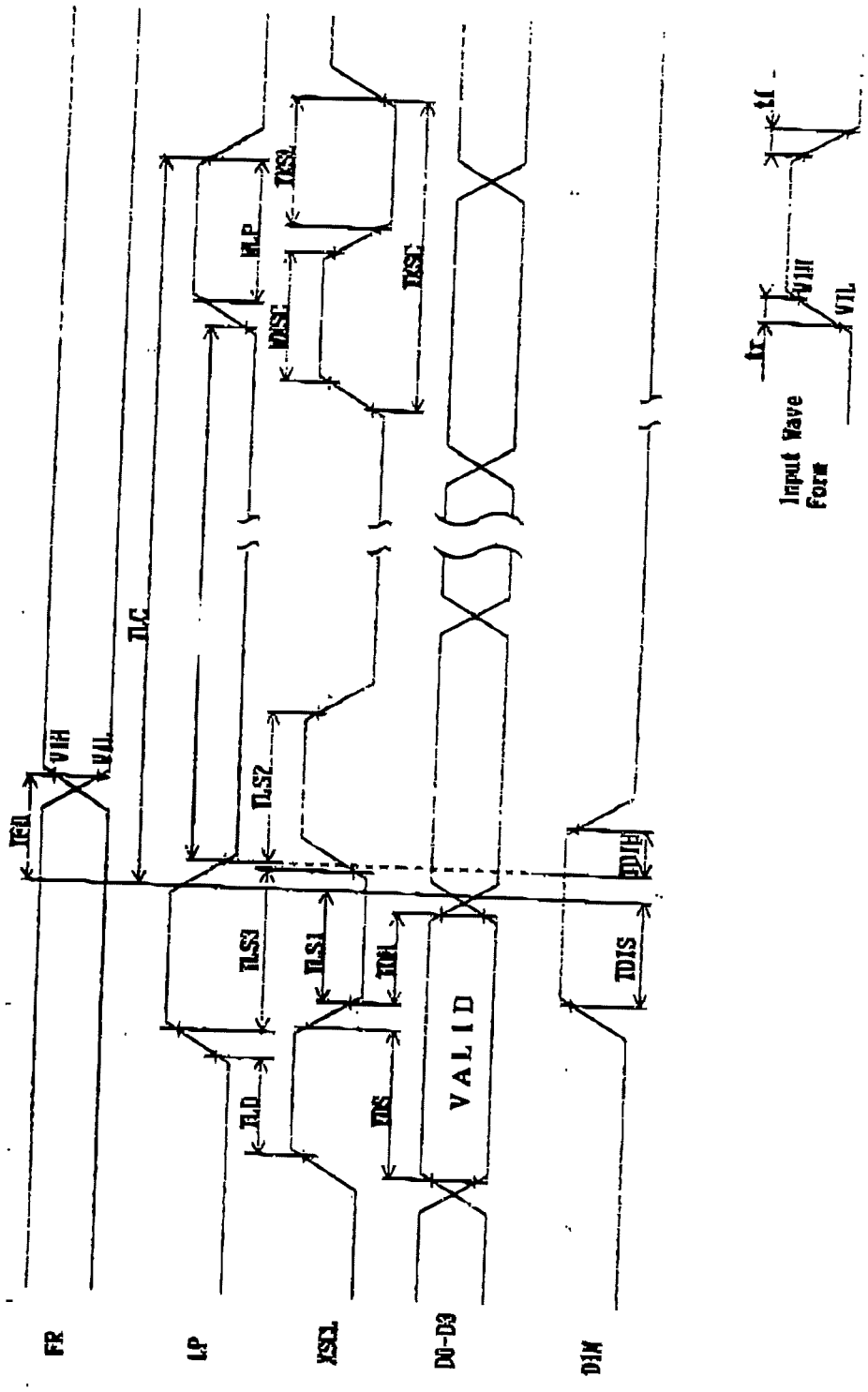
* VLCD=VDD-22V

7.2 AC Characteristics

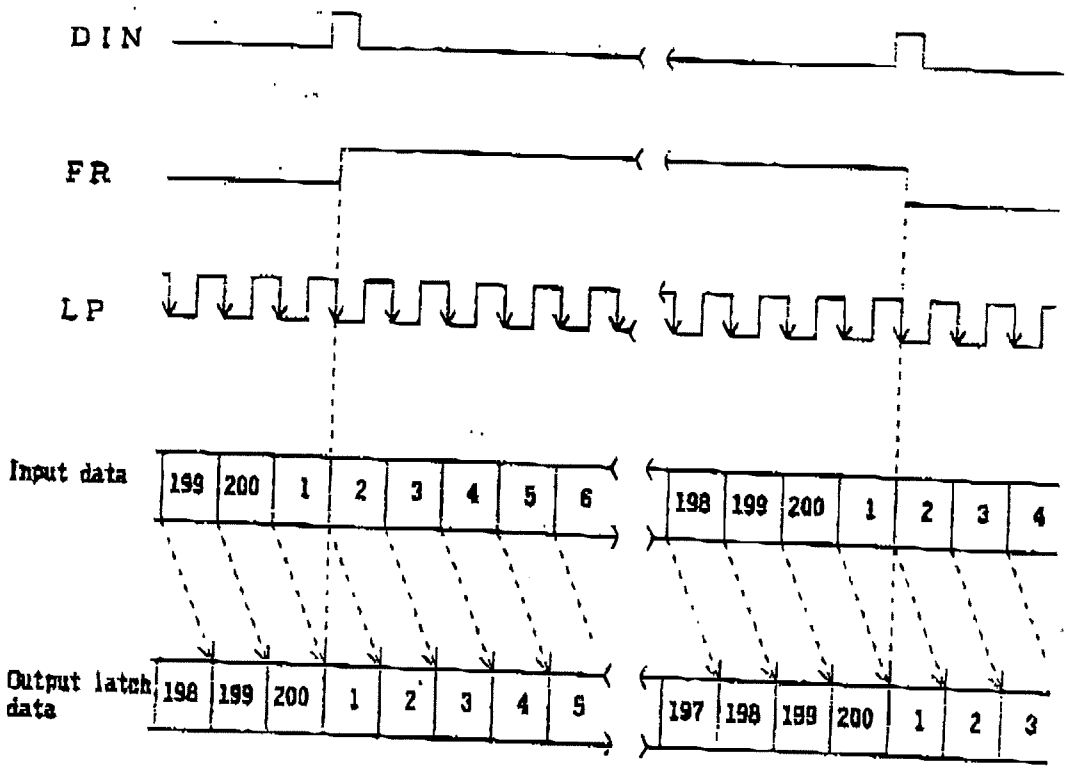
Parameter	Symbol	Standard value			Unit	Condition
		Min	Typ	Max		
FR delay time	TFD	-500	0	500	ns	VDD=5V±5%
LP period	TLC	-	57	-	us	
XSCL period	TXSC	165	-	-	ns	
LP "L" time	TLL	330	-	-	ns	
LP pulse width	WLP	70	-	-	ns	
XSCL "L" time	TXSL	70	-	-	ns	
XSCL pulse width	WXSC	70	-	-	ns	
Latch timing	TLS1 TLS2 TLS3 TLD	70 70 70 0	- - - -	- - - -	ns	
Data setup time	TDS	60	-	-	ns	
Data hold time	TDH	40	-	-	ns	
DIN setup time	TDIS	100	-	-	ns	
DIN hold time	TDIH	10	-	-	ns	
Rise & Fall time	tr,tf	-	-	*	ns	

* (TXSC-TXSL-WXSC)/2 with 50 ns Max.

7.2.1 Timing Chart of X(Column) Driver and Y(Row) Driver

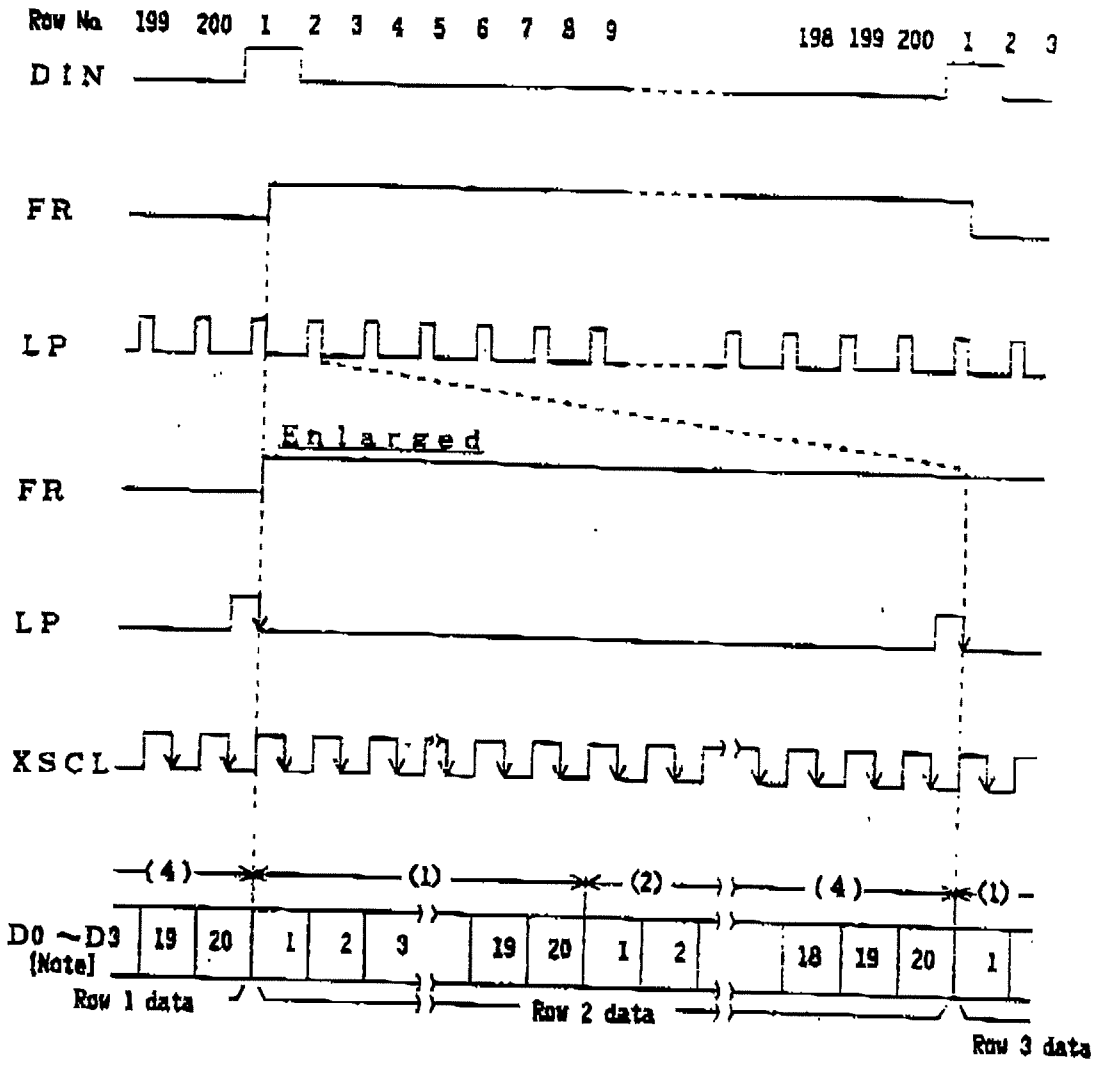


7.2.2 Relation of Input data/Output latch data



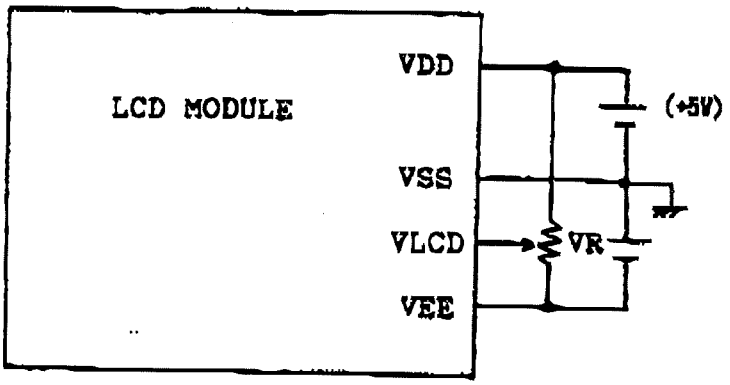
(Note)"1,2,—,199,200"indicate row numbers.

7.2.3 Timing C ·t of Input Signals



[Note 1] '(1) to (4)' of D0-D3 indicate driver chip numbers.
[Note 2] In the display, D0 to D3 are located from right to left.

8. POWER SUPPLY AND CONTRAST ADJUSTMENT



VR : Variable resistor for contrast adjustment .

Display contrast of an LCD module depends on the voltage spplied between the VDD and VLCD.
Optimum display contrast can be obtained by adjusting the VLCD voltage to set a proper LCD driving voltage.

9. Optical Characteristics

9.1 LCD Driving Conditions

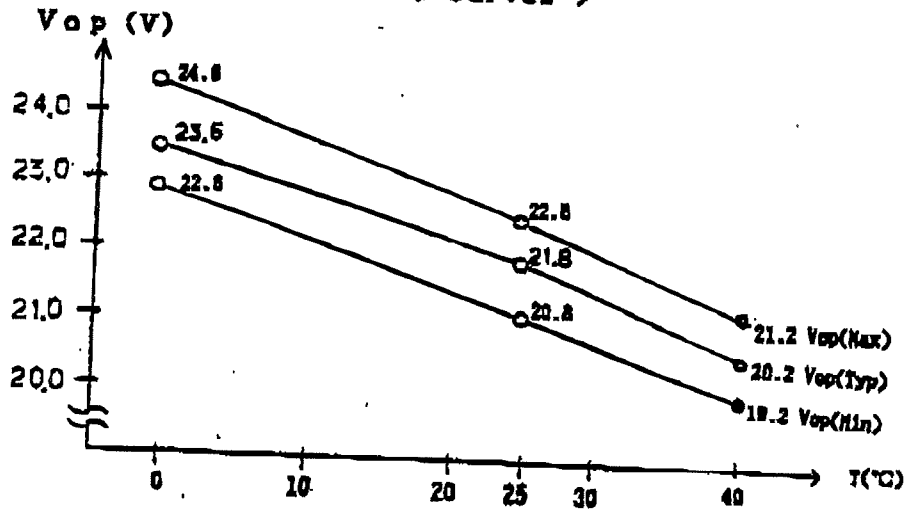
(Ta=25°C)

Item	Voltage	Duty	Bias
Standard	21.8 V	1/200	1/13

9.2 Optoelectrical Characteristics

No	Parameter	Symbol	Temperature (°C)	Standard value Min	Typ	Max	Unit	
1	Driving Voltage VDD - VLCD	Vop	0	22.6	23.6	24.6	V	Note 1
			25	20.8	21.8	22.8		Note 4
			40	19.2	20.2	21.2		
2	Response Time	Tr	0	--	600	850	ms	Note 2
			25	--	200	400		
		Tf	0	--	600	850		
			25	--	200	400		
3	Viewing Area EG7500M	θY1	25	35	--	--	DEG	Note 3
		θY2		-20	--	--		
		θX1		30	--	--		
		θX2		30	--	--		
	Viewing Area EG7500D	θY1	25	25	--	--	DEG	Note 3
		θY2		-20	--	--		
		θX1		30	--	--		
		θX2		30	--	--		
4	Contrast Ratio EG7500M	K	25	--	6	--		Note 4
	Contrast Ratio EG7500D	K	25	--	10	--		Note 4

** < Vop vs. Temperature Curves >



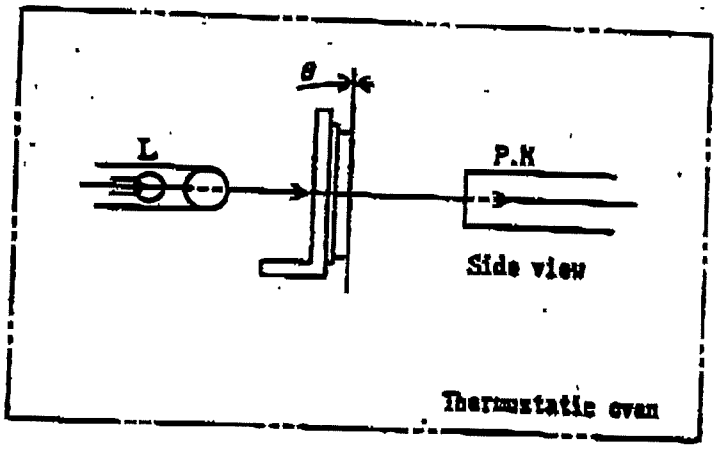
[Note 1] Optical Measuring Equipment

Equipment : Canon LC-3S brightness meter
Halogen lamp used as light source

Conditions : Spot for brightness measurement 0.3 mm
Spot from light source 10 mm

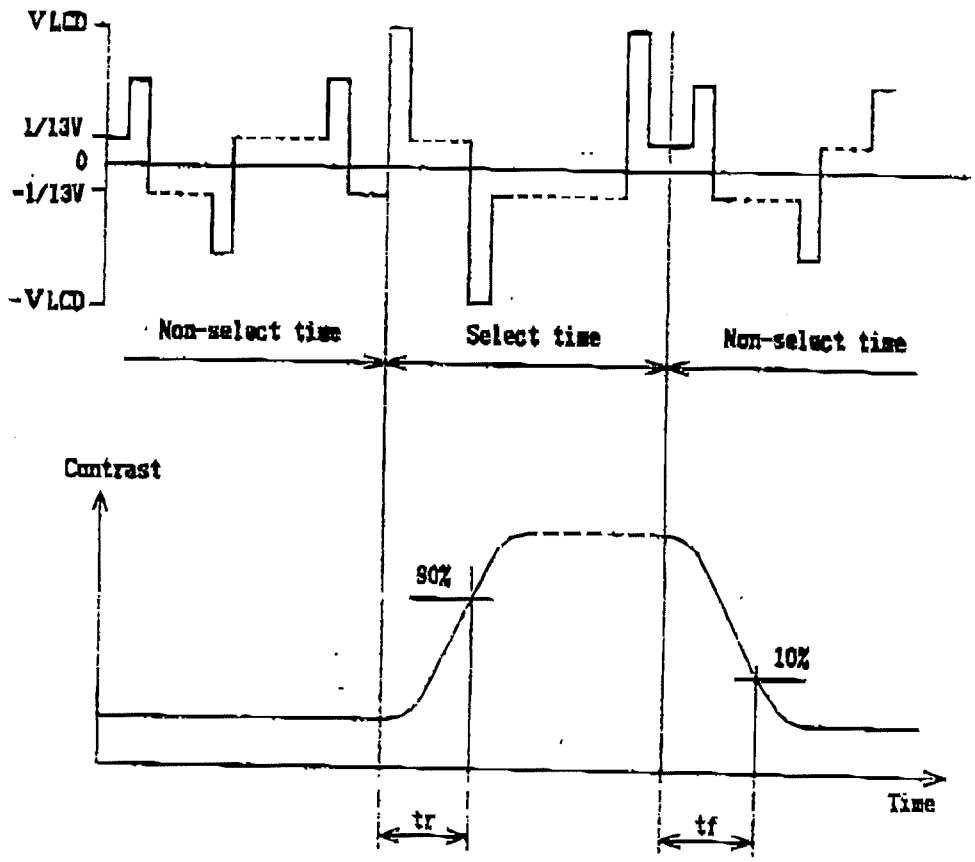
L : Light source
P.M: Light receiver of brightness meter

Fig. 1



[Note 2] Definition of response time and measuring conditions

Fig. 2



Parameter	Conditions
a) Ambient temperature	0 °C , 25 °C
b) Driving voltage	23.6 V , 21.8 V
c) Viewing angle	0 °
d) Frame frequency fF	75 Hz

[Note 3] Definition of viewing angle

Fig. 3-1

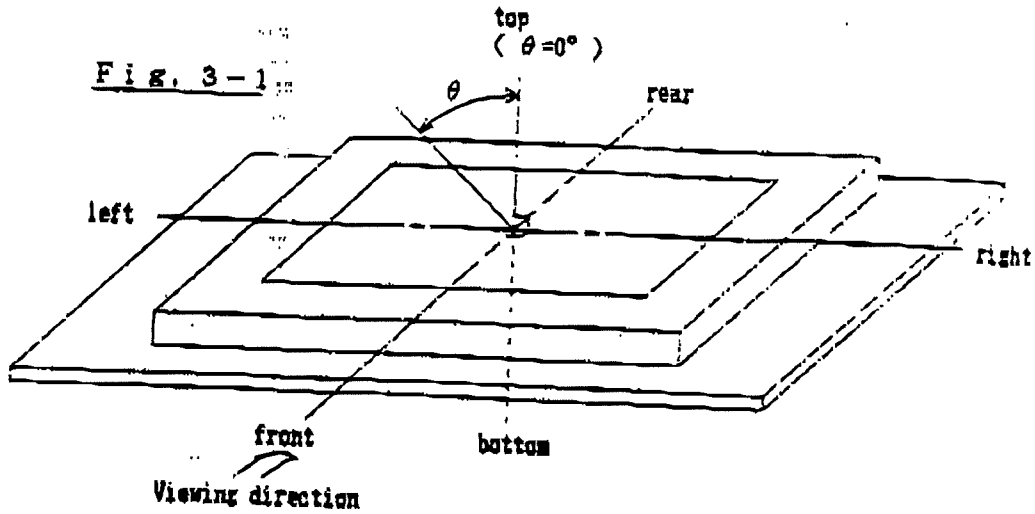
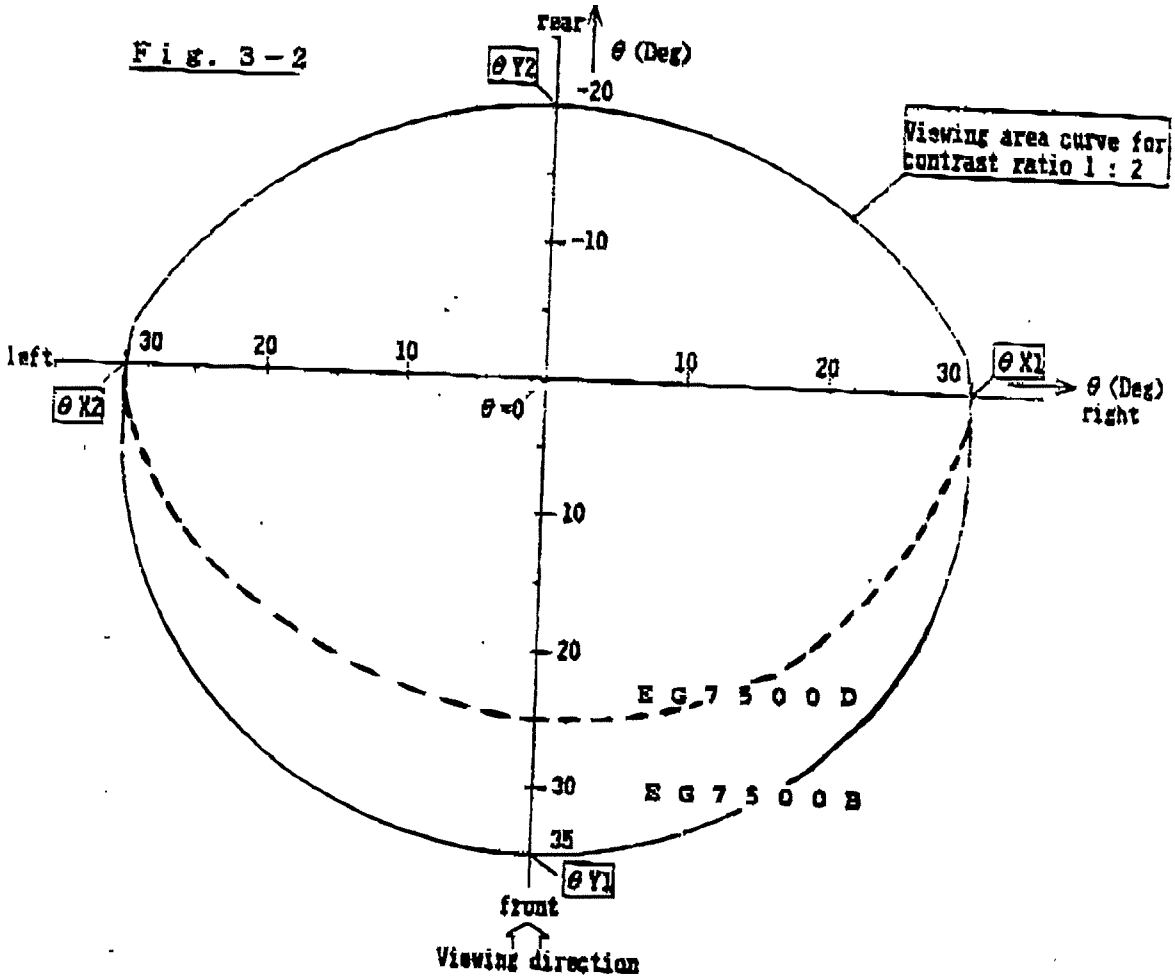


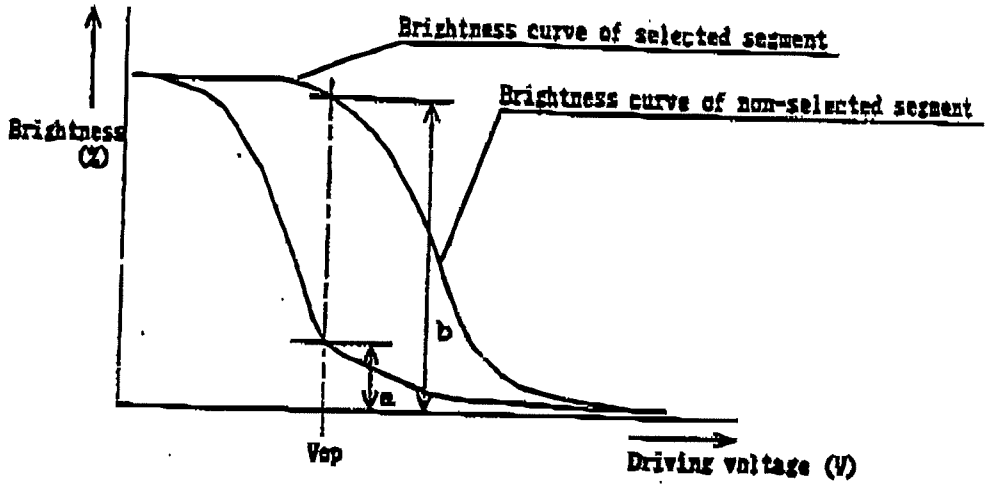
Fig. 3-2



Definition : Viewing area which gets contrast ratio 1 : 2, when operated by Vop (Typical) at 25°C .

[Note 4] Definition of contrast ratio

Fig. 4



Definition :

Contrast ratio = (Brightness in OFF state) / (Brightness in ON state) = b/a

Parameter	Conditions
a) Ambient temperature	25 °C
b) Driving voltage	21.8 V
c) Viewing angle	0 °

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10. HANDLING PRECAUTIONS

(1) The LCD panel of EPSON LCD modules consists of two thin glass plates with polarizers (with UV cut filters) which easily get damaged. Extreme care should be used when handling the display panel.

(2) When cleaning the display surface, use soft cloth (e.g., gauze) with a solvent (recommended below) and wipe lightly.

- isopropyl alcohol
- ethyl alcohol
- trichlorotrifloroethane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvents:
- water
- ketone
- aromatics

(3) The LCD modules use CMOS LSI drivers, so we recommend that you:

a) connect any unused input terminal to VDD or VSS;
b) do not input any signals before power is turned on; and
c) ground your body, work/assembly areas, and assembly equipment to protect against static electricity.

(4) Modules employ LCD elements, and must be treated as such. Avoid intense shock and falls from a height.

(5) To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

11. OPERATIONAL PRECAUTIONS

(1) If the LCD panel is driven on DC, the electrochemical reaction within it causes a rapid reduction in display performance. The duty 50%±1% of the FR signal must always be observed.

(2) Follow the power on/off sequence shown in Fig. 1 to prevent a latch-up or DC operation of the LCD module.

(3) No LCD module must exceed the absolute maximum ratings. If a module is operated with any value exceeding absolute maximum ratings, its performance will deteriorate and may no longer restore to normal.
In designing a system using LCD modules, utmost care should be taken of ambient temperature, input voltage signal fluctuations, supply voltage fluctuations, etc.

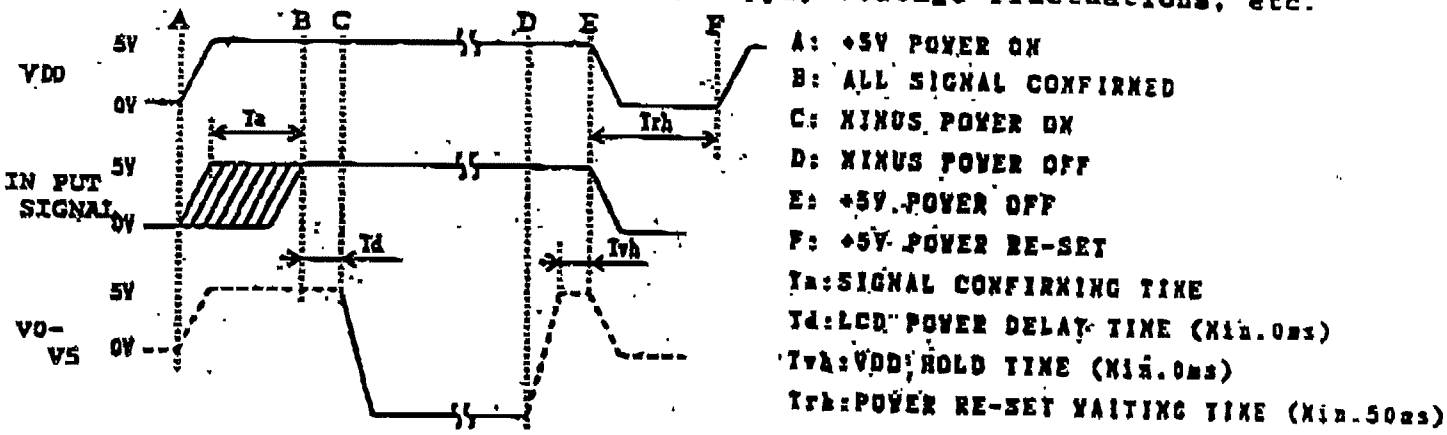

Fig. 1 Power On/Off Sequence

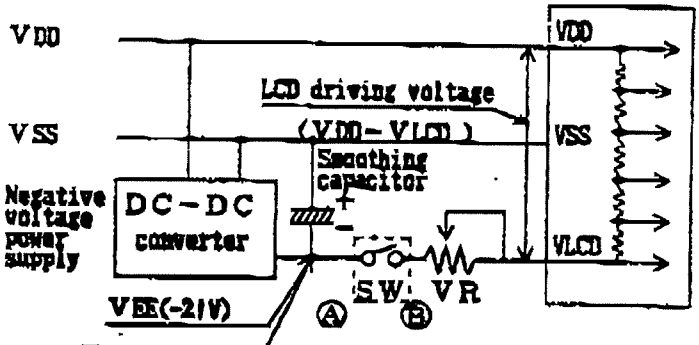

Fig. 2 Typical Power Supply Connection

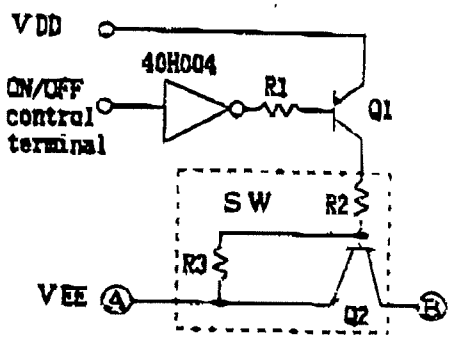

Fig. 3 Typical SW Circuit

[Note 1] The VLCD on/off operation shown in Fig. 1 indicates the swiching operation of Fig. 2.
[Note 2] Turning off the SW (Fig. 2) will open the VLCD terminal. Therefore, the LCD driveng voltage (VDD-VLCD) will become zero 100ms(Max.) later.
[Note 3] A typical circuit for the SW portion of Fig. 2 is given in Fig. 3 for reference.

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12. SPECIFICATION OF BACK LIGHT INVERTER

PARAMETER	SYMBOL	STANDARD VALUE			UNIT	CONDITION
		MIN	TYP	MAX		
SUPPLY VOLTAGE	VDB	21.6	24.0	26.4	V	NOTE 1
SUPPLY CURRENT	IDB	-	0.11	0.22	A	NOTE 1
OUTPUT VOLTAGE (Starting State)	VOB		1060		Vrms	NOTE 1
OUTPUT VOLTAGE (Stable State)	VOB		300		Vrms	NOTE 1
OUTPUT CURRENT (One Tube)	IOB		4.0		mA/AC	NOTE 1
OUTPUT FREQUENCY	FOB	20	25	30	KHz	NOTE 1

13. SPECIFICATION OF BACK LIT UNIT

PARAMETER	SYMBOL	STANDARD VALUE			UNIT	CONDITION
		MIN	TYP	MAX		
SUPPLY VOLTAGE (Starting State)	VCFL		1060		Vrms	NOTE 1
SUPPLY VOLTAGE (Stable State)	VCFL		300		Vrms	NOTE 1
SUPPLY CURRENT (One Tube)	ICFL	3	4	5	mA/AC	NOTE 1
OPERATING FREQUENCY	FCFL	20	25	30	KHz	NOTE 1
LUMINOUS WAVE LENGTH OF CFL	a	435,545,610			nm	PEAK WAVE LENGTH *1
CFL LIFE TIME		10,000			HOUR	NOTE 2
OPERATING TEMPERATURE	TOPR	5		50	°C	NOTE 3
STORAGE TEMPERATURE	TSTG	-20		60	°C	
OPERATING HUMIDITY	HOPR	30		85	%RH	*2
STORAGE HUMIDITY	HSTG	20		90	%RH	*2
INITIAL ILLUMINATION OF B/L UNIT		--	600	--	cd/m^2	NOTE 4

*1 - CFL *2 - NOT CONDENSED

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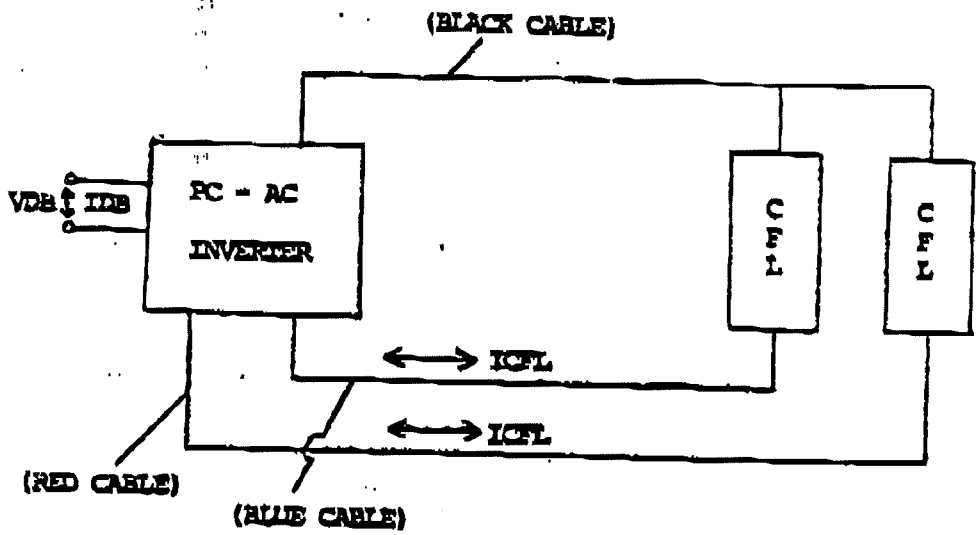
(NOTE 1)



(NOTE 2)

LIFE IS UP TO WHEN ONE OR MORE OF FOLLOWING CASES

a) WHEN CFL BECOME NOT TO LIGHT ON UNDER RATED POWER SUPPLY.

b) WHEN LENGTH OF HOMOGENEOUS EMISSION BECOMES 50% OF EFFECTIVE DISPLAY AREA.
(SHOULD BE MEASURED 3 MINUTES AFTER POWER-ON.)

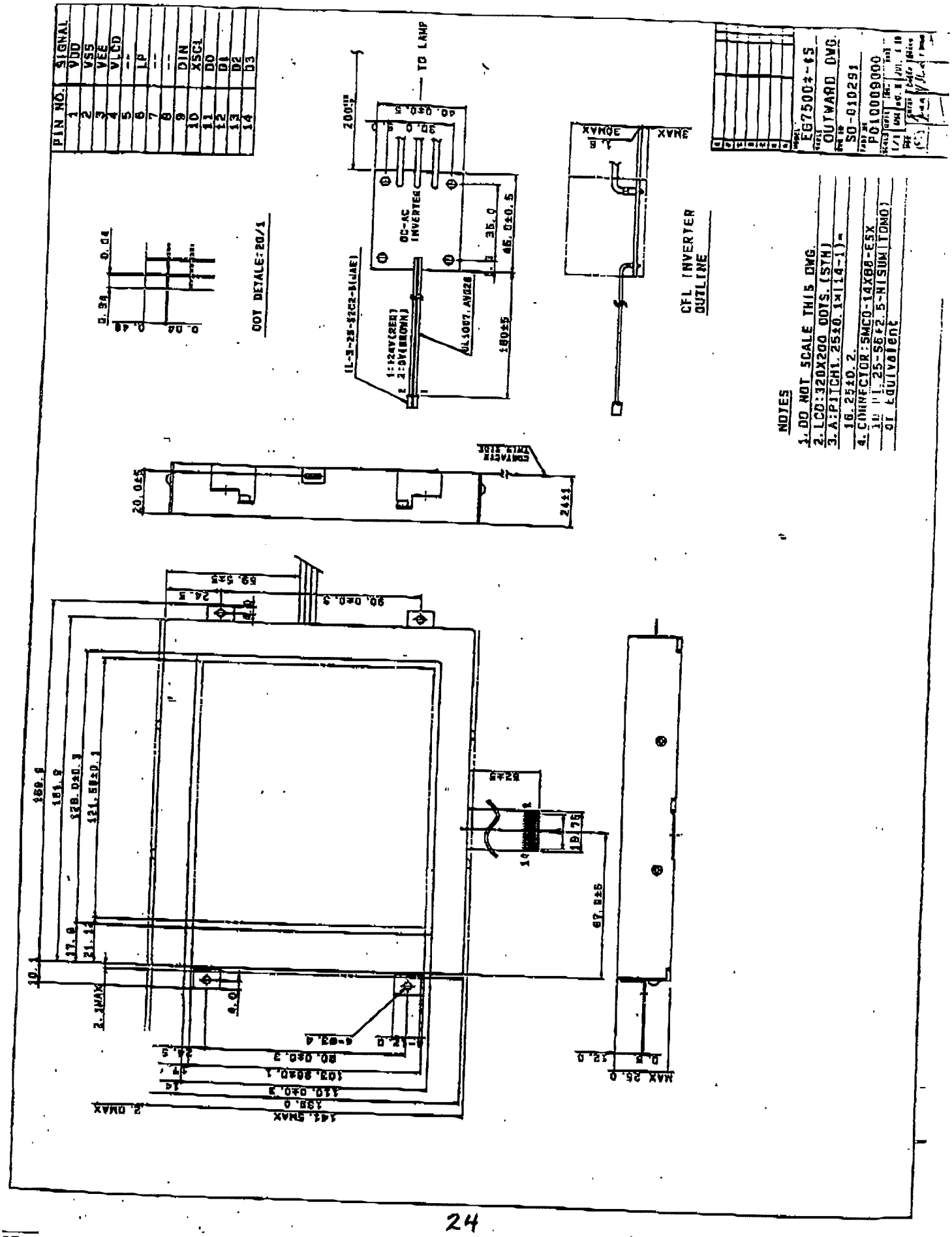
c) WHEN ILLUMINANCE BECOMES 50% OF THE INITIAL VALUE.
(SHOULD BE MEASURED 3 MINUTES AFTER POWER-ON.)

(NOTE 3)

CFL SHALL START EMISSION.
TEMPERATURE OF LAMP SHOULD BE UNDER THE OPERATING TEMPERRATURE.

(NOTE 4)

DISTANCE BETWEEN MEASURING POINT AND SURFACE OF B/L UNIT IS 300mm. (SHOULD BE MEASURED 3 MINUTES AFTER POWER-ON. IOB=6.5mA.)


PIN NO. SIGNAL
1 VDD
2 VSS
3 VEE
4 VLCD
5 --
6 LP
7 --
8 --
9 DIN
10 XSCL
11 D0
12 D1
13 D2
14 D3
TO LAMP
DC-AC INVERTER
CFL INVERTER OUTLINE
DOT DETAILE:20/1
NOTES
1. DO NOT SCALE THIS DWG.
2. LCD:320X200 DOTS.(STN)
3. A:PITCH1.25±0.1×14-1)=
16.25±0.2.
4. CONNECTOR:SMCO-14X88-ESX
or equivalent
EG7500+-5
OUTWARD DWG.
SO-010291
P010009000