SPEC. NO.	TQ3C-8EAC0-E1CWN49-01
DATE	October 20, 2004

SPEC

FOR:

TYPE:KHS038AA1BJ-G00

CONTENTS

1. Application
2. Construction and Outline
3. Mechanical Specifications
4. Absolute Maximum Ratings
5. Electrical Characteristics
6. Optical Characteristics
7. Circuit Block Diagram
8. Interface Signals
9. Interface Timing Chart
10. Data and Screen
11. Input Timing Characteristics
12. Supply Voltage Sequence Condition
13. Backlight Characteristics
14. Lot Number Identification
15. Warranty
16. Precautions for Use
17. Reliability Data / Environmental Test
18. Recommended additional circuit
19. Outline Drawing

Issued
Date: NOV.10.2004
KYOCERA
Hayato LCD Division

KYOCERA CORPORATION
KAGOSHIMA HAYATO PLANT
LCD DIVISION

This specification is subject to change without notice.
Consult Kyocera before ordering.

Original	Designed by :Engineering Dept.			Confirmed by :QA Dept.	
Issue Data	Prepared	Checked	Approved	Checked	Approved
August 25, 2003	W. Yano	M.Fujitani	H. Ohno	Y.Yoshida	S.Hayashi

Caution

1. This Kyocera LCD module has been specifically designed for use only in electronic devices in the areas of audio control, office automation, industrial control, home appliances, etc. The modules should not be used in applications where module failure could result in physical harm or loss of life, and Kyocera expressly disclaims any and all liability relating in any way to the use of the module in such applications.

2. Customer agrees to indemnify, defend and hold Kyocera harmless from and against any and all actions, claims, losses, damages, liabilities, awards, costs, and expenses, including legal fees, resulting from or arising out of Customer's use, or sale for use, of Kyocera modules in applications.

3. Kyocera shall have the right, which Customer hereby acknowledges, to immediately scrap or destroy tooling for Kyocera modules for which no Purchase Orders have been received from the Customer in a two-year period.

Revision Record

Date	Designed by: Engineering Dept.			Confirmed by: QA Dept.	
	Prepared	Checked	Approved	Checked	Approved
Oct. 20, 2004	W. Yano	M.Fujitani	H. Ohno	Y. Yoshida	S. Hayashi

Rev. No.	Date	Page	Descriptions
01	Oct. 20, 2004	4	5. Electrical Characteristics ～Change "LCD driving voltage"
		11	8-2. CFL ～Delete "LEVEL"
		19	16-3. LCD Operation ～Change comment "2"
			16-4. Storage ～Change comment "2"

1．Application

This data sheet defines the specification for a (240×R.G.B)×320 dot, STN transflective color dot matrix type Liquid Crystal Display with CFL backlight.

2．Construction and Outline

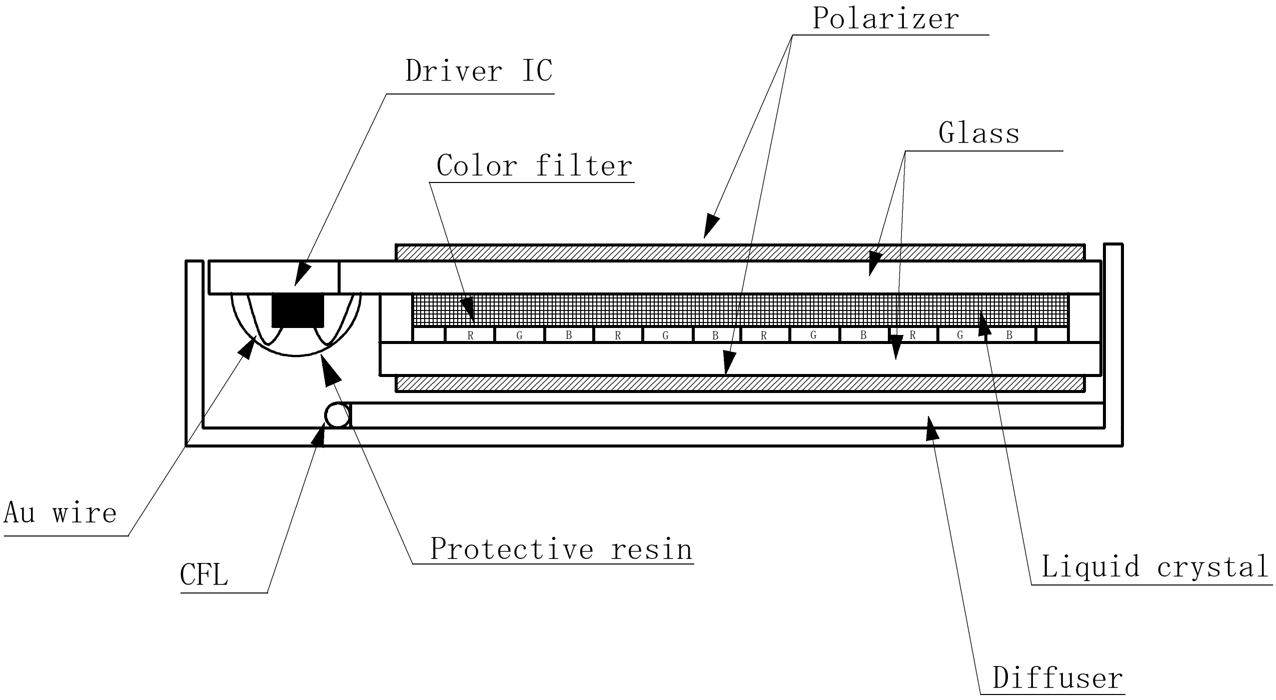
(240×R.G.B)×320 dots, COB type LCD with CFL backlight.

Backlight system : Side-edge type CFL (1 tube).

Inverter : Option.
Recommended Inverter : PH-BLC08-K3 (HITACHI MEDIA ELECTRONICS)
or equivalent.

Polarizer : Glare treatment.

Additional circuit : None


Polarizer
Driver IC
Glass
Color filter
R
G
B
R
G
B
R
G
B
R
G
B
Au wire
CFL
Protective resin
Liquid crystal
Diffuser

This drawing is showing conception only.

3. Mechanical Specifications

ITEM	SPECIFICATION	UNIT
Outline dimensions	73.0 (W) × 94.0 (H) × 6.7 (D)	mm
Effective viewing area	59.6 (W) × 78.8 (H)	mm
Dot number	(240×R.G.B) (W) × 320 (H)	Dots
Dot size	0.06 (W) × 0.22 (H)	mm
Dot pitch	0.08 (W) × 0.24 (H)	mm
Display color *1	White *2	—
Base color *1	Black *2	—
Mass	65	g

*1 Due to the characteristics of the LC material, the color vary with environmental temperature.

*2 Negative-type display

Display data "H" :R.G.B Dots ON : White
Display data "L" :R.G.B Dots OFF : Black

4. Absolute Maximum Ratings

4-1. Electrical absolute maximum ratings

ITEM	SYMBOL	MIN.	MAX.	UNIT
Supply voltage for logic	VDD	0	7.0	V
Supply voltage for LCD driving *1	V0-V5	0	38.0	V
Input signal voltage *2	Vin	0	VDD	V

*1 $V0 \geqq V1 \geqq V2 \geqq V3 \geqq V4 \geqq V5 = 0(V)$

*2 Input signal : CP,LOAD,FRM,DF,DISP,D0～D7

4-2. Environmental absolute maximum ratings

ITEM		SYMBOL	MIN	MAX	UNIT
Operating temperature	*1	Top	0	50	℃
Storage temperature	*2	T_{STO}	-20	60	℃
Operating humidity	*3	Hop	10	*4	%RH
Storage humidity	*3	H_{STO}	10	*4	%RH
Vibration		—	*5	*5	—
Shock		—	*6	*6	—

*1 LCD's display quality shall not be guaranteed at the temperature range of: below 0℃ and upper 40℃

*2 Temp. = -20℃ < 48 h , Temp = 60℃ < 168 h
Store LCD panel at normal temperature/humidity. Keep it free from vibration and shock. LCD panel that is kept at low or high temperature for a long time can be defective due to the other conditions, even if the temperature satisfies standard.
(please refer to 16. Precautions for use as detail).

*3 Non-condensation.

*4 Temp. ≦ 40℃, 85% RH Max.
Temp. > 40℃, Absolute Humidity shall be less than 85%RH at 40℃.

*5

Frequency	10〜55 Hz	Converted to acceleration value : (0.3〜9m/s^2)
Vibration width	0.15 mm	
Interval	10-55-10 Hz 1 minute	

2 hours in each direction X/Y/Z (6 hours as total)
EIAJ ED-2531.

*6 Acceleration: 490m/s^2
Pulse width : 11 ms
3 times in each direction : ±X/±Y/±Z.
EIAJ ED-2531.

５．Electrical Characteristics

VDD = +3.3V±0.3V, Temp. = 0～50℃

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage for logic		VDD	—	3.0	3.3	3.6	V
LCD driving voltage	*1	Vop =V0-V5	0 ℃	(29.8)	(30.8)	(31.8)	V
			25 ℃	(28.6)	(29.6)	(30.6)	V
			50 ℃	(28.0)	(29.0)	(30.0)	V
Input voltage		Vin	"H" level	0.8VDD	—	VDD	V
			"L" level	0	—	0.2VDD	V
Clock frequency		f_{cp}	—	2.02	2.16	10.0	MHz
Frame frequency	*2	f_{FRM}	—	70	75	80	Hz
Randomizing frequency	*3	f_{DF}		300	—	800	Hz
Current consumption for logic		IDD	*5	—	0.8	1.0	mA
			*6	—	0.6	0.8	mA
Current consumption for LCD driving	*4	IEE	*5	—	2.4	3.1	mA
			*6	—	1.1	1.4	mA
Power consumption	*4	Pdisp	*5	—	75	100	mW
			*6	—	35	46	mW

*1 Maximum contrast ratio is obtained by adjusting the LCD supply voltage (Vop= V0-V5) for driving LCD.

*2 In consideration of display quality, it is recommended that frame frequency is set in the range of 70-80Hz. When you have to use higher frame and clock frequencies, confirm the LCD's performance and quality prior to finalizing the frequency values: Generally, as frame and clock frequencies become higher, current consumption will get bigger and display quality will be degraded.

*3 It is recommended that randomizing frequency be set in the range of 300-800Hz. At finalizing the frequency ,confirm with actual tests that phenomena like flickering and/or horizontal lines do not appear on screen.

*4 Include recommended circuit. Refer 18.recommended additional circuit.

*5 Display high frequency pattern, (see below).
VDD = 3.3V , Vop = V0-V5 , f_{FRM} = 75 Hz , fcp = 2.16MHz ,Temp. = 25℃
Pattern:

```
      1 2 3 4 5 6 ------------------------- 720(dot)
  1   ■■■□□□■■■□□□■■■□□□■■■
  2   □□□■■■□□□■■■□□□■■■□□□
  3   ■■■□□□■■■□□□■■■□□□■■■
  :   □□□■■■□□□■■■□□□■■■□□□
  :   ■■■□□□■■■□□□■■■□□□■■■
  :   □□□■■■□□□■■■□□□■■■□□□
319   ■■■□□□■■■□□□■■■□□□■■■
320   □□□■■■□□□■■■□□□■■■□□□
(dot)
```

*6 Display high frequency pattern, (see below).
VDD = 3.3V , Vop = V0-V5 , f_{FRM} = 75 Hz , fcp = 2.16MHz, Temp. = 25℃
Pattern:

```
      1 2 3 4 5 6 ------------------------- 720(dot
  1   □□□□□□□□□□□□□□□□□□□□
  2   □□□□□□□□□□□□□□□□□□□□
  3   □□□□□□□□□□□□□□□□□□□□
  :   □□□□□□□□□□□□□□□□□□□□
  :   □□□□□□□□□□□□□□□□□□□□
  :   □□□□□□□□□□□□□□□□□□□□
319   □□□□□□□□□□□□□□□□□□□□
320   □□□□□□□□□□□□□□□□□□□□
(dot)
```

６. Optical Characteristics

6-1. Reflective mode

Measuring Spot = ϕ6mm , Temp. = 25℃

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Response time	Rise	Tr	$\theta = \phi = 0°$	—	(250)	(350)	ms
	Down	Td	$\theta = \phi = 0°$	—	(150)	(250)	ms
Contrast ratio		CR	$\theta = \phi = 0°$	(4.0)	(8.0)	—	—
Reflectance		ρ	—	(4.5)	(9.0)	—	%

Optimum contrast is obtained by adjusting the LCD driving voltage(Vop) while at the viewing angle of $\theta = \phi = 0°$.

＊Definition of Reflectance:

$$\rho\ (\text{Reflectance}) = \frac{\text{Measured Reflection Brightness}}{\text{Reflection Brightness against Standard White Board}} \times 100[\%]$$

＊Definition of Contrast

$$\text{CR (Contrast)} = \frac{\text{Reflectance at all pixels "White"}}{\text{Reflectance at all pixels "Black"}}$$

6-2. Transmissive mode

Measuring Spot = ϕ6mm , Temp. = 25℃

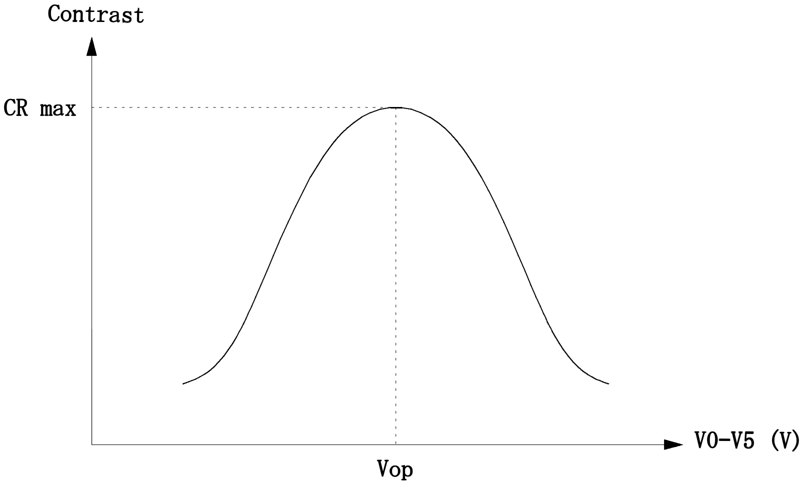
ITEM		SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT
Response time	Rise	Tr	$\theta = \phi = 0^\circ$		—	(250)	(350)	ms
	Down	Td	$\theta = \phi = 0^\circ$		—	(150)	(250)	ms
Viewing angle range		θ	CR≧2	$\phi = 0^\circ$	(-20)	—	(30)	deg.
		ϕ		$\theta = 0^\circ$	(-50)	—	(45)	deg.
Contrast ratio		CR	$\theta = \phi = 0^\circ$		(10.0)	(20.0)	—	—
Brightness		L	IL=2.5mA		(12)	(20)	—	cd/m^2
Chromaticit coordinates	Red	x	$\theta = \phi = 0^\circ$		(0.36)	(0.41)	(0.46)	—
		y			(0.22)	(0.27)	(0.32)	
	Green	x	$\theta = \phi = 0^\circ$		(0.23)	(0.28)	(0.33)	
		y			(0.31)	(0.36)	(0.41)	
	Blue	x	$\theta = \phi = 0^\circ$		(0.15)	(0.20)	(0.25)	
		y			(0.16)	(0.21)	(0.26)	
	White	x	$\theta = \phi = 0^\circ$		(0.24)	(0.29)	(0.34)	
		y			(0.26)	(0.31)	(0.36)	

Optimum contrast is obtained by adjusting the LCD driving voltage(Vop) while at the viewing angle of $\theta = \phi = 0^\circ$.

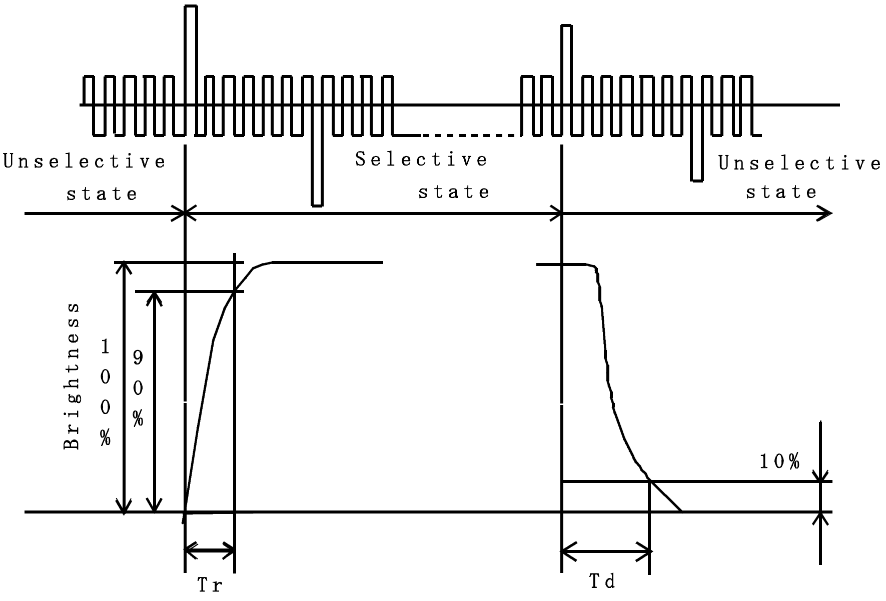
* Contrast ratio is defined as follows :

$$\mathrm{CR(Contrast)} = \frac{\text{Brightness at all pixels "White"}}{\text{Brightness at all pixels "Black"}}$$

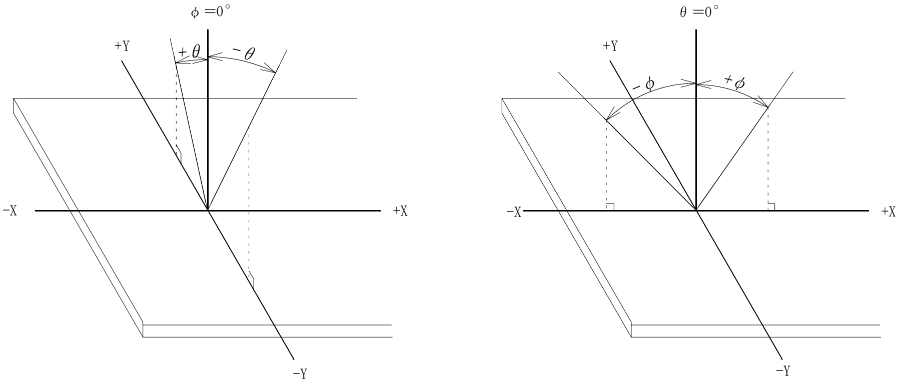
6-3. Definition of Vop



6-4. Definition of response time


Unselective state
Selective state
Unselective state
Brightness
100%
90%
10%
Tr
Td

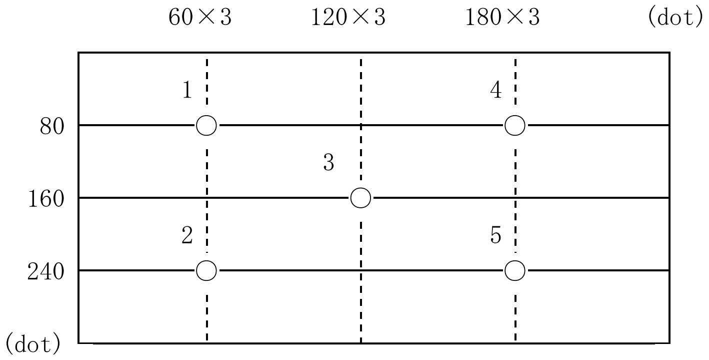
6-5. Definition of viewing angle


φ =0°
+Y
+θ
-θ
-X
+X
-Y
θ =0°
+Y
-φ
+φ
-X
+X
-Y

(θ direction)

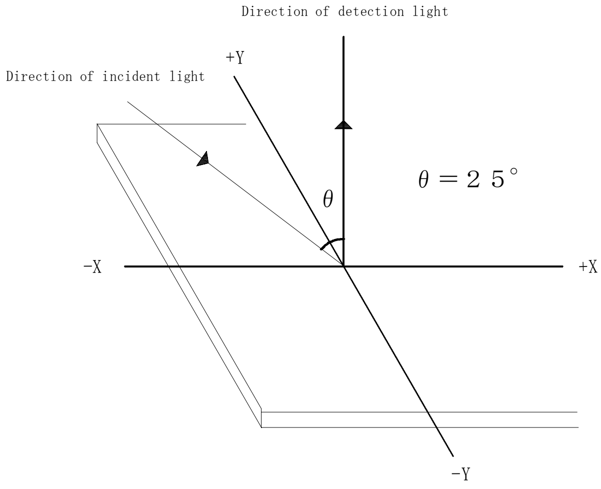
(φ direction)

6-6. Measuring points

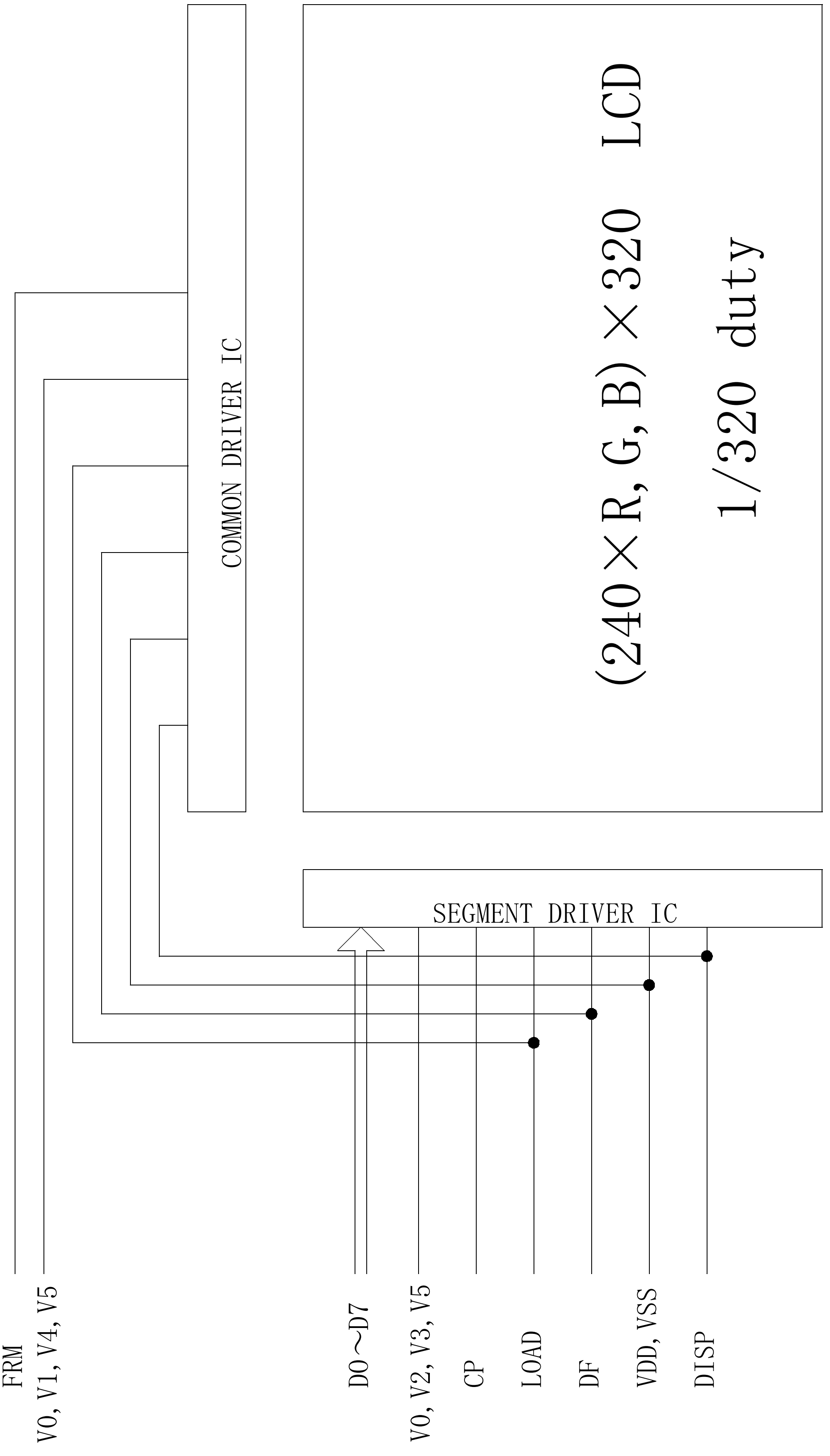

60×3
120×3
180×3
(dot)
1
4
80
3
160
2
5
240
(dot)

1) Rating is defined as the average brightness inside the viewing area.
2) 30 minutes after CFL is turned on. (Ambient Temp.=25℃)
3) The inverter should meet the eccentric conditions;
   -Sine, symmetric waveform without spike in positive and negative.
4) Measuring Inverter : PH-BLC-08-K3(HITACHI MEDIA ELECTRONICS)

6-7. Measurement method of reflectance


Direction of detection light
+Y
Direction of incident light
θ
θ＝２５°
-X
+X
-Y

7. Circuit Block Diagram



(240×R,G,B)×320 LCD
1/320 duty
COMMON DRIVER IC
SEGMENT DRIVER IC
FRM
V0,V1,V4,V5
D0～D7
V0,V2,V3,V5
CP
LOAD
DF
VDD,VSS
DISP

8．Interface signals

8-1.LCD

CN1 :

PIN NO.	SYMBOL	DESCRIPTION	LEVEL
1	FRM	Synchronous signal for driving scanning line	H
2	LOAD	Data signal latch clock	H → L
3	CP	Data signal shift clock	H → L
4	DISP	Display control signal	H(ON),L(OFF)
5	VDD	Power supply for logic	—
6	VDD	Power supply for logic	—
7	VSS	GND	—
8	DF	AC signal for driving	—
9	V0	*	—
10	V1	*	—
11	V2	*	—
12	V3	*	—
13	V4	*	—
14	V5	*	—
15	D7	Display data	H(ON),L(OFF)
16	D6		
17	D5		
18	D4		
19	D3		
20	D2		
21	D1		
22	D0		

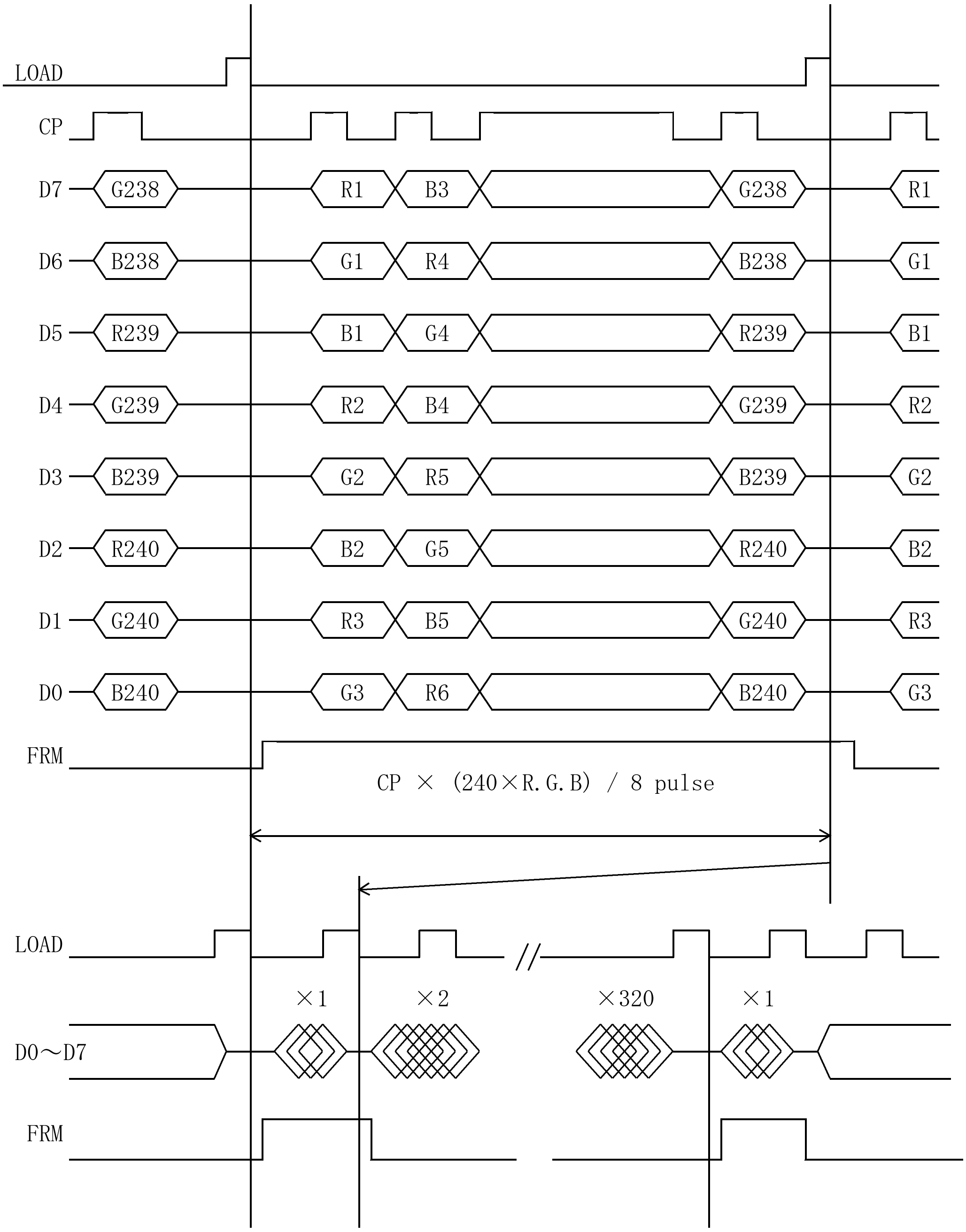
*V0 ～ V5 : Refer 18. Recommended Bias Votage for Driving LCD.

8-2. CFL

PIN No	SYMBOL	DESCRIPTION
1	HOT	Inverter output high voltage side
2	NC	—
3	COLD	Inverter output low voltage side

LCD side connector	:	BHR-03VS-1	(JST)
Recommended matching connector	:	SM02-(8.0)B-BHS-1	(JST)

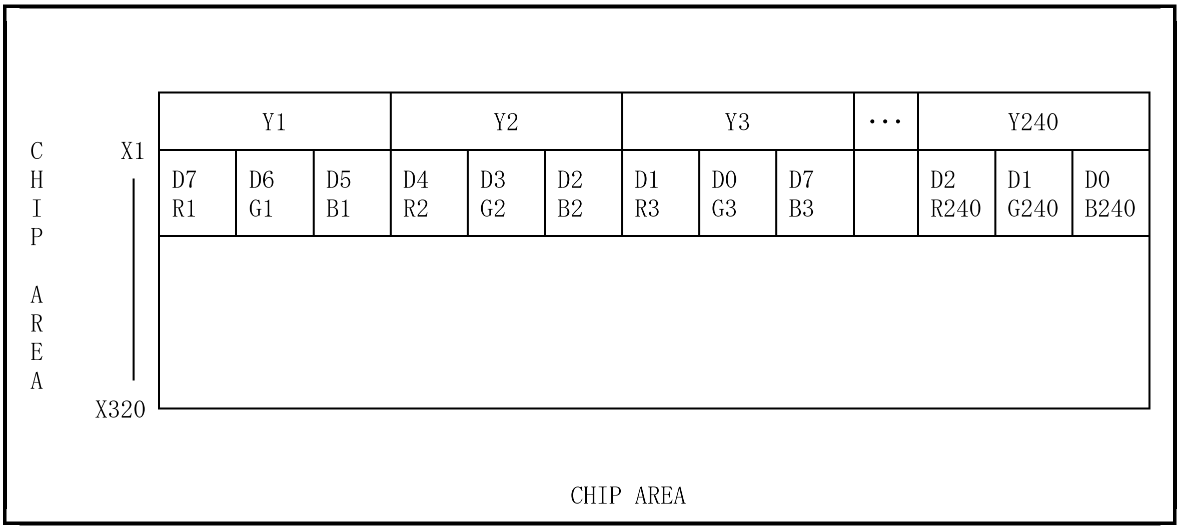
9. Interface Timing Chart


LOAD
CP
D7
G238
R1
B3
G238
R1
D6
B238
G1
R4
B238
G1
D5
R239
B1
G4
R239
B1
D4
G239
R2
B4
G239
R2
D3
B239
G2
R5
B239
G2
D2
R240
B2
G5
R240
B2
D1
G240
R3
B5
G240
R3
D0
B240
G3
R6
B240
G3
FRM
CP × (240×R.G.B) / 8 pulse
LOAD
×1
×2
×320
×1
D0～D7
FRM

＊ The cycle of load signal should be stable and continuously applied without interruption.

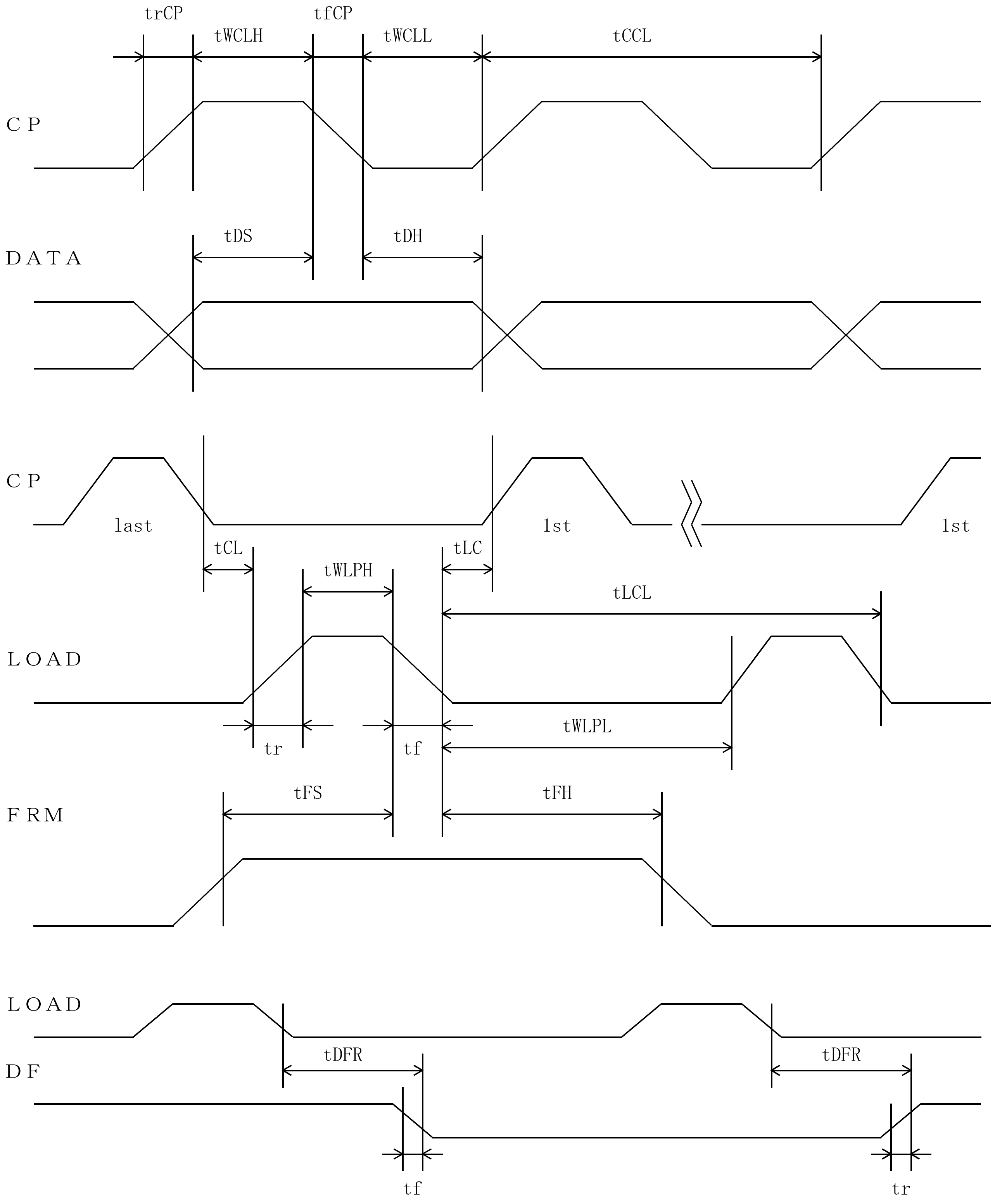
＊ The above-mentioned timing chart shows a reference to set up a LCD module, not an electrical rating.

１０．Data and Screen


CHIP AREA
X1
X320
CHIP AREA

Y1			Y2			Y3			･･･	Y240		
D7 R1	D6 G1	D5 B1	D4 R2	D3 G2	D2 B2	D1 R3	D0 G3	D7 B3		D2 R240	D1 G240	D0 B240

１１．Input Timing Characteristics


trCP
tWCLH
tfCP
tWCLL
tCCL
C P
tDS
tDH
D A T A
C P
last
1st
1st
tCL
tLC
tWLPH
tLCL
L O A D
tr
tf
tWLPL
tFS
tFH
F R M
L O A D
tDFR
tDFR
D F
tf
tr

11-1. Switchig characteristics

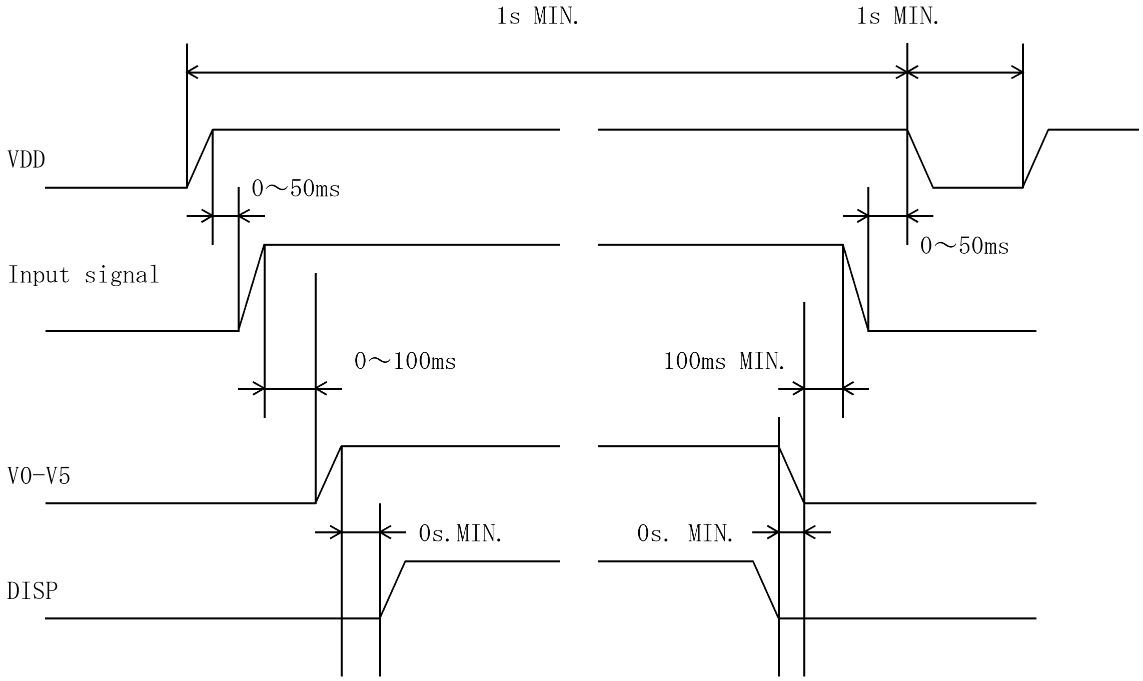
Input Characteristics ; VDD = +3.3V ± 0.3V, Temp. = 0～50 ℃

ITEM	SYMBOL	MIN.	MAX.	UNIT
CP Cycle *1,*2	tCCL	100	—	ns
CP "H" Pulse Width *2	tWCLH	40	—	ns
CP "L" Pulse Width *2	tWCLL	40	—	ns
CP Rise Up Time *2	trCP	—	30	ns
CP Fall Down Time *2	tfCP	—	30	ns
Data Set Up Time	tDS	25	—	ns
Data Hold Time	tDH	20	—	ns
LOAD "H" Pulse Width	tWLPH	100	—	ns
LOAD "L" Pulse Width	tWLPL	4900	—	ns
LOAD Cycle *3	tLCL	5000	—	ns
CP→LOAD Delay Time	tCL	0	—	ns
LOAD→CP Delay Time *4	tLC	200-tWLPH	—	ns
Input Signal Rise Up Time	tr	—	30	ns
Input Signal Fall Down Time	tf	—	30	ns
FRM Data Set Up Time	tFS	100	—	ns
FRM Data Hold Time	tFH	30	—	ns
DF Delay Time	tDFR	0	300	ns

*1 CP Cycle is adjust so that FRM signal is 75Hz.
*2 The formula of condition
①trCP + tfCP ≦ tCCL - (tWCLH + tWCLL)
②trCP, tfCP ≦ 30 ns
Please use on condition that ①,② are filled.
*3 LOAD Cycle is const.
*4 tLC ≧ 0

１２．Supply Voltage Sequence Condition

DO NOT apply DC voltage to the LCD panel. DC voltage induce irreversible electrochemical reactions and reduce LCD life. Always follow the power supply ON/OFF sequence of VDD first, input signal second, V0-V5 third and finally DISP. This will prevent DC driving of the LCD or CMOS LSI latch up as shown below.



＊ Input signal ： CP,LOAD,FRM,DF,D0～D7

＊ The above sequence should be designed as to keep each normal figure on condition that liquid crystal module is loaded on your system.

＊ Control the input signal and V0 - V5 to the above ON - OFF timing when you switch ON/OFF the display during VDD and DISP are on.
And also design the circuit as V0 - V5's OFF level become GND level.

＊ Control the suplly voltage sequence not to float all signal line when the LCD panel is driving.

１３．Backlight Characteristics

CFL ratings

Temp.＝ 0～25℃

ITEM	SYMBOL	MIN.	TYP.	MAX.	NOTE
Starting discharge Voltage *1	VS	－	－	(690) Vrms.	0 ℃
		－	－	(460) Vrms.	25 ℃
Discharging tube current *2,*3	IL	(2.0)mArms.	(2.5) mArms.	(6.0) mArms.	－
Discharging tube voltage	VL	－	(270) Vrms.	－	－
Operating life(IL= 2.5 mArms.) *4	T	(29,000) h	(44,000) h	－	－
Operating frequency	F	40 kHz	－	100 kHz	－

*1 The Non-load output voltage (VS) of the inverter should be designed to have some margin, because VS may increase due to the leak current which may be caused by wiring of CFL cables. (Reference value: (900) Vrms MIN.)

*2 We recommend that you should set the discharging tube current at lower than typical value so as to prevent the heat accumulation of CFL tube from deteriorating a performance of the LCD.

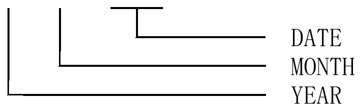
*3 Do not apply more than (6.0)mA discharging tube current. Because CFL maybe broken due to over current.

*4 When the illuminance or quantity of light has decreased to 50 % of the initial value. Average life time of CFL will be decreased when LCD is operating at lower and higher temperature.

１４．Lot Number Identification

The lot number shall be indicated on the back of the backlight case of each LCD.

ＫＨＳ０３８ＡＡ１ＢＪ－Ｇ００－ □ □－□ □



YEAR	2003	2004	2005	2006	2007	2008
CODE	3	4	5	6	7	8

MONTH	JAN.	FEB.	MAR.	APR.	MAY	JUN.
CODE	1	2	3	4	5	6

MONTH	JUL.	AUG.	SEP.	OCT.	NOV.	DEC.
CODE	7	8	9	X	Y	Z

１５．Warranty

15-1. Incoming inspection

Please inspect the LCD within one month after your receipt.

15-2. Production Warranty

Kyocera warrants its LCDs for a period of 12 months after receipt by the purchaser, and within the limits specified. Kyocera shall, by mutual agreement, replace or rework defective LCDs that are shown to be Kyocera's responsibility.

１６. Precautions for use

16-1. Installation of the LCD

1. A transparent protection plate shall be added to protect the LCD and its polarizers.
2. The LCD shall be installed so that there is no pressure on the LSI chips.
3. The LCD shall be installed flat, without twisting or bending.
4. The display window size should be the same as the effective viewing area.
5. In case you use outside frame of effective viewing area as outward appearance of your product, unevenness of its outward appearance is out of guarantee.
6. Do not pull the CFL lead wires and do not bend the root of the wires. Housing should be designed to protect CFL lead wires from external stress.
7. This Kyocera LCD module has been specifically designed for use in general electronic devices, but not for use in a special environment such as usage in an active gas. Hence, when the LCD is supposed to be used in a special environment, evaluate the LCD thoroughly beforehand and do not expose the LCD to chemicals such as an active gas.

16-2. Static Electricity

1. Since CMOS ICs are mounted directly onto the LCD glass, protection from static electricity is required. Operation should wear ground straps.
2. Aluminum foil covering the terminal electrodes should remain in place until installed.

16-3. LCD Operation

1. The LCD shall be operated within the limits specified. Operation at values outside of these limits may shorten life, and/or harm display images.
2. Adjust ″LCD driving voltage″ to obtain optimum viewing angle and contrast.
3. Operation of the LCD at temperature below the limit specified may cause image degradation and/or bubbles. It may also change the characteristics of the liquid crystal. This phenomenon may not recover. The LCD shall be operated within the temperature limits specified.

16-4. Storage

1. The LCD shall be stored within the temperature and humidity limits specified. Store in a dark area, and protected the LCD from direct sunlight or fluorescent light.
2. Always store the LCD so that it is free from external pressure onto it.

16-5. Screen Surface

1. DO NOT store in a high humidity environment for extended periods. Image degradation, bubbles, and/or peeling off of polarizer may result.
2. The front polarizer is easily scratched or damaged. Prevent touching it with any hard material, and from being pushed or rubbed.
3. The LCD screen may be cleaned with a soft cloth or cotton pad. Methanol, or Isopropyl Alcohol may be used, but insure that all solvent residue is removed.
4. Water may cause damage or discoloration of the polarizer. Clean any condensation or moisture from any source immediately.
5. Always keep the LCD free from condensation during testing. Condensation may permanently spot or stain the polarizers.

１７. Reliability Data / Environmental Test

TEST ITEM	TEST CONDITION	TEST TIME	RESULT
High Temp. Atmosphere	60℃	240 h	Display Quality : No defect Display Function : No defect Current Consumption : No defect
Low Temp. Atmosphere	-20℃	240 h	Low Temp. Bubble : None Solid Crystallization of Liquid Crystal : None Display Quality : No defect Display Function : No defect Current Consumption : No defect
High Temp. Humidity Atmosphere	40℃ 90%RH	240 h	Display Quality : No defect Display Function : No defect Peel-off of Organic Sealing : None Current Consumption : No defect
Temp. Cycle	-20℃ 0.5 h R.T. 0.5 h 60℃ 0.5 h	10cycles	Display Quality : No defect Display Function : No defect Peel-off of Organic Sealing : None Bubble on Cell : None
High Temp. Operation	50℃ Vop	500 h	Display Quality : No defect Current Consumption : No defect

＊ Each test item uses a test LCD only once. The tested LCD is not used in any other tests.

＊ The LCD is tested in circumstances in which there is no condensation.

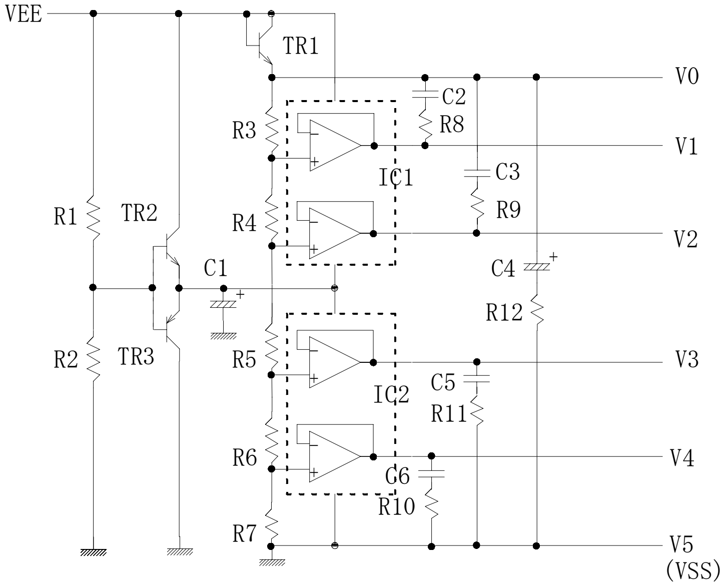
＊ The tested LCD is inspected after 24 hours of storage at room temperature and room humidity after each test is finished.

＊ The reliability test is not an out-going inspection.

＊ The results of the reliability test are for your reference purpose only.
The reliability test is conducted only to examine the LCD's capability.

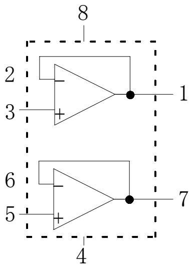
１８．Recommended additional circuit

a) Recommended Bias Voltage for Driving LCD



R3,4 = 15.0kΩ ± 0.5%
R6,7 = 15.0kΩ ± 0.5%
R5 = 220kΩ ± 1.0%

IC1, IC2



These value above are theoreticaly calculated. Fine tuning might be required in some cases.
For fine tuning value of the resistor shall be adjusted to conform with the follwing equation.

| V0-V1 | = | V1-V2 | = | V3-V4 | = | V4-V5 |

Recommended parts for Bios voltage circuit

①SEMI CONDUCTOR

Symbol	Type	Maker Name	note
IC1	MC33172D	MOTOROLA	
IC2	MC33172D	MOTOROLA	
TR1	2SC2412K	ROHM	
TR2	2SC2412K	ROHM	
TR3	2SA1037AK	ROHM	

②RESISTOR

Symbol	Characteristic	Example(Maker Name)	note
R1	100K/1608/J	CR10-104J	(KYOCERA)
R2	100K/1608/J	CR10-104J	(KYOCERA)
R3	15K/1608/D	RR0816R-153-D	(SUSUMU)
R4	15K/1608/D	RR0816R-153-D	(SUSUMU)
R5	220K/1608/F	RK73H1J-220KΩF	(KOA)
R6	15K/1608/D	RR0816R-153-D	(SUSUMU)
R7	15K/1608/D	RR0816R-153-D	(SUSUMU)
R8	15Ω/1608/J	CR10-150J	(KYOCERA)
R9	15Ω/1608/J	CR10-150J	(KYOCERA)
R10	15Ω/1608/J	CR10-150J	(KYOCERA)
R11	15Ω/1608/J	CR10-150J	(KYOCERA)
R12	15Ω/1608/J	CR10-150J	(KYOCERA)

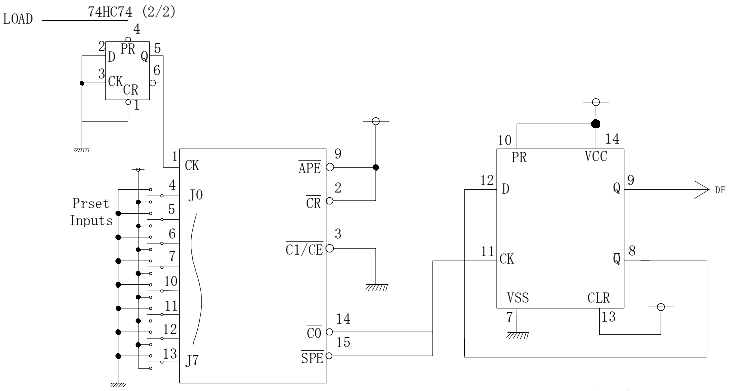
③CAPACITOR

Symbol	Characteristic	Example(Maker Name)	note
C1	4.7μ/35V	MF35FD4R7MC6 (NIPPON CHEMI-CON)	Electrolytic capacitor
C2	B/4.7μF/10V/3216/M	LMK316BJ475ML (TAIYO YUDEN)	Ceramic Capacitor
C3	B/4.7μF/10V/3216/M	LMK316BJ475ML (TAIYO YUDEN)	Ceramic Capacitor
C4	4.7μ/50V	MF50FD4R7MC8 (NIPPON CHEMI-CON)	Electrolytic capacitor
C5	B/4.7μF/10V/3216/M	LMK316BJ475ML (TAIYO YUDEN)	Ceramic Capacitor
C6	B/4.7μF/10V/3216/M	LMK316BJ475ML (TAIYO YUDEN)	Ceramic Capacitor

b) Example of Randomizing Circuit

Randomizing circuit is recommended in order to reduce "cross-talk" phenomenun of displayed images. (Tailing, vertical strips,etc)
Its detail is subject to change according to actual operating condition and application of the LCD . Should you have any question when installing an actual randomizing circuit, please ask Kyocera for details .

b-1)


LOAD
74HC74 (2/2)
4
2
PR
5
D
Q
6
3
CK
CR
1
Prset
Inputs
1
CK
4
J0
5
6
7
10
11
12
13
J7
9
APE
2
CR
3
C1/CE
14
CO
15
SPE
10
14
PR
VCC
12
D
Q
9
DF
11
CK
Q
8
VSS
CLR
7
13

HC40103
TOSHIBA

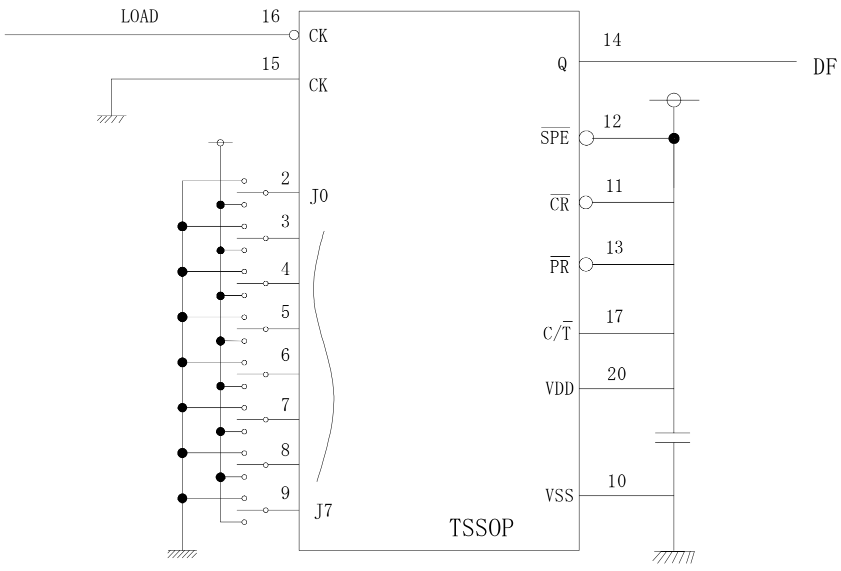
74HC74A(1/2)

Prset

76543210	A
00000000	256
00000001	X
00000010	2
00000011	3
||||||||	
11111111	255

There may be flickering on screen according to some LOAD signal frequencies.
If in happens , set PRESET INPUTS terminals to select optimized conditions .

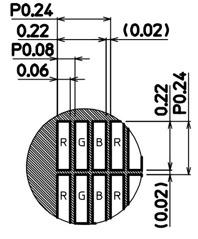
b-2)


LOAD
16
CK
15
CK
14
Q
DF
12
SPE
2
J0
11
CR
3
13
PR
4
5
17
C/T
6
20
VDD
7
8
9
10
VSS
J7
TSSOP

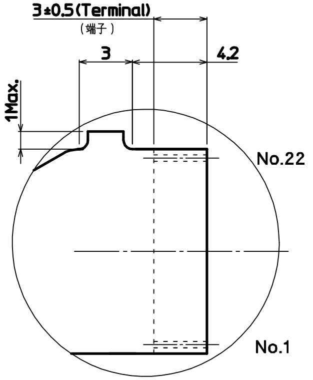
HD151011TEL

HITACHI

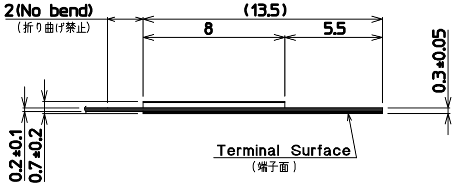
No	Description	Drawn	Checked	Checked	Approved


P0.24
0.22
(0.02)
P0.08
0.06
0.22
P0.24
(0.02)
R G B R
R G B R

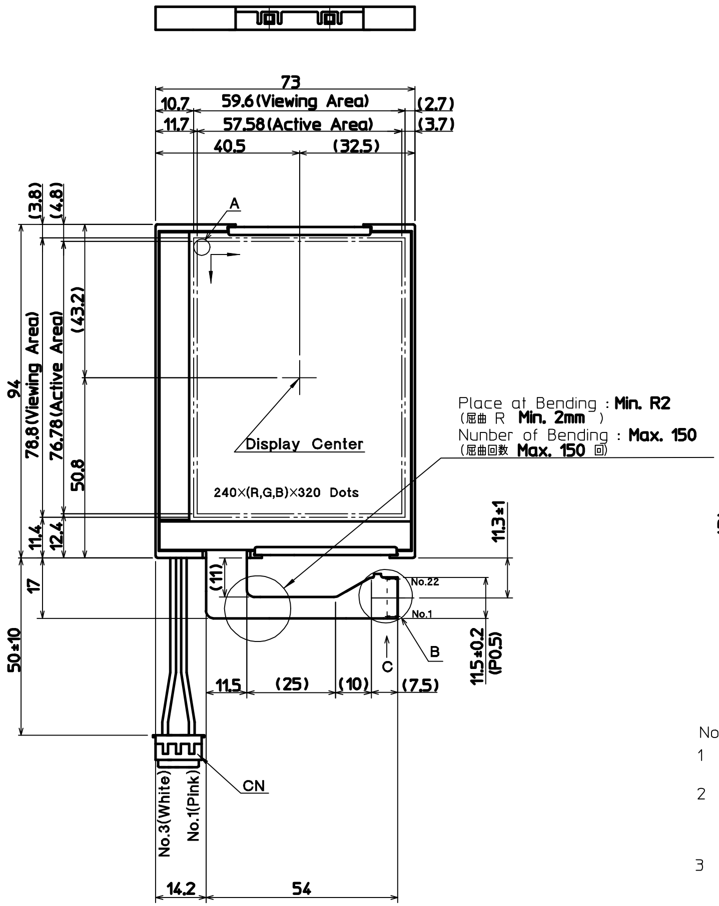
DETAIL A (NTS)
(Dot Size)

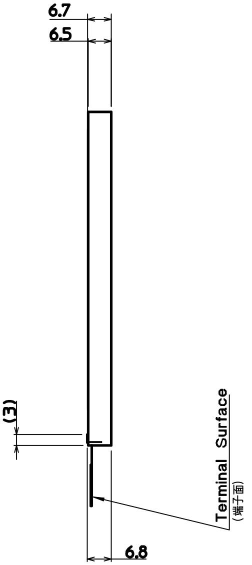

3±0.5(Terminal)
（端子）
3
4.2
1Max.
No.22
No.1

DETAIL B (5:1)


2(No bend)
（折り曲げ禁止）
(13.5)
8
5.5
0.3±0.05
0.2±0.1
0.7±0.2
Terminal Surface
（端子面）

VIEWING C (5:1)


73
10.7
59.6(Viewing Area)
(2.7)
11.7
57.58(Active Area)
(3.7)
40.5
(32.5)
(3.8)
(4.8)
A
94
78.8(Viewing Area)
76.78(Active Area)
(43.2)
50.8
11.4
12.4
Display Center
240×(R,G,B)×320 Dots
Place at Bending : Min. R2
（屈曲 R Min. 2mm ）
Nunber of Bending : Max. 150
（屈曲回数 Max. 150 回）
11.3±1
17
(11)
50±10
No.22
No.1
B
C
11.5
(25)
(10)
(7.5)
11.5±0.2
(P0.5)
CN
No.3(White)
No.1(Pink)
14.2
54


6.7
6.5
(3)
6.8
Terminal Surface
（端子面）

Note

1 Connector CN : BHR-03VS-1 (JST)
（コネクター）

2 Matching Connector : SM02-(8.0)B-BHS-1 (JST)
（適合コネクター）
FPC Matching Connector : 22FLH-SM1 (JST)
（FPC適合コネクター） 04 6239 022 001 800 (ELCO)

3 The drawing is the front view of the LCD. Information is displayed starting at the upper left hand corner, moving right then down to the lower right hand corner.
（LCDの正面図において、画像データの表示は左上コーナーから始まり、右へ進み下へ送られ右下コーナーへ向かう。）

4 Tolerance without indication: **±0.5**
（指示無き公差）

Material 材質	Treatment 処理	Approved '03.08.22	Checked	Checked '03.08.22	Drawn	Scale 1:1(5:1,NTS)	Title	KHS038AA1BJ	Year-Month-Day '03.08.21	Size 2
Quantity 製作数	Description; 備考 03012NDA	朝倉		阿部	川田原			Outline Dimensions	Drawing No. 121A5024200	

KYOCERA

SPEC.NO.	TQ3C-8EAC0-E2CWN48-00
DATE	August 25, 2003

FOR:

KYOCERA INSPECTION STANDARD

TYPE : KHS038AA1BJ-G00

KYOCERA CORPORATION
KAGOSHIMA HAYATO PLANT
LCD DIVISION

Original Issue Data	Designed by :Engineering Dept.			Confirmed by :QA Dept.	
	Prepared	Checked	Approved	Checked	Approved
August 25, 2003	W. Yano	M. Fujitani	H. Ohno	Y. Matsumoto	T. Minami

Revision Record

Date	Designed by: Engineering Dept.			Confirmed by: QA Dept.	
	Prepared	Checked	Approved	Checked	Approved

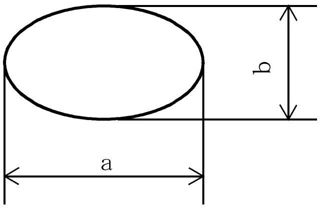
Rev. No.	Date	Page	Descriptions

Visuals specification

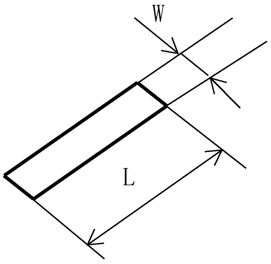
1)Note

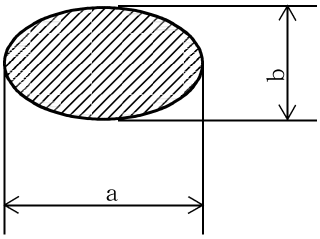
Item	Note	
General	1.When defects specified in this Inspection Standards are inspected, operating voltage(Vop) shall be set at the level where optimized contrast is available. Display quality is applied up to effective viewing area. (Bi-Level INSPECTION) 2.This inspection standard about the image quality shall be applied to any defect within the effective viewing area and shall not be applicable to outside of the area. 3.Should any defects which are not specified in this standard happen, additional standard shall be determined by mutual agreement between customer and Kyocera. 4.Inspection conditions Luminance : 500 Lux minimum . Inspection distance : 300 mm (from the sample) Temperature : 25 ± 5 ℃ Direction : right above	
Definition of Inspection item	Pinhole, Bright spot Black spot, Scratch Foreign particle	The color of a small area is different from the remainder. The phenomenon does not change with voltage.
	Contrast variation	The color of a small area is different from the remainder. The phenomenon changes with voltage.
	Polarizer (Scratch, Bubble, Dent)	Scratch, Bubble and Dent in the polarizer which can be observed in on / off state.

2)Standard

<table>
<tr><th>Inspection item</th><th>Judgement standard</th></tr>
<tr><td>Pinhole, Bright spot
Black spot,
Foreign particle</td><td>


d = (a + b) / 2

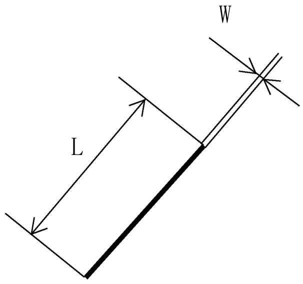
<table>
<tr><th>Category</th><th>Size (mm)</th><th>Acceptable number</th></tr>
<tr><td>A</td><td>d ≦ 0.2</td><td>neglected</td></tr>
<tr><td>B</td><td>0.2 < d ≦ 0.3</td><td>5</td></tr>
<tr><td>C</td><td>0.3 < d ≦ 0.5</td><td>3</td></tr>
<tr><td>D</td><td>0.5 < d</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>Scratch,Foreign particle</td><td>


<table>
<tr><th></th><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable No.</th></tr>
<tr><td>A</td><td>W ≦ 0.03</td><td>—</td><td>neglected</td></tr>
<tr><td>B</td><td rowspan="3">0.03< W ≦0.1</td><td>L ≦ 2.0</td><td>neglected</td></tr>
<tr><td>C</td><td>2.0 < L ≦ 4.0</td><td>3</td></tr>
<tr><td>D</td><td>4.0 < L</td><td>0</td></tr>
<tr><td>E</td><td>0.1 < W</td><td>—</td><td>According to ' Circular '</td></tr>
</table>
</td></tr>
<tr><td>Contrast variation</td><td>


d = (a + b) / 2

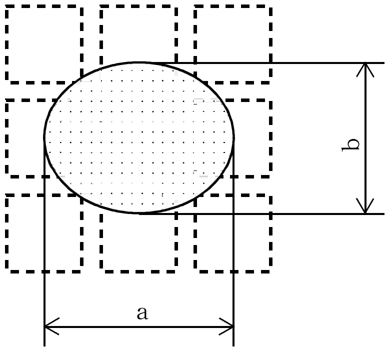
<table>
<tr><th>Category</th><th>Size (mm)</th><th>Acceptable number</th></tr>
<tr><td>A</td><td>d ≦ 0.5</td><td>neglected</td></tr>
<tr><td>B</td><td>0.5 < d ≦ 0.7</td><td>3</td></tr>
<tr><td>C</td><td>0.7 < d</td><td>0</td></tr>
</table>
</td></tr>
</table>

Inspection item	Judgement standard
Polarizer (Scratch, Bubble, Dent)	(1) Scratch



	Width (mm)	Length (mm)	Acceptable No.
A	W ≦ 0.1	—	neglected
B	0.1 ＜ W ≦0.3	L ≦ 5.0	neglected
C		5.0 ＜ L	0
D	0.3 ＜ W	—	0

(2)Bubble (dent)



d = (a + b) / 2

Category	Size (mm)	Acceptable number
A	d ≦ 0.2	neglected
B	0.2 ＜ d ≦ 0.3	5
C	0.3 ＜ d ≦ 0.5	3
D	0.5 ＜ d	0