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	LIQUID CRYSTAL DISPLAY GROUP SHARP CORPORATION SPECIFICATION	LIQUID CRYSTAL DISPLAY DIVISION I LIQUID CRYSTAL DISPLAY GROUP

DEVICE SPECIFICATION FOR

TFT-LCD Module

Model No. LK600D3LA3K

CUSTOMER'S APPROVAL

DATE

PRESENTED

BY _____

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SHARP CORPORATION

RECORDS OF REVISION

MODEL No. : LK600D3LA3K

SPEC No. : LD-K22102A

SPEC No.	DATE	REVISED No.	PAGE	SUMMARY	NOTE
LD-K22102	2010.1.20	-	-	-	1st ISSUE

	2010.6.28	A		- Reformat all over the pages.
				- Correction to misdescriptions. ▲1
				  ➢ Addition of the equivalent circuit. (P3,4)
				  ➢ Correction of Inverter spec.(P7,8,12)
				  ➢ Correction to piling number of one packing unit.(P18)
				  ➢ Correction of the caution label. (P21)
				  ➢ Addition of the description about UL. (P21)
				- Application of user's requests. ▲2
				  ➢ Addition of packing specification items.(P18)
					2nd ISSUE

1. Application

This specification applies to the color 60.0" TFT-LCD module LK600D3LA3K.

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2. Overview

This module is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver ICs, control circuit, power supply circuit, inverter circuit and back light system etc. Graphics and texts can be displayed on a 1920×RGB×1080 dots panel with one billion colors by using 8bit+FRC LVDS (Low Voltage Differential Signaling) to interface, +12V of DC supply voltages.

This module also includes the DC/AC inverter to drive the CCFT. (+24V of DC supply voltage)

And in order to improve the response time of LCD, this module applies the Over Shoot driving (O/S driving) technology for the control circuit .In the O/S driving technology, signals are being applied to the Liquid Crystal according to a pre-fixed process as an image signal of the present frame when a difference is found between image signal of the previous frame and that of the current frame after comparing them.

With this technology, image signals can be set so that liquid crystal response completes within one frame. As a result, motion blur reduces and clearer display performance can be realized.

This LCD module also adopts Double Frame Rate driving method.

With combination of these technologies, motion blur can be reduced and clearer display performance can be realized.

3. Mechanical Specifications

Parameter	Specifications	Unit
Display size	152.496 (Diagonal)	cm
	60.0 (Diagonal)	inch
Active area	1329.12(H) x 747.63 (V)	mm
Pixel Format	1920(H) x 1080(V) (1pixel = R + G + B dot)	pixel
Pixel pitch	0.69225(H) x 0.69225 (V)	mm
Pixel configuration	R, G, B vertical stripe	
Display mode	Normally black	
Open Cell Outline Dimensions [Note1]	1401.1(H) x 820.4(V) x 43.0(D)	mm
Mass	25 $\pm$ 1	kg
Surface treatment	Glare Hard coating: 2H and more	

[Note1] Outline dimensions are shown in P22, P23.

4. Input Terminals

4.1. Interface and block diagram
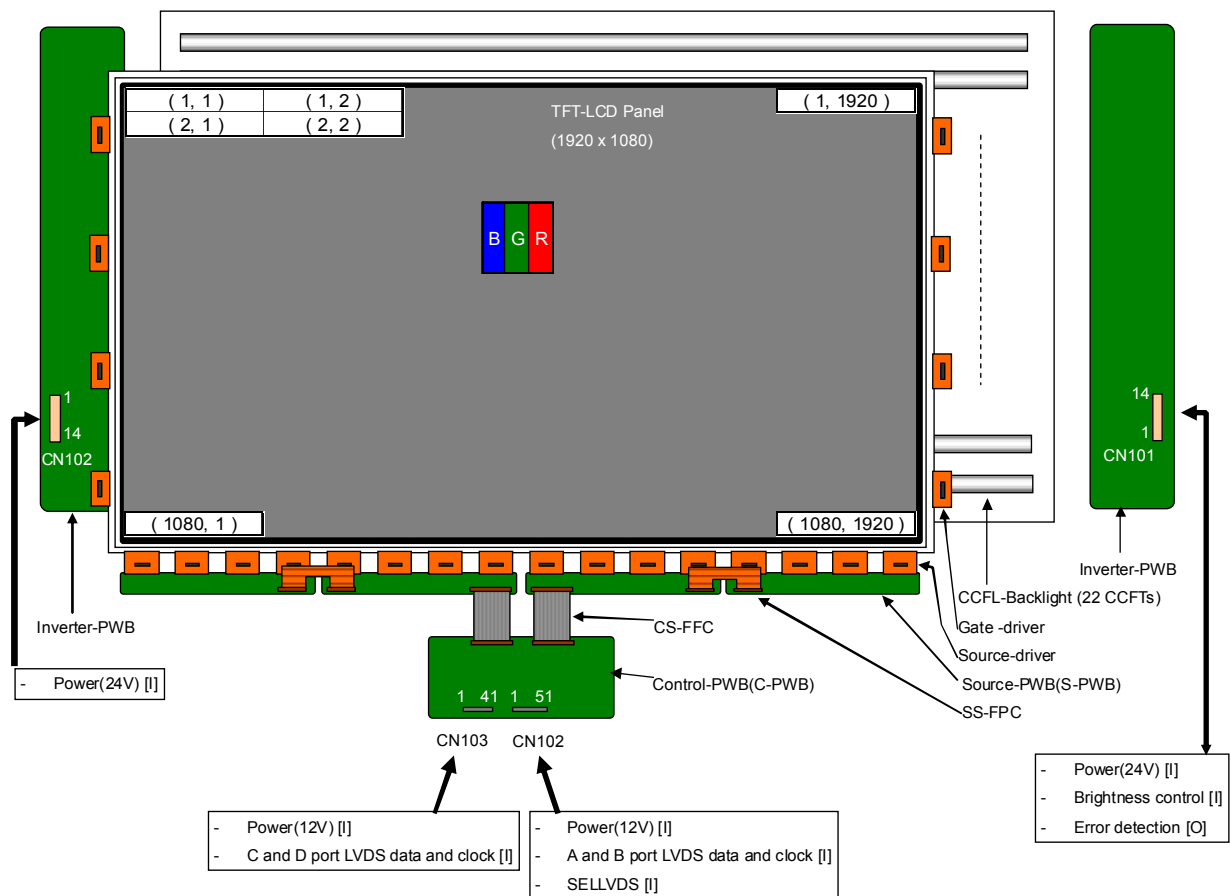
4.2. TFT panel driving

CN102 of C-PWB: Power and LVDS signal input

- Using connector: FI-RNE51SZ-HF (Japan Aviation Electronics Ind., Ltd.)
- Mating connector: FI-RE51HL, FI-RE51CL (Japan Aviation Electronics Ind., Ltd.)
- Mating LVDS transmitter: THC63LVD1023 or equivalent device

| Pin No.	Symbol	Function	Remark
1	GND		
2	Reserved	N.C	Pull up: 3.3V [Note1 ▲1]
3	Reserved	N.C	Pull up: 3.3V [Note1 ▲1]
4	Reserved	N.C	
5	Reserved	N.C	
6	Reserved	N.C	
7	SELLVDS	Select LVDS data order [Note3]	Pull down: (GND) [Note2]
8	Reserved	N.C	
9	Reserved	N.C	
10	Reserved	N.C	
11	GND		
12	AIN0-	Aport (-)LVDS CH0 differential data input	
13	AIN0+	Aport (+)LVDS CH0 differential data input	
14	AIN1-	Aport (-)LVDS CH1 differential data input	
15	AIN1+	Aport (+)LVDS CH1 differential data input	
16	AIN2-	Aport (-)LVDS CH2 differential data input	
17	AIN2+	Aport (+)LVDS CH2 differential data input	
18	GND		
19	ACK-	Aport LVDS Clock signal(-)	
20	ACK+	Aport LVDS Clock signal(+)	
21	GND		
22	AIN3-	Aport (-)LVDS CH3 differential data input	
23	AIN3+	Aport (+)LVDS CH3 differential data input	
24	AIN4-	Aport (-)LVDS CH4 differential data input	
25	AIN4+	Aport (+)LVDS CH4 differential data input	
26	GND		
27	GND		
28	BIN0-	Bport (-)LVDS CH0 differential data input	
29	BIN0+	Bport (+)LVDS CH0 differential data input	
30	BIN1-	Bport (-)LVDS CH1 differential data input	
31	BIN1+	Bport (+)LVDS CH1 differential data input	
32	BIN2-	Bport (-)LVDS CH2 differential data input	
33	BIN2+	Bport (+)LVDS CH2 differential data input	
34	GND		
35	BCK-	Bport LVDS Clock signal(-)	
36	BCK+	Bport LVDS Clock signal(+)	
37	GND		
38	BIN3-	Bport (-)LVDS CH3 differential data input	
39	BIN3+	Bport (+)LVDS CH3 differential data input	
40	BIN4-	Bport (-)LVDS CH4 differential data input	
41	BIN4+	Bport (+)LVDS CH4 differential data input	
42	GND		
43	GND		
44	GND		
45	GND		
46	GND		
47	VCC	+12V Power Supply	
48	VCC	+12V Power Supply	
49	VCC	+12V Power Supply	
50	VCC	+12V Power Supply	
51	VCC	+12V Power Supply	

CN103 of C-PWB: Power and LVDS signal input

- Using connector: FI-RNE41SZ-HF (Japan Aviation Electronics Ind., Ltd.)
- Mating connector: FI-RE41HL, FI-RE41CL (Japan Aviation Electronics Ind., Ltd.)

Pin No.	Symbol	Function	Remark
1	VCC	+12V Power Supply	
2	VCC	+12V Power Supply	
3	VCC	+12V Power Supply	
4	VCC	+12V Power Supply	
5	Reserved		
6	Reserved		
7	Reserved		
8	Reserved		
9	GND		
10	CIN0-	Cport (-)LVDS CH0 differential data input	
11	CIN0+	Cport (+)LVDS CH0 differential data input	
12	CIN1-	Cport (-)LVDS CH1 differential data input	
13	CIN1+	Cport (+)LVDS CH1 differential data input	
14	CIN2-	Cport (-)LVDS CH2 differential data input	
15	CIN2+	Cport (+)LVDS CH2 differential data input	
16	GND		
17	CCK-	Cport LVDS Clock signal(-)	
18	CCK+	Cport LVDS Clock signal(+)	
19	GND		
20	CIN3-	Cport (-)LVDS CH3 differential data input	
21	CIN3+	Cport (+)LVDS CH3 differential data input	
22	CIN4-	Cport (-)LVDS CH4 differential data input	
23	CIN4+	Cport (+)LVDS CH4 differential data input	
24	GND		
25	GND		
26	DIN0-	Dport (-)LVDS CH0 differential data input	
27	DIN0+	Dport (+)LVDS CH0 differential data input	
28	DIN1-	Dport (-)LVDS CH1 differential data input	
29	DIN1+	Dport (+)LVDS CH1 differential data input	
30	DIN2-	Dport (-)LVDS CH2 differential data input	
31	DIN2+	Dport (+)LVDS CH2 differential data input	
32	GND		
33	DCK-	Dport LVDS Clock signal(-)	
34	DCK+	Dport LVDS Clock signal(+)	
35	GND		
36	DIN3-	Dport (-)LVDS CH3 differential data input	
37	DIN3+	Dport (+)LVDS CH3 differential data input	
38	DIN4-	Dport (-)LVDS CH4 differential data input	
39	DIN4+	Dport (+)LVDS CH4 differential data input	
40	GND		
41	GND		

[Note] GND of a liquid crystal panel drive part has connected with a module chassis.

[Note1] The equivalent circuit figure of the terminal.

▲1
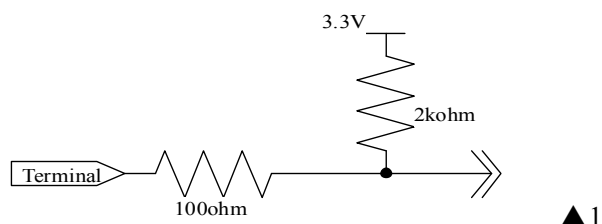
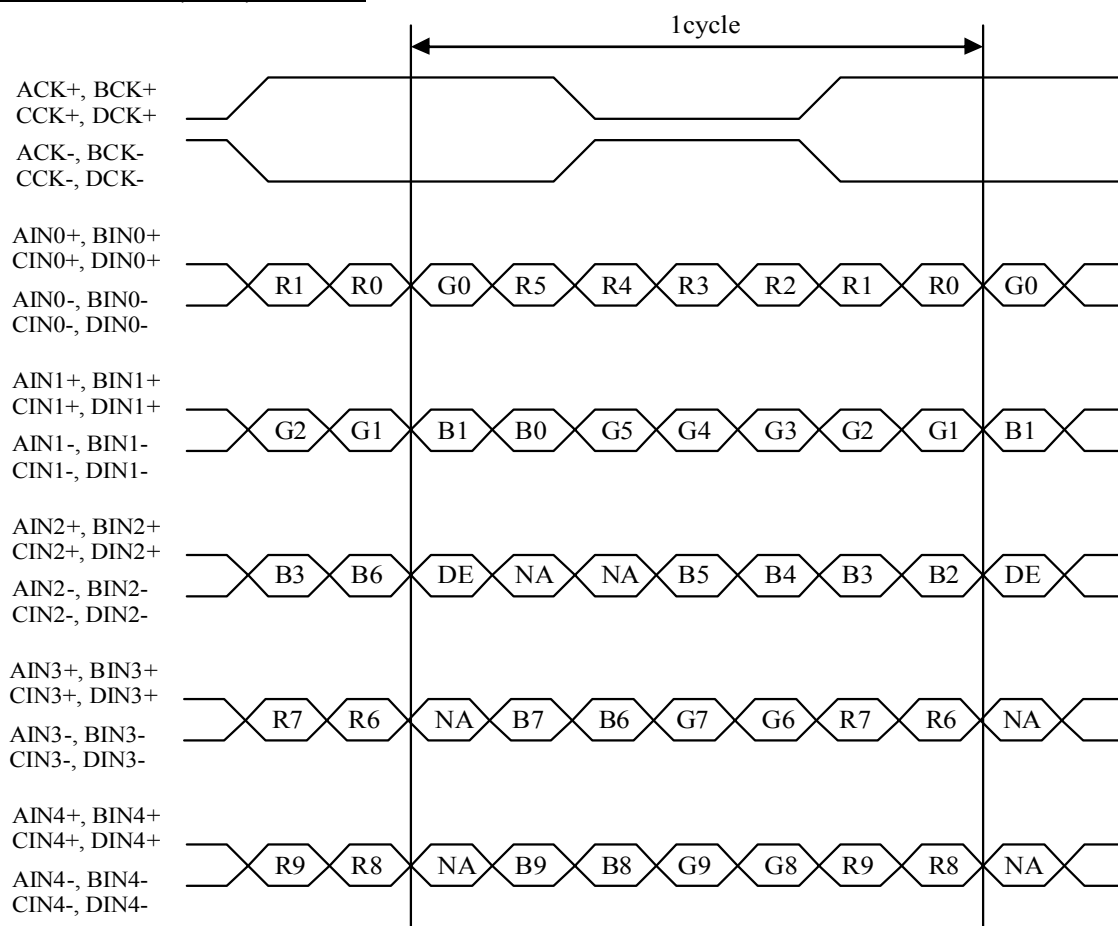[Note2] The equivalent circuit figure of the terminal.
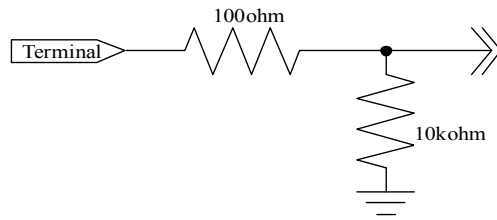
[Note3] LVDS Data order

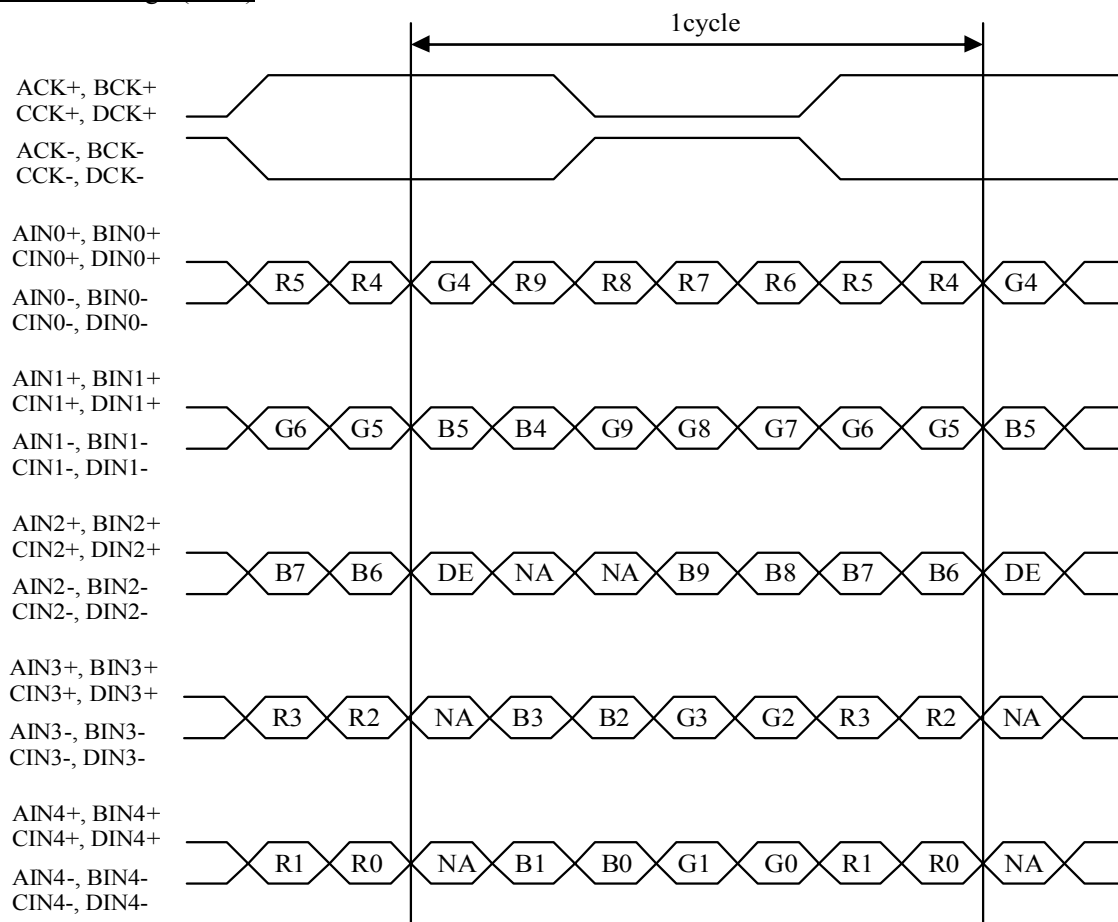| SELLVDS		
Data	L(GND) or OPEN [VESA]	H(3.3V) [JEIDA]
TA0	R0(LSB)	R4
TA1	R1	R5
TA2	R2	R6
TA3	R3	R7
TA4	R4	R8
TA5	R5	R9(MSB)
TA6	G0(LSB)	G4
TB0	G1	G5
TB1	G2	G6
TB2	G3	G7
TB3	G4	G8
TB4	G5	G9(MSB)
TB5	B0(LSB)	B4
TB6	B1	B5
TC0	B2	B6
TC1	B3	B7
TC2	B4	B8
TC3	B5	B9(MSB)
TC4	NA	NA
TC5	NA	NA
TC6	DE(*)	DE(*)
TD0	R6	R2
TD1	R7	R3
TD2	G6	G2
TD3	G7	G3
TD4	B6	B2
TD5	B7	B3
TD6	N/A	N/A
TE0	R8	R0(LSB)
TE1	R9(MSB)	R1
TE2	G8	G0(LSB)
TE3	G9(MSB)	G1
TE4	B8	B0(LSB)
TE5	B9(MSB)	B1
TE6	N/A	N/A

NA: Not Available
(*)Since the display position is prescribed by the rise of DE(Display Enable) signal, please do not fix DE signal during operation at "High".

SELLVDS= Low (GND) or OPEN

1cycle

ACK+, BCK+ CCK+, DCK+

ACK-, BCK- CCK-, DCK-

AIN0+, BIN0+ CIN0+, DIN0+

AIN0-, BIN0- CIN0-, DIN0-

R1 R0 G0 R5 R4 R3 R2 R1 R0 G0

AIN1+, BIN1+ CIN1+, DIN1+

AIN1-, BIN1- CIN1-, DIN1-

G2 G1 B1 B0 G5 G4 G3 G2 G1 B1

AIN2+, BIN2+ CIN2+, DIN2+

AIN2-, BIN2- CIN2-, DIN2-

B3 B6 DE NA NA B5 B4 B3 B2 DE

AIN3+, BIN3+ CIN3+, DIN3+

AIN3-, BIN3- CIN3-, DIN3-

R7 R6 NA B7 B6 G7 G6 R7 R6 NA

AIN4+, BIN4+ CIN4+, DIN4+

AIN4-, BIN4- CIN4-, DIN4-

R9 R8 NA B9 B8 G9 G8 R9 R8 NA

SELLVDS= High (3.3V)

1cycle

ACK+, BCK+ CCK+, DCK+

ACK-, BCK- CCK-, DCK-

AIN0+, BIN0+ CIN0+, DIN0+

AIN0-, BIN0- CIN0-, DIN0-

R5 R4 G4 R9 R8 R7 R6 R5 R4 G4

AIN1+, BIN1+ CIN1+, DIN1+

AIN1-, BIN1- CIN1-, DIN1-

G6 G5 B5 B4 G9 G8 G7 G6 G5 B5

AIN2+, BIN2+ CIN2+, DIN2+

AIN2-, BIN2- CIN2-, DIN2-

B7 B6 DE NA NA B9 B8 B7 B6 DE

AIN3+, BIN3+ CIN3+, DIN3+

AIN3-, BIN3- CIN3-, DIN3-

R3 R2 NA B3 B2 G3 G2 R3 R2 NA

AIN4+, BIN4+ CIN4+, DIN4+

AIN4-, BIN4- CIN4-, DIN4-

R1 R0 NA B1 B0 G1 G0 R1 R0 NA

DE: Display Enable, NA: Not Available (Fixed Low)

4.3. Backlight driving

CN101 of Inverter-PWB: +24V DC power supply and inverter control

- Using connector: 20022WR-14AML(YEONHO)
- Mating connector: 20022HS-14L (YEONHO) or equivalent

Pin No.	Symbol	Function	Default(OPEN)	Input Impedance (min)	Remark
1	V_{INV}	+24V	-		
2	V_{INV}	+24V	-		
3	V_{INV}	+24V	-		
4	V_{INV}	+24V	-		
5	V_{INV}	+24V	-		
6	GND		-		
7	GND		-		
8	GND		-		
9	GND		-		
10	GND		-		
11	ERR	Error Detection		Open Collector	[Note1]
12	Von/off	Inverter ON/OFF	Inverter OFF	min.196kohm ▲1	[Note2]
13	Reserved	For LCD module internal usage, should be open			
14	Pdim	Brightness Control	3.3V : pull up Brightness 100%	min.235kohm ▲1	[Note3]

CN102 of Inverter-PWB: +24V DC power supply

- Using connector: 20022WR-14AML (YEONHO)
- Mating connector: 20022HS-14L (YEONHO) or equivalent

| Pin No.	Symbol	Function	Default(OPEN)	Input Impedance	Remark
1	V_{INV}	+24V	-		
2	V_{INV}	+24V	-		
3	V_{INV}	+24V	-		
4	V_{INV}	+24V	-		
5	V_{INV}	+24V	-		
6	GND		-		
7	GND		-		
8	GND		-		
9	GND		-		
10	GND		-		
11	Reserved	For LCD module internal usage, should be open			
12	Reserved	For LCD module internal usage, should be open			
13	Reserved	For LCD module internal usage, should be open			
14	Reserved	For LCD module internal usage, should be open			

[Note1] Error Detection

	MIN	TYP	MAX
Normal	-	-	0.8V ▲1
Abnormal	(Open Collector)		

[Note2] Inverter ON/OFF

Input voltage	Function
0V	Inverter : OFF
3.3V	Inverter : ON

[Note3] Brightness Control (Pulse Dimming)

Pin No.14 is used for the control of the PWM duty with input pulse from (100Hz to 240Hz).
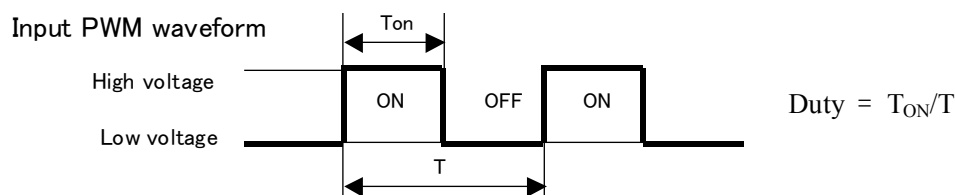
$$Duty = T_{ON}/T$$

		MIN	TYP	MAX	Remark
Pulse signal	[Hz]	100	-	240	
DUTY(T_{ON}/T)	[%]	15	<->	100	Ta=25°C
Dimming level (luminance ratio)	[%]	10	<->	100	Ta=25°C Pulse signal=(120Hz)
Low voltage	V	-	0	0.6	
High voltage	V	3.0	3.3	3.6	

[Note] In case of using Pulse Dimming, be careful so that the Pdim signal (Pin 14) doesn't have glitch. ▲1

4.4. The backlight system characteristics

The backlight system is direct type with 22 CCFTs (Cold Cathode Fluorescent Tube).
The characteristics of the lamp are shown in the following table. The value mentioned below is at the case of one CCFT.

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Life time	T_L	-	60000	-	Hour	[Note]

[Note]
- Lamp life time is defined as the time when brightness becomes 50% of the original value in the continuous operation under the condition of Ta=25°C and brightness control (V_{BRT}=100%).
- Above value is applicable when the long side of LCD module is placed horizontally (Landscape position).
  (Lamp lifetime may vary if LCD module is in portrait position due to the change of mercury density inside the lamp.)

5. Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Unit	Remark
Input voltage (for Control)	V_I	Ta=25°C	-0.3 ~ 3.6	V	[Note1]
12V supply voltage (for Control)	VCC	Ta=25°C	0 ~ + 14	V	
Input voltage (for Inverter)	V_{ON} V_{BRT} V_{BRT} sel	Ta=25°C	0 ~ + 6	V	
24V supply voltage (for Inverter)	V_{INV}	Ta=25°C	0 ~ +29	V	
Storage temperature	Tstg	-	-25 ~ +60	°C	[Note2]
Operation temperature (Ambient)	Topa	-	0 ~ +50	°C	

[Note 1] SELLVDS

[Note 2] Humidity 95%RH Max.(Ta≤40°C)

　　　　Maximum wet-bulb temperature at 39°C or less. (Ta>40°C)

　　　　No condensation.

6. Electrical Characteristics

6.1. Control circuit driving

Ta=25°C

Parameter		Symbol	Min.	Typ.	Max.	Uniit	Remark
+12V supply voltage	Supply voltage	Vcc	11.4	12	12.6	V	[Note 1]
	Current dissipation	Icc	-	0.8	2.9	A	[Note 2]
	Inrush current	$I_{RUSH}1$	-	7.5	-	A	t1=500us [Note 6]
		$I_{RUSH}2$	-	3.4	-	A	t1>5ms
Permissible input ripple voltage		V_{RP}	-	-	100	mV_{P-P}	Vcc = +12.0V
Input Low voltage		V_{IL}	0	-	0.7	V	[Note 3]
Input High voltage		V_{IH}	2.3	-	3.3	V	
Input leak current (Low)		I_{IL1}	-	-	100	μA	$V_I = 0V$ [Note 4]
Input leak current (High)		I_{IH1}	-	-	100	μA	$V_I = 3.3V$ [Note 4]
Terminal resistor		R_T	-	100	-	Ω	Differential input
Input Differential voltage		$|VID|$	200	400	600	mV	[Note 5]
Differential input common mode voltage		VCM	$|VID|/2$	1.2	2.4-$|VID|/2$	V	[Note 5]

[Note] V_{CM}: Common mode voltage of LVDS driver.

[Note1]

Input voltage sequences

0 < t1 < 20ms

20ms < t2 < 5s

20ms < t3 < 5s

0 < t4 < 1s

1s < t5-1

1s < t5-2

0 < t6 -1

0 < t6 -2

1s < t7

Dip conditions for supply voltage

a) V2 ≤ Vcc < V1

td < 10ms

b) Vcc < V2

This case is based on input voltage sequences.
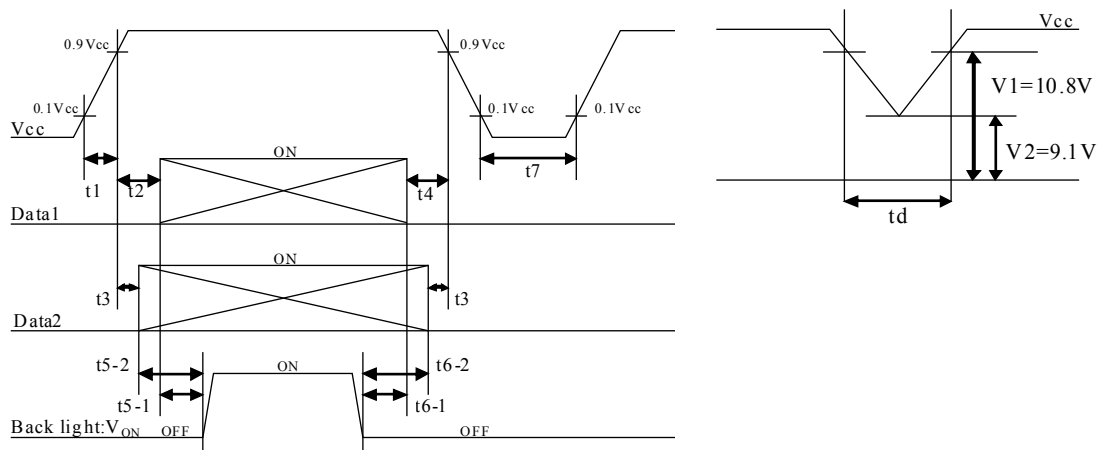
※ Data1: ACK±, AIN0±, AIN1±, AIN2±, AIN3±, AIN4±,BCK±, BIN0±, BIN1±, BIN2±, BIN3±, BIN4±
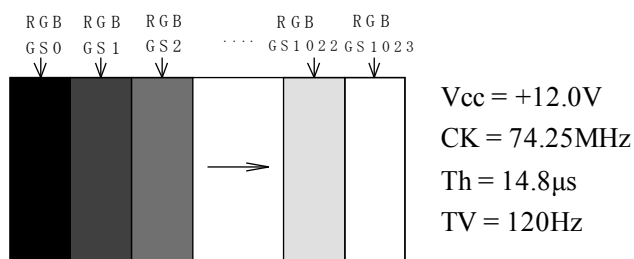CCK±, CIN0±, CIN1±, CIN2±, CIN3±, CIN4±, DCK±, DIN0±, DIN1±, DIN2±, DIN3±, DIN4±
*V_{CM} voltage pursues the sequence mentioned above.

※ Data2: SELLVDS

[Note] About the relation between data input and backlight lighting, please base on the above-mentioned input sequence. When back light is switched on before panel operation or after a panel operation stop, it may not display normally. But this phenomenon is not based on change of an incoming signal, and does not give damage to a liquid crystal display.

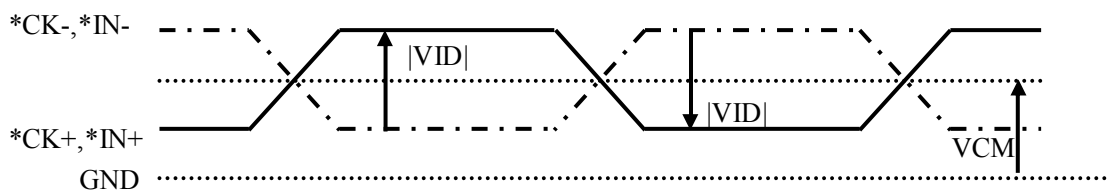[Note2] Typical current situation: 1024 gray-bar patterns. (Vcc = +12.0V)
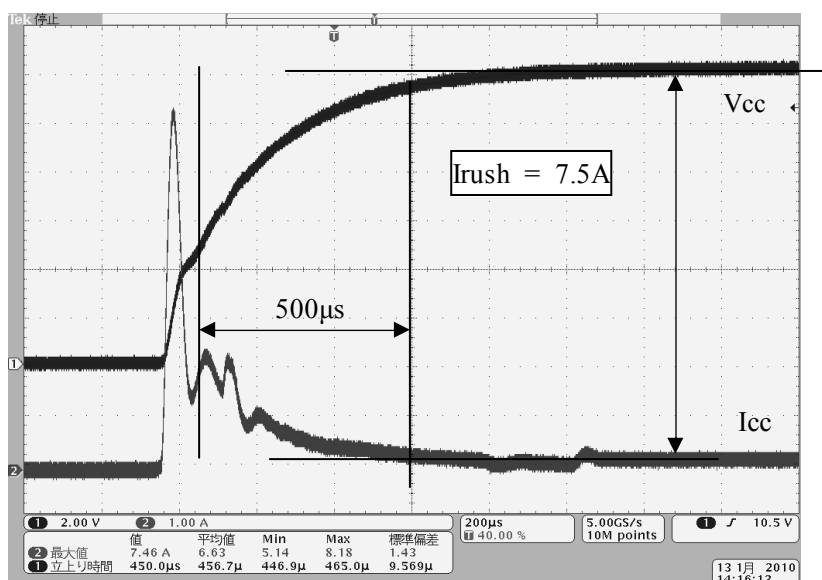The explanation of RGB gray scale is seen in section 8.


```
RGB   RGB   RGB           RGB     RGB
GS0   GS1   GS2    ....   GS1022  GS1023
```

Vcc = +12.0V
CK = 74.25MHz
Th = 14.8μs
TV = 120Hz

[Note3] SELLVDS

[Note4] SELLVDS

[Note5] ACK±, AIN0±, AIN1±, AIN2±, AIN3±, AIN4±, BCK±, BIN0±, BIN1±, BIN2±, BIN3±, BIN4±
CCK±, CIN0±, CIN1±, CIN2±, CIN3±, CIN4±, DCK±, DIN0±, DIN1±, DIN2±, DIN3±, DIN4±

[Note6] Vcc12V inrush current waveform


Irush = 7.5A

500μs

6.2. Inverter driving for backlight

The back light system is direct type with 22 CCFTs (Cold Cathode Fluorescent Tube).

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
+24V	Current dissipation 1	I_{INV1}	-	14.0	15.5	A	V_{INV} = 24V, Ta = 25°C DUTY = 100% [Note 1,2]
	Current dissipation 2 ▲1	I_{INV2}	-	12.2	13.7	A	
	Inrush current	I_{RUSH}	-	-	15.5	A	
	Supply voltage	V_{INV}	22.8	24.0	25.2	V	
Permissible input ripple voltage		V_{RF}	-	-	1.0	V_{p-p}	V_{INV} = +24.0V
Input voltage (Low)		V_{ONL}	0	-	0.8	V	$V_{ON/OFF}$, Pdim_sel
Input voltage (High)		V_{ONH}	2.3	-	3.6	V	
Operating frequency ▲1		fop	52	-	53	kHz	

[Note1] 1) V_{INV}-turn-on condition
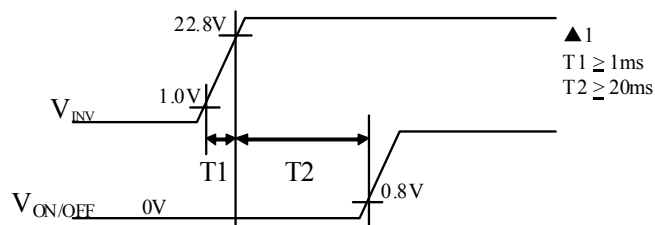
2) V_{INV}-turn-off condition
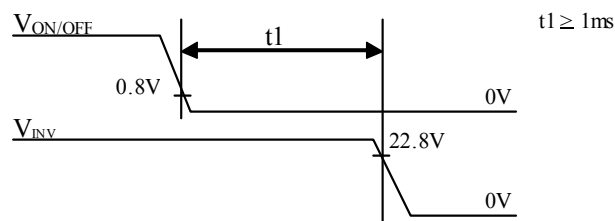
[Note2] Current dissipation 1: Definition within 60 minutes after turn on. (Rush current is excluded.)
　　　　Current dissipation 2: Definition more than 60minutes after turn on.
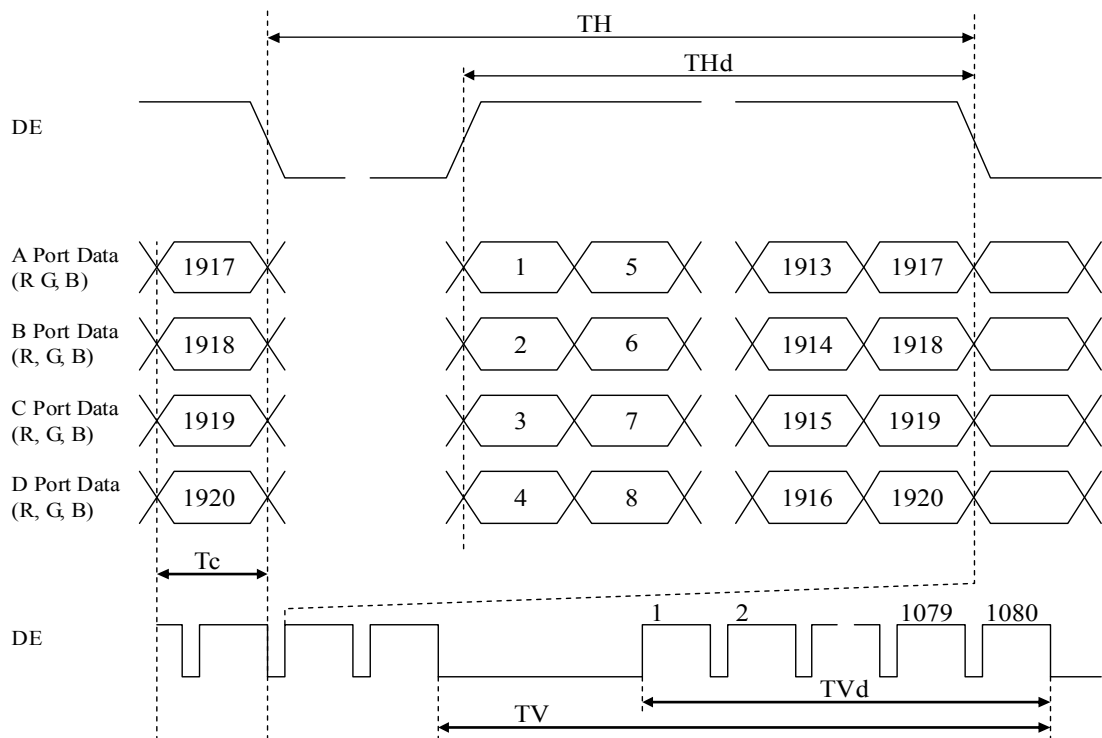
7. Timing characteristics of input signals

7.1. Timing characteristics

Timing diagrams of input signal are shown in below figure.

| Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Clock	Frequency	1/Tc	67	74.25	80.0	MHz	
Data enable signal	Horizontal period	TH	525	550	650	clock	
			7.1	7.41	8.0	μs	
	Horizontal period (High)	THd	480	480	480	clock	
	Vertical period	TV	1120	1125	1400	line	
			94	120	122	Hz	
	Vertical period (High)	TVd	1080	1080	1080	line	

[Note]

- When vertical period is very long, flicker and etc. may occur.
- Please turn off the module after it shows the black screen.
- Please make sure that length of vertical period should become of an integral multiple of horizontal length of period. Otherwise, the screen may not display properly.
- As for your final setting of driving timing, we will conduct operation check test at our side, please inform your final setting.

Timing diagram of input signal

7.2. LVDS signal characteristics
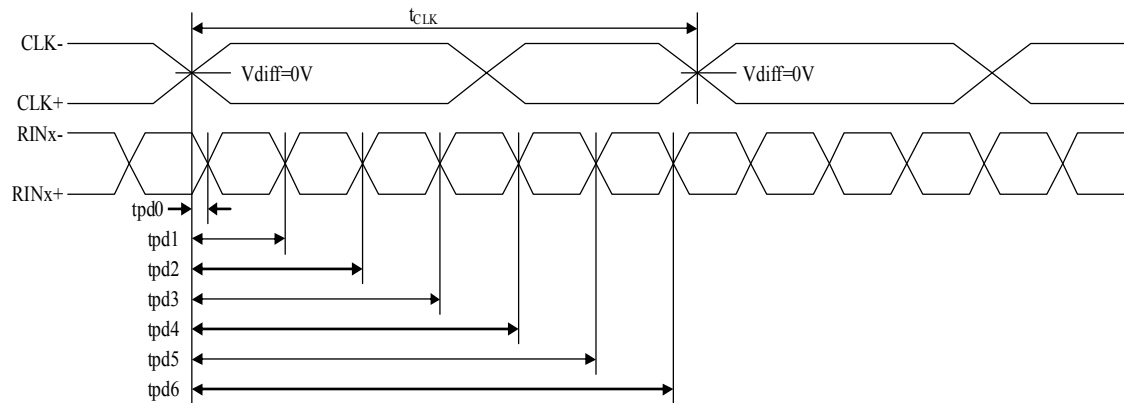
Item		Symbol	Min.	Typ.	Max.	Unit
Data position	Delay time, CLK rising edge to serial bit position 0	tpd0	-0.25	0	0.25	ns
	Delay time, CLK rising edge to serial bit position 1	tpd1	$1*t_{CLK}/7-0.25$	$1*t_{CLK}/7$	$1*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 2	tpd2	$2*t_{CLK}/7-0.25$	$2*t_{CLK}/7$	$2*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 3	tpd3	$3*t_{CLK}/7-0.25$	$3*t_{CLK}/7$	$3*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 4	tpd4	$4*t_{CLK}/7-0.25$	$4*t_{CLK}/7$	$4*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 5	tpd5	$5*t_{CLK}/7-0.25$	$5*t_{CLK}/7$	$5*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 6	tpd6	$6*t_{CLK}7-0.25$	$6*t_{CLK}/7$	$6*t_{CLK}/7+0.25$	

8. Input Signal, Basic Display Colors and Gray Scale of Each Color

Colors & Gray Scale			R0 R1 R2 R3 R4 R5 R6 R7 R8 R9	G0 G1 G2 G3 G4 G5 G6 G7 G8 G9	B0 B1 B2 B3 B4 B5 B6 B7 B8 B9
Basic Color	Black	–	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
	Blue	–	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1
	Green	–	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0
	Cyan	–	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1
	Red	–	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
	Magenta	–	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1
	Yellow	–	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0
	White	–	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1
Gray Scale of Red	Black	GS0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
	---	GS1	1 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
	---	GS2	0 1 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
	---	---			
	---	---			
	---	GS1021	1 0 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
	---	GS1022	0 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
	Red	GS1023	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
Gray Scale of Green	Black	GS0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
	---	GS1	0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
	---	GS2	0 0 0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
	---	---			
	---	---			
	---	GS1021	0 0 0 0 0 0 0 0 0 0	1 0 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0
	---	GS1022	0 0 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0
	Green	GS1023	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0
Gray Scale of Blue	Black	GS0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
	---	GS1	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0
	---	GS2	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0 0 0
	---	---			
	---	---			
	---	GS1021	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	1 0 1 1 1 1 1 1 1 1
	---	GS1022	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1 1
	Blue	GS1023	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1

- 0: Low level voltage / 1: High level voltage
- Each basic color can be displayed in 1024 gray scales from 10 bits data signals. According to the combination of total 30 bits data signals, one billion-color display can be achieved on the screen.

9. Optical characteristics

Ta=25°C, Vcc=12.0V, V_{INV}=24.0V, V_{BRT}=100%, Timing=120Hz (typ. value)

| Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	$\theta21$ $\theta22$	CR≧10	70	88	-	Deg.	[Note1,4]
	Vertical	$\theta11$ $\theta12$		70	88	-	Deg.	
Contrast ratio		CRn		3500	4500	-	-	[Note2,4]
Response time		τ_{DRV}			4		ms	[Note3,4,5]
Luminance	White	x	θ=0 deg.	Typ.-0.03	0.280	Typ.+0.03	-	[Note4]
		y		Typ.-0.03	0.290	Typ.+0.03	-	
	Red	x		Typ.-0.03	0.648	Typ.+0.03	-	
		y		Typ.-0.03	0.342	Typ.+0.03	-	
	Green	x		Typ.-0.03	0.286	Typ.+0.03	-	
		y		Typ.-0.03	0.602	Typ.+0.03	-	
	Blue	x		Typ.-0.03	0.144	Typ.+0.03	-	
		y		Typ.-0.03	0.073	Typ.+0.03	-	
Luminance	White	Y_L		400	500	-	cd/m^2	
Luminance uniformity	White	δw		-	-	1.6		[Note6]

- Measurement condition: Set the value of V_{BRT} to maximum luminance of white.
- The measurement shall be executed 60 minutes after lighting at rating.

[Note] The optical characteristics are measured using the following equipment.


Detector (EZ-CONTRAST/Photodiode)

Middle of the screen (θ=0°)

TFT-LCD Module
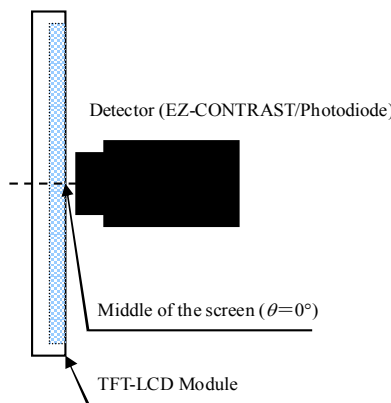
Measurement of viewing angle range and Response time.
-Viewing angle range: EZ-CONTRAST
- Response time: Photodiode

Detector (SR-3A-L1)

400mm

Field=1°

Middle of the screen (θ=0°)

TFT-LCD Module
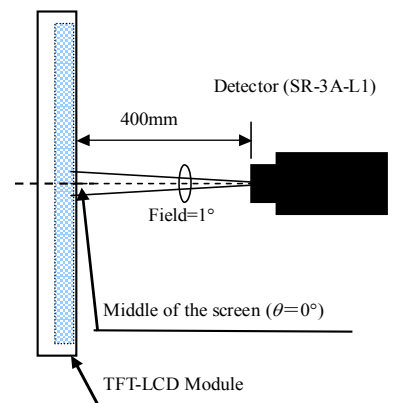
Measurement of Contrast, Luminance, Chromaticity.

[Note1] Definitions of viewing angle range:

Normal line

$\theta22$ $\theta11$ $\theta21$

$\theta12$

6 o'clock direction
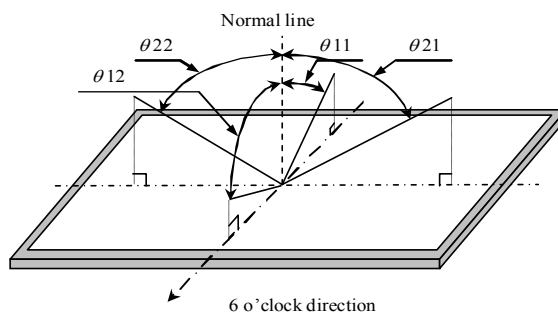
[Note2] Definition of contrast ratio

The contrast ratio is defined as the following.

$$\text{Contrast Ratio} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

[Note3] Definition of response time

The response time (τ_d and τ_r) is defined as the following figure and shall be measured by switching the input signal for "any level of gray (0%, 25%, 50%, 75% and 100%)" and "any level of gray (0%, 25%, 50%, 75% and 100%)".

	0%	25%	50%	75%	100%
0%		tr: 0%-25%	tr: 0%-50%	tr: 0%-75%	tr: 0%-100%
25%	td: 25%-0%		tr: 25%-50%	tr: 25%-75%	tr: 25%-100%
50%	td: 50%-0%	td: 50%-25%		tr: 50%-75%	tr: 50%-100%
75%	td: 75%-0%	td: 75%-25%	td: 75%-50%		tr: 75%-100%
100%	td: 100%-0%	td: 100%-25%	td: 100%-50%	td:100%-75%	

t*:x-y --- response time from level of gray(x) to level of gray(y)

$$\tau r = \Sigma(\text{tr}:x-y)/10, \quad \tau d = \Sigma(\text{td}:x-y)/10$$
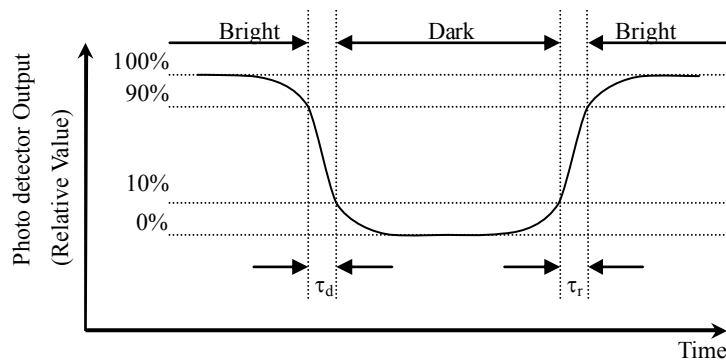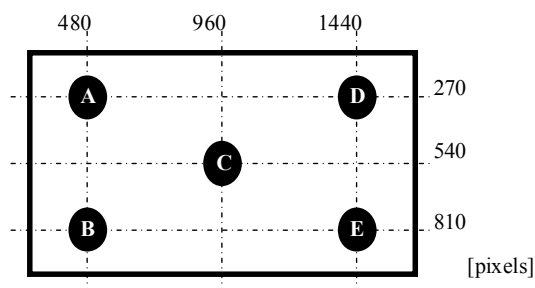

[Note4] This value shall be measured at center of the screen.

[Note5] This value is valid when O/S driving is used at typical input time value.

[Note6] This value is calculated as the following with five measurements. (A~E)

$$\delta w = \frac{\text{Maximum luminance of five points (brightness)}}{\text{Minimum luminance of five points (brightness)}}$$

10. Reliability test item

No.	Test item	Condition
1	High temperature storage test	Ta = 60°C, 240h
2	Low temperature storage test	Ta = -25°C, 240h
3	High temperature and high humidity operation test	Ta = 40°C, 95%RH, 240h (No condensation)
4	High temperature operation test	Ta = 50°C, 240h
5	Low temperature operation test	Ta = 0°C, 240h
6	Vibration test (non-operation)	Frequency: 10~57Hz/Vibration width (one side), 0.075mm : 58~500Hz/Acceleration: 9.8 m/s² Sweep time: 11 minutes Test period: 3 hours (1h for each direction of X, Y, Z)
7	Shock test (non-operation)	Maximum acceleration: 294m/s² Pulse width: 11ms, sinusoidal half wave Direction: +/-X, +/-Y, +/-Z, once for each direction.
8	ESD test	At the following conditions, it is a thing without incorrect operation and destruction. (1)Non-operation: Contact electric discharge ±10kV Non-contact electric discharge ±20kV (2)Operation: Contact electric discharge ±8kV Non-contact electric discharge ±15kV Conditions: 150pF, 330ohm

[Result evaluation criteria]

Under the display quality test condition with normal operation state, there shall be no change, which may affect practical display function.

11. Packing form ▲2

<One packing unit>
Size   1515(W) x 1120(D) x 1054(H) [mm]
Mass   250kg maximum
Piling number   4 maximum ▲1
<Component parts of one packing unit>
Mass of one box   226kg
 - Quantity   8 modules
 - Mass of one module   25kg ± 1kg
 - Total mass of cardboard   14kg
 - Total mass of cushion   4kg
Mass of palette   19kg
[Note] Outline dimensions are shown P24.

12. Carton storage condition

Temperature   0°C to 40°C
Humidity   95% RH or less
Reference condition 20°C to 35°C, 85% RH or less (summer)
                     5°C to 15°C, 85% RH or less (winter)
                     the total storage time (40°C, 95% RH) : 240h or less
Sunlight   Be sure to shelter a production from the direct sunlight.
Atmosphere   Harmful gas, such as acid and alkali which bites electronic components and/or wires must not be detected.
Notes   Be sure to put cartons on palette or base, don't put it on floor, and store them with removing from wall.
                     Please take care of ventilation in storehouse and around cartons, and control changing temperature is within limits of natural environment.
Storage life   1 year.

13. Label

13.1. Module Serial Label

a) Overview

This label is stuck on the backlight chassis.
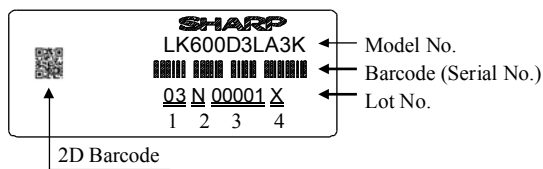
b) How to express Lot No.

Model No.	1	2	3	4
LK600D3LA3KX	(03)	N	(00001)	X
LK600D3LA3KJ	(03)	F	(00001)	J

Suffix Code

Serial No.

Factory Code
- N: NSEC
- F: D.ID

Production Year & Month

13.2. PPID Label

a) Overview

This label is stuck on the backlight chassis.

H: 70 x V: 15 mm

b) How to express and record

Model No.	1	2	3	4	5	6	7	8	9	10	11
LK600D3LA3KX	SP	00D00	0	I	L	SJ	A	NJ	0	(011)	(9999)
LK600D3LA3KJ	SP	00D01	0	I	L	SJ	A	CN	0	(011)	(9999)

Serial No.
- 0000~9999

Production date
- (ex. 2010.Jan.1st)

Module line
- No meaning

Module location
- NJ: Nanjing, China (NSEC)
- CN: Chunan, Korea (D.ID)

Cell line
- A: G10

Cell location
- SJ: Sakai, Japan

Gate IC
- L: TOSHIBA

Source IC
- I: SHARP

Revision
- 0: Rev.0

Model No. (Size & Resolution & Version)
00: 60inch   D: Full-HD   00: LK600D3LA3KX
                                01: LK600D3LA3KJ

Supplier code
- SP: SHARP

13.3. Packing Label

This label is stuck on the each packing box.

ex) LK600D3LA3KX

```
社内品番 : (4S) LK600D3LA3KX
         ┌─────────────────────┐
         │   Barcode(①)        │
         └─────────────────────┘
LotNO.    : (1T) 2010.  *.  **
     ┌──────────────────┐
     │  Barcode(②)      │
     └──────────────────┘
Quantity  : (Q)      *     pcs
     ┌──────────────────┐
     │  Barcode(③)      │
     └──────────────────┘
ユーザ品番  :
シャープ物流用ラベルです。
```

① Model No.& Suffix Code
② Lot No.
③ Quantity

14. Precautions

a) Be sure to turn off the power supply when inserting or disconnecting the cable.

b) This product is using the parts (inverter, CCFT etc), which generate the high voltage. Therefore, during operating, please don't touch these parts.

c) Brightness control voltage is switched for "ON" and "OFF", as shown in below figure. Voltage difference generated by this switching, $\triangle V_{INV}$, may affect a sound output, etc. when the power supply is shared between the inverter and its surrounding circuit. So, separate the power supply of the inverter circuit with the one of its surrounding circuit.
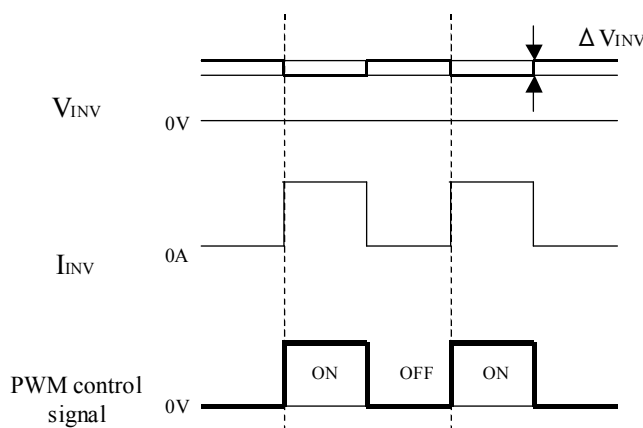
d) Be sure to design the cabinet so that the module can be installed without any extra stress such as warp or twist.

e) Since the front polarizer is easily damaged, pay attention not to scratch it.

f) Since long contact with water may cause discoloration or spots, wipe off water drop immediately.

g) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

h) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.

i) Since CMOS LSI is used in this module, take care of static electricity and take the human earth into consideration when handling.

j) The module has some printed circuit boards (PCBs) on the back side, take care to keep them form any stress or pressure when handling or installing the module; otherwise some of electronic parts on the PCBs may be damaged.

k) Observe all other precautionary requirements in handling components.

l) When some pressure is added onto the module from rear side constantly, it causes display non-uniformity issue, functional defect, etc. So, please avoid such design.

m) When giving a touch to the panel at power on supply, it may cause some kinds of degradation. In that case, once turn off the power supply, and turn on after several seconds again, and that is disappear.

n) When handling LCD module and assembling them into cabinets, please be noted that long-term storage in the environment of oxidization or deoxidization gas and the use of such materials as reagent, solvent, adhesive, resin, etc. which generate these gasses, may cause corrosion and discoloration of the LCD modules.

o) This LCD module is designed to prevent dust from entering into it. However, there would be a possibility to have a bad effect on display performance in case of having dust inside of LCD module. Therefore, please ensure to design your TV set to keep dust away around LCD module.

p) This LCD module passes over the rust.

q) Adjusting Vcom has been set optimally before shipment, so do not change any adjusted value. If adjusted value is changed, the specification may not be satisfied.

r) Disassembling the module can cause permanent damage and should be strictly avoided.

s) Please be careful since image retention may occur when a fixed pattern is displayed for a long time.

t) The chemical compound, which causes the destruction of ozone layer, is not being used.

u) Cold cathode fluorescent lamp in LCD PANEL contains a small amount of mercury. Please follow local ordinances or regulations for disposal. This sentence is displayed on the backside of the module by below label.

▲1
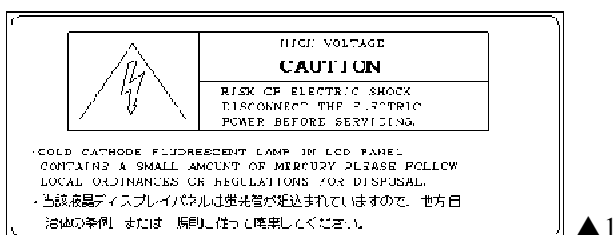
v) This LCD is appropriate to UL. Below figure shows the UL label. This label is stuck on the backlight chassis.
   ▲1

Factory code

w) This module is corresponded to RoHS.

x) When any question or issue occurs, it shall be solved by mutual discussion.

LD-K22102A-22

TFT-LCD MODULE OUTLINE DIMENSIONS

LK600D3LAxx

Section B-B

Detail:B
TOP 5PLACE

Detail:A
SIDE 6PLACE

Section A-A

68

43

63

1401.1(BEZEL OUTLINE)
1386
1220
620

1338.1(BEZEL OPENING)

1329.12(ACTIVE AREA)

747.63(ACTIVE AREA)

756.6(BEZEL OPENING)

ACTIVE AREA CENTER

BEZEL OPENING

ACTIVE AREA

1)TOLERANCE X-DIRECTION A:4.49±2.0
2)TOLERANCE Y-DIRECTION B:4.49±2.0
3)OBLIQUITY OF DISPLAY AREA |C-D|<2.0
BEZEL/DISPLAY POSITION

403
462

820.4(BEZEL OUTLINE)

9
43
39.8
27
2.6
2.5

6.5
25
5.5
11.6

25
5
12
6.5

23
27
39.8
43
7.05

NOTE)
1.UNSPECIFIED TOLERANCE TO BE ±2.0

TFT-LCD MODULE OUTLINE DIMENSIONS

LK600D3LA××

NOTE)
1. UNSPECIFIED TOLERANCE TO BE ±2.0

EMBOSS FOR MOUNTING
HEIGHT=7
φ4 dowel (Height:1.5mm)
M3
Detail:d
1 PLACE

EMBOSS FOR MOUNTING
HEIGHT=8
φ4 dowel (Height:1.5mm)
M4
Detail:e
4 PLACE

EMBOSS FOR MOUNTING
HEIGHT=3
Detail:f
1 PLACE

EMBOSS FOR MOUNTING
HEIGHT=7
φ4 dowel (Height:1.5mm)
Detail:f
2 PLACE

EMBOSS FOR MOUNTING
HEIGHT=7
M3
Detail:g
2 PLACE

EMBOSS FOR MOUNTING
HEIGHT=10
2-φ4 dowel (Height:1.5mm)
3-M4
M3
19.5
45.8
40
60
Detail:h
2 PLACE

EMBOSS FOR MOUNTING
HEIGHT=8
φ4 dowel (Height:1.5mm)
M4
Detail:c
1 PLACE

EMBOSS FOR MOUNTING
HEIGHT=3
φ4 dowel (Height:1.5mm)
M3
Detail:b
4 PLACE

EMBOSS FOR MOUNTING
HEIGHT=8
M4
Detail:a
8 PLACE

ANGLE FOR MOUNTING
HEIGHT=11

STUD FOR MOUNTING
HEIGHT=7
φ4 dowel (Height:1.5)
M3
Detail:x
1 PLACE

Section x-x

Section k-k

EMBOSS FOR MOUNTING
HEIGHT=12
φ3.4 dowel (Height:1.5mm)
45°
7.5
6.75
7.25
5.85
6.35
Detail:k
2 PLACE

EMBOSS FOR MOUNTING
HEIGHT=5

EMBOSS FOR MOUNTING
HEIGHT=7
φ4 dowel (Height:1.5mm)
M3
Detail:j
2 PLACE

EMBOSS FOR MOUNTING
HEIGHT=9
φ4 dowel (Height:1.5mm)
M4
Detail:i
4 PLACE

300.7
285
70
31.2
143.2
200
263.2
213

(121.15)
517.6
474.5
425.5
383
350
205
200
229
210
180.5
195
200
216.5
280
340
383
425.5
474.7
480
180.5
470
580.4
580.4

358.5
345.5
344.5
323
285
185
145.2
95
40.8
29.2
2.2
31.2
74.8
98.7
143.2
217.8
263.2
250
270
300
325
349
350
355
213

M4 M3

139.95
133.7
100
96.5
10

φ2.7Br
φ4 dowel (Height:1.5mm)

Parts Name	Material
Packing Case(Top)	Cardboard
Pack Add(Bottom)	PS
Pack Add(TopA)	PS
Pack Add(TopB)	PS
Packing Case(Front Frame)	Cardboard
Cardboard Prop	Cardboard
Plywood Palette	Plywoods
Antistatic Bag	PE(t=20μ)

Plywood Palette

PP BELT(x4)

60" Module

Antistatic Bag

R.C.

There is R.C. marking on the this side.

Packing Case(Top)

Packing Case(Front Frame)

Cardboard Prop

Pack Add(TopB)

60" Module

Pack Add(TopA)

Pack Add(Bottom)

LK600D3LA3K*

The Reliability Test Form
(Shock test & Vibration test)

Module Side : M4 (19 points)
Base Plate Side : M5 (23 points)

Base Plate

LK600D3LA3K

M5

Angle

M4

Angle

8-Stand Mounting

Please fix TV stand to this eight mounting
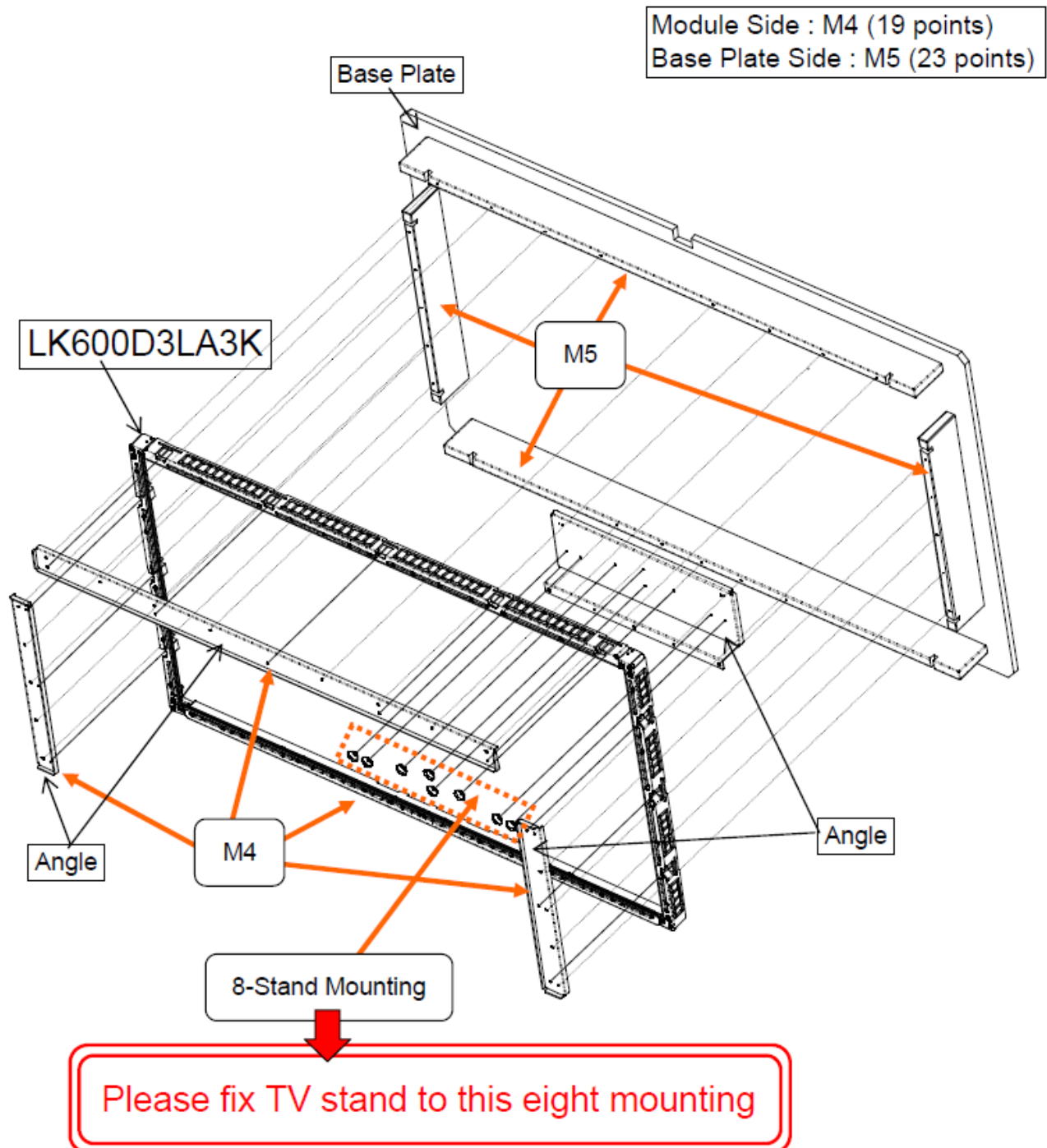
The reliability is guaranteed only when the following mount position is used to fix the module.