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| APPROVED BY: DATE | LIQUID CRYSTAL DISPLAY GROUP | PAGE    23 Pages |
| | SHARP CORPORATION | APPLICABLE DIVISION |
| | | ■DUTY PANEL DEVELOPMENT CENTER |
| | | □TFT DEVELOPMENT CENTER |
| | | □LCD PRODUCTS DEVELOPMENT CENTER |
| | | □EL PRODUCTION DEPT. |
| | S P E C I F I C A T I O N | |

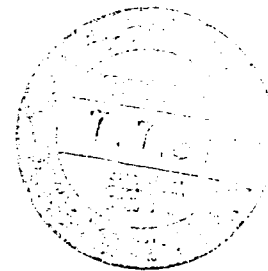DEVICE SPECIFICATION for

Passive Matrix COLOR LCD Module

(640×480 dots)

Model No.

# LM64C27P

□CUSTOMER'S APPROVAL

DATE _____

BY _____

PRESENTED

BY  FOR _J. C_____

Y.Inoue

DEPARTMENT GENERAL MANAGER

ENGINEERING DEPARTMENT II

DUTY PANEL DEVELOPMENT CENTER

LIQUID CRYSTAL DISPLAY GROUP

SHARP CORPORATION

# SHARP

| SPEC No. | MODEL No. |
|---|---|
| LC95415A | **LM64C27P** |

**DOC. FIRST ISSUE**

APR. 24. 1995

## RECORDS OF REVISION

**IDENT. DATA No.**

| DATE | REF. PAGE PARAGRAPH DRAWING No. | REVISED No. | SUMMARY | CHECK & APPROVAL |
|---|---|---|---|---|
| Feb.27.1995 | Page 2 , 17 | ⚠ | R E V I S E D (Viewing area) | *Y. Inoue* |
| | | | | |
| | | | | |
| | | | | |

1. Application
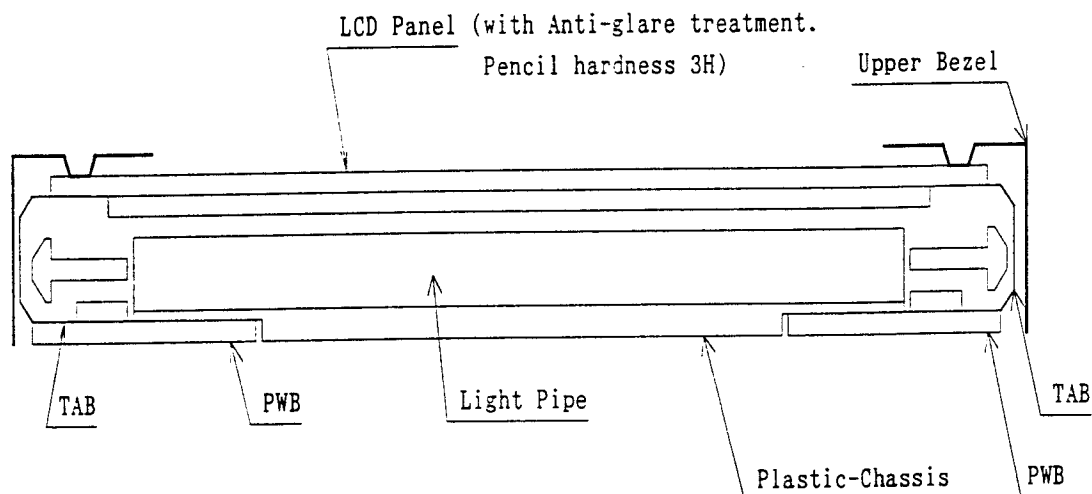
   This data sheet is to introduce the specification of LM64C26P, Passive Matrix type
   Color LCD Module.

2. Construction and Outline

   Construction: 640×480 dots color display module consisting of an LCD panel,
   PWB(printed wiring board) with electric components mounted onto,
   TAB(tape automated bonding) to connect the LCD panel and PWB
   electrically, and plastic chassis with CCFT back light and bezel
   to fix them mechanically.
   Signal ground(VSS) is connected with the metal bezel.
   DC/DC converter is built in.



LCD Panel (with Anti-glare treatment. Pencil hardness 3H)   Upper Bezel

TAB   PWB   Light Pipe   Plastic-Chassis   TAB   PWB

   Outline      : See Fig. 10
   Connection   : See Fig. 10 and Table 6

3. Mechanical Specifications

<u>Table 1</u>

| Parameter | Specifications | Unit |
|---|---|---|
| Outline dimensions | 221.0(W)×156.0(H)×8.2 MAX(D) | mm |
| Active area | 170.855(W)×128.135(H) | mm |
| Viewing area | 175.4(W)×132.7(H) | |
| Display format | 640(W)×480(H)  full dots | — |
| Dot size | 0.089×RGB(W)×0.267(H) | mm |
| Dot spacing | 0.025 | mm |
| *1 Base color | Normally black  *2 | — |
| Weight | Approx. 310 | g |

*1 Due to the characteristics of the LC material, the colors vary
   with environmental temperature.

*2 Negative-type display
   Display data "H" : ON  → transmission
   Display data "L" : OFF → light isolation

4. Absolute Maximum Ratings
 4-1 Electrical absolute maximum ratings

<u>Table 2</u>

| Parameter | Symbol | MIN. | MAX. | Unit | Remark |
|---|---|---|---|---|---|
| Supply voltage (Logic) | $V_{DD}-V_{SS}$ | 0 | 6.0 | V | Ta=25 ℃ |
| Input  voltage | $V_{IN}$ | -0.3 | $V_{DD}+0.3$ | V | Ta=25 ℃ |

4-2 Environmental Conditions

Table 3

| Item | Tstg | | Topr | | Remark |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| Ambient temperatuer | -25 ℃ | +60 ℃ | 0 ℃ | +40 ℃ | Note 4) |
| Humidity | Note 1) | | Note 1) | | No condensation |
| Vibration | Note 2) | | Note 2) | | 3 directions (X/Y/Z) |
| Shock | Note 3) | | Note 3) | | 6 directions (±X±Y±Z) |

Note 1) Ta≦40 ℃.....95 % RH Max

Ta＞40 ℃.....Absolute humidity shall be less than Ta=40 ℃/95 % RH.

Note 2)

Table 4

| Frequency | 10 Hz～57 Hz | 57 Hz～500 Hz |
|---|---|---|
| Vibration level | − | 9.8 m/s² |
| Vibration width | 0.075 mm | − |
| Interval | 10 Hz～500 Hz～10 Hz/11.0 min | |

2 hours for each direction of X/Y/Z (6 hours as total)

Note 3) Accerelation : 490 m/s²

Pulse width  : 11 ms

3 times for each direction of ±X/±Y/±Z

Note 4) Care should be taken so that the LCD module may not be subjected to the temperature out of this specification.

5. Electrical Specifications

5-1 Electrical characteristics

Table 5        Ta=25 ℃,$V_{DD}$=3.3 V±0.3V

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply voltage (Logic) | $V_{DD}-V_{SS}$ | Ta=0~40℃ | 3.0 | 3.3 | 3.6 | V |
| Contrast adjust voltage | Vcon -Vss | Ta=0 ℃ | 0.8 | — | — | V |
| | | Ta=25 ℃ | 1.35 | 1.95 | 2.55 | V |
| | | Ta=40 ℃ | — | — | 2.80 | |
| Input signal voltage | $V_{IN}$ | "H" level | $0.8V_{DD}$ | — | $V_{DD}+0.3$ | V |
| | | "L" level | -0.3 | — | $0.2V_{DD}$ | V |
| Input leakage current (Logic) | $I_{ILL}$ | "H" level | — | — | 1.0 | μA |
| | | "L" level | -1.0 | — | — | |
| | $I_{ILV}$ | Vcont=2.8V | -1.0 | — | 1.0 | mA |
| Supply current(Logic) | $I_{DD}$ | Note 2) | — | 180 | 270 | mA |
| Power consumption | Pd | Note 2) | — | 600 | 900 | mW |
| Rush Current (Logic) | $I_{DD}$ | Ta=25 ℃,Note 1)-① | — | — | 2 A × 5 | ms |
| | | Ta=25 ℃,Note 1)-② | — | — | 1 A × 0.6 | ms |

Note 1) Under the following conditions.;Logic voltage($V_{DD}$) should be designed

to supply following Inrush current.

① Immediately after the rise of DISP signal.

② Under the situation that DISP signal is on and kept steady.

Vdd

YD etc

DISP

Idd
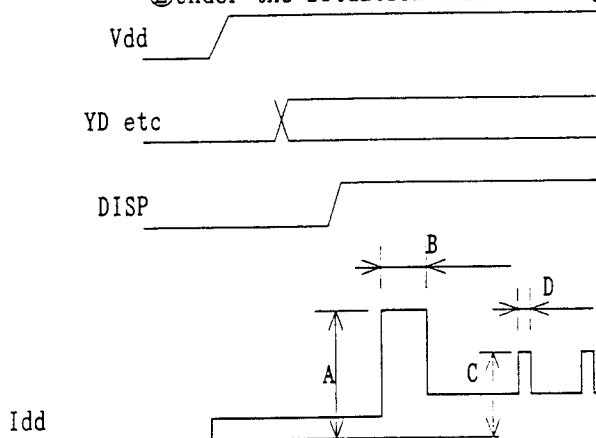
Measurement Curcuit:TMD-18-3
(Vdd Power Supply) (TAKASAGO)

A: 2   A   MAX

B: 5   ms MAX

C: 1   A   MAX

D: 0.6   ms MAX

Note 2) Under the following conditions.;

Vcon-Vss : contrast max.(1.95 V TYP)

$V_{DD}$-Vss=3.3 V,Frame frequency=73 Hz,Display pattern = black/white stripe pattern.

Display pattern ■■■■■■■■■■■■■■■■■■■■■■
□□□□□□□□□□□□□□□□□□□□□
■■■■■■■■■■■■■■■■■■■■■■
□□□□□□□□□□□□□□□□□□□□□

This value is direct current.

5-3 Interface signals

○LCD　　　　　　　　　　Table 6

| Pin No | Symbol | Description | Level |
|---|---|---|---|
| 1 | DU0 | Display data signal (Upper) | H(ON), L(OFF) |
| 2 | $V_{ss}$ | Ground potential | — |
| 3 | DU1 | Display data signal (Upper) | H(ON), L(OFF) |
| 4 | YD | Scan start-up signal | "H" |
| 5 | DU2 | Display data signal (Upper) | H(ON), L(OFF) |
| 6 | LP | Input data latch signal | "H"→"L" |
| 7 | DU3 | Display data signal (Upper) | H(ON), L(OFF) |
| 8 | $V_{ss}$ | Ground potential | — |
| 9 | $V_{ss}$ | Ground potential | |
| 10 | XCK | Data input clock signal | "H"→"L" |
| 11 | DL4 | Display data signal (Lower) | H(ON), L(OFF) |
| 12 | $V_{CON}$ | Contrast adjust voltage | — |
| 13 | DL5 | Display data signal (Lower) | H(ON), L(OFF) |
| 14 | $V_{DD}$ | Power supply for logic and LCD(3.3 V) | — |
| 15 | $V_{ss}$ | Ground potential | — |
| 16 | $V_{DD}$ | Power supply for logic and LCD(3.3 V) | — |
| 17 | DL6 | Display data signal (Lower) | H(ON), L(OFF) |
| 18 | DISP | Display control signal | H(ON), L(OFF) |
| 19 | DL7 | Display data signal (Lower) | H(ON), L(OFF) |
| 20 | NC | — | — |
| 21 | $V_{ss}$ | Ground potential | — |
| 22 | DU7 | Display data signal (Upper) | H(ON), L(OFF) |
| 23 | DL0 | Display data signal (Lower) | H(ON), L(OFF) |
| 24 | DU6 | Display data signal (Upper) | H(ON), L(OFF) |
| 25 | DL1 | Display data signal (Lower) | H(ON), L(OFF) |
| 26 | DU5 | Display data signal (Upper) | H(ON), L(OFF) |
| 27 | $V_{ss}$ | Ground potential | — |
| 28 | DU4 | Display data signal (Upper) | H(ON), L(OFF) |
| 29 | DL2 | Display data signal (Lower) | H(ON), L(OFF) |
| 30 | $V_{ss}$ | Ground potential | — |
| 31 | DL3 | Display data signal (Lower) | H(ON), L(OFF) |

○CCFT

| Pin No | Symbol | Description | Level |
|---|---|---|---|
| 1 | HV | High voltage lineal (from Inverter) | — |
| 2 | NC | | — |
| 3 | GND | Ground line (from Inverter) | — |

NOTE) Pin No. and its location are shown in Fig.10.

○LCD

　　　Used　connector:DF9B-31P-1V (HIROSE)

　　　Mating connector:DF9B-31S-1V (HIROSE)

○CCFT

　　　Used　connector:BHR-03VS-1　(JST)

　　　Mating connector:SM03(4.0)B-BHS or SM02(8.0)B-BHS (JST)

　　Except above connector shall be out of guaranty

COLUMN

(1,1) (1,2) (1,639) (1,640)

(2,1) (2,2) (2,639) (2,640)

ROW

6 4 0×3 (R G B)
×4 8 0 d o t s

(479,1) (479,2) (479,639)(479,640)

(480,1) (480,2) (480,639)(480,640)

☐: Lower SEG Drivers
Lower data(DL0～7)

▨: Upper SEG Drivers
Upper data(DU0～7)

Fig.1 Dot chart of display area

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| DU7 | R(1,1) | B(1,3) | G(1,6) | | R(1,9) | B(1,11) | G(1,14) |
| DU6 | G(1,1) | R(1,4) | B(1,6) | | G(1,9) | R(1,12) | B(1,14) |
| DU5 | B(1,1) | G(1,4) | R(1,7) | | B(1,9) | G(1,12) | R(1,15) |
| DU4 | R(1,2) | B(1,4) | G(1,7) | | R(1,10) | B(1,12) | G(1,15) |
| DU3 | G(1,2) | R(1,5) | B(1,7) | | G(1,10) | R(1,13) | B(1,15) |
| DU2 | B(1,2) | G(1,5) | R(1,8) | | B(1,10) | G(1,13) | R(1,16) |
| DU1 | R(1,3) | B(1,5) | G(1,8) | | R(1,11) | B(1,13) | G(1,16) |
| DU0 | G(1,3) | R(1,6) | B(1,8) | | G(1,11) | R(1,14) | B(1,16) |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| DL7 | R(241,1) | B(241,3) | G(241,6) | | R(241,9) | B(241,11) | G(241,14) |
| DL6 | G(241,1) | R(241,4) | B(241,6) | | G(241,9) | R(241,12) | B(241,14) |
| DL5 | B(241,1) | G(241,4) | R(241,7) | | B(241,9) | G(241,12) | R(241,15) |
| DL4 | R(241,2) | B(241,4) | G(241,7) | | R(241,10) | B(241,12) | G(241,15) |
| DL3 | G(241,2) | R(241,5) | B(241,7) | | G(241,10) | R(241,13) | B(241,15) |
| DL2 | B(241,2) | G(241,5) | R(241,8) | | B(241,10) | G(241,13) | R(241,16) |
| DL1 | R(241,3) | B(241,5) | G(241,8) | | R(241,11) | B(241,13) | G(241,16) |
| DL0 | G(241,3) | R(241,6) | B(241,8) | | G(241,11) | R(241,14) | B(241,16) |

Fig.2 Data input timing chart

Table. 7 Interface timing ratings(Ta=0∼40 ℃,VDD=3.3 V±0.3 V)

| Item | Symbol | Rating MIN. | Rating TYP. | Rating MAX. | Unit |
|---|---|---|---|---|---|
| Frame cycle  *1 | tFRM | 7.69 | | 16.94 | ms |
| YD signal "H" level set up time | tHYS | 100 | | | ns |
| "H" level hold time | tHYH | 100 | | | ns |
| "L" level set up time | tLYS | 100 | | | ns |
| "L" level hold time | tLYH | 100 | | | ns |
| LP signal "H" level pulse width | tWLPH | 350 | | | ns |
| LP signal clock cycle    *3 | tLP | 10 | | 70 | us |
| XCK signal clock cycle | tCK | 82 | | | ns |
| "H" level clock width | tWCKH | 30 | | | ns |
| "L" level clock width | tWCKL | 30 | | | ns |
| Data set up time | tDS | 25 | | | ns |
| hold time | tDH | 30 | | | ns |
| LP↑ allowance time from XCK↓ | tLS | 200 | | | ns |
| XCK↑ allowance time from LP↓ | tLH | 200 | | | ns |
| Input signal rise/fall time  *2 | tr,tf | | | 20 | ns |

$V_{IH} = 0.8V_{DD}$
$V_{IL} = 0.2V_{DD}$
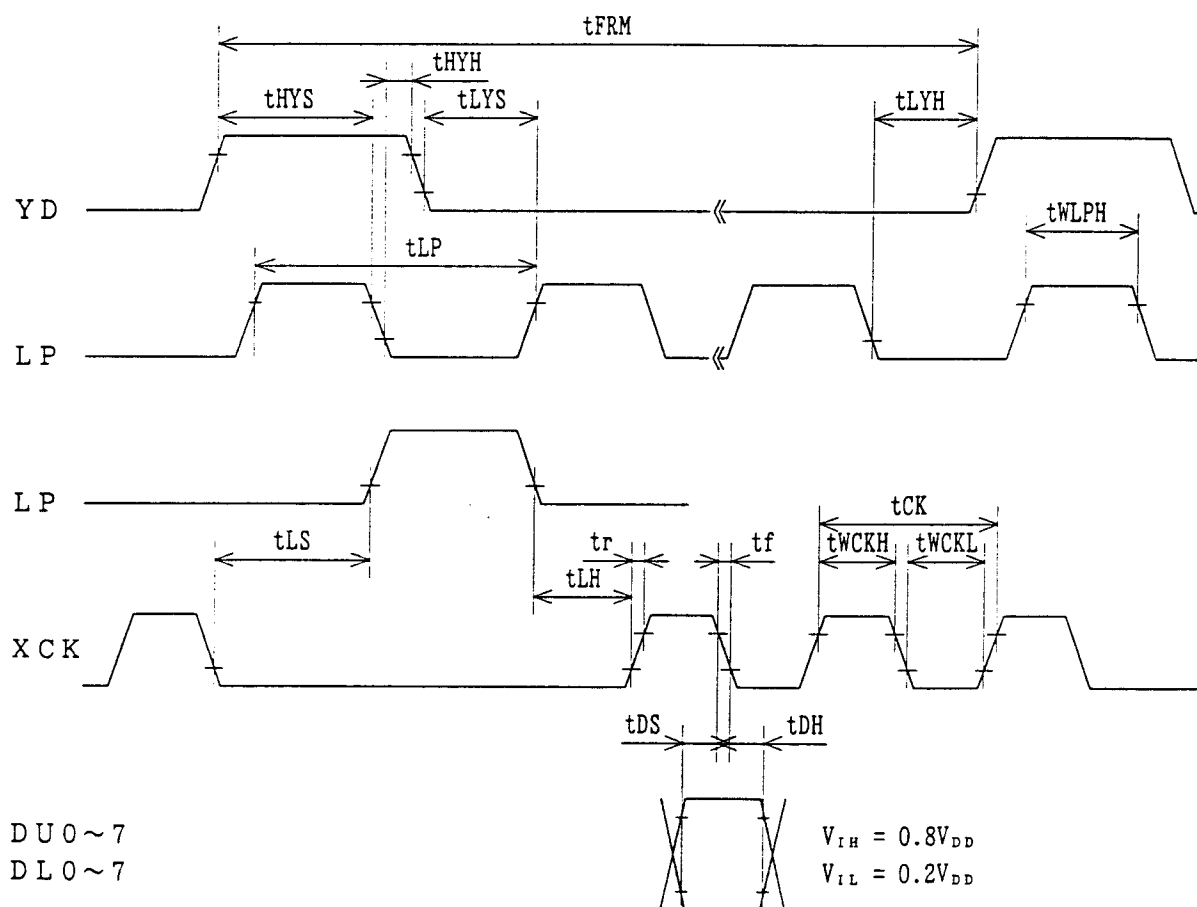
Fig. 3 Interface timing chart

*1 LCD unit functions at the minimum frme cycle of 7.69 ms(Maximum frame frequency of
130 Hz).
Owing to the characteristics of LCD unit,"shadowing" will become more eminent as
frame frequency goes up,whle flicker will be reduced.

According to our experiments,frame cycle of 12.8 ms Min. or frame frequency of 78 Hz
Max. will demonstrate optimum display quality in terms of flicker and "shadowing".
But since judgement of display quality is subjective and display quality such as
"shadowing" is patturn dependent,it is recommended that decision of frame frequency,
to which power consumption of the LCD unit is propotional,be made based on your
own through testing on the LCD unit with every possible patterns displayed on it.

*2 $(t_{CK}-t_{WCKH}-t_{WCKL})/2 \geqq 10$ ns ・・・10 ns MAX

$(t_{CK}-t_{WCKH}-t_{WCKL})/2 < 10$ ns ・・・$(t_{CK}-t_{WCKH}-t_{WCKL})/2$ MAX

*3 The intervals of 1 LP fall and the next must be always the same
when the LCD UNIT is active driving.
And LP's must be input continuously.

6. Module Driving Method

6.1 Circuit configuration

Fig.9 shows the block diagram of the module's circuitry.

6.2 Display Face Configuration

The display consists of 640×3(R,G,B)×480 dots as shown in Fig.1.

The interface is single panel with double drive to be driven at 1/244 duty ratio.

6.3 Input Data and Control Signal

The LCD driver is 240 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits. Input data for each row (640×3 R,G,B) will be sequentially transferred in the form of 8 bit parallel data through shift registers from top left of the display together with clock signal(XCK).

When input of one row (640 × 3,R,G,B dots) is completed, the data will be latched in the form of parallel data corresponding to the signal electrodes by the falling edge of latch signal (LP). Then, the corresponding drive signals will be transmitted to the 640 × 3 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal (YD) has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st row of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD. While the data of 1st row are being displayed, the data of 2nd row are entered. When data for 640×3 dots have been transferred, they will be latched by the falling edge of LP, switching the display to the 2nd row.

Such data input will be repeated up to the 240th row of each display segment, from upper row to lower rows, to complete one frame of display by time sharing method.

Simultaneously the same scanning sequence occur at the lower panel.

Then data input proceeds to the next display frame.

YD generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction in LC
materials, causing deterioration of the materials, drive wave-form shall be inverted
at every display frame to prevent the generation of such DC voltage. Control Signal
M plays such a role.

Because of the characteristics of the CMOS driver LSI, the power consumption of
the display module goes up with the clock frequency of XCK.
To minimize data transfer speed of XCK clock the LSI has the system
of transferring 8 bit parallel data through the 8 lines of shift registers.
Thanks to this system the power consumption of the display module is minimized.

In this circuit configuration, 8 bit display data shall input to data input
pins of DU0~7 and DL0~7.

Furthermore, the display module has bus line system for data input to minimize the
power consumption with data input terminals of each driver LSI being  activated
only when relevant data input is fed.

Data input for column electrodes and chip select of driver LSI are made as
follows:

The driver LSI at the left end of the display face is first selected, and the
adjacent driver LSI right next side is selected when data of 240 dot (30XCK)
is fed. This process is sequentially continued until data is fed to the driver
LSI at the right end of the display face. This process is followed simultaneously
both at the top and bottom column drivers LSI's.

Thus data input will be made through 8 bit bus line sequentially from the left
end of the display face.

Since this display module contains no refresh RAM, it requires the above data and
timing pulse inputs even for static display.

The timing chart of input signals are shown in Fig. 3 and Table 7.

7.Optical Characteristics

Ta = 25 ℃,$V_{DD}$ = 3.3 V,Vcon-$V_{SS}$ = Vmax

<u>Table 8</u>

Following spec are based upon the electrical measuring conditions,
on which the contrast of perpendicular direction ($\theta$x=$\theta$y=0 °)will be MAX.

| Parameter | | Symbol | Condition | | MIN. | TYP. | MAX. | Unit | Remark |
|---|---|---|---|---|---|---|---|---|---|
| Viewing angle range | | $\theta$x | Co>5.0 | $\theta$y= 0 ° | -30 | - | 30 | dgr. | Note1) |
| | | $\theta$y | | $\theta$x= 0 ° | -15 | - | 25 | dgr. | |
| Contrast ratio | | C o | $\theta$x= $\theta$y= 0 ° | | - | 25 | - | | Note2) |
| Response time | Rise | $\tau$ r | $\theta$x= $\theta$y= 0 ° | | - | 230 | 300 | ms | Note3) |
| | Decay | $\tau$ d | $\theta$x= $\theta$y= 0 ° | | - | 80 | 110 | ms | |
| Unit chromaticity | White | x | $\theta$x= $\theta$y= 0 ° | | - | 0.248 | - | — | |
| | | y | $\theta$x= $\theta$y= 0 ° | | - | 0.329 | - | — | |

Note 1) The viewing angle range is defined as shown Fig.4.

Note 2) Contrast ratio is defined as follows:

$$C o = \frac{\text{Luminance(brightness) all pixels ``White'' at Vmax}}{\text{Luminance(brightness) all pixels ``dark '' at Vmax}}$$

Vmax is defined in Fig.6.

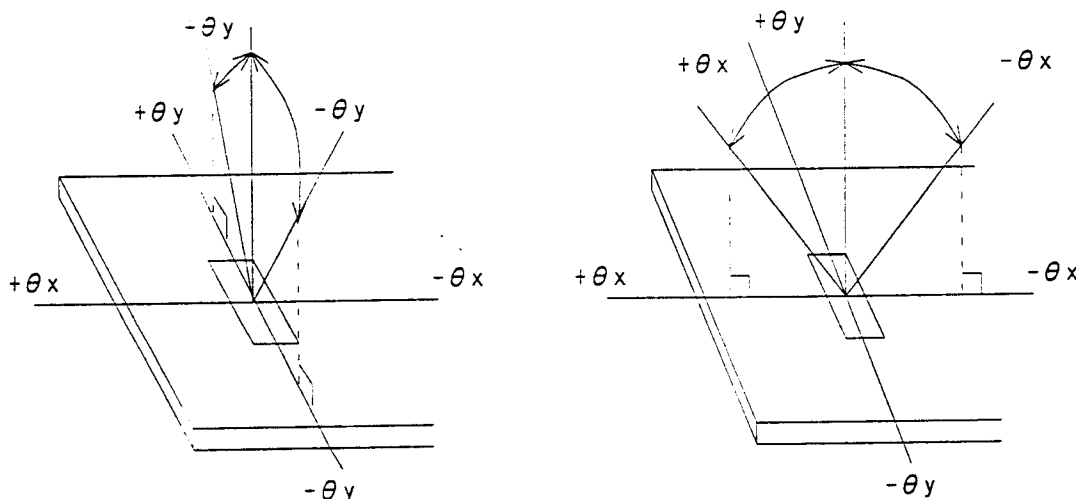

Fig.4   Definition of Viewing Angle

Note 3)  The response characteristics of photo-detector output are measured as
shown in Fig.7,assuming that input signals are applied so as to select
and deselect the dots to be measured, in the optical characteristics
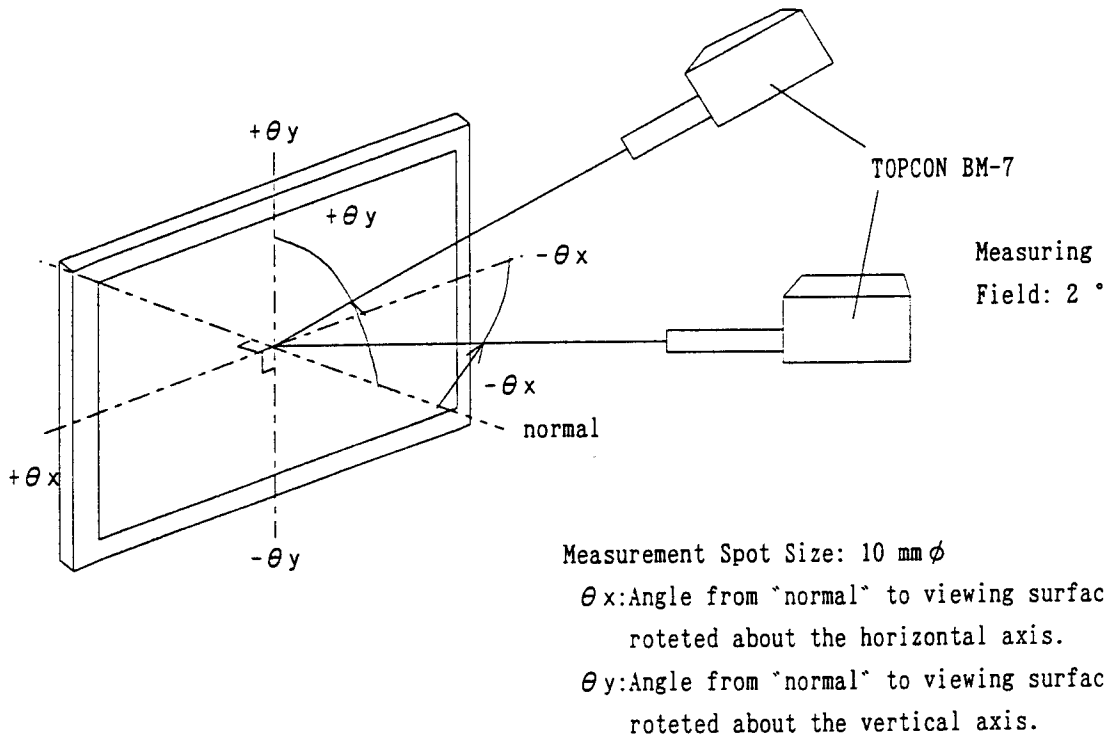test method shown in Fig.8.

TOPCON BM-7

Measuring
Field: 2 °

Measurement Spot Size: 10 mm $\phi$

$\theta$ x:Angle from "normal" to viewing surface
    roteted about the horizontal axis.

$\theta$ y:Angle from "normal" to viewing surface
    roteted about the vertical axis.

Fig. 5  Optical Characteristics Test Method I



Fig. 6  Definition of V$_{Max}$

Response time
Detector

TEKTRONIX
TYPE549
STORAGE
OSCILLOSCOPE

← Photo-detector

← Visual sensitivity
modulator

← Lens

$\theta$

Polarizer

→ Liquid crystal
panel

Light
source

Fig.7  Optical Characteristics Test Method II

[ Drive waveform ]

1/244 Duty Ratio

driving

voltage

Non-select
waveform ——×—— select waveform ——×—— Non-select
waveform

[ Response waveform ]

Photo-
detector
output

100 %  90 %

10 %

τr

τd

τr: Rise time
τd: Decay time
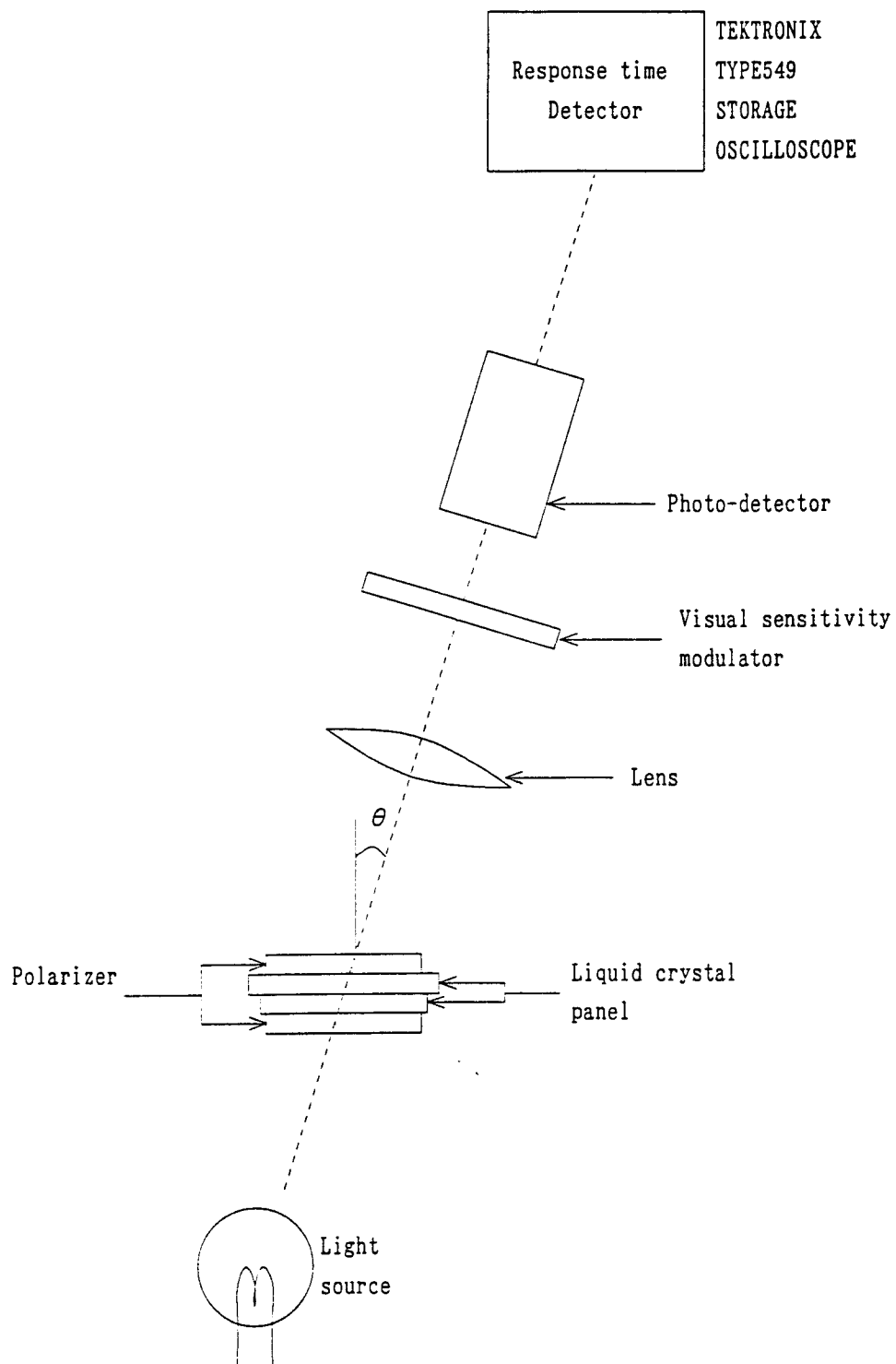
Fig.8  Definition of Response Time

DU0~DU7
DL0~DL7  CMOS
XCK      Buffer
LP       I.C.
YD
DISP

DISP

Sequence
Control
Circuit

*1 MG

COM Drivers

RGBR

RGBR

640×3(RGB)×480
LCD PANEL

SEG Drivers (Upper)
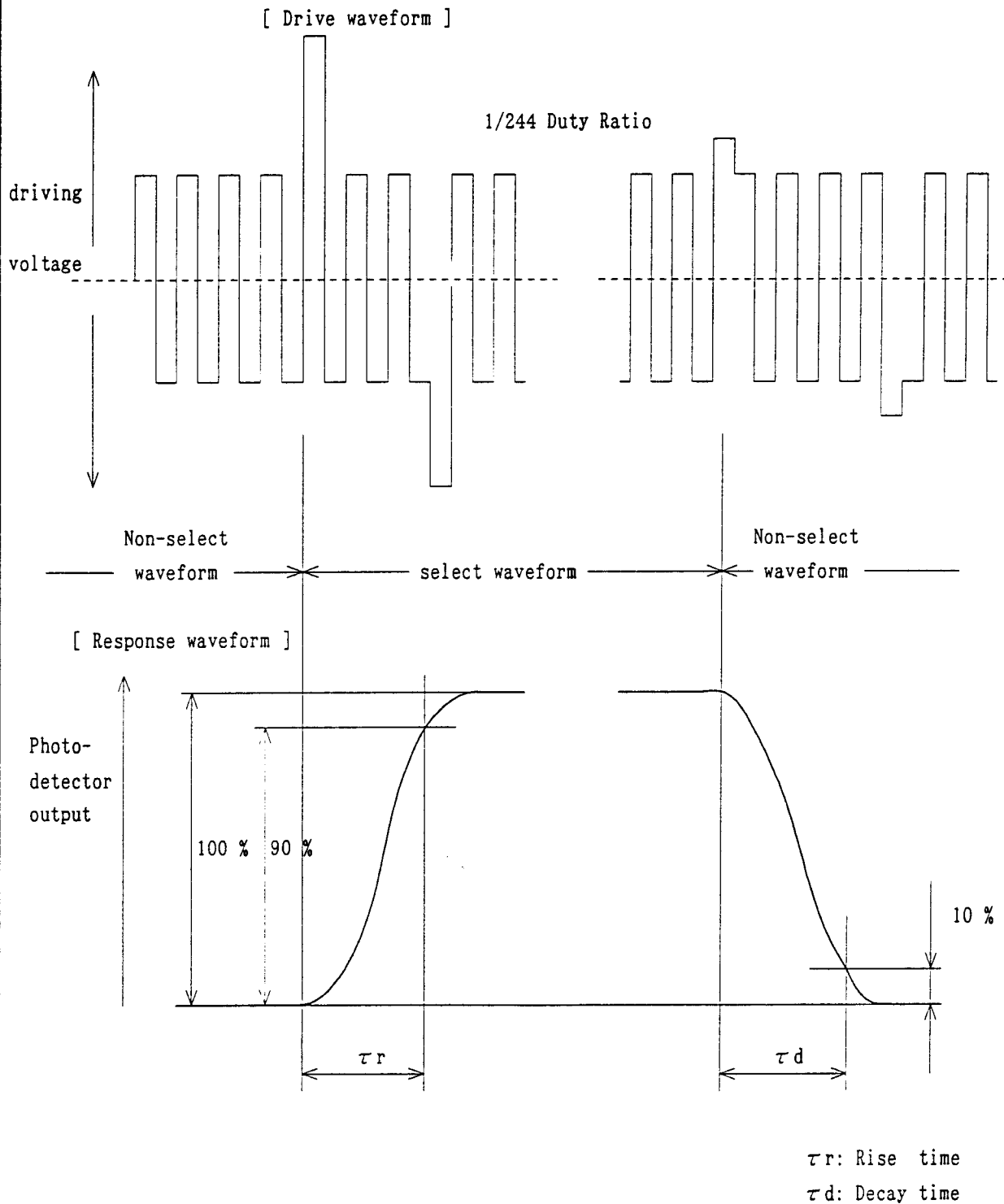
SEG Drivers (Lower)

Inverter

CCFT
B/L

*2 BG

VEE

V_DD
V_SS      DC/DC
Vcon     Converter
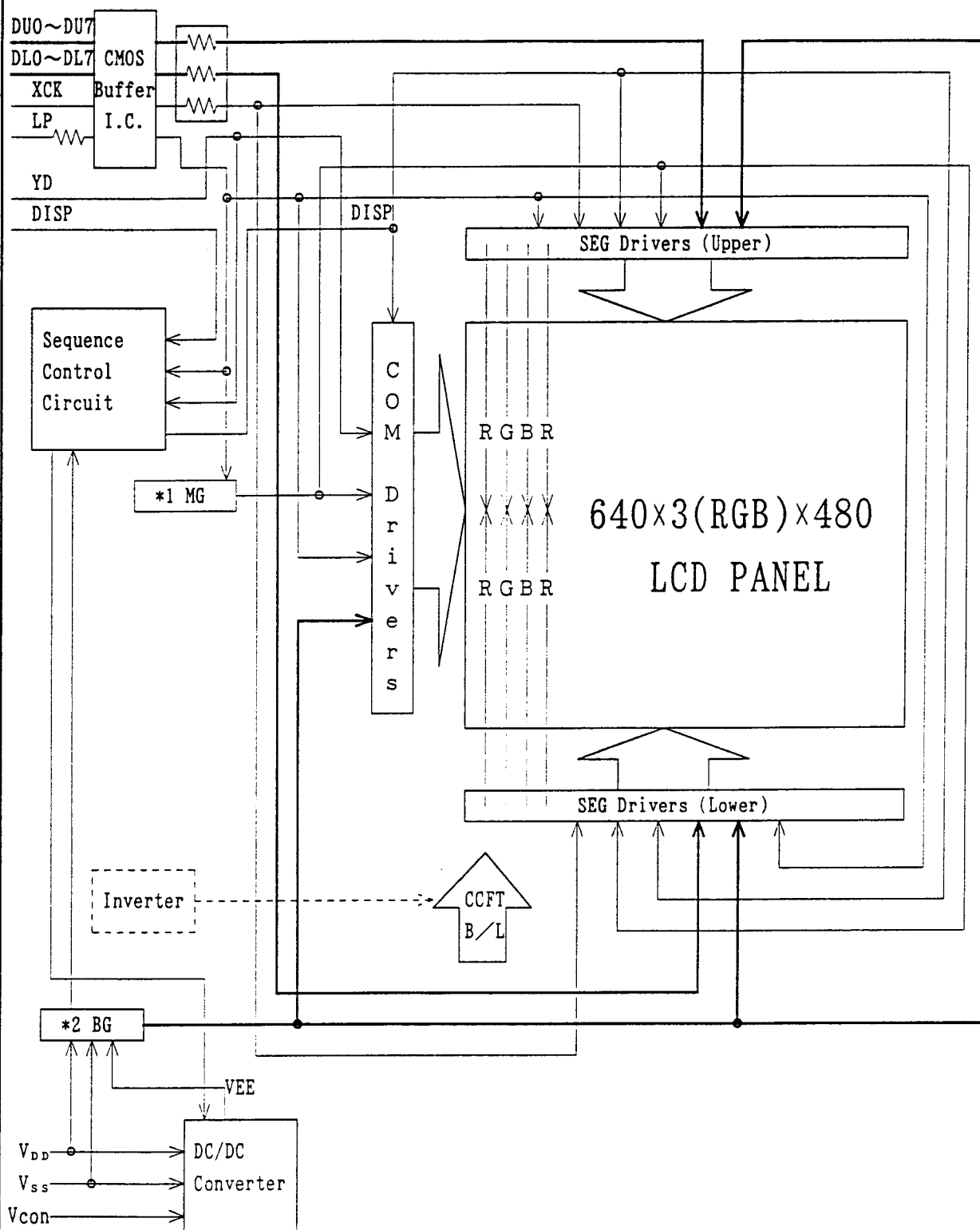
Fig.9 Circuit block diagram

*1 MG: M GENERATOR CIRCUIT
*2 BG: BIAS GENERATOR & PROTECTION CIRCUIT

A17

3:?.4

221:?.?

216:?.?

(108.95)

4.8:?.?
4.5:?.1

18.9:?.?

180.5:?.?(BEZEL OPENNING ARE

φ2.7:?.?

3min

3min

2-R1.5

2.3 △
2-5min

BLACK MAS

ACTIVE ARE

(73.2)

(BEZEL OPENNING AREA)

(105.25)

156:?.5
146.4:?.?

2.3 △
2-5min

137.4:?.?(BEZEL OPENNING AREA)

(32)

P0.089
0.064

31  30

①

1    2

| R | G | B | R | G |
|---|---|---|---|---|
| R | G | B | R | G | B |

P0.267
0.242

2-R1.35

2.3 △
2-5min

3min
3:?.?

640XR·

2.7:?.?

3.5min

2-R2

3min

215:?.4

7.7:?.?
4.35:?.?
2.5:?.?

3.5min
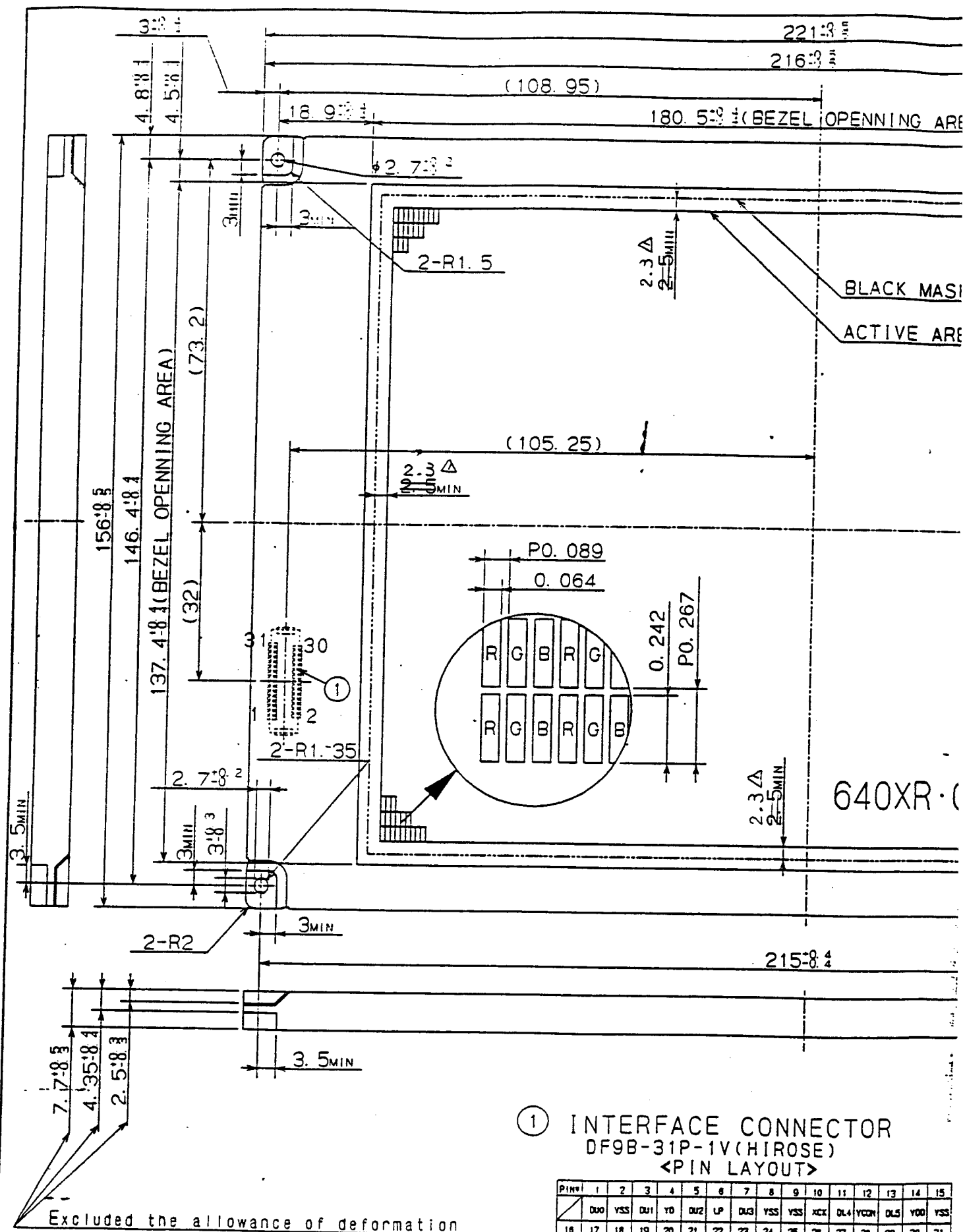
① INTERFACE CONNECTOR
DF9B-31P-1V(HIROSE)
<PIN LAYOUT>

| PIN | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DU0 | VSS | DU1 | YD | DU2 | LP | DU3 | VSS | VSS | XCK | DL4 | YCON | DL5 | VDD | VSS |
| 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
| VDD | DL6 | DISP | DL7 | NC | VSS | DU7 | DL0 | DU6 | DL1 | DU5 | VSS | DU4 | DL2 | VSS | DL3 |

Excluded the allowance of deformation

Fig-10

出 図
ISSUE

...NING AREA)

A-A'

CK MASK AREA

IVE AREA (170.855×128.135)

BEZEL

A-A' SECT

LCD

(0.3)

12

$31.5^{-8.4}$

$3^{-8.2}$

4-R1

2-R1.5$^{-8.1}$

3MIN

2.3 △
2.5MIN

109.3$^{-8.4}$

50 ±5

4-R2

3

2

1

(30.3)

12

4-R1

3.5MIN

(6.7)

0XR·G·Bx480DOTS

BEZEL/DISPLAY POSITION

BEZEL OPENNING AREA
ACTIVE AREA

Y
X
C
D
B
A

1) TOLERANCE X-direction A:4.62±0.8
2) TOLERANCE Y-direction B:4.63±0.8
3) OBLIQUITY of DISPLAY AREA (C-D)<0.8

② CCFT CONNECTOR
BHR-03VS-1(JST)
<PIN LAYOUT>

| PIN° | 1 | 2 | 3 |
|------|----|----|-----|
| | HV | NC | GND |

指示なき寸法公差は $+0.5 \over -0.5$
UNSPECIFIED TOL TO BE

| | | DATE | RIVISE | | PREP'd | MODEL | NAME | LCD UNIT OUTLINE DIMENSIONS |
|---|---|---|---|---|---|---|---|---|
| | △1 | Feb.27.1995 | change | | X.H | LM64C27P | | |

| MATERIAL | THICKNESS | FINISH | SCALE | SYMBOL | 640XR·G·Bx480DOTS 1/240DUTY |
|---|---|---|---|---|---|

PARTS CODE

| DESIGN | TRACE | CHECK | CHECK | APPROVE | SHARP CORPORATION | DATE | 1994·09·14· |
|---|---|---|---|---|---|---|---|

シャープ株式会社 液晶（事本）
発行部門 DUTY PANEL. DEV. ENG. DEPT2

DRAWING. No

14 15
VDD YSS
30 31
YSS OL3

8.Characteristics of Backlight

　　　The ratings are given on condition that the following conditions are satisfied.

1) Rating (Note)

| Parameter | Min | Typ | Max | Unit |
|-----------|-----|-----|-----|------|
| Brightness | 50 | 70 | — | cd/m² |

2) Measurement circuit: CXA-M10L-L (TDK) (at IL=5.0 mArms)

3) Measurement equipment: BM-7 (TOPCON Corporation)

4) Measurement conditions

　　4-1 Measurement circuit voltage: DC=9.2 V (Typ), at primary side

　　4-2 LCD: All digits WHITE, $V_{DD}$=3.3 V,Vcon-Vss=Vmax,DU0～7="H"(WHITE),DL0～7="H"(WHITE)

　　4-3 Ambient temperature: 25 ℃

　　　　Measurement shall be executed 30 minutes after turning on.

5) Used lamp: HMBS26D10W144CAL/X HARISON ELECTRIC CO.,LTD.　: 1 pc

　　5-1 Rating

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remark |
|-----------|--------|------|------|------|------|--------|
| Lamp voltage | $V_L$ | – | 350 | – | Vrms | — |
| Lamp current | $I_L$ | 4.0 | 5.0 | 6.0 | mArms | (*1) |
| Lamp power consumption | $P_L$ | – | 1.75 | – | W | (*2) |
| Lamp frequency | $F_L$ | 25 | – | 45 | kHz | — |
| Kick-off voltage | $V_s$ | – | – | 800 | Vrms | Ta=25℃ |
|  |  | – | – | 900 | Vrms | Ta=0℃ (*3) |
| Lamp life time | $L_L$ | 10000 | – | – | h | — |

　　　　　　　　　Within no conductor closed. (CCFT only)

　　　(*1) It is recommended that IL be not more than 5.0 mArms so that heat
　　　　　radiation of CCFT backlight may least affect the display quality.

　　　(*2) Power consumption excluded inverter loss.

　　　(*3) The circuit voltage(VS) of the inverter should be designed to have
　　　　　some margin(reference value:1 200. VrmsMIN),because VS may be
　　　　　increased due to the leak current in case of the LCD unit.

　　5-2 Operating life

　　　　The operating life time is 10 000 hours or more at 5.0 mA.

　　　　(Operating life with CXA-M10L-L or equivalent.)

　　　　The inverter should meet the following conditions to keep the specified
　　　　life time of used lamp;

　　　　-Sine, symmetric waveform without spike in positive and negative.

　　　　-Output frequency range: 25 KHz～45 KHz

　　　　Make sure the operating conditions by executing the burn-in enough time.

The operating life time is defined as having ended when any of
the following conditions occur; 25±1 ℃
-When the voltage required for initial discharge has reached
110 % of the initial value
-When the illuminence or quantity of light has decreased to
50 % of the initial value

(NOTE) Rating are defined as the average brightness inside the viewing
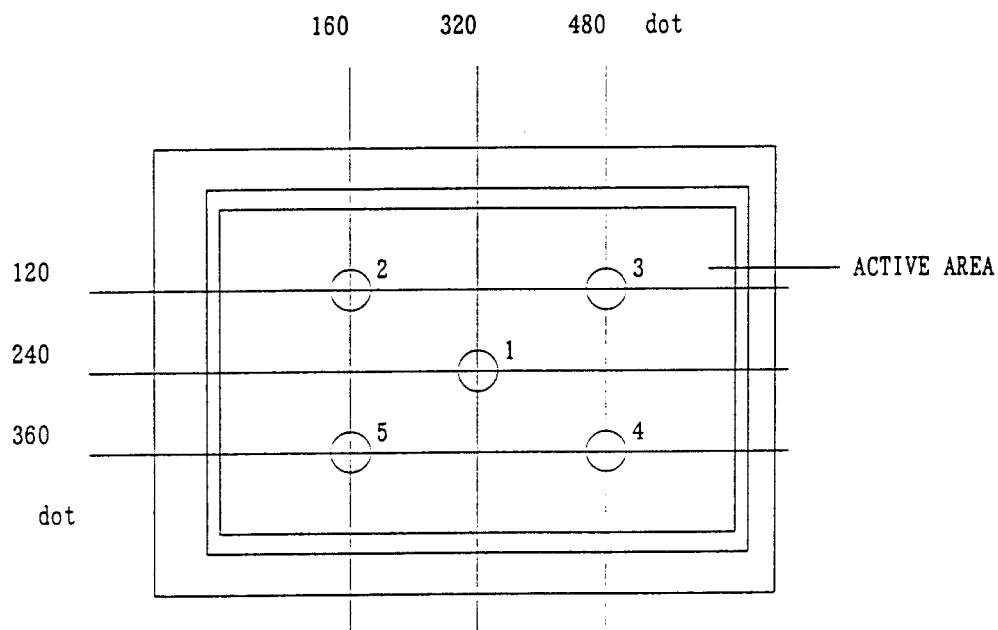area specified in Fig.11.

Fig.11 Measureing points (1~5)

**SHARP**

9. Precautions

   1)  Industrial (Mechanical)design of the product in which this LCD module will be incorporated must be made that the viewing angle characteristics of the LCD may be optimized.

This module's viewing angle is illustrated in Fig.12.

         $\theta y$ MIN $<$ viewing angle $<$ $\theta y$ MAX

         (For the specific values of $\theta$ymin. $\theta$ymax. refer to the table 9.)

Please consider the optimum viewing conditions according to the purpose when installing the module.
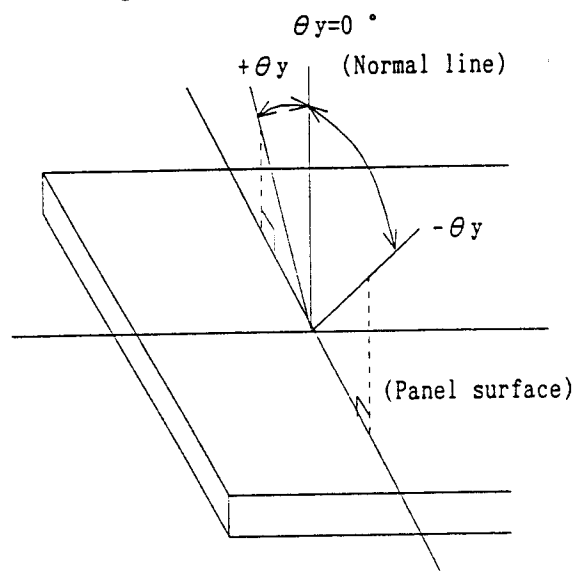


Fig.12  Dot matrix LCD viewing angle

   2)  This module is installed using mounting holes metal PBC or bezel.

When installing the module, pay attention and handle carefully not to allow any undue stress such as twist or bend.

A transparent acrylic resin board or other type of protective panel should be attached to the front of the module to protect the polarizer, LCD cells,etc.

3) Since the front polarizer is easily damaged. Please pay attention not to scratch on its face.

4) If the surface of the LCD cells needs to be cleaned, wipe it swiftly with cotton or other soft cloth. If still not completely clear, blow on its and wipe.

5) Water droplets, etc, must be wiped off immediately since they may cause color changes, staining, etc, if remained for a long time.

6) Since LCD is made of glass plates, dropping the module or banging it against hard objects may cause cracking or fragmentation.

7) CMOS LSIs are equipped in this module, so care must be taken to avoid the electro static charge, by earthing human body, etc. Take the following measures, to protect the module from the electric discharge via mounting tabs from the main system the electrified with static electricity.
   (1) Earth the metallic case of the main system (contact of the module and main system).
   (2) Insulate the module and main system by attaching insulating washers made of bakelite or nylon,etc.

8) The module should be driven according to the specified ratings to avoid malfunction of parmanent damage. DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating waveform by continuous application of the signal M. Especially the power ON/OFF sequence shown on next page is strongly recommended to avoid latch-up of drive LSIs and application of DC voltage to LCD panel.

9) Since leakage current, which may be caused by routing of CCFT cables,etc., may affect the brightness of the display, the inverter has to be designed taking the leakage current into consideration. Thorough evaluation of the LCD unit/inverter built into its host equipment shall be conducted, therefore, to ensure the specified brightness.

10) Avoid to expose the module to the direct sun-light, strong ultraviolet light, etc. for a long time.

11) If stored at temperatures below specified storage temperature, the LC may freeze and be deteriorated. If storage temperature exceed the specified rating. the molecular orientation of the LC may change to that of a liquid, and they may not revert to their original state. As for as possible always store at normal room temperature.

12) Disassembling the LCD module can cause permanent damege and should be strictly avoided.

Supplt voltage sequence condition
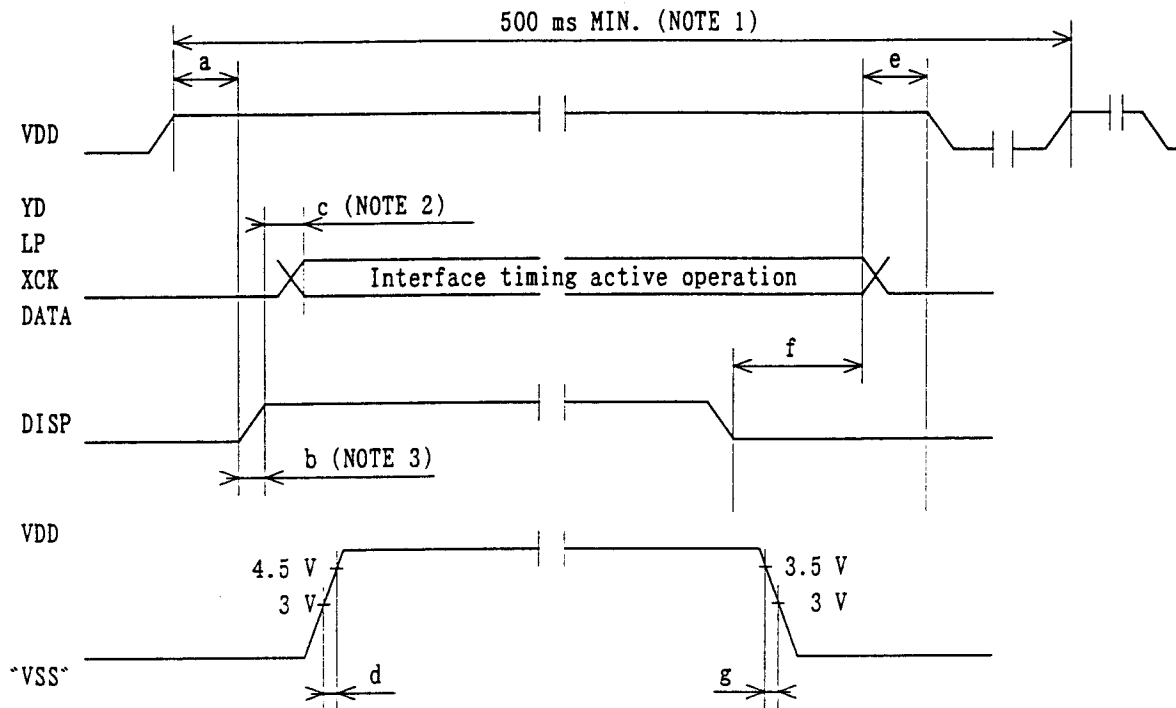


| | POWER ON | |
|---|---|---|
| SYMBOL | Allowable value | |
| a | 0 ms MIN. | 1 s MAX. |
| b | — | 100 ns MAX. |
| c | 50 ms MIN. | — |
| d | — | 25 ms MAX. |

| | POWER OFF | |
|---|---|---|
| SYMBOL | Allowable value | |
| e | 0 ms MIN. | 1 s MAX. |
| f | 0 ms MIN. | 1 s MAX. |
| g | 1 ms MIN. | — |

(NOTE 1)  Power ON/OFF cycle time. All signals and power line shall be in accordance with above sequence in case of power ON/OFF.

(NOTE 2)  In this period, YD and LP shall be "L" level.

(NOTE 3)  Except VDD=DISP.

9. Applicable inspection standard
      The LCD module shall meet the following inspection standard
            :S-U-014


10. This specification describes display quality in case of no gray scale.
    Since display quality can be affected by gray scale methods, display quality
    shall be carefully evaluated for the usability of the LCD MODULE in case gray
    scale is displayed on the LCD MODULE.




WARNING
    DON'T USE ANY MATERIALS WHICH EMIT FOLLOWING GAS FROM EPOXY RESIN (AMINES'
    HARDENER) AND SILICONE ADHESIVE AGENT (DEALCOHOL OR DEOXYM) TO PREVENT CHANGE
    POLORIZER COLOR OWING TO GAS.