SHARP

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		APPLICABLE DIVISION ■Mobile LCD DIVISION I
	SPECIFICATION	

DEVICE SPECIFICATION
for TFT LCD Module Model No.

LS024J3LX01

SHARP

SPEC No.	MODEL No.
MB1-1C102-056	LS024J3LX01

RECORDS OF REVISION

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NOTICE

○ The application examples in these specification sheets are provided to explain the representative applications of the device and are not intended to guarantee any industrial property right or other rights or license you to use them. SHARP assumes no responsibility for any problems related to any industrial property right of a third party resulting from the use of the device.

○ The device listed in these specification sheets was designed and manufactured for use in Telecommunication equipment (terminals)

○ In case of using the device for applications such as control and safety equipment for transportation (aircraft, trains, automobiles, etc.), rescue and security equipment and various safety related equipment which require higher reliability and safety, take into consideration that appropriate measures such as fail-safe functions and redundant system design should be taken.

○ Do not use the device for equipment that requires an extreme level of reliability, such as aerospace applications, telecommunication equipment (trunk lines), nuclear power control equipment and medical or other equipment for life support.

○ SHARP assumes no responsibility for any damage resulting from the use of the device which does not comply with the instructions and the precautions specified in these specification sheets.

○ Contact and consult with a SHARP sales representative for any questions about this device.

[For handling and system design]

(1) Do not scratch the surface of the polarizer film as it is easily damaged.

(2) If the cleaning of the surface of the LCD panel is necessary, wipe it swiftly with cotton or other soft cloth. Do not use organic solvent as it damages polarizer.

(3) Water droplets on polarizer must be wiped off immediately as they may cause color changes, or other defects if remained for a long time.

(4) Since this LCD panel is made of thin glass, dropping the module or banging it against hard objects may cause cracks or fragmentation

(5) Certain materials such as epoxy resin (amine's hardener) or silicone adhesive agent (de-alcohol or de-oxym) emits gas to which polarizer reacts (color change). Check carefully that gas from materials used in system housing or packaging do not hart polarizer.

(6) Liquid crystal material will freeze below specified storage temperature range and it will not get back to normal quality even after temperature comes back within specified temperature range. Liquid crystal material will become isotropic above specified temperature range and may not get back to normal quality. Keep the LCD module always within specified temperature range.

(7) Do not expose LCD module to the direct sunlight or to strong ultraviolet light for long time.

(8) If the LCD driver IC (COG) is exposed to light, normal operation may be impeded. It is necessary to design so that the light is shut off when the LCD module is mounted.

(9) Do not disassemble the LCD module as it may cause permanent damage.

(10) As this LCD module contains components sensitive to electrostatic discharge, be sure to follow the instructions in below.

① Operators

Operators must wear anti-static wears to prevent electrostatic charge up to and discharge from human body.

② Equipment and containers

Process equipment such as conveyer, soldering iron, working bench and containers may possibly generate electrostatic charge up and discharge. Equipment must be grounded through 100Mohms resistance. Use ion blower.

③ Floor

Floor is an important part to leak static electricity which is generated from human body or equipment.

There is a possibility that the static electricity is charged to them without leakage in case of insulating floor, so the countermeasure(electrostatic earth: $1 \times 10^8 \Omega$) should be made.

④Humidity

Proper humidity of working room may reduce the risk of electrostatic charge up and discharge. Humidity should be kept over 50% all the time.

⑤Transportation/storage

Storage materials must be anti-static to prevent causing electrostatic discharge.

⑥Others

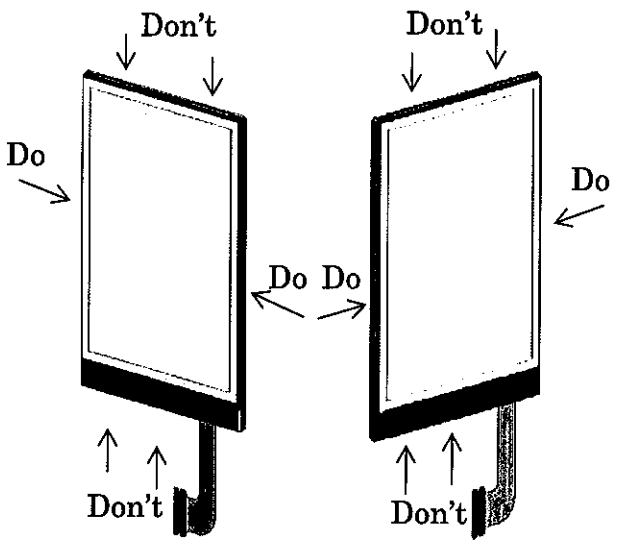
Protective film is attached on the surface of LCD panel to prevent scratches or other damages. When removing this protective film, remove it slowly under proper anti-ESD control such as ion blower.

(11) Hold LCD very carefully when placing LCD module into the system housing. Do not apply excessive stress or pressure to LCD module. Do not to use chloroprene rubber as it may affect on the reliability of the electrical interconnection.

(12) Do not hold or touch LCD panel to flex interconnection area as it may be damaged.

(13) As the binding material between LCD panel and flex connector mentioned in 12) contains an organic material, any type of organic solvents are not allowed to be used. Direct contact by fingers is also prohibited.

(14) When carrying the LCD module, place it on the tray to protect from mechanical damage. It is recommended to use the conductive trays to protect the CMOS components from electrostatic discharge. When holding the module, hold the Plastic Frame of LCD module so that the panel, COG and other electric parts are not damaged.



(15) Do not touch the COG's patterning area. Otherwise the circuit may be damaged.

(16) Do not touch LSI chips as it may cause a trouble in the inner lead connection.

(17) Place a protective cover on the LCD module to protect the glass panel from mechanical damages.

(18) LCD panel is susceptible to mechanical stress and even the slightest stress will cause a color change in background. So make sure the LCD panel is placed on flat plane without any continuous twisting, bending or pushing stress.

(19) Protective film is placed onto the surface of LCD panel when it is shipped from factory. Make sure to peel it off before assembling the LCD module into the system. Be very careful not to damage LCD module by electrostatic discharge when peeling off this protective film. Ion blower and ground strap are recommended.

(20) Make sure the mechanical design of the system in which the LCD module will be assembled matches specified viewing angle of this LCD module.

(21) This LCD module does not contain nor use any ODS (1,1,1-Trichloroethane, CCL4) in all materials used, in all production processes.

[For operating LCD module]

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) At the shipment, adjust the contrast of each LCD module with electric volume. LCD contrast may vary from panel to panel depending on variation of LCD power voltage from system.

(3) As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable.

[Precautions for Storage]

(1) Do not expose the LCD module to direct sunlight or strong ultraviolet light for long periods. Store in a dark place.

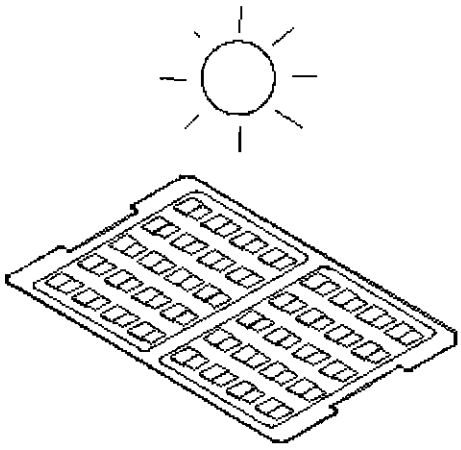
(2) The liquid crystal material will solidify if stored below the rated storage temperature and will become an isotropic liquid if stored above the rated storage temperature, and may not retain its original properties. Only store the module at normal temperature and humidity (25±5°C,60±10%RH) in order to avoid exposing the front polarizer to chronic humidity.

(3) Keeping Method

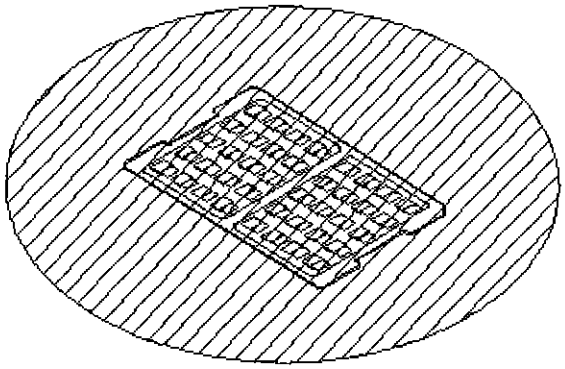
a. Don't keeping under the direct sunlight.

b. Keeping in the tray under the dark place.

DON'T



DO



(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) Be sure to prevent light striking the chip surface.

[Other Notice]

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) As electrical impedance of power supply lines (VCC-VSS) are low when LCD module is working, place the de-coupling capacitor near by LCD module as close as possible.

(3) Reset signal must be sent after power on to initialize LSI. LSI does not function properly until initialize it by reset signal.

(4) Generally, at power on, in order not to apply DC charge directly to LCD panel, supply logic voltage first and initialize LSI logic function including polarity alternation. Then supply voltage for LCD bias. At power off, in order not to apply DC charge directly to LCD panel, execute Power OFF sequence and Discharge command.

(5) Don't touch to PWB surface, exposed IC chip, electric parts and other parts, to any electric, metallic materials.

(6) No bromide specific fire-retardant material is used in this module.

(7) Do not display still picture on the display over 2 hours as this will damage the liquid crystal.

[Precautions for Discarding Liquid Crystal Modules]

COG: After removing the LSI from the liquid crystal panel, dispose of it in a similar way to circuit boards from electronic devices.

LCD panel: Dispose of as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal panel only contains an extremely small amount of liquid crystal (approx.100mg) and therefore it will not leak even if the panel should break.

-Its median lethal dose (LD50) is greater than 2,000 mg/kg and a mutagenetic (Aims test: negative) material is employed.

FPC: Dispose of as similar way to circuit board from electric device.

Contents

1. Application

This data sheet is to introduce the specification of LS024J3LX01 active matrix 16,777,216 color LCD module.
Main color LCD module is controlled by Driver IC.

If any problem occurs concerning the items not stated in this specification, it must be solved sincerely by both parties after deliberation.

2. Construction and Outline

Construction: LCD panel, Driver (COG), FPC with electric components,
4 White LED lump, prism sheet, diffuser, light guide and reflector, plastic frame to fix them mechanically.

Outline: See page 28

Connection: 24 pins;

There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.

In order to realize thin module structure, double-sided adhesive tapes are used to fix LCD panels. As these tapes do not guarantee to permanently fix the panels, LCD panel may rise from the module when shipped from factory.

So please make sure to design the system to hold the edges of LCD panel by the soft material such as sponge
when LCD module is assembled into the cabinet.

3. Mechanical Specification

Table 1

Outline Dimensions(typ)		38.6(W)×60.4(H)×1.9(D)	mm
Main LCD Panel	Active area	33.60(W)×50.40(H)	mm
	Display format	320(columns)×480(rows)	-
	Dot pitch	0.105(W)×0.105(H)	mm
	Base color Notes	Normaly black	-
Mass		9.3	g

Notes:

1. Display module general parameters

4. Absolute Maximum Ratings

(4-1) Electrical absolute maximum ratings

Table 2

Parameter (requirement)	Symbol	Rating	Unit
Power Supply Voltage (2.75V)	V_{DD}	-0.3 to +3.5	V
Power Supply Voltage (1.8V)	V_{DDI}	-0.3 to +2.2	V
Logic Signal Input Voltage	V_I	-0.3 to +2.25	V
Logic Signal Output Voltage	V_O	-0.3 to +2.25	V

(4-2) Environment Conditions

Table 3

Item	Top		Tstg		Remark
	Min	Max	Min	Max	
Ambient temperature	-15℃	+70℃	-30℃	+80℃	Note2
Humidity	Note 1		Note 1		No condensation

Notes :

1. Ta ≤ 40 °C.....95 % RH Max
2. Ta > 40 °C.....Absolute humidity shall be less than Ta=40 °C /95 % RH.

As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable. Be sure not to exceed the rated voltage, otherwise a malfunction may occur.

(5-2) LED back light

At main panel the back light uses 4pcs edge light type white LED.

Table 5

Item	Value			Unit
	Min	Nominal	Max	
Forward voltage (Vf) @ If	N/A	3.2	3.5	V
Forward current for LED (If)	-	18	-	mA
Number of LED components	4 pcs			
Connection type (Serial / Parallel / Other)	All 4 LEDs in Series			

LED lamp: NSSW006

*4pcs of LED

*Please consider Allowable Forward Current on used temperature
(refer to Ambient Temperature vs. Allowable Forward Current curve)

■ Ambient Temperature vs. Allowable Forward Current

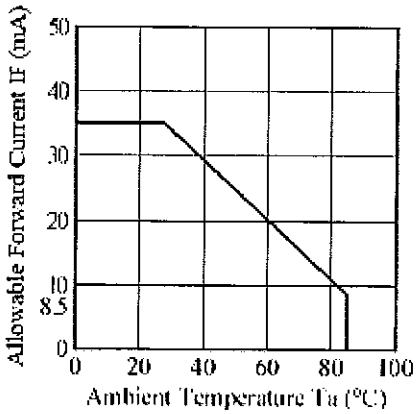


Fig.2

*Schematics drawing of lighting

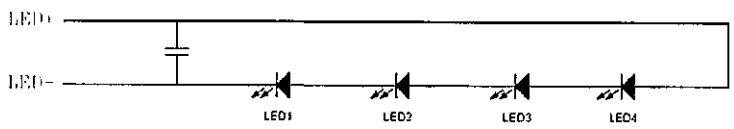


Fig.3

(5-3) Interface signals

Table 6

Pin No	Symbol	Description	I/O(1)	Remarks
1	TP		-	
2	TP		-	
3	XRES	Reset	I	
4	XCS	Chip Select	I	
5	SCL	Clock	I	
6	DIN	Data In	I	
7	DOUT	Data Out	O	
8	GND	Ground	-	0V
9	VDDI	Power supply for LCD	-	typ=1.8V
10	VDD	Power supply for LCD	-	typ=2.75V
11	LED-	Input current for LED components.	-	
12	LED+	Input current for LED components.	-	If=18mA
13	GND	Ground	-	0V
14	D1+	Data 1 channel+	I	
15	D1-	Data 1 channel-	I	
16	GND	Ground	-	0V
17	CLK+	Clock channel+	I	
18	CLK-	Clock channel-	I	
19	GND	Ground	-	0V
20	D0+	Data 0 channel+	I	
21	D0-	Data 0 channel-	I	
22	GND	Ground	-	0V
23	TP		-	
24	TP		-	

Notes:

1. The direction is named with respect to the display module, I = from host to module, O = from module to host.

Table 7

Assembled on	Item	Description
Phone PWB	Connector type	FPC LIF Connector
	Pin amount	24
	Manufacturer	JAE
	Part number	CD002-1296-K126

Connector pin layout of the display module is presented in Fig.4

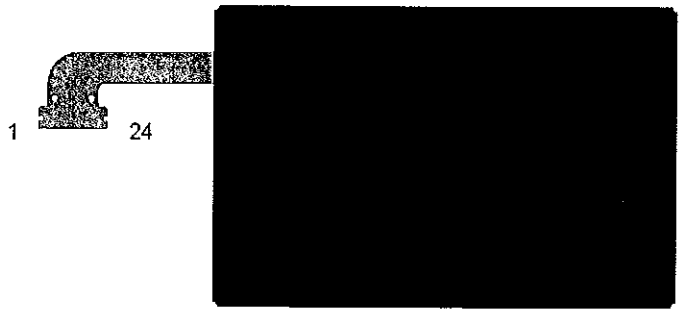


Fig.4 Connector pin layout of display module, bottom view of Module

(5-4) 3-wire 9bit Serial Interface Timing Diagrams

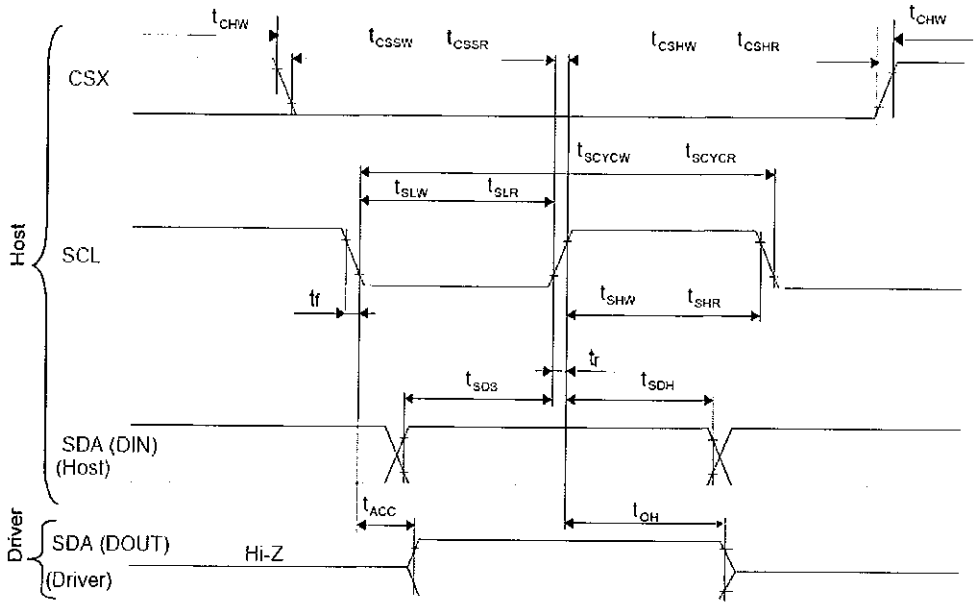


Fig.5

Table 8

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Serial Clock Cycle(Write)	t_{SCYCW}	SCL	100			ns
SCL High pulse width(Write)	t_{SHW}	SCL	35			ns
SCL Low pulse width(Write)	t_{SLW}	SCL	35			ns
Data setup time(Write)	t_{SDS}	SDA	30			ns
Data hold time(Write)	t_{SDH}	SDA	30			ns
Serial Clock Cycle(Read)	t_{SCYCR}	SCL	150			ns
SCL High pulse width(Read)	t_{SHR}	SCL	60			ns
SCL Low pulse width(Read)	t_{SLR}	SCL	60			ns
Access time(1)	t_{ACC}	SDA	10		50	ns
Output disable time	t_{OH}	SDA	15		50	ns
CSX High pulse width	t_{CHW}	CSX	40			ns
CSX-SCL time(Write)	t_{CSSW}	CSX	30			ns
	t_{CSHW}	CSX	30			ns
CSX-SCL time(Read)	t_{CSSR}	CSX	60			ns
	t_{CSHR}	CSX	60			ns

Notes:

1. Ta = -30 - +70 °C, VDDI=1.65V-1.95 V, VDD= 2.3-2.9V, VSS=0V
2. The output signal's rise and fall times are stipulated to be from TBD to 15 ns.
3. The input signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

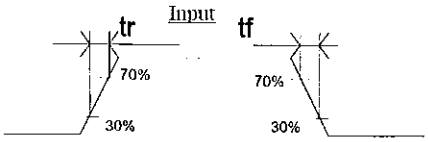


Fig.6

(5-5) General Timing for LVDS Interface

Table 9

Item	Symbol	Min.	Typ.	Max.	Unit
Pixel Clock Frequency	PCLK	8.0		11.4	MHz
Pixel Clock Cycle	t_{CLK}	87.7		125.0	ns
Clock-to-Clock Position Jitter	$t_{CLKjitter}$	0		300	ps
Clock-to-Data Position Jitter	$t_{DATAjitter}$	0		330	ps
Ideal t_{pos0} Position	t_{pos0}	0	0	0	ns
Ideal t_{pos1} Position	t_{pos1}	$(1/15)*t_{CLK}$	$(1/15)*t_{CLK}$	$(1/15)*t_{CLK}$	ns
Ideal t_{pos2} Position	t_{pos2}	$(2/15)*t_{CLK}$	$(2/15)*t_{CLK}$	$(2/15)*t_{CLK}$	ns
Ideal t_{pos3} Position	t_{pos3}	$(3/15)*t_{CLK}$	$(3/15)*t_{CLK}$	$(3/15)*t_{CLK}$	ns
Ideal t_{pos4} Position	t_{pos4}	$(4/15)*t_{CLK}$	$(4/15)*t_{CLK}$	$(4/15)*t_{CLK}$	ns
Ideal t_{pos5} Position	t_{pos5}	$(5/15)*t_{CLK}$	$(5/15)*t_{CLK}$	$(5/15)*t_{CLK}$	ns
Ideal t_{pos6} Position	t_{pos6}	$(6/15)*t_{CLK}$	$(6/15)*t_{CLK}$	$(6/15)*t_{CLK}$	ns
Ideal t_{pos7} Position	t_{pos7}	$(7/15)*t_{CLK}$	$(7/15)*t_{CLK}$	$(7/15)*t_{CLK}$	ns
Ideal t_{pos8} Position	t_{pos8}	$(8/15)*t_{CLK}$	$(8/15)*t_{CLK}$	$(8/15)*t_{CLK}$	ns
Ideal t_{pos9} Position	t_{pos9}	$(9/15)*t_{CLK}$	$(9/15)*t_{CLK}$	$(9/15)*t_{CLK}$	ns
Ideal t_{pos10} Position	t_{pos10}	$(10/15)*t_{CLK}$	$(10/15)*t_{CLK}$	$(10/15)*t_{CLK}$	ns
Ideal t_{pos11} Position	t_{pos11}	$(11/15)*t_{CLK}$	$(11/15)*t_{CLK}$	$(11/15)*t_{CLK}$	ns
Ideal t_{pos12} Position	t_{pos12}	$(12/15)*t_{CLK}$	$(12/15)*t_{CLK}$	$(12/15)*t_{CLK}$	ns
Ideal t_{pos13} Position	t_{pos13}	$(13/15)*t_{CLK}$	$(13/15)*t_{CLK}$	$(13/15)*t_{CLK}$	ns
Ideal t_{pos14} Position	t_{pos14}	$(14/15)*t_{CLK}$	$(14/15)*t_{CLK}$	$(14/15)*t_{CLK}$	ns

Notes:

1. Ta = -30 to 70 °C (to +85 °C no damage), VDDI = 1.65 – 1.95V, VSS (DGND) = 0V

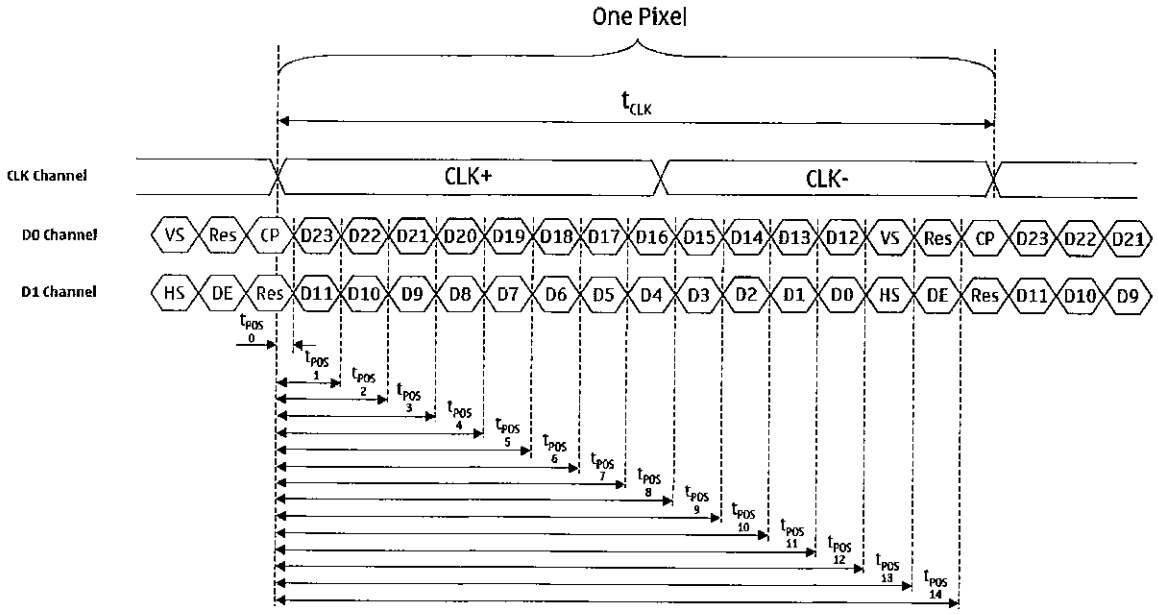


Fig.7

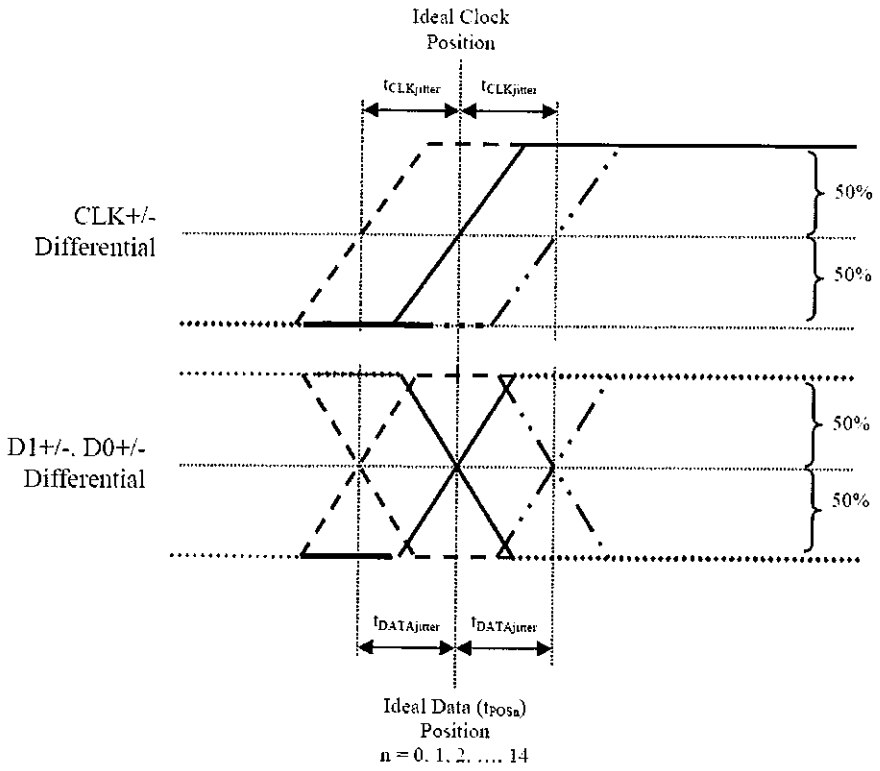

Ideal Clock
Position
tCLKjitter
tCLKjitter
CLK+/-
Differential
50%
50%
D1+/-. D0+/-
Differential
50%
50%
tDATAjitter
tDATAjitter
Ideal Data (tPOSn)
Position
n = 0. 1. 2. 14

Fig.8

(5-6) General Timing Diagram for RGB

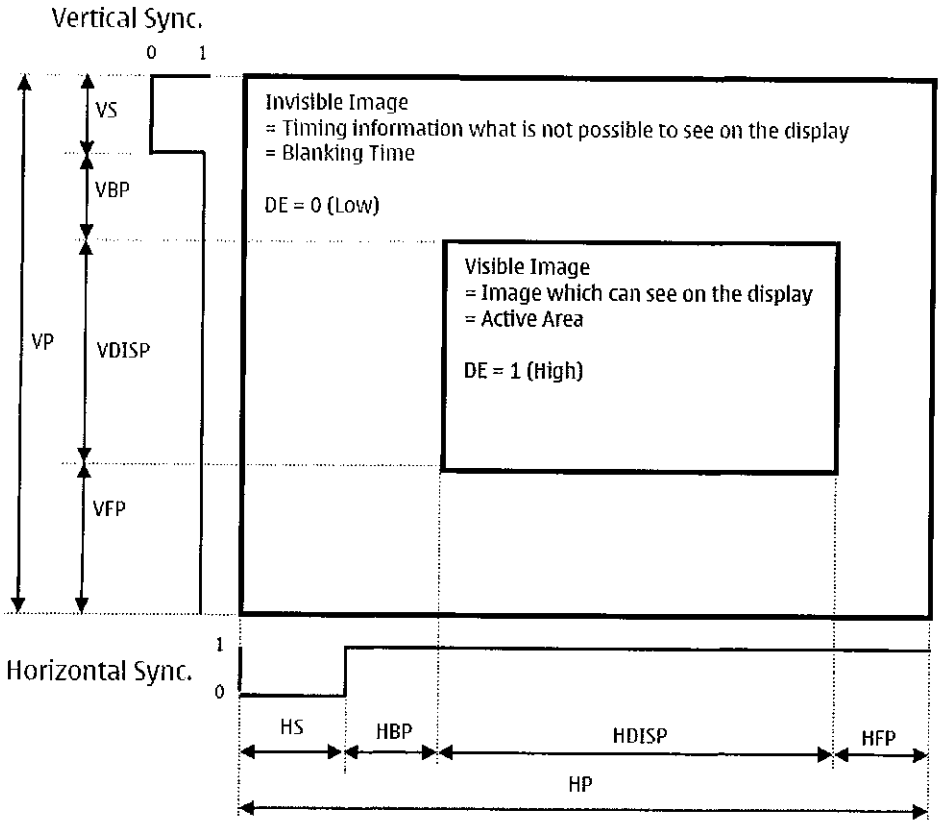


Fig.9

5. Electrical Specifications

(5-1) Electrical characteristics

Table 4

Parameter(requirement)		Condition	Symbol	Specification			Unit
				min	typ	max	
Power Supply Voltage		Operating Voltage	V_{DD}	2.6	2.75	2.90	V
Power Supply Voltage (logic)		I/O Supply Voltage	V_{DDI}	1.65	1.8	1.95	V
Logic High Level Input Voltage		IN= -10uA	V_{IH}	0.7V_{DDI}	-	VDDI	V
Logic Low Level Input Voltage		IN= - +0uA	V_{IL}	0.0	-	0.3 V_{DDI}	V
Logic High Level Output Voltage		I_{OUT} = -1mA	V_{OH}	0.8 V_{DDI}	-	VDDI	V
Logic Low Level Output Voltage		I_{OUT} = +1mA	V_{OL}	0.0	-	0.2 V_{DDI}	V
Differential Input Voltage for Clock		CLK+/-	V_{DIFCLK}	87.5	100	200	mV
Differential Input Voltage for Data		D0+/-, D1+/-	$V_{DIFDATA}$	87.5	100	200	mV
Input Common Mode Voltage for Clock		CLK+/-	V_{CMCLK}	0.6	0.9	1.2	V
Input Common Mode Voltage for Data		D0+/-, D1+/-	V_{CMDATA}	0.6	0.9	1.2	V
Differential Input Low Level Threshold Voltage for Clock		CLK+/-	V_{THLCLK}	-40	-	-	mV
Differential Input High Level Threshold Voltage for Clock		CLK+/-	V_{THHCLK}	-	-	40	mV
Differential Input Low Level Threshold Voltage for Data		D0+/-, D1+/-	$V_{THLDATA}$	-40	-	-	mV
Differential Input High Level Threshold Voltage for Data		D0+/-, D1+/-	$V_{THHDATA}$	-	-	40	mV
Differential Termination Resistor		CLK+/-, D0+/-, D1+/-	R_{TERM}	80	100	120	Ω
Self Bias Resistor		CLK+/-, D0+/-, D1+/-	$R_{SELFBIAS}$	-	-	50	kΩ
Logic High Level Leakage			I_{LIH}	-	-	1	uA
Logic Low Level Leakage			I_{LIL}	-1	-	-	uA
Input Leakage Current +		CLK+, D0+, D1+	I_{IN+}	-	-	90	uA
Input Leakage Current -		CLK-, D0-, D1-	I_{IN-}	-90	-	-	uA
Current Consumption	Partial Mode off Idle Mode off Sleep Out Mode	All pixels white(1)	IDDI	-	1.0	-	mA
			IDD	-	11.2	-	mA
		All pixels black(1)	IDDI	-	1.0	-	mA
			IDD	-	8.0	-	mA
	Sleep In Mode	N/A(1)	IDDI	-	0.04	-	mA
			IDD	-	0.005	-	mA

Notes:

1. Conditions : Ta = 25°C, VDD = 2.75V, VDDI = 1.8V,Refresh rate=60Hz.
   Ambient temperature,Ta = -15°C to +70°C operational
   Measurement Point

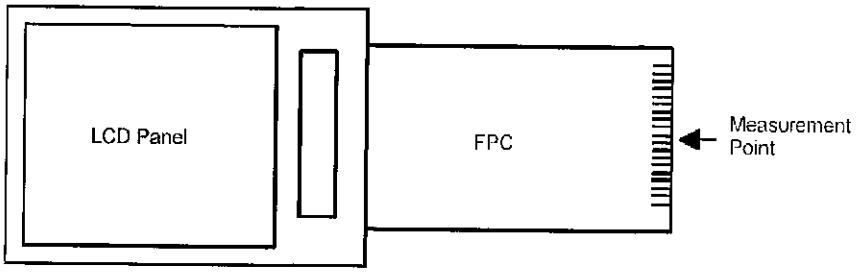


Fig.1

(5-7) Vertical Timing for RGB

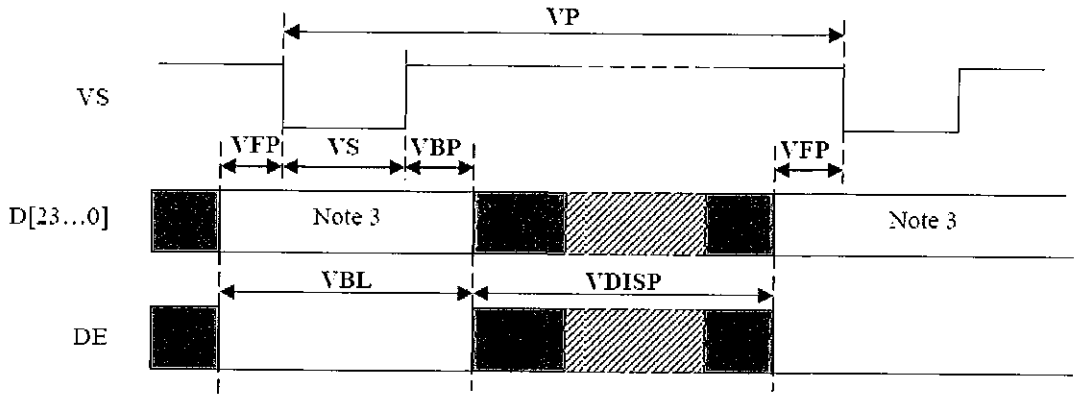


Fig.10

Table 10

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Vertical cycle	VP		486		490	line
Vertical low pulse width	VS		2		4	line
Vertical front porch	VFP		2		4	line
Vertical back porch	VBP		2		4	line
Vertical data start point		VS+VBP	4		8	line
Vertical blanking period	VBL	VFP+VS+VBP	6		10	line
Vertical active area		VDISP		480		line
Vertical Refresh Rate	VRR		50		65	Hz

Notes:

1. Ta = -30 - +70°C, VDDI = 1.65 – 1.95 V, VDD = 2.3 – 2.9 V, VSS = 0 V
2. Signal rise and fall times are equal or less than 20 ns.
3. Measuring of input signals are using 0.30 x VDDI for low state and 0.70 x VDDI for high state.
4. Data lines can be set to "High" or "Low" during blanking time – Don't care.

(5-8) Horizontal Timing for RGB

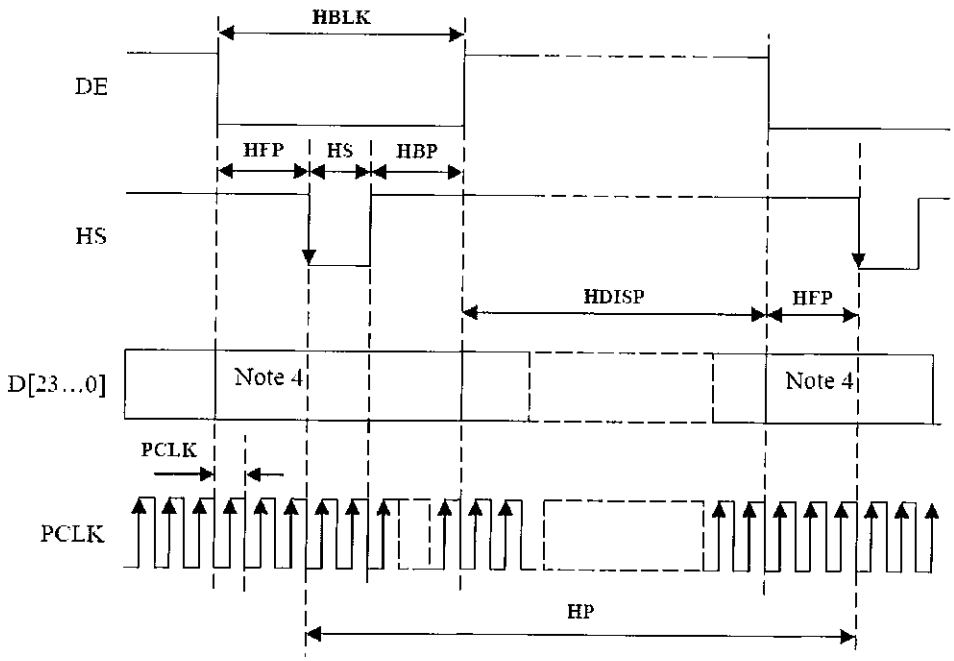


Fig.11

Table 11

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
HS cycle	HP		352		528	PCLK
HS low Pulse width	HS		2		256	PCLK
Horizontal back porch	HBP		2		256	PCLK
Horizontal front porch	HFP		2		256	PCLK
Horizontal data start point		HS+HBP	30		206	PCLK
Horizontal blanking period	HBLK	HFP+HS+HBP	32		208	PCLK
Horizontal active area	HDISP			320		PCLK
Pixel clock frequency When RGB I/F is running	PCLK	VRR=50Hz~ 60Hz	8.0		11.4	MHz

Notes:

1. Ta = -30 - +70°C, VDDI = 1.65 – 1.95 V, VDD = 2.3 – 2.9 V, VSS = 0 V
2. Signal rise and fall times are equal or less than 20 ns.
3. Measuring of input signals are using 0.30 x VDDI for low state and 0.70 x VDDI for high state.
4. HP is multiples of eight PCLK.
5. Data lines can be set to "High" or "Low" during blanking time – Don't care.

(5-9) /Reset Input Timing

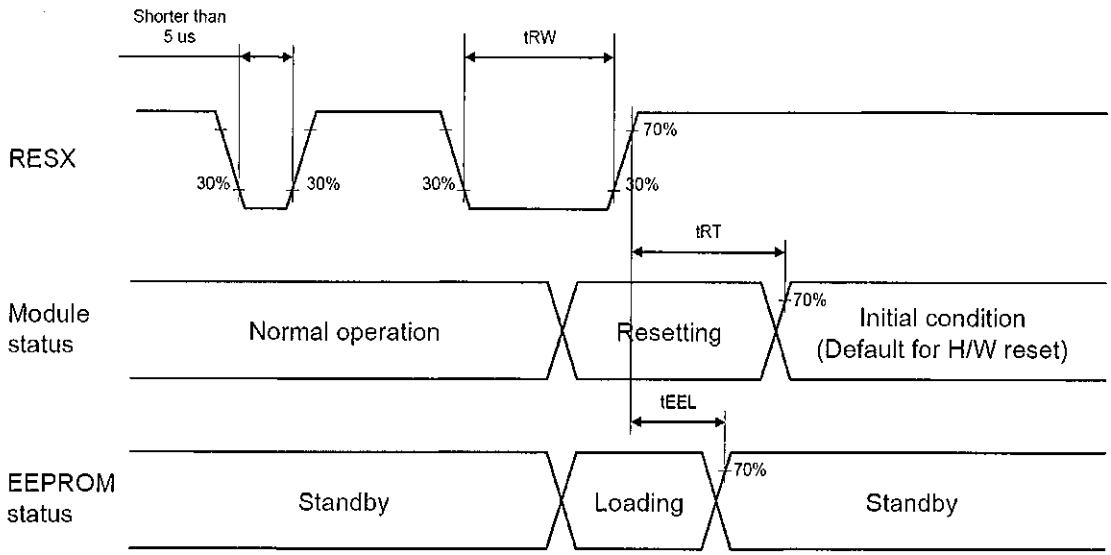


Fig.12

Table 12

Parameter	Symbol	Condition	Specification			Unit
			Min	Typ	Max	
Reset pulse width	tRW	Note 3,4	10			us
Reset time	tRT	Note 1,2,5			5,120	ms
EEPROM load time	tEEL	Note 1			5	ms

Notes:

1. tRT includes the time required to load initialization data from EEPROM.
2. The display is blanked following the falling edge of RESX and continues to remain blank during tRT.

Since the initial condition is 'Sleep In', 'Display OFF', the display will in face remain blank until 'Sleep Out', 'Display ON' commands are received.

3. False trigger rejection applies to RESX.
4. Noise spike rejection applies to RESX.(See Fig.13, tPSPIKE= Max20ns)
5. 5mS in 'Sleep In' mode, 120mS in 'Sleep Out' mode.

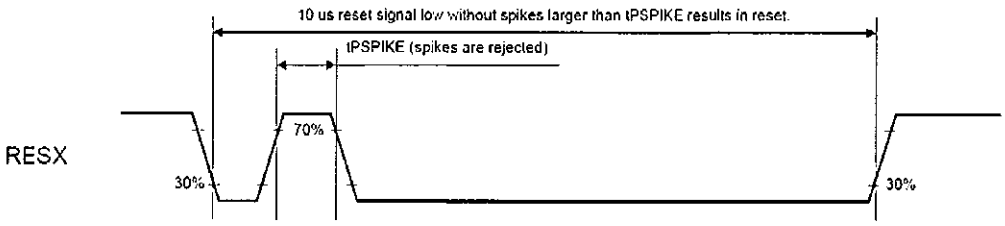


Fig.13

(5-10) Schematic of LCD module system

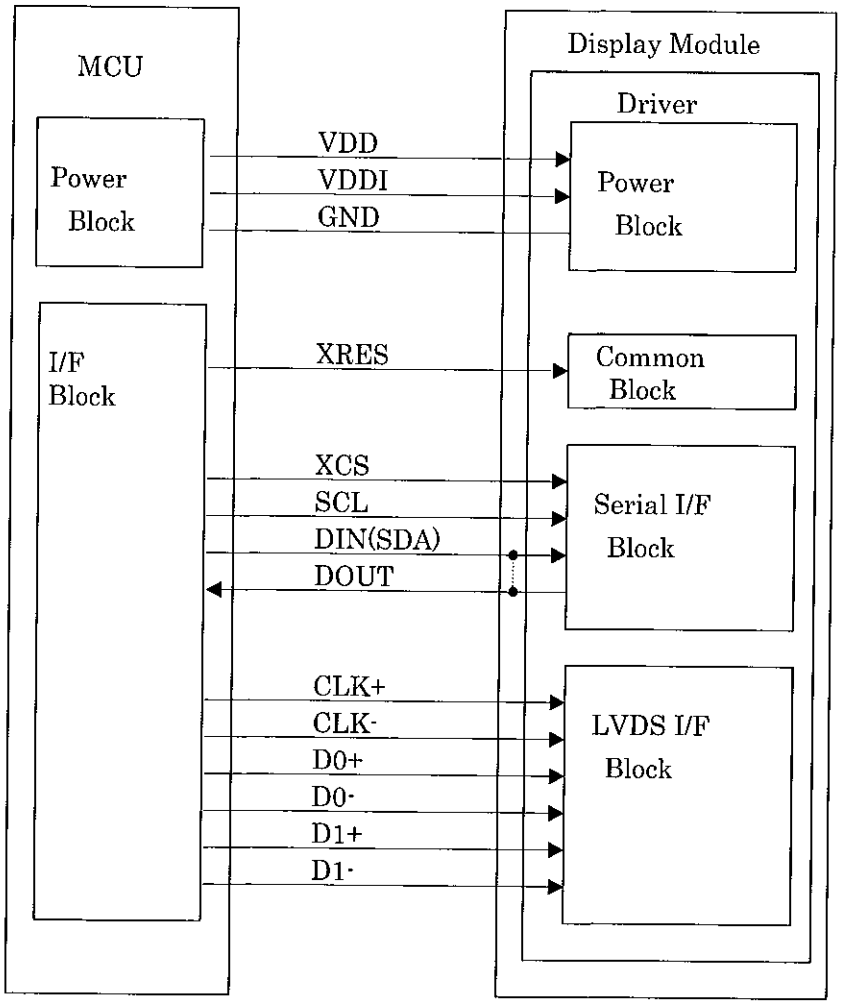


Fig.14

6. Optical Characteristics

Table 13

Parameter	Symbol	Condition	Typ	Unit	Remark
Brightness	Br	θ_1=0°	370	cd/m²	Note 1, 2
Contrast	Co	θ_1=0°	540	-	Note 1, 2, 3
Viewing Angle (Contrast)	φ=0°	θ_1=15°	190	-	Note 1, 2, 3
	φ=90°		190		
	φ=180°		210		
	φ=270°		215		
	φ=0°	θ_1=30°	60	-	Note 1, 2, 3
	φ=90°		65		
	φ=180°		65		
	φ=270°		70		
	φ=0°	θ_1=45°	30	-	Note 1, 2, 3
	φ=90°		30		
	φ=180°		30		
	φ=270°		35		
Response Time	τr1	θ_1=0°	7	ms	Note 4
	τr2		15		
White Chromaticity	u'	θ_1=0°	0.185	-	-
	v'		0.464		
NTSC ratio	-	θ_1=0°	81	%	

*VDD=2.75,Ta = 25℃

Notes:

1. Definition of range of visual angle

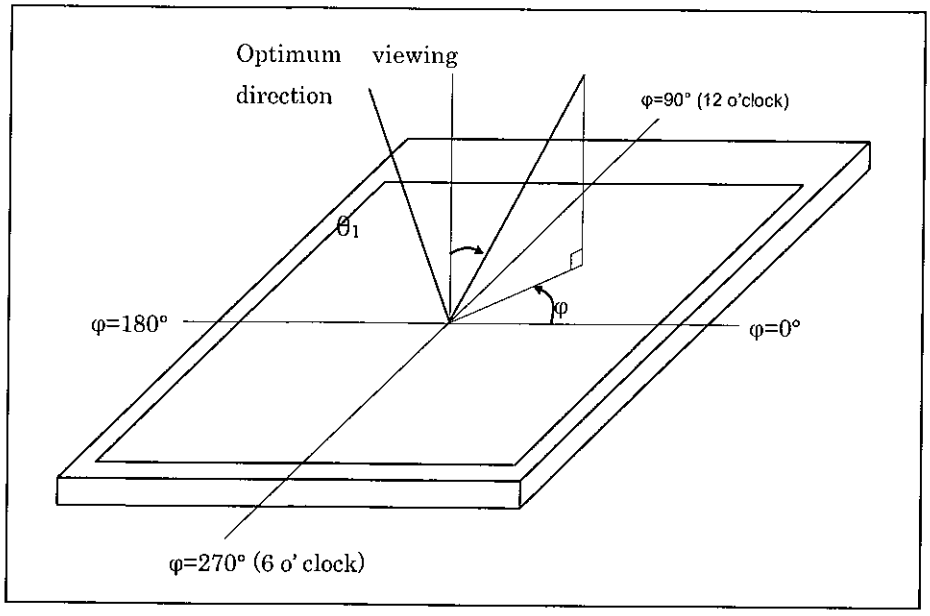


Fig.15

2. Brightness is measured as follows, and is defined as the brightness of all pixels "White" at the center of display area on optimum contrast.

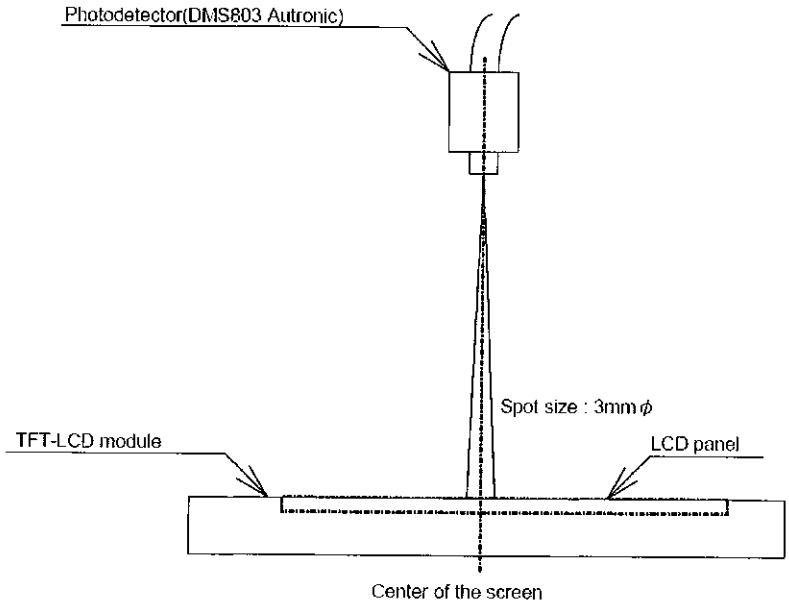


Fig. 16

3. Contrast ratio is defined as follows:

$$Co = \frac{\text{Luminance(brightness) all pixcels "White"}}{\text{Luminance(brightness) all pixcels "Black"}}$$

4. Response time is defined as follows:

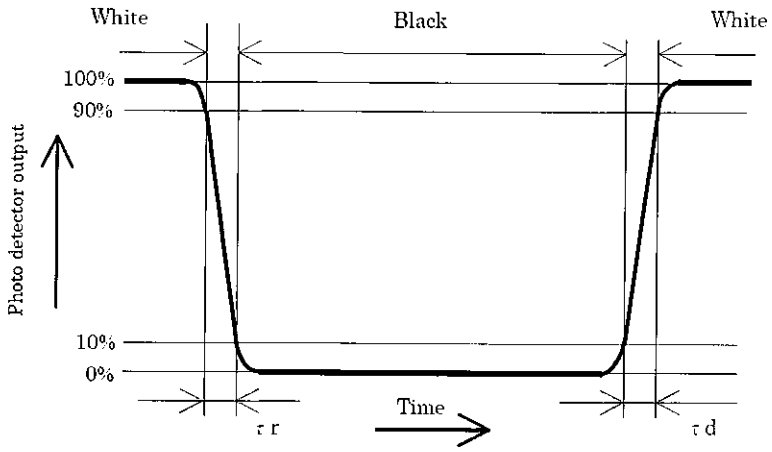


Fig. 17

7. Command List

Table 14

Op-code (Hex)(1)	Mnemonic	Function	Type(4)
00	NOP	No operation	C+0
01	SWRESET	Software Reset	C+0
04	RDDIDIF	Read display ID information(3)	R+d3
05	RDNUMPE	Read Number of ParityErrors(3)	R+1
06	RDRED	Read Red colour(3)	R+1
07	RDGREEN	Read Green colour(3)	R+1
08	RDBLUE	Read Blue colour(3)	R+1
09	RDDST	Read display status(3)	R+d4
0A	RDDPM	Read Display Power Mode(3)	R+1
0B	RDDMADCTL	Read Display MADCTL(3)	R+1
0C	RDDCOLMOD	Read Display Pixel Format(3)	R+1
0D	RDDIM	Read Display Image Mode(3)	R+1
0E	RDDSM	Read Display Signal Mode(3)	R+1
0F	RDDSDR	Read Display Self Diagnostic Result	R+1
10	SLPIN	Sleep In(3)	C+0
11	SLPOUT	Sleep Out	C+0
12	PTLON	Partial mode on(3)	C+0
13	NORON	Normal mode on(3)	C+0
26	GAMSET	Gamma set(3)	W+1
28	DSPOFF	Display off(3)	C+0
29	DSPON	Display on(3)	C+0
2A	CASET	Column address set	W+4
2B	PASET	Page address set	W+4
2C	RAMWR	Memory write	W+n
30	PLTAR	Partial area(3)	W+4
36	MADCTL	Memory data access control(3)	W+1
B0 to D9	-	Reserved(2)	
DA	RDID1	Read ID1(3)	R+1
DB	RDID2	Read ID2(3)	R+1
DC	RDID3	Read ID3(3)	R+1
DE to FF	-	Reserved(2)	

Notes:

1. Undefined commands are treated as NOP (00h) command.

2. B0h to D9h and DEh to FFh are defined by Sharp. Before shipping, and by agreement with Sharp, these commands can be made available to the customer. By default these commands operate as NOP.

3: Commands which affect the displayed image, (10h, 12h, 13h, 26h, 28h, 29h, 30h and 36h), take effect during the Vertical sync pulse when the display module is in 'Sleep Out' mode to avoid abnormal visual effects. During 'Sleep In' mode, these commands take effect immediately. Read commands, (04h, 05h, 06h, 07h, 08h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, DAh, DBh, DCh), are updated immediately both in 'Sleep In' mode and 'Sleep Out' Mode.

4. C=command, W=write, R=read, +=number of following parameters, (in Bytes), d=dummy clock cycle.

8. Initial Sequence

During power on, 'RESX' must be applied for a minimum of 10us after both VDD and VDDI have been applied. 'RESX' can be undefined during power-on but must be applied subsequently to ensure correct LCD controller operation. VDDI and VDD can be applied in any order.

During power-off, if the LCD controller is in 'Sleep Out' mode, VDD and VDDI must be powered down a minimum of 120ms after RESX has been released. If the LCD controller is in 'Sleep In' mode, VDDI and VDD can be powered down a minimum of 0ms after 'RESX' has been released. VDDI and VDD can be powered down in any order.

'CSX' can be applied at any time. 'RESX' has priority over 'CSX'.

(8.1) Case 1 - RESX line is held high or unstable by host at power-on

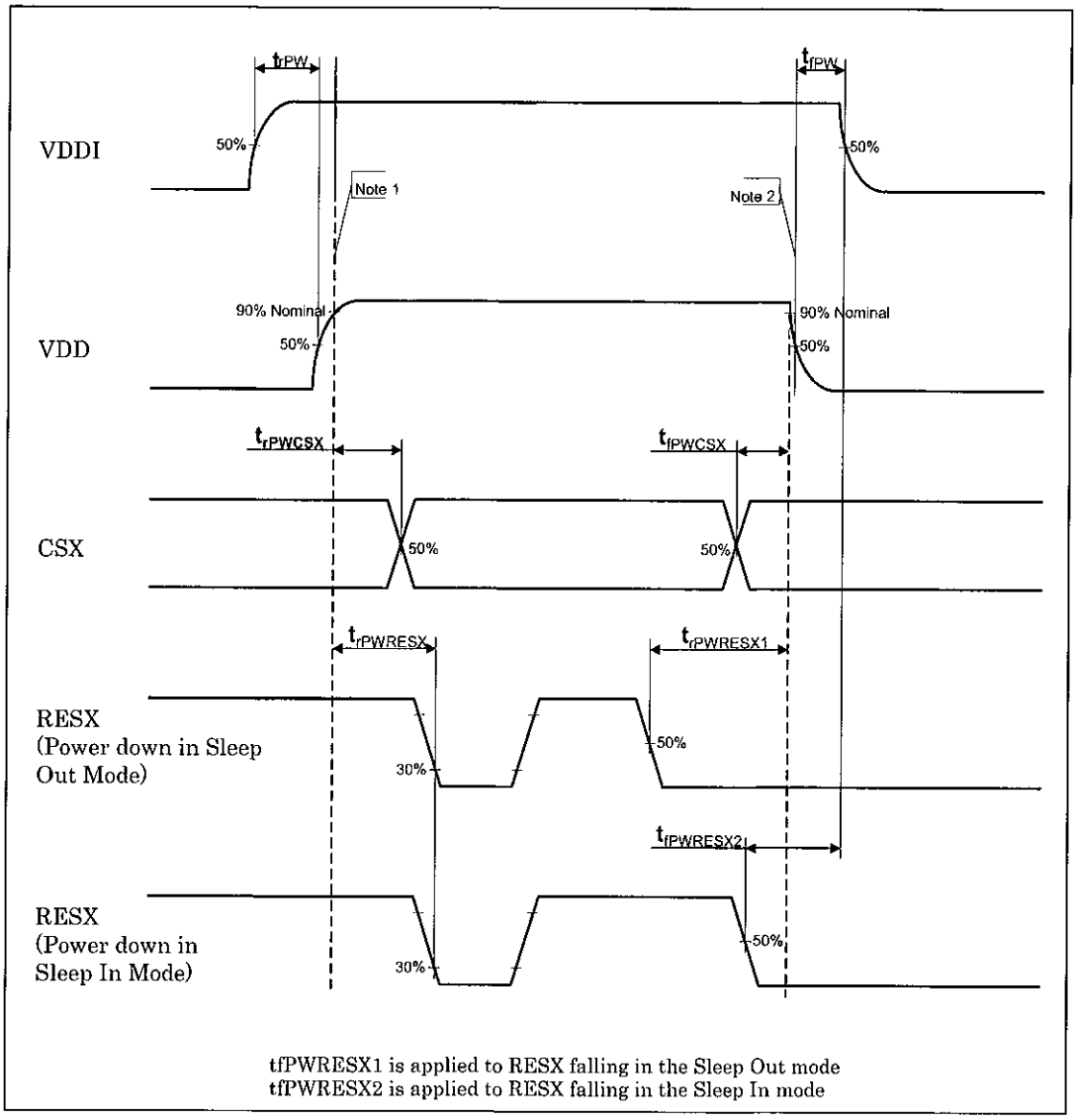


Fig.18

Notes:

1. Time when the latter signal rises up to 90% of its typical value, e.g. when VDD comes later. This time is defined at the cross point of 90% of 2.75V, not 2.3V.

2. Time when the former signal falls down to 90% of its typical value, e.g. when VDD falls earlier. This time is defined at the cross point of 90% of 2.75V, not 2.3V.

Table 15

Parameter	Value
trPW	+/- no limit
tfPW	+/- no limit
trPWCSX	+/- no limit
tfPWCSX	+/- no limit
trPWRESX	+ no limit
tfPWRESX1	min 120mS
tfPWRESX2	+ no limit

(8.2) Case 2 - RESX line is held low by host at power-on

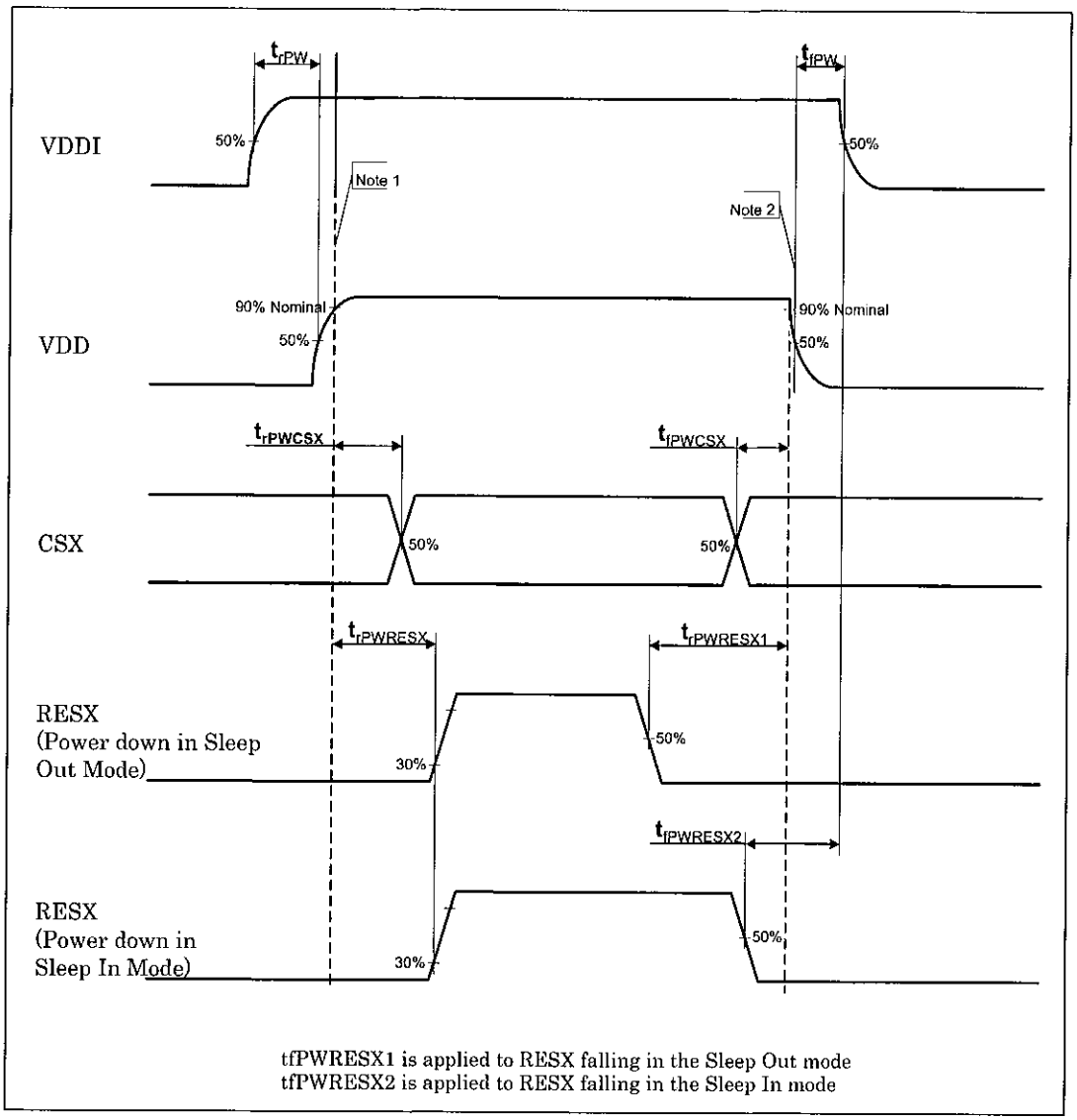


Fig.19

Notes:

1. Time when the latter signal rises up to 90% of its typical value, e.g. when VDD comes later. This time is defined at the cross point of 90% of 2.75V, not 2.3V.

2. Time when the former signal falls down to 90% of its typical value, e.g. when VDD falls earlier. This time is defined at the cross point of 90% of 2.75V, not 2.3V.

Table 16

Parameter	Value
trPW	+/- no limit
tfPW	+/- no limit
trPWCSX	+/- no limit
tfPWCSX	+/- no limit
trPWRESX	min 10 us
tfPWRESX1	min 120mS
tfPWRESX2	min 0mS

Notes:

There will be no damage to the display module if the above power sequences are not met.

There will be no abnormal visible effects on the display panel during the sequence.

There will be no abnormal visible effects on the display between the end of power on sequence and before entering Sleep Out mode. Also between entering Sleep In mode and power off sequence.

There are no limits for RESX timings during power on sequence. (e.g. from the undefined level to high or low, when the first RESX low pulse after VDD and VDDI are powered-on, etc.)

(8.3) Uncontrolled power-off

Uncontrolled power-off (e.g. the battery is removed without following the proper power-off sequence), will not damage the LCD module or cause the LCD module to inflict any damage on the host. If the LCD module is currently displaying an image, this image may persist for some time. The image will fade however as the LC pixels naturally discharge. Although difficult to predict, the time taken for the discharge process is maximum 10 seconds. Once the LC pixels are fully discharged, the display will appear to be blank.

9. LCD module FPC Circuit diagram

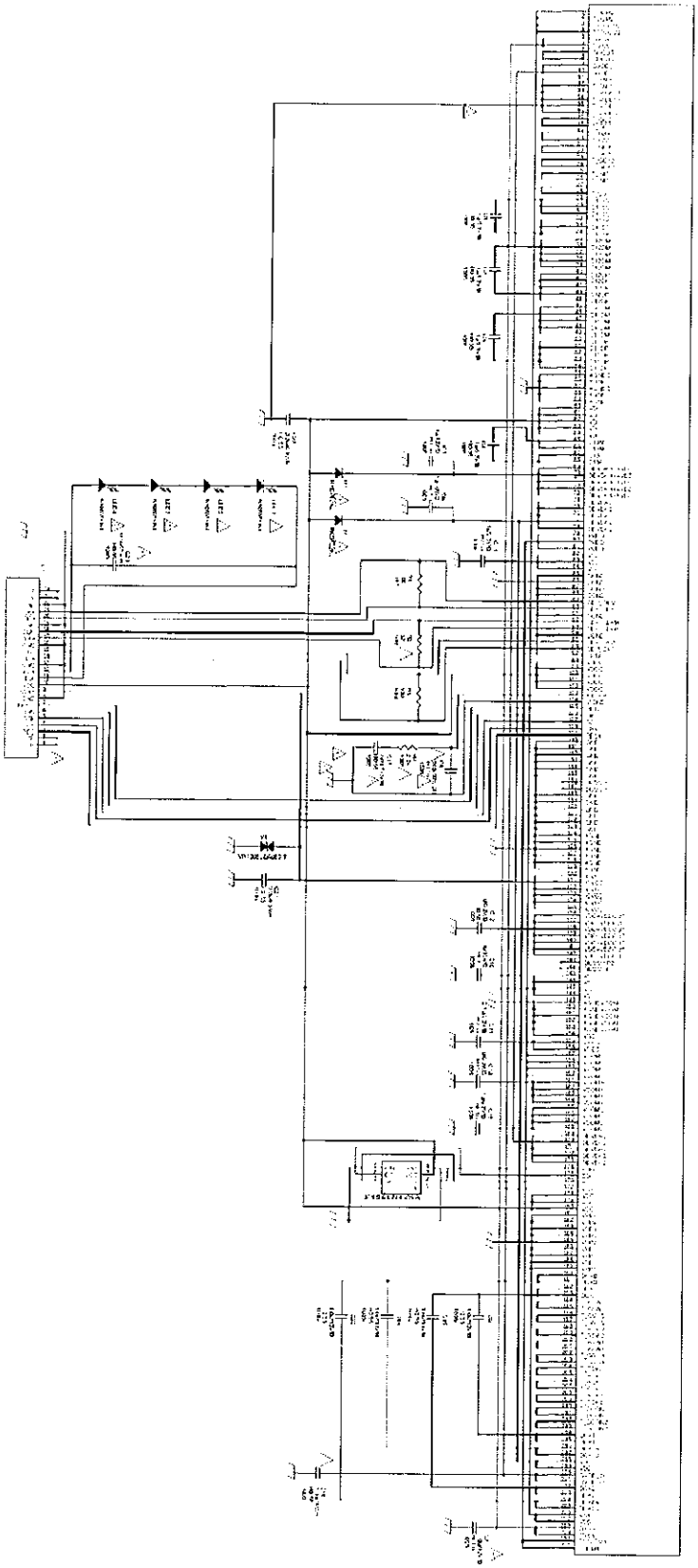


Fig.20

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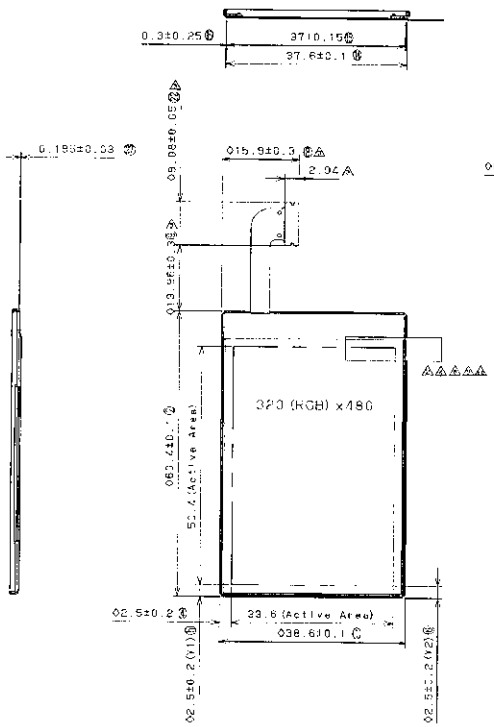
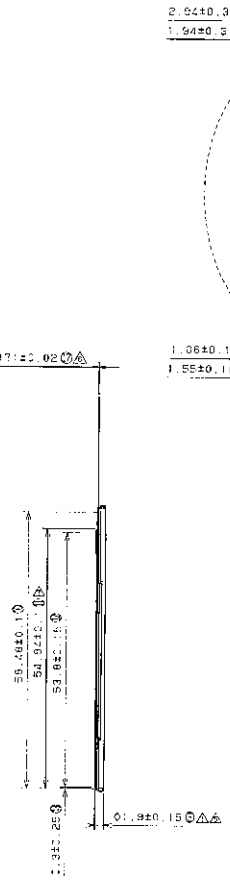
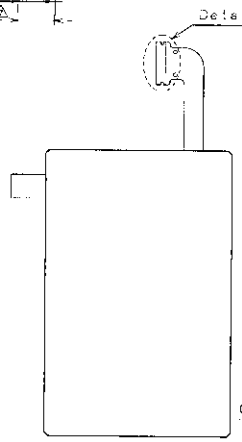
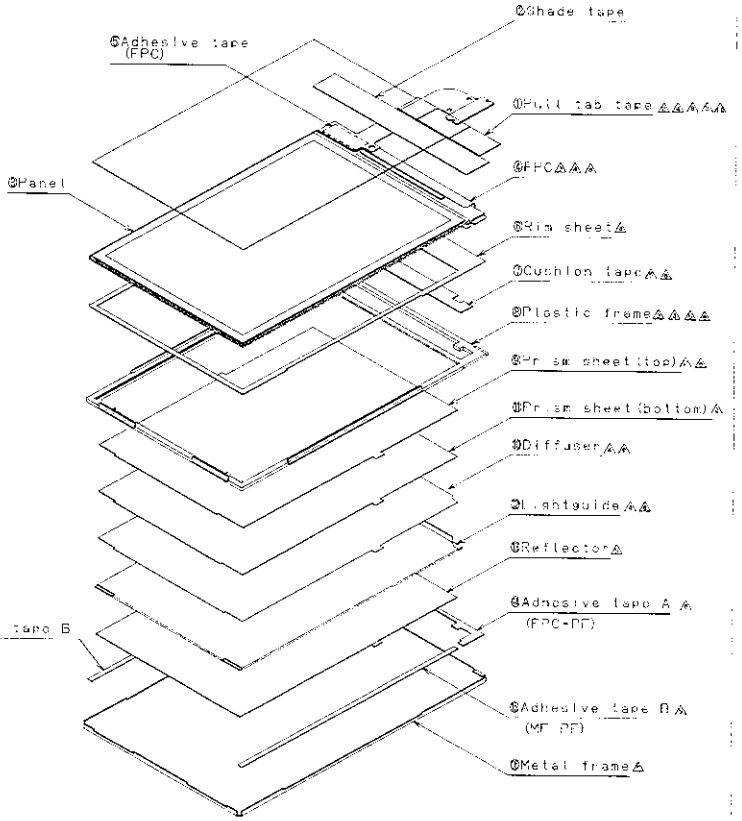
TENTATIVE

NOTE:
This drawing still tentative, because we are under development. There may be changes of this drawing in future.









5	06.Feb.08	Cushion, PF, MF, reflector and adhesive (MF-PF) changed.	4	24.Sep.06	Pull-tab tape turned back to 90 degrees.
4	06.Feb.06	Pull-tab, FPC, PF, diffuser, Rim sheet and LG changed.	3	18.Aug.06	Pull-tab tape changed
3	10.Oct.07	Connector changed from 10PH to ZIF.	2	9.Jun.06	Shape changed
2	12.Sep.07	Prism sheets changed.	1	15.Mar.06	Black diamonds changed to white and dimension added
1	11.Sep.07	Thickness increased.	0	06.Feb.06	Dimension added

改訂記事 REVISION

DESIGNER	DRAFTER	DSN. CK	DSN. CK	ENG. APPD	
S.Abe	S.Aoe	K.Kikuchi	H.Yamashiya	モバイル液晶第1事業部第1開発部	

SHARP CORPORATION

ORIGINAL MODEL: S024JB_X01*

対象、仕様: 2.4" HVGA (320x480)

MATERIAL / FINISH

尺度 SCALE: 1/1

単位 UNIT: mm

原寸サイズ ORIGINAL SIZE: A3

日付 DATE: 05.Apr.07

名称 NAME: LCD Module /LCDモジュール

コード CODE: *

図番 DRAWING: MS-074-01C 改訂 REV: 1C

11. Packaging Specification

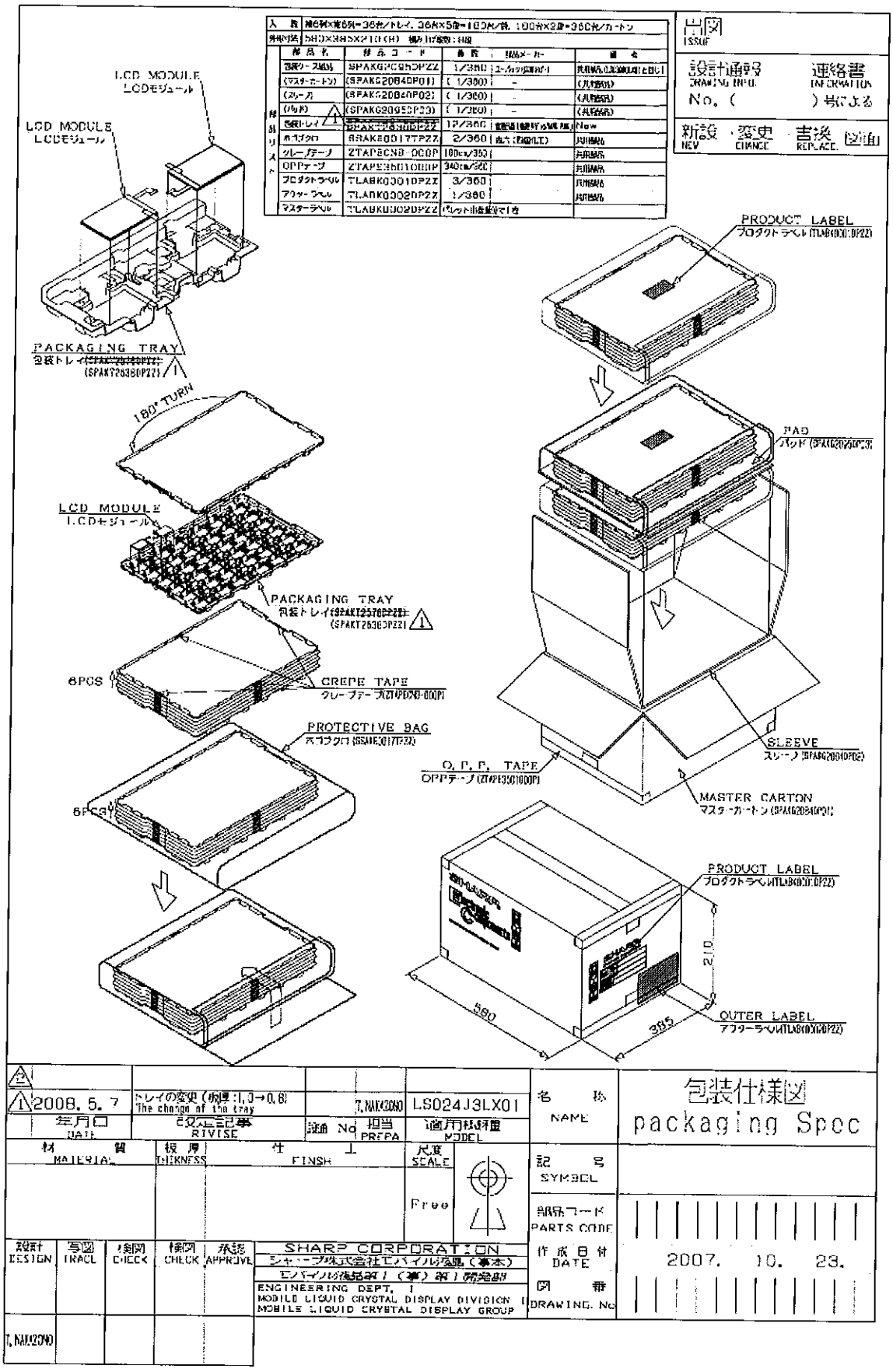


Fig.22