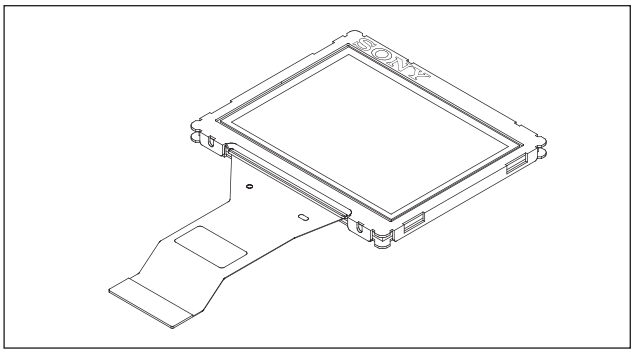
SONY

ACX306AK

3.86cm (1.5 Type) NTSC/PAL Color LCD Panel

Description

The ACX306AK is a 3.86cm diagonal active matrix TFT-LCD panel addressed by low temperature poly-crystalline silicon transistors with built-in peripheral driving circuitry. This panel provides full-color representation for NTSC and PAL systems. In addition, RGB dots are arranged in a delta pattern that provides smooth picture quality without fixed color patterns compared to vertical stripe and mosaic patterns.



Features

- Number of active dots: 118,000, 3.86cm (1.5 Type) in diagonal
- Horizontal resolution: 240 TV lines
- Optical transmittance: 6.5% (typ.)
- High contrast ratio with normally white mode: 200 (typ.)
- Built-in H and V driving circuitry (built-in input level conversion circuit, 3V drive possible)
- Low voltage, low power consumption: 12V drive: 43mW (panel block, typ.)
- Smooth pictures with a RGB delta arrangement
- Supports NTSC/PAL
- Built-in picture quality improvement circuit
- Up/down and/or right/left inverse display function
- LR (low reflectance) surface treatment provides an easy-to-see display even outdoors
- Dirt-resistant surface treatment
- Narrow frame

Element Structure

- Active matrix TFT-LCD panel with built-in peripheral driving circuitry using low temperature polycrystalline silicon transistors
- Number of pixels

  Total number of dots: 494 (H) × 242 (V) = 119,548

  Number of active dots: 490 (H) × 240 (V) = 117,600
- Module dimensions

  Package dimensions: 38 (W) × 32.6 (D) × 2.2 (H) (mm)

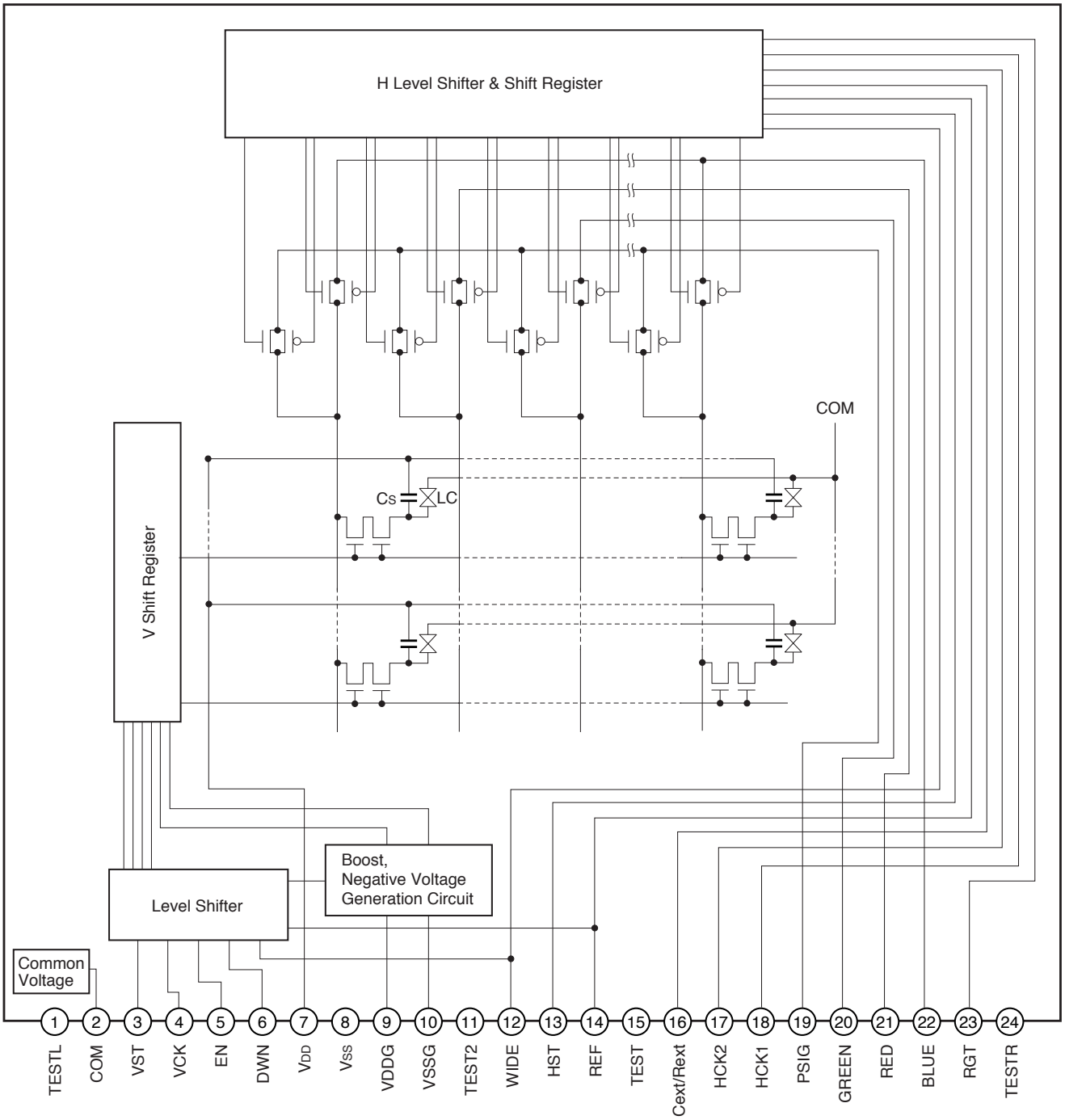
  Effective display dimensions: 31.115 (H) × 30.360 (V) (mm)

Applications

LCD monitors, etc.

Block Diagram

The panel block diagram is shown below.



Absolute Maximum Ratings (V_{SS} = 0V)

• H driver supply voltage	V_{DD}, Cext/Rext	–1.0 to +17	V
• V driver boost supply voltage	VDDG	V_{DD} – 1.0 to +18	V
• V driver negative supply voltage	VSSG	–3.0 to +1.0	V
• Common voltage of panel	COM	–1.0 to +17	V
• H driver input pin voltage	HST, HCK1, HCK2, RGT, WIDE	–1.0 to +17	V
• V driver input pin voltage	VST, VCK, EN, DWN, REF	–1.0 to +15	V
• Video signal, uniformity improvement signal input pin voltage			
	GREEN, RED, BLUE, PSIG	–1.0 to +13	V
• Operating temperature	Topr	–10 to +60	°C
• Storage temperature	Tstg	–30 to +85	°C

Operating Conditions of Panel Block

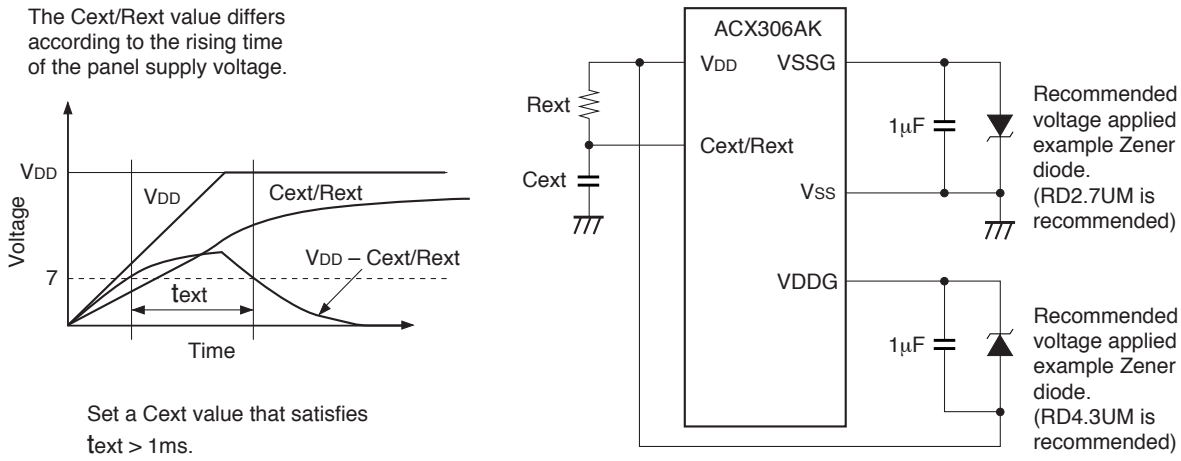
1. Input/output supply voltage conditions*1 (V_{SS} = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	11.4	12.0	12.6	V
	Cext/Rext*2	V_{DD} – 3.4	12.0	—	V
VDDG output voltage setting	VDDG	14.0	15.0	16.3	V
VSSG output voltage setting*3	VSSG	–2.3	–1.8	–1.5	V
Resistor connected to Cext/Rext pin*2	Rext	—	10	160	kΩ

*1 The V_{DD} typical voltage setting is noted as 12.0V in these specifications.

*2 Connect the resistor and capacitor to the Cext/Rext pin as shown in the figure below.

*3 For the VDDG, VSSG output setting, connect an external smoothing capacitor and a voltage stabilizing Zener diode as shown in the figure below.



2. Panel input signal voltage conditions (V_{SS} = 0V)

Item		Symbol	Min.	Typ.	Max.	Unit
H/V driver input voltage	(Low)	VIL	–0.3	0.0	0.3	V
	(High)	VIH	2.6	3.0	5.5	V
REF input voltage		VREF	VIH/2 – 0.3	VIH/2	VIH/2 + 0.3	V
Video signal center voltage*4		VVC	5.8	6.0	6.2	V
Video signal input range*4		Vsig	1.0	VVC ± 4.0	VDDG – 4.0 (10.5V or less)	V
Uniformity improvement signal*4		Vpsig	VVC ± 2.3	VVC ± 2.5	VVC ± 2.7	V
Common voltage of panel (Ta = 25°C)		Vcom	VVC – 0.6	VVC – 0.5	VVC – 0.4	V

*4 Input video and uniformity improvement signals should be input the voltage amplitude symmetrical to VVC as shown in Fig. 1.

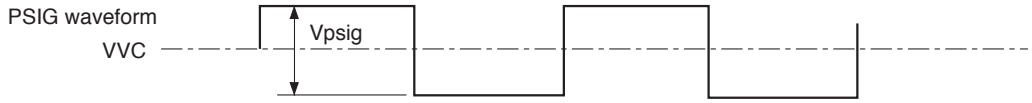


Fig. 1

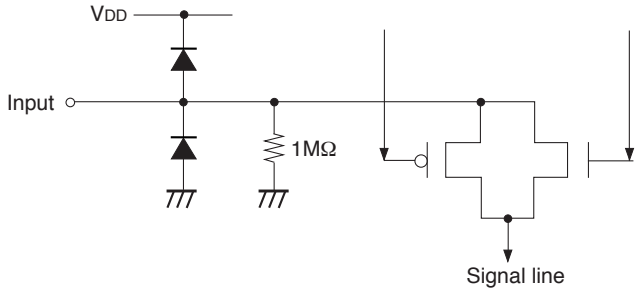
Pin Description of Panel Block

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	TESTL	Panel test output; no connection	13	HST	Start pulse input for H shift register drive
2	COM	Common voltage input of panel	14	REF	Level shifter circuit REF voltage input
3	VST	Start pulse input for V shift register drive	15	TEST	Panel test output; no connection
4	VCK	Clock input for V shift register drive	16	Cext/ Rext	Time constant power supply input for H shift register drive
5	EN	Gate selection pulse enable input	17	HCK2	Clock input for H shift register drive
6	DWN	V shift register drive direction signal input	18	HCK1	Clock input for H shift register drive
7	V_{DD}	Power supply input for V driver	19	PSIG	Uniformity improvement signal input
8	V_{SS}	H and V driver GND	20	GREEN	Video signal (G) input to panel
9	VDDG	Boost power supply setting for V driver	21	RED	Video signal (R) input to panel
10	VSSG	Negative power supply setting for V driver	22	BLUE	Video signal (B) input to panel
11	TEST2	No connection inside the panel. (with 1MΩ terminating resistor)	23	RGT	H shift register drive direction signal input
12	WIDE	Uniformity improvement signal control pulse input	24	TESTR	Panel test output; no connection

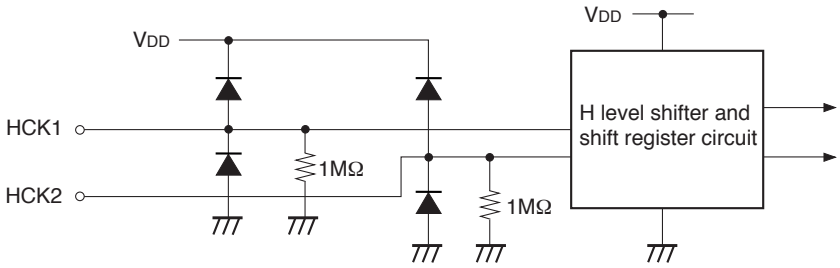
Input Equivalent Circuits of Panel Block

To prevent static charges, protective diodes are provided for each pin except the power supplies. In addition, protective resistors are added to all pins except the video signal input pins. All pins are connected to V_{SS} with a high resistance of 1MΩ (typ.). The equivalent circuit of each input pin is shown below: (Resistor value: typ.)

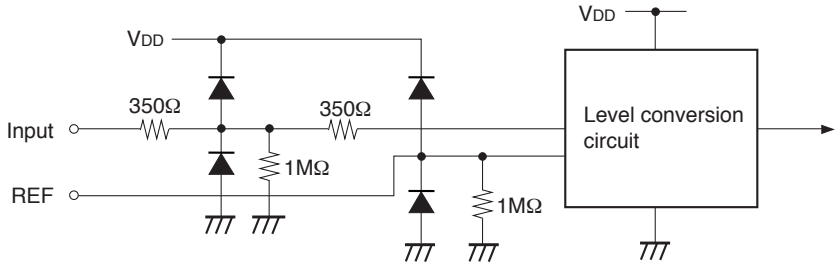
(1) RED, GREEN, BLUE, PSIG



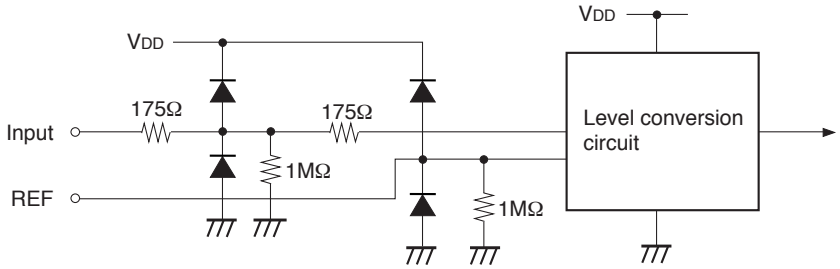
(2) HCK1, HCK2



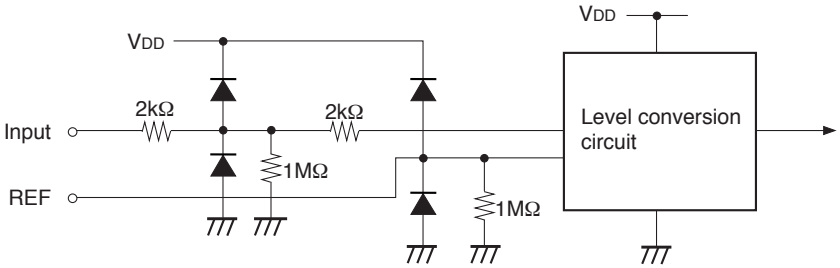
(3) WIDE, REF



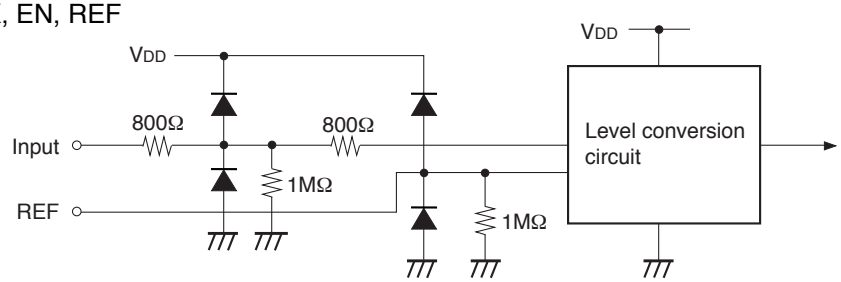
(4) HST



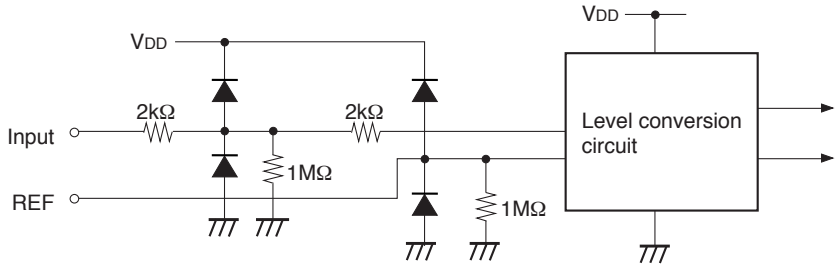
(5) RGT, REF



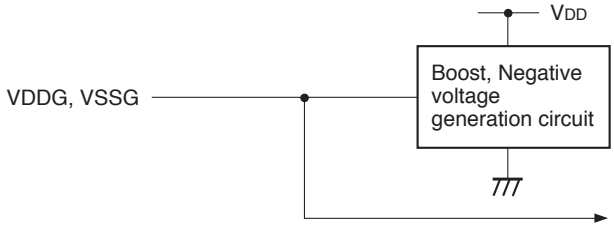
(6) VST, VCK, EN, REF



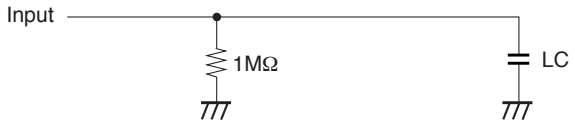
(7) DWN, REF



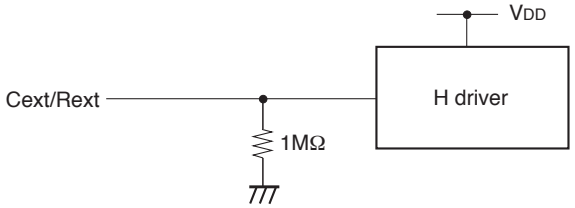
(8) VDDG, VSSG



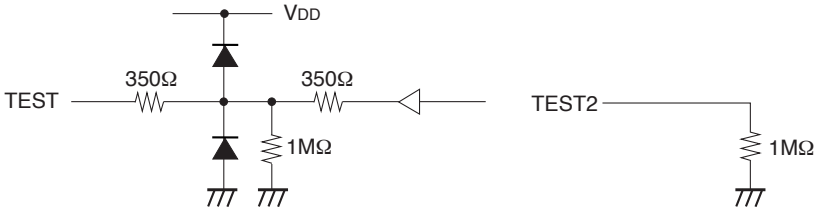
(9) COM



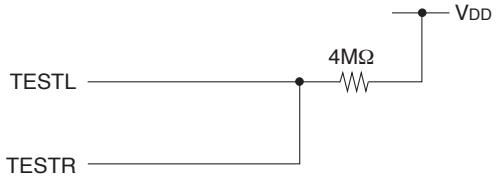
(10) Cext/Rext



(11) TEST, TEST2



(12) TESTL, TESTR

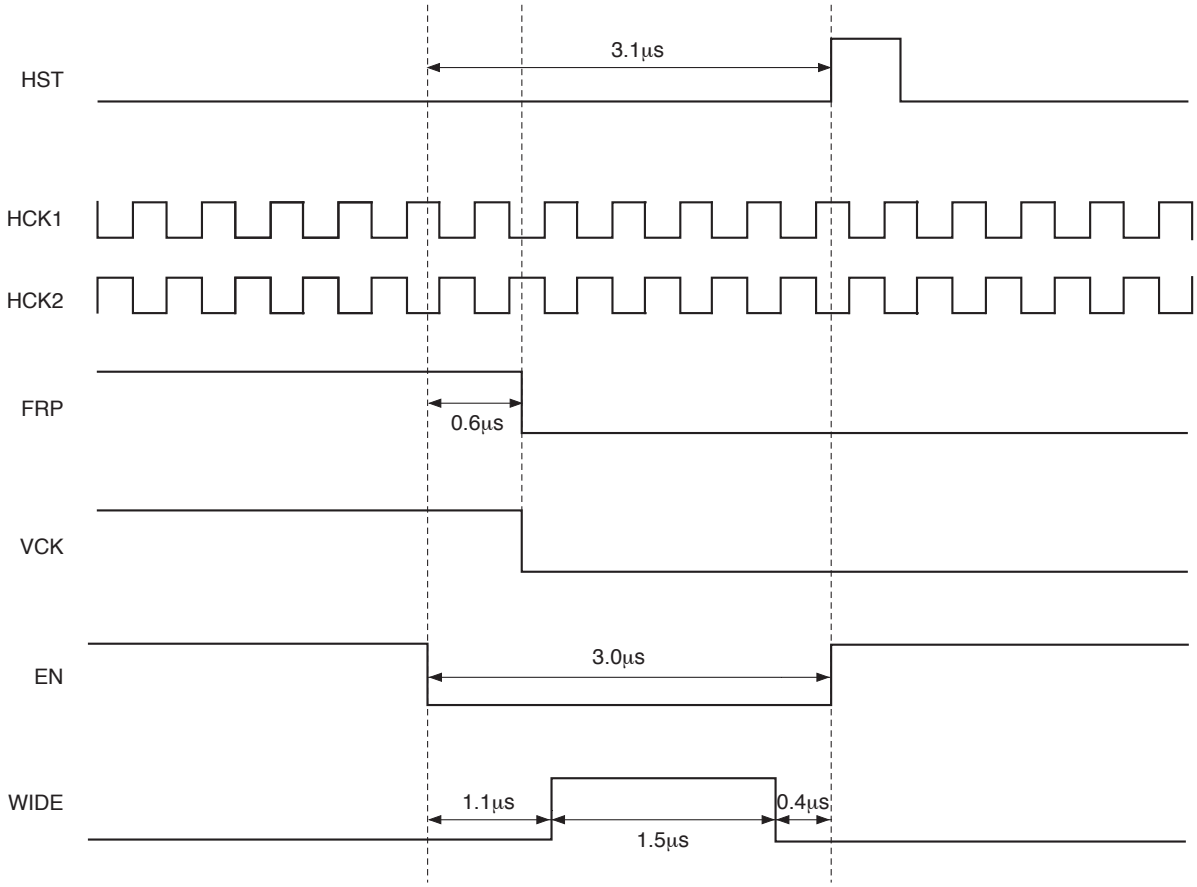


Clock Timing Conditions of Panel Block (VIH = 3.0V, V_{DD} = 12V, Ta = 25°C)

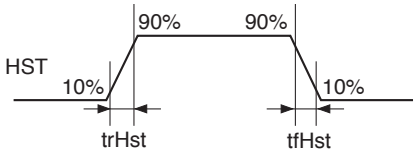
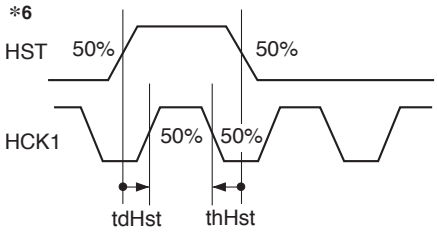
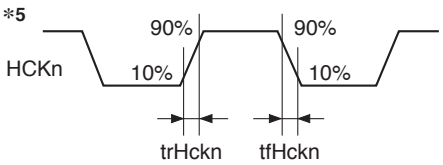
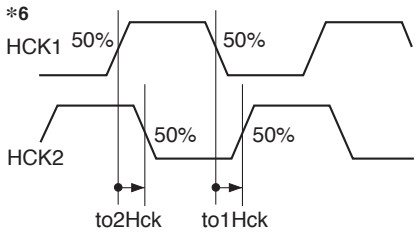
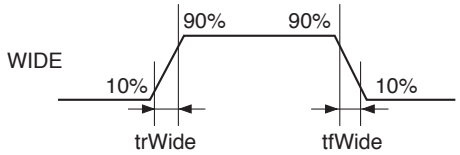
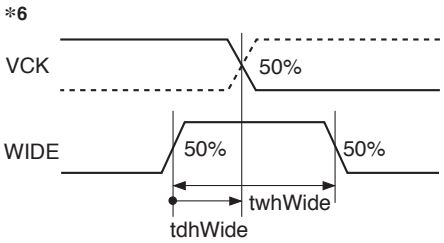
	Item	Symbol	Min.	Typ.	Max.	Unit
HST	HST rise time	trHst	—	—	30	ns
	HST fall time	tfHst	—	—	30	
	HST data setup time	tdHst	300	333	363	
	HST data hold time	thHst	–30	0	30	
HCK	HCKn*5 rise time	trHckn	—	—	30	
	HCKn*5 fall time	tfHckn	—	—	30	
	HCK1 fall to HCK2 rise time	to1Hck	–15	0	15	
	HCK1 rise to HCK2 fall time	to2Hck	–15	0	15	
VST	VST rise time	trVst	—	—	100	
	VST fall time	tfVst	—	—	100	
	VST data setup time	tdVst	30	32	34	μs
	VST data hold time	thVst	–30	–32	–34	
VCK	VCK rise time	trVckn	—	—	100	ns
	VCK fall time	tfVckn	—	—	100	
EN	EN rise time	trEn	—	—	100	
	EN fall time	tfEn	—	—	100	
	EN fall to VCK rise/fall time	tdEn	500	600	700	
	EN pulse width	twEn	2900	3000	3100	
WIDE	WIDE rise time	trWide	—	—	100	
	WIDE fall time	tfWide	—	—	100	
	WIDE (H) rise to VCK rise/fall time	tdhWide	–0.4	–0.5	–0.6	μs
	WIDE (H) pulse width	twhWide	1.4	1.5	1.6	

*5 HCKn means HCK1 and HCK2. (fHCKn = 1.5MHz)

Horizontal Standard Timing



<Horizontal Shift Register Driving Waveforms>

Item		Symbol	Waveform	Conditions
HST	HST rise time	trHst		• HCKn*5 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	HST fall time	tfHst		
	HST data setup time	tdHst		• HCKn*5 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	HST data hold time	thHst		
HCK	HCKn*5 rise time	trHckn		• HCKn*5 duty cycle 50% to1Hck = 0ns to2Hck = 0ns tdHst = 333ns thHst = 0ns
	HCKn*5 fall time	tfHckn		
	HCK1 fall to HCK2 rise time	to1Hck		• tdHst = 333ns thHst = 0ns
	HCK1 rise to HCK2 fall time	to2Hck		
*7 WIDE	WIDE rise time	trWide		
	WIDE fall time	tfWide		
	WIDE rise to VCK rise/ fall time	tdhWide		
	WIDE pulse width	twhWide		

*6 Definitions:

The right-pointing arrow (•→) means +.

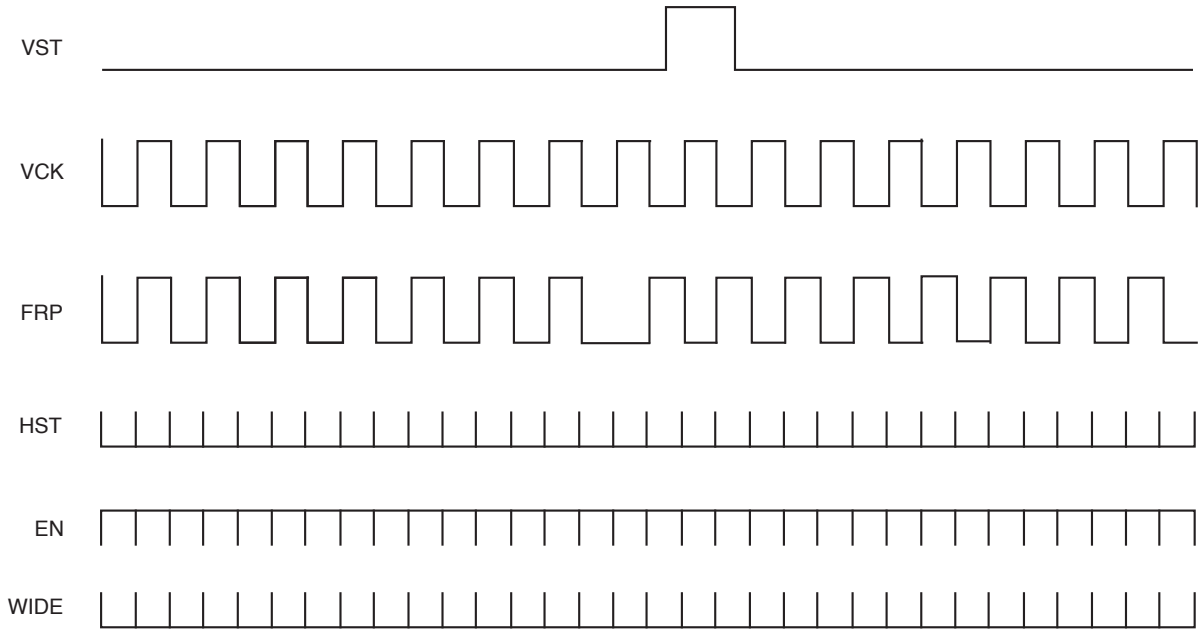
The left-pointing arrow (←•) means –.

The black dot at an arrow (•) indicates the start of measurement

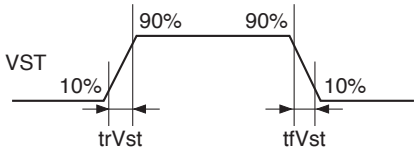
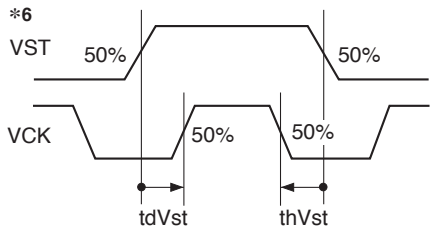
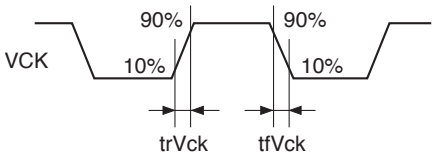
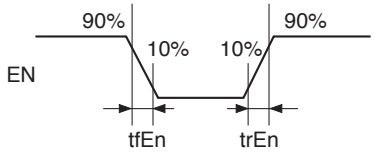
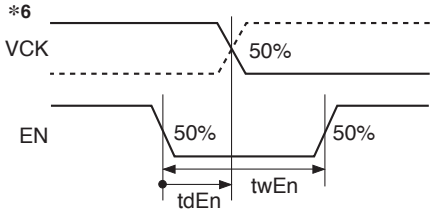
*7 WIDE represents every 1H pulse as shown in Horizontal Timing.

Vertical Standard Timing

NTSC 4:3 (in case of EVEN field)



<Vertical Shift Register Driving Waveforms>

Item		Symbol	Waveform	Conditions
VST	VST rise time	trVst		• VCK duty cycle 50% to1Vck = 0ns to2Vck = 0ns
	VST fall time	tfVst		
	VST data setup time	tdVst		• VCK duty cycle 50% to1Vck = 0ns to2Vck = 0ns
	VST data hold time	thVst		
VCK	VCK rise time	trVck		• VCK duty cycle 50% to1Vck = 0ns to2Vck = 0ns tdVst = 32μs thVst = –32μs
	VCK fall time	tfVck		
EN	EN rise time	trEn		• VCK duty cycle 50% to1Vck = 0ns to2Vck = 0ns
	EN fall time	tfEn		
	EN fall to VCK rise/fall time	tdEn		
	EN pulse width	twEn		

Electrical Characteristics of Panel Block (Ta = 25°C, V_{DD} = 12.0V, VIH = 3.0V, VREF = 1.5V)

1. Horizontal drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
HCKn input pin capacitance		CHckn	—	55	65	pF	
HST input pin capacitance		CHst	—	30	50	pF	
Video signal input pin capacitance		Csig	—	120	150	pF	
Psig input pin capacitance (4:3 display)		Cpsig	—	5.2	8.0	nF	
Input pin current	HCK1	I Hck1	–600	–300	—	μA	HCK1: actual driving
	HCK2	I Hck2	–600	–300	—	μA	HCK2: actual driving
	HST	I Hst	–200	–100	—	μA	HST = GND
	RGT	I RGT	–150	–50	—	μA	RGT = GND
	REF	I REF	–900	–300	—	μA	REF = VIH/2

HCKn: HCK1, HCK2 (1.5MHz)

2. Vertical drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
VCK input pin capacitance		CVck	—	15	20	pF	
VST input pin capacitance		CVst	—	15	20	pF	
Input pin current	VCK	I Vck	–150	–50	—	μA	VCK = GND
	VST	I Vst	–150	–50	—	μA	VST = GND
	EN	I En	–150	–50	—	μA	EN = GND
	DWN	I DWN	–150	–50	—	μA	DWN = GND
	WIDE	I WIDE	–150	–50	—	μA	WIDE = GND

3. Total power consumption of the panel

Item		Symbol	Min.	Typ.	Max.	Unit
Total power consumption of the panel (NTSC)	(Ta = 25°C)	PWR25	—	43	55	mW
	(Ta = 60°C)	PWR60	—	—	75	mW

4. Pin input resistance

Item	Symbol	Min.	Typ.	Max.	Unit
Pin – V_{SS} input resistance 1	Rin1	0.5	1	—	MΩ

Electro-optical Characteristics (Ta = 25°C, NTSC mode)

Item			Symbol	Measurement method	Min.	Typ.	Max.	Unit
Contrast ratio		25°C	CR_{25}	1	100	200	—	—
		60°C	CR_{60}		100	180		
Panel transmittance*1			T	2	6.0	6.5	—	%
Chromaticity	R	X	Rx	3	0.595	0.625	0.655	CIE standards
		Y	Ry		0.310	0.340	0.370	
	G	X	Gx		0.240	0.270	0.300	
		Y	Gy		0.580	0.610	0.640	
	B	X	Bx		0.120	0.150	0.180	
		Y	By		0.08	0.110	0.140	
V-T characteristics*1	V_{90}	25°C	$V_{90\text{-}25}$	4	1.30	1.50	1.70	V
		60°C	$V_{90\text{-}60}$		1.30	1.50	1.70	
	V_{50}	25°C	$V_{50\text{-}25}$		1.70	1.90	2.10	
		60°C	$V_{50\text{-}60}$		1.70	1.90	2.10	
	V_{10}	25°C	$V_{10\text{-}25}$		2.30	2.50	2.70	
		60°C	$V_{10\text{-}60}$		2.30	2.50	2.70	
Half tone color reproduction range*1		R – G	V_{50RG}	5	–0.115	–0.080	–0.045	V
		B – G	V_{50BG}		0	0.03	0.05	
Response time*1	ON time	0°C	ton0	6	—	70	90	ms
		25°C	ton25		—	17	25	
	OFF time	0°C	toff0		—	120	180	
		25°C	toff25		—	30	75	
Flicker*1		60°C	F	7	—	–60	–30	dB
Image retention time*1		60°C	YT1	8	—	—	rank C	s
Viewing angle range		CR ≥ 10	θT θB θL θR	9	15 50 35 35	20 60 40 40	—	Degree (°)
Surface reflection ratio		θ = 0°	Rf	10	—	0.9	1.5	%
Cross talk*1		25°C	CTK	11	—	0.9	1.5	%

*1 Conforms to the measurement results for the discrete panel.

<Electro-optical Characteristics Measurement>

Basic measurement conditions

(1) Driving voltage

V_{DD} = 12.0V, VIH = 3.0V, VREF = 1.5V

VVC = 6.0V, VCOM = 5.5V, Vpsig = 6.0 ± 2.5V

(2) Measurement temperature

25°C unless otherwise specified.

(3) Measurement point

One point in the center of the screen unless otherwise specified.

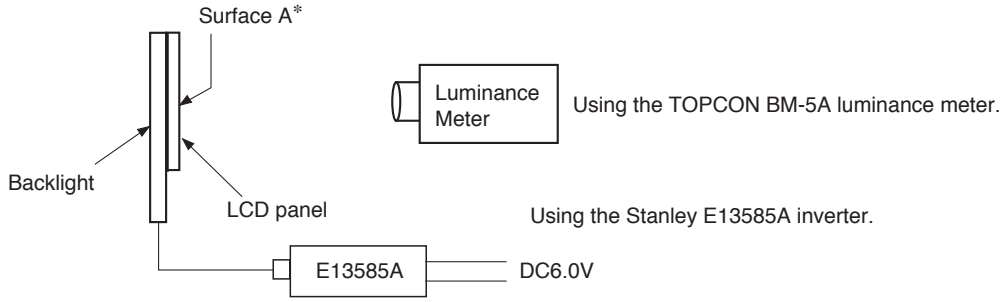
(4) Measurement systems

Three types of measurement systems are used as shown below.

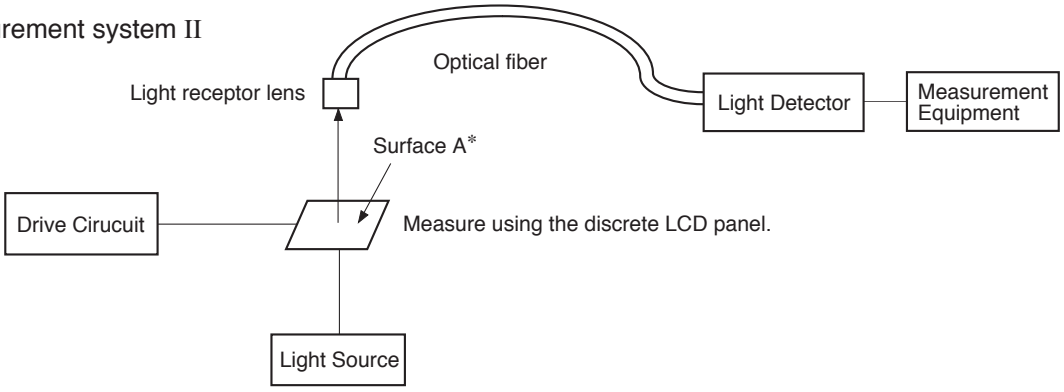
(5) R, G and B input signal voltage Vsig

Vsig = 6.0 ± V_{AC} [V] (V_{AC}: signal amplitude)

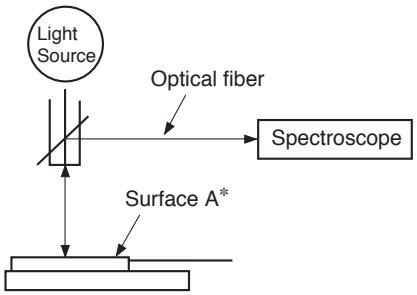
• Measurement system I



• Measurement system II



• Measurement system III



* Surface A: See the Package Outline.

1. Contrast Ratio

Contrast ratio (CR) is given by the following formula.

CR = L (White)/L (Black)

L (White): Surface luminance of the TFT-LCD panel at the input signal amplitude V_{AC} = 0.5V.

L (Black): Surface luminance of the panel at V_{AC} = 4.0V.

Both luminosities are measured by System I.

2. Optical Transmittance of Panel

Optical transmittance (T) is given by the following formula.

T = L (White)/Luminance of Backlight × 100 [%]

3. Chromaticity

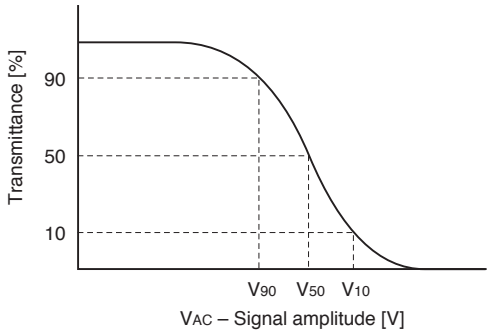
Chromaticity of the panels is measured by System I. Raster modes of each color are defined by the representations at the input signal amplitude conditions shown in the table below. System I uses x and y of the CIE standards as the chromaticity here.

		Signal amplitudes (V_{AC}) supplied to each input		
		R input	G input	B input
Raster	R	0.5	4.0	4.0
	G	4.0	0.5	4.0
	B	4.0	4.0	0.5
	W	0.0	0.0	0.0

(Unit: V)

4. V-T Characteristics

V-T characteristics, or the relationship between signal amplitude and the transmittance of the panel, are measured by System II by inputting the same signal amplitude V_{AC} to each input pin. V_{90}, V_{50}, and V_{10} correspond to the voltages which define 90%, 50%, and 10% of transmittance respectively.

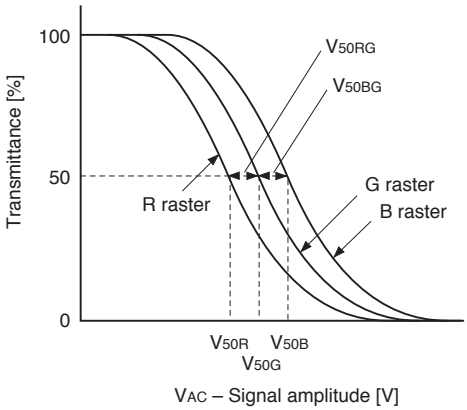


5. Half Tone Color Reproduction Range

The half tone color reproduction range of LCD panels is characterized by the differences between the V-T characteristics of R, G and B. The differences of these V-T characteristics are measured by System II. System II defines signal voltages of each R, G and B raster mode which correspond to 50% of transmittance, V_{50R}, V_{50G} and V_{50B}, respectively. V_{50RG} and V_{50BG}, that is to say the differences between V_{50R} and V_{50G} and between V_{50B} and V_{50G}, are given by the following formulas respectively.

$V_{50RG} = V_{50R} - V_{50G}$

$V_{50BG} = V_{50B} - V_{50G}$

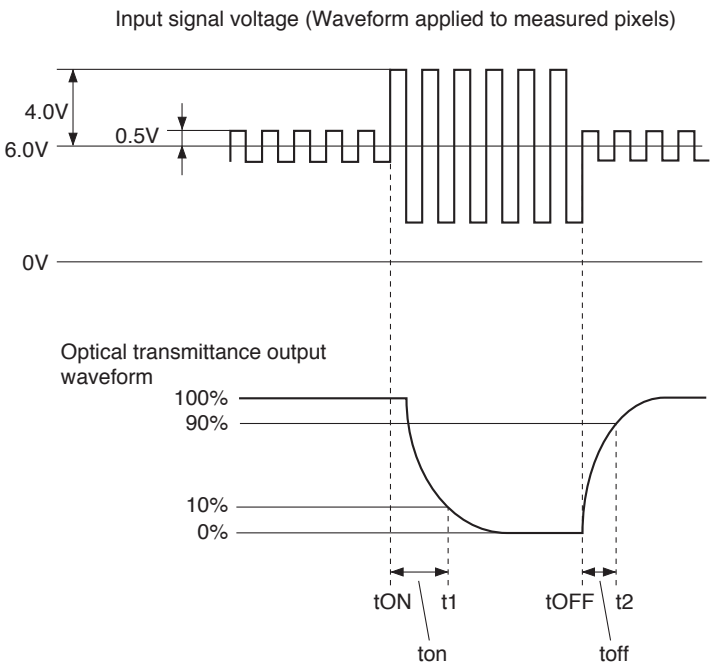


6. Response Time

Response times ton and toff are measured by System II by applying the input signal voltages in the figure to the right to each input pin. These times are defined by the following formulas.

ton = t1 – tON
toff = t2 – tOFF
t1: time which gives 10% transmittance of the panel.
t2: time which gives 90% transmittance of the panel.

The relationships between t1, t2, tON and tOFF are shown in the figure to the right.



7. Flicker

Flicker (F) is given by the following formula. DC and AC components (NTSC: 30Hz, rms; PAL: 25Hz, rms) of the panel output signal for gray raster* mode are measured by a DC voltmeter and a spectrum analyzer in System II.

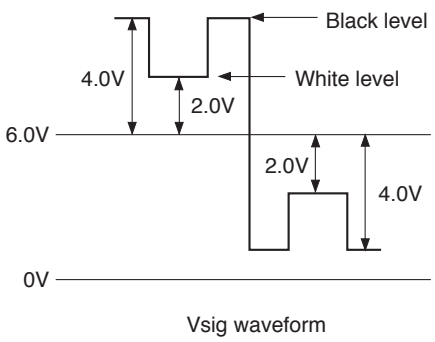
F [dB] = 20 log {AC component/DC component}

* R, G, B input signal voltage for gray raster mode is given by Vsig = 6.0 ± V_{50} [V]
where: V_{50} is the signal amplitude which gives 50% of transmittance in V-T curve.

8. Image Retention Time

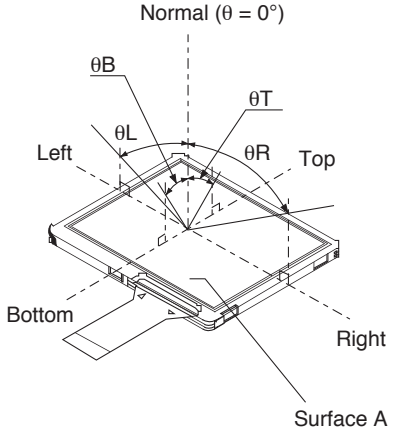
Image retention time is given by the following procedures.
Apply the monoscope pattern* to the LCD panel for 1 minute and then change to a gray scale signal (Vsig = 6.0 ± V_{AC} [V]; V_{AC} = 3 to 4V). Judging by sight at the V_{AC} that holds the maximum image retention, measure the time for the residual image to disappear.

* Monoscope pattern input conditions
Vsig = 6.0 ± 4.0 or 6.0 ± 2.0 [V]
(shown in the figure to the right)
Vcom = 5.5V



9. Definition of Viewing Angle Range

Viewing angle range is measured by System I. The contrast ratio (CR) is measured at the angles defined in the figure to the right and the range where CR ≥ 10 is taken as the viewing angle range.
Measure with surface A* facing upwards.
* Surface A: See the Package Outline.



10. Surface Reflection Ratio

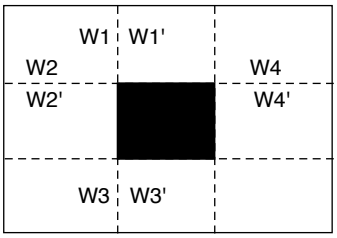
Surface reflection ratio (Rf) is given by the following formula.

Rf = Reflected optical luminance of the panel surface A*/Reflected optical luminance of Al (wafer) × 100 [%]

The incident and reflected angles of light are both 0°.
Both luminosities are measured by System III.
* Surface A: See the Package Outline.

11. Cross Talk

Cross talk is determined by the luminance differences between adjacent areas represented by Wi' and Wi (i = 1 to 4) around the black window (Vsig = 4.0V/1V).

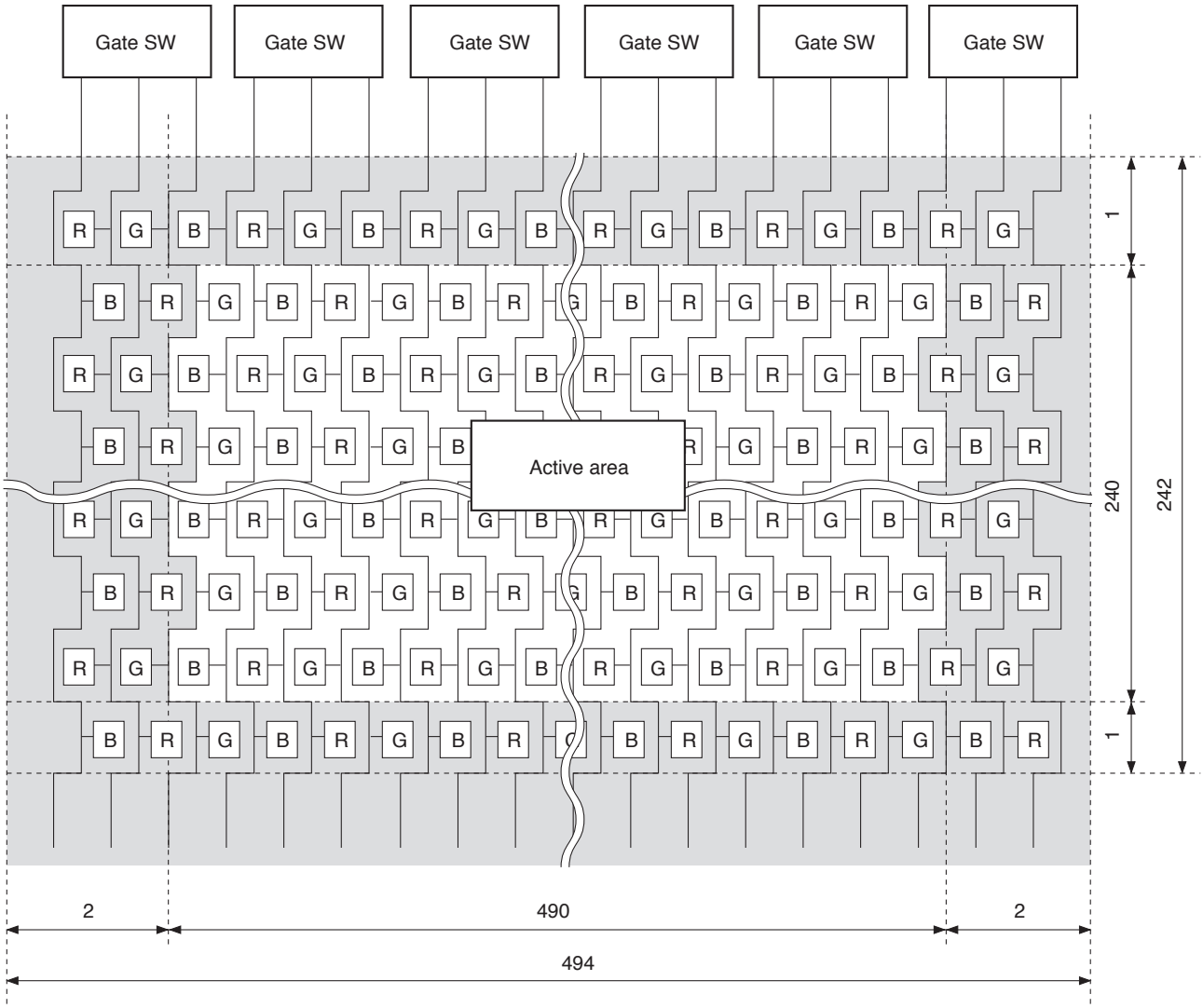


Cross talk value $CTK = \left| \frac{Wi' - Wi}{Wi} \right| \times 100$ [%]

Description of Panel Block Operation

1. Color Coding

The color filters are coded in a delta arrangement. The shaded area is used for the dark border around the display.



2. Description of LCD Panel Operations

- A vertical driver, which consists of vertical shift registers, enable-gates and buffers, applies a selected pulse to each of 240 line electrodes sequentially one line electrode at a time in a single horizontal scanning period.

- The selected pulse is output when the enable pin goes to high level. PAL signal pulse elimination display is possible by using the enable pin and simultaneously controlling VCK.

- A horizontal driver, which consists of horizontal shift registers, gates and CMOS sample-and-hold circuitry, applies selected pulses to each of 490 signal electrodes sequentially in a single horizontal scanning period. These pulses are used to supply the sampled video signal to the row signal lines.

- The scanning direction of the horizontal shift registers can be switched with the RGT pin. The scanning direction is left to right (right scan) for RGT pin at high level (2.6 to 5.5V), and right to left (left scan) for RGT pin at low level (0V). In addition, the scanning direction of the vertical shift registers can be switched with the DWN pin. The scanning direction is top to bottom for DWN pin at high level (2.6 to 5.5V), and bottom to top for DWN pin at low level (0V). (These scanning directions are from a front view.)

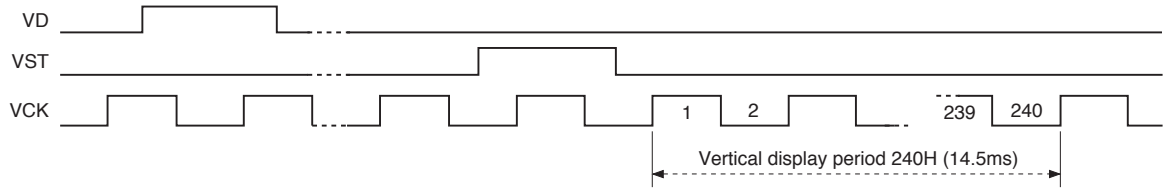
- The vertical and horizontal drivers address one pixel, and then thin film transistors (TFTs; two TFTs for one pixel) turn on to apply a video signal to the pixel. The same procedures lead to the entire 240 × 490 pixels to display a picture in a single vertical scanning period.

- Pixel dots are arranged in a delta pattern, where sets of RGB pixels are positioned shifted by 1.5 dots against adjacent horizontal lines. The horizontal driver output pulse must be shifted by 1.5 dots for each horizontal line against the horizontal sync signal to apply a video signal to each pixel properly.

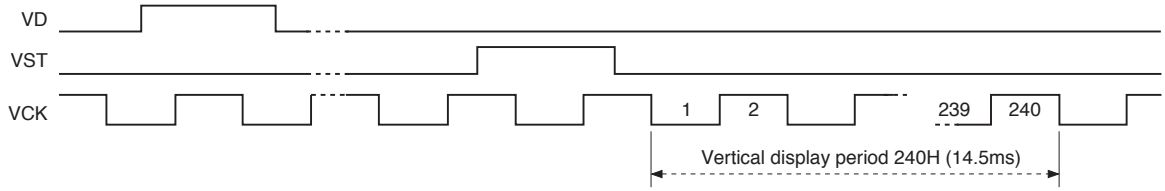
- The video signal should be input with the polarity-inverted every horizontal cycle.

- The relationships between the vertical shift register start pulse VST and the vertical display period, and between the horizontal shift register start pulse HST and the horizontal display period are shown below for top to bottom and left to right scan.

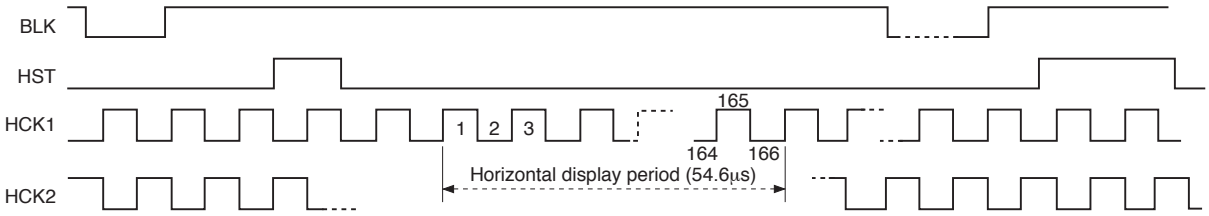
(1) Vertical display period (DWN: high level)



(2) Vertical display period (DWN: low level)



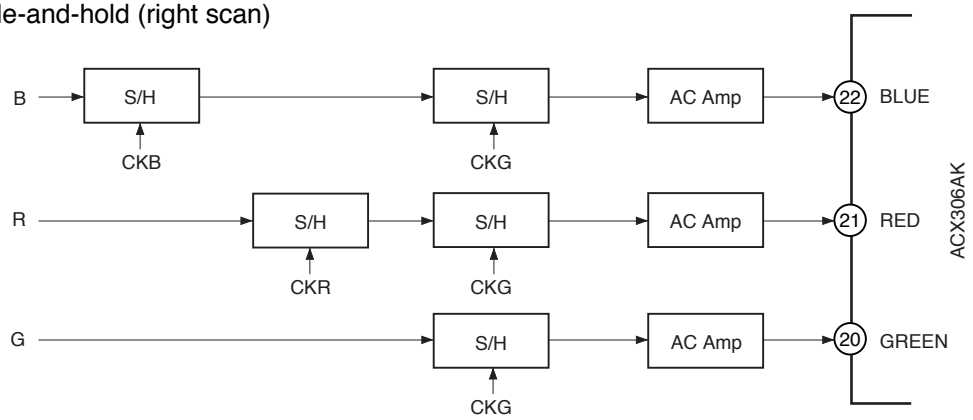
(3) Horizontal display period (RGT: high level)



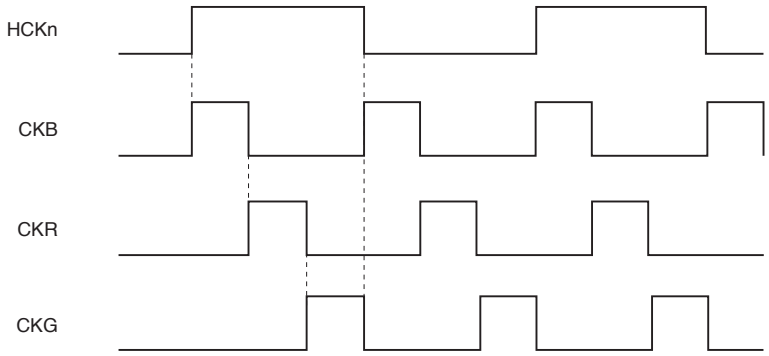
3. RGB Simultaneous Sampling

The horizontal driver samples R, G and B video signal simultaneously, which requires phase matching between the R, G and B signals to prevent the horizontal resolution from deteriorating. Thus phase matching by an external signal delay circuit is needed before applying the video signal to the LCD panel.
Two methods are applied for the delaying procedure: Sample-and-hold and Delay circuit. These two block diagrams are as follows.
The ACX306AK has a right/left inversion function. The following phase relationship diagram indicates the phase setting for right scan (RGT = high level). For left scan (RGT = low level), the phase setting should be inverted for the B and G signals.

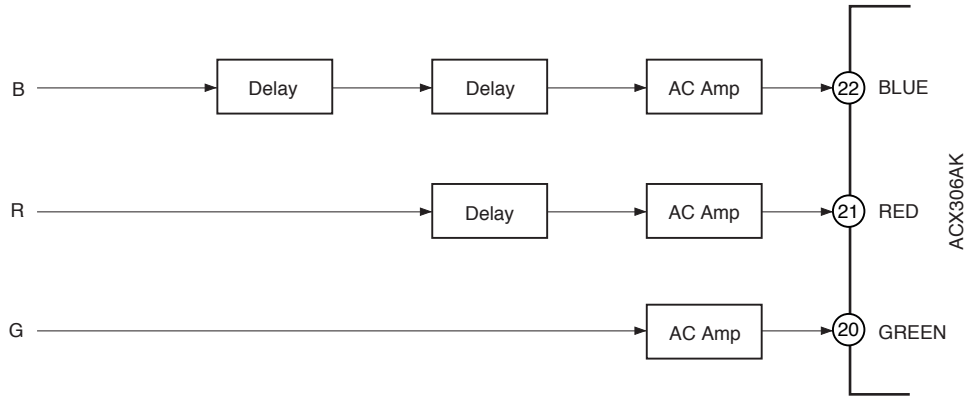
(1) Sample-and-hold (right scan)



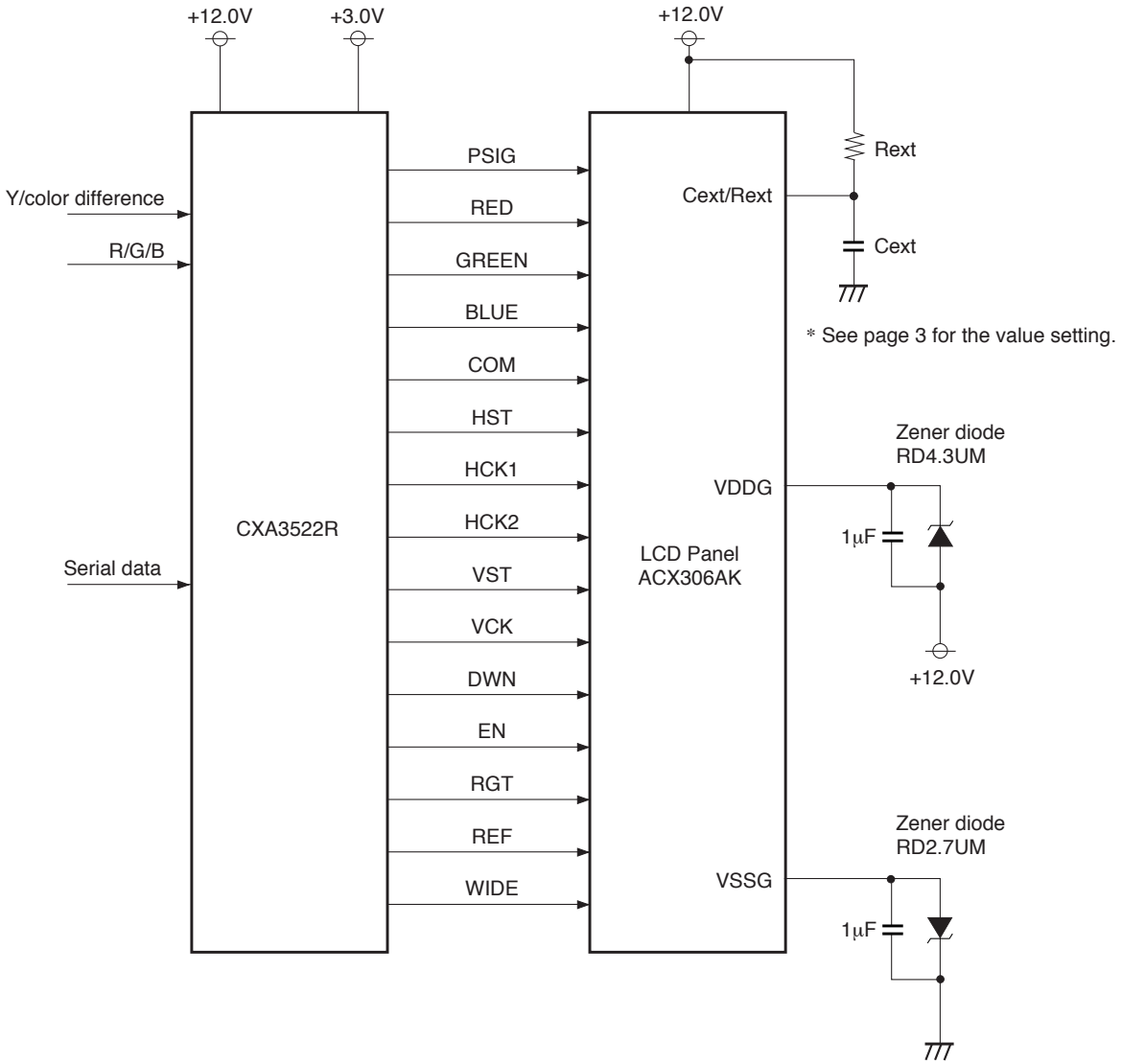
<Phase relationship of delaying sample-and-hold pulses> (right scan)



(2) Delay element (right scan)



System Configuration



Notes on Handling

(1) Static charge prevention

Be sure to take the following protective measures. TFT-LCD panels are easily damaged by static charges.

a) Use non-chargeable gloves, or simply use bare hands.
b) Use an earth-band when handling.
c) Do not touch any electrodes of a panel.
d) Wear non-chargeable clothes and conductive shoes.
e) Install grounded conductive mats on the working floor and working table.
f) Keep panels away from any charged materials.
g) Use ionized air to discharge the panels.

(2) Protection from dust and dirt

a) Operate in a clean environment.
b) When delivered, the panel surface (Polarizer) is not covered by a protective sheet. Take care of handling it so as not to damage the polarizer.
c) Do not touch the polarizer surface. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on the surface.
d) Use ionized air to blow dust off the panel.

(3) Others

a) Do not twist or bend the flexible PC board especially at the connecting region because the board is easily deformed.
b) Do not drop the panel.
c) Do not twist or bend the panel or panel frame.
d) Keep the panel away from heat sources.
e) Do not dampen the panel with water or other solvents.
f) Avoid storage or use the panel at high temperatures or high humidity, as this may result in damage.

Package Outline Unit: mm