SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	AM240320H5TNQW-00H
APPROVED BY	
DATE	

□Approved For Specifications

☑ Approved For Specifications & Sample

CHECKED BY	ORGANIZED BY
	CHECKED BY

RECORD OF REVISION

Revision Date	Page	Contents	Editor
2006/05/16	-	New Release	Jason
2006/06/26	-	Rename TF240320-27-0 to AM240320H5TNQW-00H	Jason
2006/7/11	4	Modify the Environment	Jason
2006/7/11	16	Add the Register Description interpretation	Jason
2006/7/20	4	Modify the operation and storage environment.	Eric
	27	Added the dot defect of inspection quality criteria.	Eric

1 Features

LCD 2.2 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) for mobile-phone or handy electrical equipments. The LCD adopts one backlight with High brightness 3-lamps white LED.

(1) Construction: 2.2" a-Si color TFT-LCD with White LED Backlight and FPC.

- (2) LCD : 2.1 Amorphous-TFT 2.2 inch display, transmissive, Normally white type, 12 o'clock.
 - 2.2 240(RGB)X320 dots Matrix,1/320 Duty.
 - 2.3 LCD controller is HX8312A.
 - 2.4 Real 262K colors display:
 - Red-5bit, Green-6bit, Blue-5bit
- (3) 8-bit or 16-bit high speed bus interface and high speed RAM-write function.
- (4) Direct data display with display RAM.

LCD Internal RAM capacity: 172,800bytes

(5) MPU interface: 8 bits or 16 bits 80-serise parallel interface is available.

2 Mechanical specifications

Dimensions and weight

	<u> </u>		
Item		Specifications	Unit
External shape dimensions		*1 40.1 (W) x 52.816(H) x 3.995(TMax.)	mm
Main	Pixel pitch	0.1395 (W) x 0.1395(H)	mm
LCD	Active area	33.48 (W) x 44.64 (H)	mm
LOD	Viewing area	35.24 (W) x 46.24 (H)	mm
	Weight	10.5	g

*1. This specification is about External shape on shipment from AMPIRE.

3 Absolute max. ratings and environment

3-1 Abs	solute	max.	ratings
---------	--------	------	---------

Ta=25°C GND=0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power Supply for Logic	VDD – GND	-0.3	+4.0	V	
Power Input Voltage	Vci	-0.3	+4.6	V	
Power Supply for LED backlight	LED A – LED K	-0.5	+12	V	
Input voltage	VIN	-0.5	VDD+0.5	V	

3-2 Environment

Item	Specifications	Remarks
Storage	Max. +80°C	Note 1:
temperature	Min. –30 °C	Non-condensing
Operating	Max. +70 °C	Note 1:
temperature	Min20 °C	Non-condensing

Note 1 : Ta \leq +40 °C · · · Max.85%RH

Ta>+40 °C · · · The max. humidity should not exceed the humidity with 40 °C 85%RH.

4 Electrical specifications

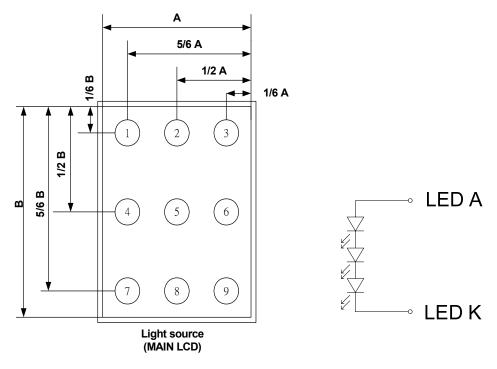
				(V _{DD}	=2.8V, 1	ā=25 °C)
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IC power voltage	V_{DD}		2.2	2.8	3.3	V
Power input voltage	Vci		2.5	-	3.3	V
High-level input voltage	V _{IHC}		0.8V _{DD}		V _{DD}	V
Low-level input voltage	V _{ILC}		0		$0.2V_{DD}$	V
Consumption current of VDD	I _{DD}		-	2.5	4	mA
Consumption current of LED	I _{LED}	V _{LED} =9.8V	-	15	20	mA

※ 1. 1/320 duty

4-2 LED back light specification

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Forward voltage	V _f	I _f =15mA	9.3	9.8	10.8	V	
Reverse voltage	Vr		-	-	12	V	
Forward current	۱ _f	3-chip Serial	12	15	20	mA	
Power Consumption	P _{BL}	I _f =20mA	-	196	-	mW	
Uniformity (with L/G)	- I _f =15mA 80% *1						
Bare LED Luminous intensity	V _f I _f	20mA	3600	-	-	cd/m ²	
Luminous color	White						
Chip connection		3 chip serial connection					

LCM measure position:



*1 Uniformity (LT):
$$\frac{Min(P1 \sim P9)}{Max(P1 \sim P9)} \times 100 \ge 80\%$$

5 Optical characteristics

5.1 Optical characteristics

(1/320 Duty in case except as specified elsewhere Ta = 25° C)

LED backlight transmissive module:

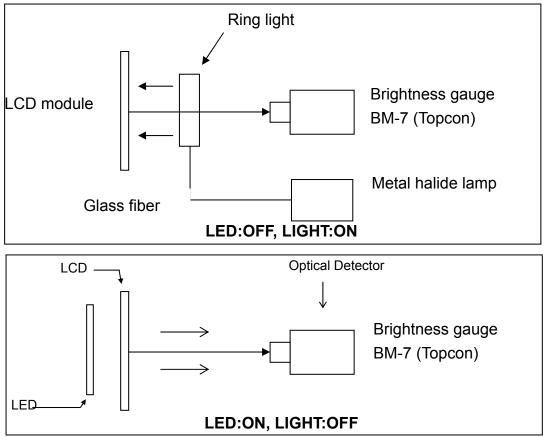
Item	Symbol	Temp.	Min.	Std.	Max.	Unit	Conditions
Response	Tr	25 °C	-	10	25	ms	θ =0 °° , φ =0 °
time	Tf	25 °C	-	20	40	1115	(Note 2)
Contrast ratio	CR	25 °C	150	200	-	-	$\theta = 0^{\circ}, \phi = 0^{\circ}$ LED:ON, LIGHT:OFF (Note 4)
Transmittance	Т	25 °C	-	6.9	-	%	
Visual angle range front and rear	θ	25 °C		(<i>θ</i> f) 35 (<i>θ</i> b) 60		De- gree	φ = 0°, CR \ge 10 LED:ON LIGHT:OFF (Note 3)
Visual angle range left and right	θ	25 °C	(<i>θ</i> I) 60 (<i>θ</i> r) 60		De- gree	φ =90°, CR \geq 10 LED:ON LIGHT:OFF (Note 3)	
Visual angle direction priority				12:00			(Note 5)
Brightness				200		Cd/ m2	I _{LED} =20mA, Full White pattern

Item	Symbol	-	Transmissive	Conditions	
	Gymbol	Min.	Std.	Max.	Conditions
Red	х	0.615	0.645	0.645	$\theta = 0^\circ$, $\varphi = 0^\circ$
	У	0.343	0.373	0.373	
Green	х	0.307	0.337	0.337	$\theta = 0^\circ$, $\varphi = 0^\circ$
	У	0.563	0.593	0.593	, , -
Blue	х	0.133	0.163	0.163	$\theta = 0^\circ$, $\varphi = 0^\circ$
	У	0.150	0.180	0.180	, , -
White	х	0.309	0.339	0.339	$\theta = 0^\circ$, $\varphi = 0^\circ$
	У	0.350	0.380	0.380	

Main LCD: (1/320 Duty Ta = 25°C)

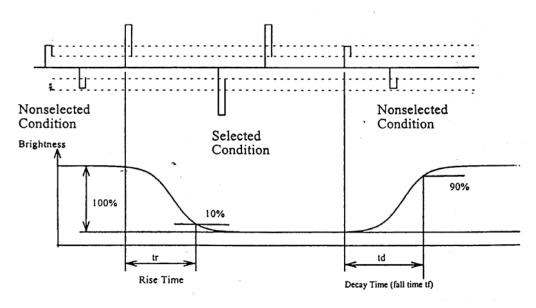
Light source

Item	Symbol		Value	Conditions	
Rem	Gymbol	Min.	Std.	Max.	Conditions
Light source	х	0.28	0.315	0.34	$\theta = 0^{\circ}$, $\varphi = 0^{\circ}$
Light course	У	0.28	0.305	0.34	
LED brightness		3600	_	_	Unit: cd/m ²
		5500	-		(I _{LED} =20mA)

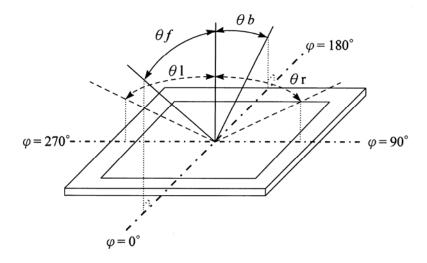


NOTE 1: Optical characteristic measurement system

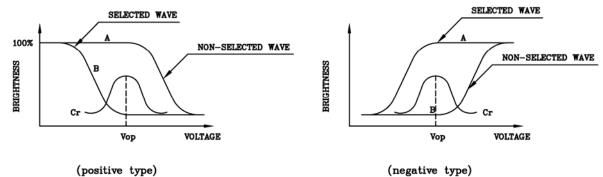
NOTE 2: Response tome definition



NOTE 3: $\varphi \cdot \theta$ definition

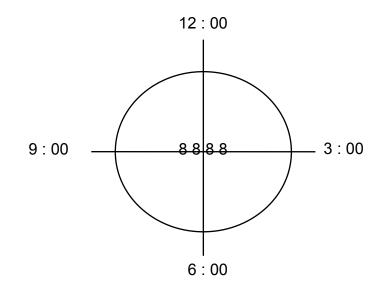






Contrast Ratio : Cr=A/B

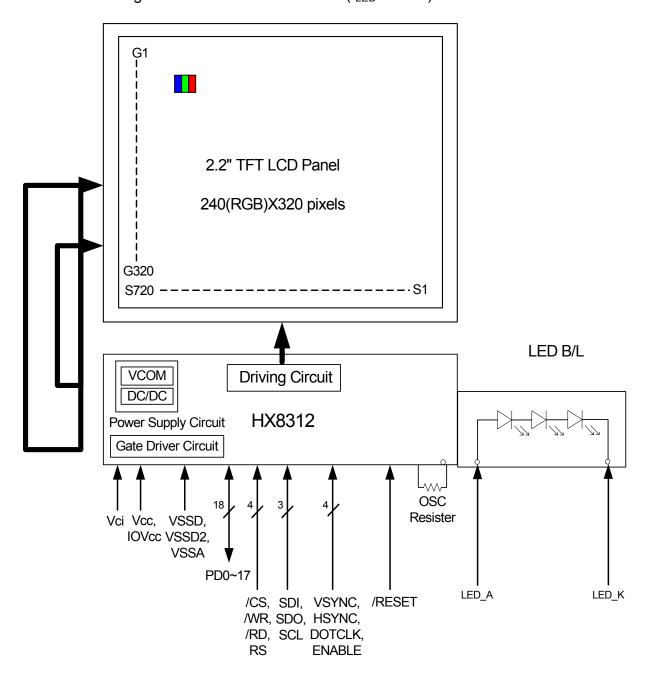
NOTE 5: Visual angle direction priority



6 Block Diagram

Block diagram (Main LCD)

Display format:A-Si TFT transmissive, Normally white type, 12 o'clock.Display mode:Normally whiteDisplay composition:240 x RGB x 320 pixelsLCD Driver :HX8312Back light:White LED x 3 (I_{LED}=20mA)



7 Interface specifications

Pin No.	Terminal	Functions	
1	LED_A	LED Backlight anode connection	
2	LED_A	LED Backlight anode connection	
3	LED_K	LED Backlight cathode connection	
4	LED_K		
5	TDX2	Selection the Serial bus interface mode. L:16-bit, H: 8-bit	
6	BWSO	Selection the Serial bus interface mode. L:16-bit, H: 8-bit	
7	/RESET	LCD Reset terminal, active "L"	
8	DB15		
9	DB14		
10	DB13		
11	DB12		
12	DB11		
13	DB10		
14	DB9		
15	DB8	Data Bus for 8-bits, 80-series MPU (MPU4 、 7 type)	
16	DB7		
17	DB6		
18	DB5		
19	DB4		
20	DB3		
21	DB2		
22	DB1		
23	DB0		
24	NC	No Connection	
25	NC	No Connection	
26	/RD	Read clock terminal, active "L" (80 series interface)	
27	/WR	Write clock terminal, active "L" (80 series interface)	
28	RS	The signal for register index or register command select . Low: Register index or internal status (in read operation); High: Register command.	

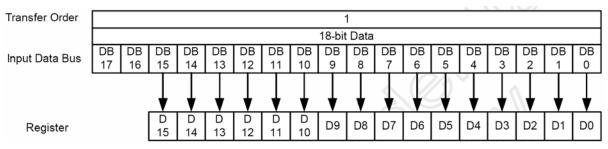
29	/CS	Chip select signal. Low: chip can be accessed; High: chip cannot be accessed.	
30	VCC	Power supply for the internal logic circuit. (VCC=2.2~3.3V)	
31	VCC		
32	NC	No Connection	
33	VCI	Power supply for Step-up circuit. (VCi=2.5~3.3V)	
34	VSS	GND-terminal.	
35	VSS	GND-terminal.	
36	NC	No Connection	
37	NC	No Connection	
38	NC	No Connection	
39	NC	No Connection	

7.1 System interface

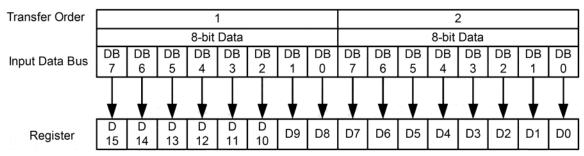
IM bits setting and the type of system interface for LCD

Interface	External S	etting Pin	Bus	Bit number	Transferring Method of	Transferring Method of
Туре	BWS0	DTX2	Width	in a pixel	RAM data	Command
MPU4	0	0	16-bit Parallel	16bits	16-bit twice	16-bit twice
MPU7	1	1	8-bit Parallel	16bits	8-bit twice	8-bit twice

MPU4 Type

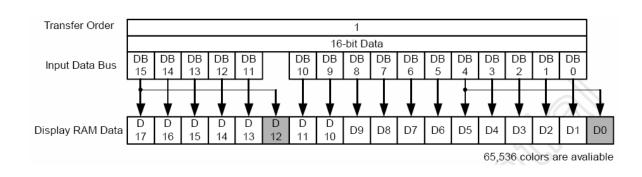


MPU7 Type



7.2 80-system MPU4 type

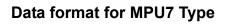
IN the MPU4 type, The 16-bit data written to display RAM is expanded to 18-bit bus data automatically in the LSI. D12 of the display data RAM is compensated by the data from DB7 in the first transfer and D0 of the display data RAM is compensated by the data from DB4 in the second transfer.

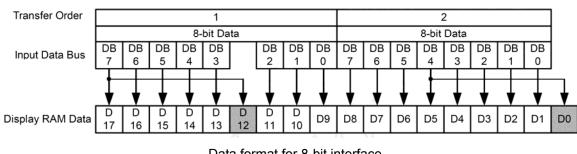


Data format for MPU4 Type

7.3 80-system MPU7 type (8-bitX2)

IN the MPU7 type, The 16-bit data written to display RAM is expanded to 18-bit bus data automatically in the LSI. D12 of the display data RAM is compensated by the data from DB7 in the first transfer and D0 of the display data RAM is compensated by the data from DB4 in the second transfer.





Data format for 8-bit interface

8 INSTRUCTION DESCRIPTIONS

The RS pin specifies whether the access is to the register command or to the display data RAM. The input data for register command is consist of 16 bits. The upper 8 bits (D15-8) are address and the lower 8 bits (D7-0) are data.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		Reg	gister /	Addres	s						Com	mand			

The following shows the relation between register command allocation and input data bus in different MPU type input data format.

The display RAM data is consist of 18 bits which include R-, G-, B-dot display level information. The (D17-12) bits are R-dot display level (D17 is MSB); (D11-6) bits are G-dot display level (D11 is MSB); (D5-0) bits are B-dot display level (D5 is MSB).

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

The following shows the relation between display RAM data allocation and input data bus in different MPU type input data format.

8.1 Register Description (Driver IC: HX8312)

Register	Bit	Symbol	Function	Configuration
				ontrol register 1
	D7	DISP1		All source output as "0" or "1" selection
	יט	DISPT	Source output data selection.	Refer to "10.2 " All "0" or "1" Source Output Display "
	D6	DISP0	Source output data selection.	All source output as "0" or "1" selection Refer to "10.2 " All "0" or "1" Source Output Display "
R0 (R00h)	D5	ADC	Specifies source output and display RAM address mapping.	Refer to 4.1 "Relation between the Display RAM Address and the Source Output Channel"
. ,	D4	DTY	Specifies partial display mode.	"0" : Normal display mode. "1" : Partial display mode. Refer to "5. Partial Display Mode".
default "A0"h	D3	STBY	Specifies stand-by mode.	"0" : Normal operation. "1" : Stand-by mode.
	D2	COLOR	Specifies color mode.	"0" : 262,144 color mode. "1" : 8 color mode. Refer to "9 8-color Display Mode".
	D1	-	-	-
	D0	GSM	Gate scan selection in partial-off display areas.	 "0": Normal scan in non-display area "1": Configures the scanning cycle in non-display area by the number of the R52 register.
			C	ontrol register 2
	D7	ADX	RAM X address increment direction after one write or read operation .	"0" : From X0 to X239 Refer to "4.2. Display RAM Access" "1" : From X239 to X0 *Note : ADX = "1" setting is prohibited when RGB interface circuit is in use.
R1 (R01h)	D6	ADR	RAM Y address increment direction after one write or read operation .	"0" : Y0 to Y319 Refer to "4.2. Display RAM Access" "1" : Y319 to Y0 *Note : ADR = "1" setting is prohibited when RGB interface circuit is in use.
	D5	-	-	-
default	D4	-	-	-
"00"h	D3	-	-	-
	D2	-	-	-
	D1	LTS	Specifies setting period of calibration.	"0" : 1line period = tcal "1" : 1 line period = tcal x 2 Refer to "3.3 Internal Clock Mode".
	D0	OSCST BY	Oscillation control.	"0" : Starts oscillation. "1" : Stops oscillation.
			RGB interf	ace register 2
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	VMODE	Vsync interface selection.	"0": Normal Refer to "Table 9-1". "1": Uses Vsync interface.
R2 (R02h)	D3	WNRGB	RGB interface writing mode selection.	"0" : Requires 1 frame data. "1" : Requires data only for the window area. Refer to "9.1.6 Restriction when using the RGB interface circuit".
	D2	RGBS	RGB interface writing mode selection.	"0" : Capture mode. Refer to "Table 9-1". "1" : Through mode.
default "00"h	D1	DISPCK	Specifies display timing at RGB interface circuit.	"0" : Internally synchronized display mode by SYSCLK. "1" : Externally synchronized display mode by Vsync and Hsync. Refer to "Table 9-1".
	D0	NWRGB	RGB interface pin control.	"0" : Writes to the display data RAM via the system interface circuit. "1" : Writes to the display data RAM via the RGB interface circuit. Refer to "Table 9-1".

				Reset register 1
	D7	-	-	Nesel legislel I
D 2	D7 D6	-	-	-
R3				-
(R03h)	D5	-	-	
	D4	-	-	-
	D3	-	-	-
default	D2	-	-	-
"00"h	D1	-	-	-
	D0	RES	Reset command for the	"0" : Normal operation.
	00	KE0	HX8312A	"1" : Reset Operation.
			RA	M access control register
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
R5				"0" : Normal writing mode.
(R05h)	D4	WAS	Specifies window area	"1" : Window area access mode.
· /	5.	111.0	access mode.	Refer to "4.3. Window Area Access Mode".
	D3	-	1	
default	20			"0" : X address increment, then Y address increment.
"00"h			Specifies the address	"1" : Y address increment, then X address increment,
	D2	AM	increment direction.	*Note: This setting is invalid when RGB interface circuit is in use.
			increment direction.	Refer to "4.2. Access to the Display Data RAM".
	D1	-	-	
	D0	-	-	·
	20		1	Data reverse register
	D7	-	-	
R6	D6	-	-	- -
(R06h)	D0	-	-	-
(RUOII)	D3	-	-	-
	D4	-	-	-
default	D3	-	-	-
"00"h			-	
00 11	D1	-		
	D0	REV	Reverse the source	"0": Data "0000"h; Source output: V63 at VCOML
			output data voltage	"1": Data "0000"h; Source output V0 at VCOML
			•	splay size control register
R13	D7	-	-	•
(R0Dh)	D6	-	-	-
(D5	-	-	-
	D4	-	-	-
default	D3	-	-	-
"00"h	D2	NSO1	Specify source output	Refer to "4.1 Relation between the Display RAM Address and the
	D1	NSO0	size.	Source Output Channel".
	D0	-	-	-
			Partial n	on-display area color register 1
	D7	-	-	-
	D6	-	-	-
R14	D5	-	-	-
(R0Eh)	D4	-	-	-
(D3	-	-	- -
	D3	-	-	-
default	D2 D1	-	-	
"00"h		-	-	"0" : Displays the color specified in the P15 register
00 H			Specifies the color of	"0" : Displays the color specified in the R15 register.
	D0	PSEL	the partial non-display	"1" : Displays the most significant bit of the display RAM data.
			area	Refer to "5.2 Display Color Selection and Gate Scan Method in
				Partial Non-Display Areas".

			Partial n	on-display area color register 2
	D7		-	
	D6	-	-	-
R15	D5	-	-	-
("0F"h)				
(0F 1)	D4	-	-	-
	D3	-	-	
default	D2	PGR	Specifies display data	"0" : Displays "0".
"00"h			for pixel R.	"1" : Displays "1".
00 11	D1	PGG	Specifies display data	"0" : Displays "0".
			for pixel G.	"1" : Displays "1".
	D0	PGB	Specifies display data	"0" : Displays "0".
			for pixel B.	"1" : Displays "1". window area starting register 1 , 2
R16	D7	-	-	-
(R10h)	D6	-	-	-
(,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	D5	-	-	-
	D4	-	-	•
default	D3	-	-	•
"00"h	D2	-	-	-
	D1	-	-	-
	D0	P1SL8		
	D7	P1SL7		
R17	D6	P1SL6		
(R11h)	D5	P1SL5	Specify the starting line	
	D4	P1SL4	number of the first	Set within the range of "000"h - "13F"h.
	D3	P1SL3	display window area.	
default	D2	P1SL2		
"00"h	D1	P1SL1		
	D0	P1SL0		
			Second displa	ay window area starting register 1 , 2
D40	D7	-	-	-
R18	D6	-	-	-
(R12h)	D5	-	-	-
	D4	-	-	-
default	D3	-	-	-
"00"h	D2	-	-	-
	D1	-	-	-
	D0	P2SL8		
	D7	P2SL7	1	
R19	D6	P2SL6	1	
(R13h)	D5	P2SL5	Specify the starting line	
,	D4	P2SL4	number of the second	Set within the range of "000"h - "13F"h.
	D3	P2SL3	display window area.	U L L L
default	D2	P2SL2		
"00"h	D1	P2SL1		
	D0	P2SL0		
			First display w	vindow area display line number 1 , 2
-	D7	-	-	-
R20	D6	-	-	-
(R14h)	D5	-	-	-
	D4	-	-	-
1.6.1	D3	-	-	-
default	D2	-	-	-
"00"h	D1	-	-	-
	DO	P1AW8		
	D7	P1AW7	1	
R21	D6	P1AW6	1	
(R15h)	D5	P1AW5	Specify the display line	
(ixion)	D3	P1AW5 P1AW4	number of the first	Set within the range of "001"h - "140"h.
	D4	P1AW4 P1AW3	display window area.	
default	D3 D2	P1AW3 P1AW2	alopiay window alea.	
"00"h				
	D1 D0	P1AW1 P1AW0	-	
		PIAWU		

R22 (R16h) Second display window area display line number 1, 2 P24 D6 - - D6 - - - D4 - - - D7 P2AW7 - - D0 P2AW8 - - R10 D5 Specify the display line display window area. Set within the range of 000"h - "13F"h. default D2 P2AW3 - - Worth D1 P2AW1 - - D4 P2AW1 - - - Gatal D2 P2AW3 - - Gatal D2 P2AW1 - - D4 P2AW1 - - - D3 - - - -				• • · · · ·	
TL2 D6 . . . Mithin D2 D4 D6 D0 P2AW8 . . . D4 P2AW0 rumber of the second . . default D2 P2AW0 . . . D0 P2AW0 Controls the VR2 '0" 'VR2 regulator off. . D6 VR10N regulator . . . D6 VR10N regulator off. . . . D6 VCLN Controls the step-up '0" 'VCL step-up crout 2 off. . D4 VGON Controls the DC/DC '1" : D0/DH step-up crout 2 off. . D6 VR2S				Second display	window area display line number 1 , 2
(R16h) D6 - - - 04 - - - - 04 - - - - 05 - - - - 07 P24W3 - - - 08 P2AW8 - - - 10 P2AW3 Specify the display line number of the second sipslay window area. Set within the range of 000"h - "13F"h. 101 P2AW3 sipslay window area. Set within the range of 000"h - "13F"h. 102 P2AW3 Specify the display line number of the second sipslay window area. TO ''YR2 regulator off. 102 P2AW3 Set within the range of 000"h - "13F"h. Set within the range of 000"h - "13F"h. 103 - - - - - 104 VR2ON Controls the VR2 "0": VR2 regulator off. - 105 VCLON Controls the step-up ''O": VCL step-up circuit 2 off. - - 105 VCLON Controls the DC/OC ''O": DC/DC conveter off. ''O": DC/DC conveter off	R22	D7	-	-	-
D5 - - default "00"h D3 - - D3 - - - D1 P2AWB Specify the display line particle within the range of 000"h - "13F"h. D3 P2AWB Number of the second display window area. Set within the range of 000"h - "13F"h. default D3 P2AWB Power Supply System Control Register 1 D0 P2AWD Power Supply System Control Register 1 D1 Particle Sthe VR2 "0" 'VR2 regulator off. D5 VCLON Controls the step-up 'U" 'VR2 regulator off. D4 VGON Controls the step-up 'U" 'VCL step-up circuit off. D2 DVDHON Circuit 3 for VCL. "1" 'CD US tep-up circuit off. D2 DVDHON Circuit 3 for VCL. "1" 'DU US tep-up circuit off. D2		D6	-	-	-
default imorth D4 D2 - - 00 P2AW8 D7 - - 01 P2AW8 D7 - - 02 P2AW8 D7 - - 03 P2AW8 D7 - - 04 P2AW8 D7 Specify the display line D7 - 04 P2AW3 D7 Specify the display window area. Set within the range of 000"h - "13F"h. default D3 P2AW3 D7 Specify the display window area. Set within the range of 000"h - "13F"h. default 03 P2AW3 D7 VR20N Controls the VR2 "0" : VR2 regulator off. regulator. "1" : VR2 regulator off. "1" : VR1 regulator off. "1" : VR1 regulator off. regulator. "1" : VR1 regulator off. "1" : VR1 regulator off. "1" : VR1 regulator off. default D6 VR10N Controls the step-up '0" : VC1 setp-up circuit off. "1" : VC1 setp-up circuit off. 02 DVDHON Controls the step-up '0" : DD/D1 step-up circuit off. "1" : DD/D2 converter off. 04 U2 DVDHON Controls the step-up '0" : DD/D1 step-up circuit off.<	(((101))	D5	-	-	-
default "00"h D3 00 P2AWB R3 D6 P2AWB . . . R4 D7 P2AWG prumber of the second display window area. . D3 P2AW3 mumber of the second display window area. . . D4 P2AW3 . . . 00"h D1 P2AW3 . . 00"h D1 P2AW3 . . 00 P2AW3 . . . 00 P2AW0 00 P2AW0 . Controls the VR2 . . 10 P2AW3 10 10 10 <th></th> <th></th> <th>-</th> <th>-</th> <th></th>			-	-	
"00"h D2 . . . 00 P2AW8 - - - 01 . - - - 00 P2AW8 - - - 01 P2AW6 specify the display line number of the second display window area. - 01 P2AW3 display window area. Set within the range of 000"h - "13F"h. default 02 P2AW3 display window area. Set within the range of 000"h - "13F"h. default 00 P2AW3 Controls the VR2 "0": VR2 regulator off. "regulator. - - - - 05 VCLON Controls the VR2 "0": VR1 regulator off. "10" VR2 regulator. "1": VR1 regulator off. 04 VGON Controls the step-up "0": VR1 regulator off. 03 - - - - 04 VGON Controls the step-up "0": DC/DC converter off. "1": DC/DC converter off. 04 VB2SEL2 Specify the output	1.6.14				
D1 . . . 00 P2AW8 . . 07 P2AW7 . . 06 P2AW6 Specify the display line number of the second display window area. . 00'th D2 P2AW2 . . 00'th D2 P2AW0 . . Packat 00'th D2 P2AW0 . . Packat 00'th D2 P2AW0 01 02 Ntool of counts the VR1 02 DVDHON Controls the VR					
D0 P2AW6 P2AW6 D5 P2AW6 P2AW6 D5 Specify the display line number of the second display window area. Set within the range of 000"h - "13F"h. default "00"h D2 P2AW3 D1 P2AW4 D2 Specify the display window area. Set within the range of 000"h - "13F"h. default "00"h D2 P2AW3 D1 P2AW3 D2 Specify the display window area. Set within the range of 000"h - "13F"h. default "00"h D3 P2AW1 D1 P2AW1 P2AW1 Power Supply System Control Register 1 D7 VR20N Controls the VR2 regulator. "0" : VR2 regulator off. "1" : VR1 regulator off. D6 VR10N Controls the step-up circuit 0 fm "1" : VR1 regulator off. "1" : VR1 regulator off. D3 Ocntrols the step-up circuit 1 for DVDL. "1" : VDL step-up circuit 2 off. "1" : VDL step-up circuit 2 off. D1 Ocntrols the DC/DC '0" : DC/DC converter off. "1" : DD/DC douted 2 on. D4 VR2SEL1 Specify the output - - D2 DVDVHON Controls the VR2 - - D4 VR2SEL1 Specify the output - -	"00"h				
R23 (R17h) D7 D5 P2AW7 P2AW3 D3 Specify the display line display window area. Set within the range of 000"h - "13F"h. default "00"h D3 P2AW3 D2 Specify the display line display window area. Set within the range of 000"h - "13F"h. default "00"h D3 P2AW3 D2 P2AW3 P2AW2 Power Supply System Control Register 1 00 P2AW0 Power Supply System Control Register 1 Power Supply System Control Register 1 00 P2AW0 Controls the VR2 "0" : VR1 regulator off. regulator. "1" : VR2 regulator off. 100 P2AW0 Controls the step-up "0" : VR1 regulator off. "1" : VR2 regulator off. 101 D4 VGON Controls the step-up "0" : VR1 step-up circuit 0ff. 103 "0" : VR1 step-up circuit 2 off. "1" : DDVDH step-up circuit 0ff. 102 DDVDHON Controls the DC/DC "0" : DC/DC converter off. 101 D4 VR2SEL1 voltage of the VR1 - 102 VR2SEL1 voltage of the VR1 - 103 VR3SEL1 voltage of the VR1 - 104				-	•
R23 (R17h) D6 P2AW6 P2AW3 D2 Specify the display line number of the second display window area. Set within the range of 000"h - "13F"h. default "00"h D2 P2AW3 D1 P2AW3 P2AW3 D1 Specify the display line number of the second display window area. Set within the range of 000"h - "13F"h. default "00"h D2 P2AW3 D1 P2AW3 P2AW3 D1 Power Supply System Control Register 1 D7 VR20N Controls the VR2 regulator. "0" 'VR 2 regulator off. "regulator on. "0" 'VR 2 regulator off. D6 VR10N Controls the VR1 "0" 'VR 1 regulator off. "1" 'VR1 regulator off. D4 VGON Controls the step-up circuit 3 for VCL. "0" 'VCL step-up circuit 0.ff. D3 Controls the step-up circuit 1 for DD/DH "1" 'Step-up circuit 2 off. "1" 'D/DC converter off. D1 Controls the DC/DC "0" 'D/DVDH step-up circuit 0.ff. "1" 'D/DC converter off. D4 VR2SEL1 Value of the VR2 value of the VR2 - D2 DD/VHON Controls the DC/DC "1" 'D/DC converter off. D2 VR2SEL2 Specify the output - D6 VR2SEL1					
(RT7h) D5 P2AW3 P2AW4 D3 Specify the display line number of the second display window area. Set within the range of 000"h - "13F"h. default "00"h D2 P2AW2 D2 P2AW3 P2AW2 Set within the range of 000"h - "13F"h. default "00"h D3 P2AW3 D2 P2AW3 P2AW2 Set within the range of 000"h - "13F"h. R24 (R18h) D P2AW3 D2 P2AW3 P2AW2 Set within the range of 000"h - "13F"h. B VCLON Controls the VR2 regulator "1" VR2 regulator off. "1" VR2 regulator off. D6 VR10N Controls the step-up circuit 3 for VCL. "1" VR1 regulator off. "1" VR2 regulator off. default "00"h D5 VCLON Controls the step-up circuit 2. "1" VR1 regulator off. D2 DDVDHON Controls the step-up circuit 2. "1" DDVDH step-up circuit off. D1 Controls the DC/DC "0" DDVDH step-up circuit off. D2 DDVDHON Controls the DC/DC "0" DDVDH step-up circuit off. D6 VR2SEL1 Voltage of the VR2 - D6 VR2SEL1 Voltage of the VR2 - D2					
D4 P2AW4 D2 number display window area. Set within the range of 000"h - "13F"h. 00"h D2 P2AW3 D1 P2AW3 D2 P2AW3 D1 P2AW3 D1 P2AW3 D1 P2AW4 D1 P2AW4 D1 D7 VR20N Controls the VR2 regulator. "0": VR2 regulator off. "1": VR1 regulator on. D6 VR10N Controls the VR1 "0": VR2 regulator on. "1": VCL step-up circuit off. D6 VCLON Controls the step-up circuit 3 or VCL "1": VCL step-up circuit on. D4 VGON Controls the step-up circuit 2. "1": VCL step-up circuit 0. D7 VR2DNON Controls the step-up circuit 1. "1": VCL step-up circuit 0. D3 "0" DVDH step-up circuit 0. "1": DVDH step-up circuit 0. D1 Controls the DC/DC converter. "1": DVDVH step-up circuit 0. D2 DDVDHON Controls the VR2 - D6 VR3SEL2 Specify the output voltage of the VR2 - D3 VR1SEL2 Specify the output voltage of the VR1 - D3 VR1SEL2 Specify the output voltage of the VR1					
default "00"h 02 P2AW2 D2 display window area. 00"h 02 P2AW2 D1 P2AW2 P2AW0 00 P2AW0 0 00 P2AW0 0 00 P2AW0 0 01 P2AW0 0 02 VR20N Controls the VR2 regulator off. regulator off. 0 05 VCLON Controls the step-up circuit 3 for VCL. "0" 'VR1 regulator off. 05 VCLON Controls the step-up circuit 2 off. "1" 'VR1 regulator off. 04 VGON Controls the step-up circuit 1 off. "1" 'VDVDH step-up circuit off. 03 - Controls the step-up circuit 1 off. "1" : DDVDH step-up circuit off. 04 VGSEL1 Specify the output voltage of the VR2 - 04 VR2SEL1 Specify the output voltage of the VR2 - 04 VR1SEL2 Specify the output voltage of the VR1 - 04 VR1SEL2 Specify the output voltage of the VR1 - 02 VR1SEL0 regulator. - 04	(R17h)	D5			
default "00"h D2 P22W20 D0 P22W0 Power Supply System Control Register 1 D0 P22W0 "0": VR2 regulator off. "regulator on. D6 VR10N Controls the VR2 regulator. "0": VR2 regulator on. D6 VR10N Controls the VR1 "0": VR1 regulator on. D6 VR10N Controls the step-up "0": VR1 regulator on. D6 VR10N Controls the step-up "0": Step-up circuit off. 13		D4	P2AW4	number of the second	Set within the range of 000"h - "13F"h.
"00"h D0 P2AWU Power Supply System Control Register 1 D7 VR2 ON Controls the VR2 "0": VR2 regulator off. 10 VR10N Controls the VR1 "0": VR1 regulator off. 11 VR2 regulator. "1": VR2 regulator off. 12 VR2 regulator. "1": VR1 regulator off. 15 VCLON Controls the step-up "0": VR1 regulator on. 10 VGON Controls the step-up "0": VR1 regulator on. 10 Controls the step-up "0": Step-up circuit 2 off. 102 DDVDHON Controls the step-up "0": DD/DH step-up circuit off. 101 Controls the DC/DC "0": DD/DC converter off. 11 DE VR2SEL0 Specify the output 10 DC VR2SEL1 volage of the VR2 - 10 VR2SEL0 regulator. - 103 VR1SEL1 volage of the VR1 - 105 VR2SEL0 regulator. - 104 VR1SEL1 volage of the VR1 -		D3	P2AW3	display window area.	
"00"h D1 P2AW1 Power Supply System Control Register 1 D7 VR20N Controls the VR2 "0": VR2 regulator off. "00"h D6 VR10N Controls the VR1 "0": VR2 regulator on. D6 VR10N Controls the VR1 "0": VR1 regulator on. D6 VCL0N Controls the step-up circuit 3 for VCL. "0": VR2 regulator on. D4 VGON Controls the step-up circuit 2. "0": VR1 regulator on. D2 DDVHON Controls the step-up circuit 2. "0": DDVDH step-up circuit 2 on. D1 Controls the Step-up circuit 1 for DDVDH. "0": DD/DH step-up circuit 0 ff. D1 Controls the DC/DC "0": DD/DC converter off. D5 VR2EL2 Specify the output "1": DC/DC converter off. D5 VR2EL2 Specify the output - VR3EL2 Specify the output - D4 VR15EL1 voltage of the VR1 - D5 VR2EL2 Specify the output - D4 VR15EL1 voltage of the VR1 -	default	D2	P2AW2		
Power Supply System Control Register 1 D7 VR2ON Controls the VR2 regulator "0": VR2 regulator on. D8 VR1ON Controls the VR1 "1": VR2 regulator on. D6 VR1ON Controls the VR1 "1": VR2 regulator on. D6 VR1ON Controls the step-up for: VCL step-up circuit off. Controls the step-up "0": VR1 regulator on. D4 VGON Controls the step-up for: VCL step-up circuit off. D3	"00"h				
Power Supply System Control Register 1 D7 VR2ON Controls the VR2 regulator '0': VR2 regulator off. D6 VR1ON Controls the VR1 regulator '0': VR1 regulator off. D6 VR1ON Controls the step-up circuit 3 for VCL '0': VR1 regulator off. D8 VCLON Controls the step-up circuit 3 for VCL '1': VR2 tep-up circuit off. D4 VGON Controls the step-up circuit 2. '1': '1': Step-up circuit 2. D1 Controls the step-up circuit 1 for DDVDH. '1': DDVDH step-up circuit 0. D1 Controls the DC/DC '0': DD/DC converter off. D1 Power Supply System Control Register 2 D6 VR2SEL2 Specify the output regulator. O/DC converter off. D4 VR1SEL1 voltage of the VR2 - D6 VR2SEL2 Specify the output regulator. - D4 VR1SEL1 voltage of the VR1 - D4 VR1SEL2 Specify the output regulator. - D6 - - - D6 - - -					
R24 (R18h) D7 VR20N Controls the VR2 regulator. '1': 'VR1 regulator on. b6 VR10N Controls the VR1 regulator. '1': 'VR1 regulator on. '1': 'VR1 regulator on. b7 VR20N Controls the VR1 regulator. '1': 'VR1 regulator on. '1': 'VR1 regulator on. b6 VR10N Controls the step-up circuit 2 step-up circuit off. '1': 'VR1 regulator on. b7 VR20N Controls the step-up circuit 2 off. '1': 'VR1 regulator on. b7 VR20N Controls the step-up circuit 2 off. '1': 'VR1 regulator off. b7 VR20N Controls the step-up circuit 1 for DDVDH. '1': 'DDVDH step-up circuit off. b1 '0' Controls the DC/DC '0': 'DC/DC converter off. b1 'Or vR2SEL2 Specify the output 'D1' b1 'Or VR2SEL1 voltage of the VR2 ' b2 VR1SEL2 Specify the output ' b2 VR1SEL1 voltage of the VR2 ' b2 VR1SEL1 voltage of the VR2 ' b2 VR1SEL0 ' ' </th <th></th> <th>00</th> <th>1 ZAWO</th> <th>Power Su</th> <th>Innly System Control Register 1</th>		00	1 ZAWO	Power Su	Innly System Control Register 1
D// VR2ON regulator "1": VR2 regulator on. P6 VR1ON Controls the VR1 "0": VR1 regulator on. P6 VR1ON Controls the step-up "0": VR1 regulator on. P6 VCLON Controls the step-up "0": VCL step-up circuit on. P7 VGON Controls the step-up "0": Step-up circuit 2 on. P6 VGON Controls the step-up "0": DOVDH step-up circuit 0. D1 - - "1": VC2 converter on. D1 - - "1": DDVDH step-up circuit on. D1 - - "0": DC/DC converter on. D1 - - - D2 DPCON Controls the DC/DC "0": DC/DC converter on. P7 VR2SEL1 votage of the VR2 - D6 VR2SEL2 Specify the output - D2 VR1SEL1 votage of the VR1 - D3 VR1SEL2 Specify the output - D4 R25 D6 - -					
R24 (R18h) D6 VR10N Controls the VR1 regulator. "0": VR1 regulator on. b5 VCLON Controls the step-up circuit 3 for VCL. "1": VCL step-up circuit off. b6 VRON Controls the step-up circuit 2 off. "1": VCL step-up circuit 2 off. b1 Controls the step-up "0": DDVDH step-up circuit 2 off. "1": DDVDH step-up circuit 0. b2 DDVDHON Controls the DC/DC "0": DD/DH step-up circuit 0. "1": DDVDH step-up circuit 0. b1		D7	VR2ON		11: VP2 regulator on
R24 (R18h) D5 VR10N regulator. "1": VR1 regulator on. b5 VCLON Controls the step-up "0": VCL step-up circuit off. default D4 VGON Controls the step-up "0": VCL step-up circuit 2 off. D2 DDVDHON Controls the step-up "0": DDVDH step-up circuit 2 on. "0": DDVDH step-up circuit 0 ff. D1 Controls the DC/DC "0": DDVDH step-up circuit off. "1": DC/DC converter off. D1 DCON Controls the DC/DC "0": DC/DC converter off. D1 Controls the DC/DC "1": DC/DC converter on. D6 VR2SEL2 Specify the output D6 VR2SEL1 voltage of the VR2 D4 VR1SEL1 voltage of the VR1 D2 VR1SEL1 voltage of the VR1 D3 VR1SEL1 voltage of the VR1 D2 VR1SEL1 voltage of the VR1 D3 VR1SEL1 voltage of the VR1 D4 VR1SEL2 Specify the step-up D5 - - D6 - -<		\vdash		Controle the VD4	I . VRZ regulator off
R24 (R18h) D5 VCLON Controls the step-up circuit 3 for VCL. '''' : VCL step-up circuit off. default D3 Controls the step-up '''' : Step up circuit 2 off. ''0''h D2 DDVDHON Controls the step-up '''' : Step up circuit 2 off. ''0''h D2 DDVDHON Controls the step-up '''' : DDVDH step-up circuit off. ''1' D1 Controls the DC/DC '''' : DDVDH step-up circuit off. D1 Controls the DC/DC '''' : DD/DC converter off. D0 DCON Controls the DC/DC '''' : DC/DC converter off. 00''h VR2SEL2 Specify the output - D5 VR2SEL1 voltage of the VR2 - D6 VR2SEL1 voltage of the VR1 - D2 VR1SEL1 voltage of the VR1 - D1 - - - D2 VR1SEL1 voltage of the VR1 - D2 VR1SEL1 voltage of the VR1 - D2 VR1SEL1 voltage of the VR1 - <tr< th=""><th></th><td>D6</td><td>VR10N</td><td></td><td>U VRT regulator on</td></tr<>		D6	VR10N		U VRT regulator on
(R18h) D5 VCLON Controls the step-up 0 :: VCL step-up circuit on. default ::::::::::::::::::::::::::::::::::::	R24				1 VR1 regulator on.
default Difference Controls the step-up The volume Volume 00"h Difference Controls the step-up "0" : DDVDH step-up circuit 2 off. 02 DDVDHON Controls the step-up "0" : DDVDH step-up circuit 2 off. 01 "1" : DDVDH step-up circuit off. 01 "1" : DDVDH step-up circuit off. 01 "1" : DC/DC converter off. 02 DDVD CON Controls the DC/DC 03 "1" : DC/DC converter off. 04 VR2SEL2 Specify the output 05 VR2SEL1 voltage of the VR2 04 VR1SEL2 Specify the output 04 VR1SEL2 Specify the output 05 VR2SEL1 voltage of the VR1 04 VR1SEL2 Specify the output 05 - - 00 - - 01 - - 02 VR1SEL1 voltage of the VR1 03 VR1SEL1 voltage of the VR1 04 - -		D5	VCLON		
default "00"h D4 VSON circuit 2. "1": Step up circuit 2 on. "00"h D3	(,				
default "00"h The step up circuit 2 on. The step up circuit 2 on. D2 DDVDHON Controls the step-up circuit 1 for DDVDH. "0": DDVDH step-up circuit off. D1			VGON		
"00"h D3 Controls the step-up circuit 1 for DDVDH. "0": DDVDH step-up circuit off. "1": DDVDH step-up circuit on. D1	default		VOON	circuit 2.	"1" : Step up circuit 2 on.
D2 DDVDHON Controls the step-up "0": DDVDH step-up circuit off. D1		D3			
D2 DD/DHON circuit 1 for DD/DH. "1": DD/DH step-up circuit on. D1 - - - D0 DCON Controls the DC/DC converter off. "0": DC/DC converter on. P0 DC Specify the output - D6 VR2SEL2 Specify the output - D6 VR2SEL1 voltage of the VR2 - D4 VR1SEL2 Specify the output - D5 VR2SEL0 regulator. - D4 VR1SEL2 Specify the output - D3 VR1SEL1 voltage of the VR1 - D4 VR1SEL0 regulator. - D0 - - - D0 - - - D6 - - - D5 - - - - D4 - - - - D2 FS3 Specify the step-up - - D2 FS0 <t< th=""><th>00 11</th><th></th><th>DDVDUON</th><th>Controls the step-up</th><th>"0" : DDVDH step-up circuit off.</th></t<>	00 11		DDVDUON	Controls the step-up	"0" : DDVDH step-up circuit off.
D1 Controls Controls Converter 00 DCON Controls the DC/DC "0": DC/DC converter off. "1": DC/DC converter on. Power Supply System Control Register 2 07 VR2SEL1 Specify the output voltage of the VR2 - D5 VR2SEL1 voltage of the VR2 - D4 VR1SEL2 Specify the output voltage of the VR1 - D4 VR1SEL1 voltage of the VR1 - D2 VR1SEL0 regulator. - D1 - - - D0 - - - D0 - - - D0 - - - D0 - - - D4 - - - D5 - - - D5 - - - D4 - - - D2 FS3 Specify the step-up circuit 1 frequency - D5 -			DDVDHON		"1" : DDVDH step-up circuit on.
D0 DCON Controls the DC/DC converter. "0" : DC/DC converter off. "1" : DC/DC converter off. "1" : DC/DC converter off. "1" : DC/DC converter off. R25 D7 VR2SEL2 Specify the output voltage of the VR2 - D4 VR1SEL2 Specify the output voltage of the VR2 - - D4 VR1SEL1 voltage of the VR1 - - D0 - - - - D1 - - - - D2 VR1SEL2 Specify the step-up - - D4 - - - - - D2 FS3 Specify the step-up - - -		D1			
D0 DCON converter. "1": DC/DC converter on. Power Supply System Control Register 2 Power Supply System Control Register 2 R25 (R19h) D6 VR2SEL2 Specify the output D4 VR2SEL1 voltage of the VR2 - D4 VR1SEL2 Specify the output - D3 VR1SEL1 voltage of the VR1 - D2 VR1SEL0 regulator. - D1 - - - D2 VR1SEL0 regulator. - D0 - - - D1 - - - D3 FS3 Specify the step-up - D3 FS3 Specify the step-up - D3 FS3 Specify the step-up - D4 - - - D4 - - - D4 Specify the step-up - - D4 - - - D4				Controls the DC/DC	"0" : DC/DC converter off.
Power Supply System Control Register 2 PT VR2SEL2 Specify the output voltage of the VR2 - D5 VR2SEL0 regulator. - D4 VR1SEL2 Specify the output voltage of the VR1 - D4 VR1SEL0 regulator. - D1 - - - D0 - - - D1 - - - D2 VR1SEL0 regulator. - D1 - - - D0 - - - D1 - - - D2 FS3 Specify the step-up - D2 FS0 circuit 2and 3 frequency - D1 FS1 Specify the step-up - D2		D0	DCON		
R25 (R19h) D7 VR2SEL2 Specify the output voltage of the VR2 - D6 VR2SEL0 regulator. - D4 VR1SEL2 Specify the output - D4 VR1SEL2 Specify the output - D3 VR1SEL0 regulator. - D1 - - - D0 - - - D0 - - - D0 - - - D0 - - - D6 - - - D6 - - - D5 - - - D5 - - - D5 - - - D1 FS1 Specify the step-up - D2 FS2 circuit 1 frequency - D1 FS1 Specify the step-up - D6 - - -					
R25 (R19h) D6 VR2SEL0 voltage of the VR2 - D5 VR2SEL0 regulator. - D4 VR1SEL2 Specify the output - D3 VR1SEL1 voltage of the VR1 - D0 VR1SEL0 regulator. - D0 - - - D1 - - - D2 FS3 Specify the step-up - D2 FS2 circuit 2 and 3 frequency - D1 FS1 Specify the step-up - D2 FS2 circuit 1 frequency - D0 FS0 circuit 2 and 3 frequency - D1 VSEL2 Specify the step-up - D2 FS2			VR2SEL2		
D5 VR2SEL0 regulator. D4 VR1SEL2 Specify the output - D3 VR1SEL1 voltage of the VR1 - D2 VR1SEL0 regulator. - D1 - - - D0 - - - D0 - - - D6 - - - D6 - - - D6 - - - D5 - - - D4 - - - D5 - - - D5 - - - D4 - - - D2 FS3 Specify the step-up - D1 FS1 Specify the step-up - D0 FS0 circuit 1 frequency - D6 - - - D5 - - - <tr< th=""><th>R25</th><th></th><th></th><th></th><th></th></tr<>	R25				
D4 VR1SEL2 Specify the output voltage of the VR1 - ''''''''''''''''''''''''''''''''''''	(R19h)				
default "00"h D3 VR1SEL1 regulator. voltage of the VR1 regulator. - D1 - - - D0 - - - - D1 D2 - - - D4 - - - - D4 - - - - D2 FS2 circuit 2and 3 frequency - - D1 FS1 Specify the step-up circuit 1 frequency - - D2 FS2 circuit 2and 3 frequency - - R27 D6 - - - <	. ,				
D2 VR1SEL0 regulator. D1 - - D0 - - D0 - - D0 - - Power Supply System Control Register 3 - D7 - - D6 - - D5 - - D4 - - D4 - - D3 FS3 Specify the step-up D4 - - D2 FS2 circuit 2and 3 frequency D1 FS1 Specify the step-up D0 FS0 circuit 1 frequency D0 FS0 circuit 1 frequency D0 FS0 circuit 2 and 3 frequency D1 FS1 Specify the step-up D0 FS0 circuit 1 frequency D1 FS1 Specify the step-up D1 FS2 - D2 Specify the step-up - D4					
''00"h D2 VR1SEL0 regulator. D1 - - - D0 - - - R26 (R1Ah) D7 - - - D5 - - - - default "05"h D3 FS3 Specify the step-up circuit 2and 3 frequency - D1 FS1 Specify the step-up circuit 1 frequency - - D0 FS3 Specify the step-up circuit 1 frequency - - D0 FS0 circuit 1 frequency - - D1 FS1 Specify the step-up circuit 1 frequency - - D0 FS0 circuit 1 frequency - - D1 FS1 Specify the step-up circuit 1 frequency - - D2 FS2 circuit 1 frequency - - D3 Specify the output - - - D4 - - - - D4 -	default				-
D1 - - - D0 - - - Power Supply System Control Register 3 - - D7 - - - D6 - - - - D4 - - - - D5 - - - - D4 - - - - D5 - - - - D2 FS2 circuit 2and 3 frequency - - D0 FS0 circuit 1 frequency - - D0 FS1 Specify the step-up - - R27 D6 - - - D4 - - -<		D2	VR1SEL0	regulator.	
Power Supply System Control Register 3 R26 (R1Ah) D7 - - - D6 - - - - D4 - - - - D4 - - - - D3 FS3 Specify the step-up D2 - - D2 FS2 circuit 2and 3 frequency D1 - - D1 FS1 Specify the step-up circuit 1 frequency - - D0 FS0 circuit 1 frequency - - D6 - - - - D6 - - - - D6 - - - - D5 - - - - D3 VSEL2 Specify the output voltage of the VS and - - D2 VSEL0 VDH regulator. - - D1 VSEL0 VDH regulator. - D0 PGON		D1	-	-	-
R26 (R1Ah) D7 - - - D6 - - - - D4 - - - - D2 FS3 Specify the step-up circuit 2and 3 frequency - D1 FS1 Specify the step-up circuit 1 frequency - D0 FS0 circuit 1 frequency - D6 - - - D5 - - - D4 - - - D3 VSEL2 Specify the output voltage of the VS and - D1 VSEL0 VDH regulator. - D0 PGON Cont		D0	-	-	-
R26 (R1Ah) D6 - - - D5 - - - - D4 - - - - D3 FS3 Specify the step-up circuit 2and 3 frequency - D1 FS1 Specify the step-up circuit 1 frequency - D0 FS0 circuit 1 frequency - D7 - - - P6 - - - R27 (R1Bh) D5 - - D4 - - - D3 VSEL2 Specify the output voltage of the VS and - D2 VSEL1 voltage of the VS and - D1 VSEL0 VDH regulator. - D0 R20N Controls				Power Su	Ipply System Control Register 3
R26 (R1Ah) D6 - - - D5 - - - - D4 - - - - D3 FS3 Specify the step-up circuit 2and 3 frequency - D1 FS1 Specify the step-up circuit 1 frequency - D0 FS0 circuit 1 frequency - D7 - - - P6 - - - R27 (R1Bh) D5 - - D4 - - - D3 VSEL2 Specify the output voltage of the VS and - D2 VSEL1 voltage of the VS and - D1 VSEL0 VDH regulator. - D0 R20N Controls	Bee	D7	-	-	-
D5 - - - D4 - - - - D4 - - - - D3 FS3 Specify the step-up D2 - - D1 FS1 Specify the step-up circuit 1 frequency - D0 FS0 circuit 1 frequency - D0 FS0 circuit 1 frequency - Power Supply System Control Register 4 - - D7 - - - R27 (R1Bh) D5 - - D4 - - - D3 VSEL2 Specify the output voltage of the VS and - D3 VSEL2 Specify the output voltage of the VS and - D1 VSEL0 VDH regulator. - D0 PGON Controls the VS and '0": VS and VDH regulator off.			-	-	-
D4 - - - D3 FS3 Specify the step-up circuit 2and 3 frequency - D1 FS1 Specify the step-up circuit 1 frequency - D0 FS0 circuit 1 frequency - D0 FS0 circuit 1 frequency - D7 - - - R27 (R1Bh) D5 - - D4 - - - D3 VSEL2 Specify the output voltage of the VS and - D1 VSEL0 VDH regulator. - D0 PGON Controls the VS and '0": VS and VDH regulator off.	(R1Ah)				
default "05"h D3 FS3 Specify the step-up circuit 2and 3 frequency - D1 FS1 Specify the step-up circuit 1 frequency - - D0 FS0 circuit 1 frequency - - D0 FS0 circuit 1 frequency - - R27 D6 - - - R18h D5 - - - D3 VSEL2 Specify the output voltage of the VS and - D3 VSEL2 Specify the output voltage of the VS and - D2 VSEL1 voltage of the VS and - D1 VSEL0 VDH regulator. -					
Uterating D2 FS2 circuit 2and 3 frequency - ''05''h D1 FS1 Specify the step-up circuit 1 frequency - D0 FS0 circuit 1 frequency - - D7 - - - - R27 D6 - - - R1Bh) D5 - - - D3 VSEL2 Specify the output voltage of the VS and - D3 VSEL2 Specify the output voltage of the VS and - ''0A''h D1 VSEL0 VDH regulator. - D0 RCON Controls the VS and ''0'' : VS and VDH regulator off.					-
D1 FS1 Specify the step-up circuit 1 frequency - D0 FS0 circuit 1 frequency - Power Supply System Control Register 4 - - D7 - - - D6 - - - D5 - - - D3 VSEL2 Specify the output voltage of the VS and - D3 VSEL2 Specify the output voltage of the VS and - D1 VSEL0 VDH regulator. - D0 PGON Controls the VS and "0" : VS and VDH regulator off.	default				-
D0 FS0 circuit 1 frequency - Power Supply System Control Register 4 D7 - - D6 - - - D4 - - - D3 VSEL2 Specify the output voltage of the VS and - 02 VSEL1 voltage of the VS and - 01 VSEL0 VDH regulator. "0" : VS and VDH regulator off.	"05"h				
Power Supply System Control Register 4 D7 - - D6 - - D5 - - D4 - - D3 VSEL2 Specify the output voltage of the VS and - D1 VSEL0 VDH regulator. - D0 PGON Controls the VS and "0" : VS and VDH regulator off.					-
R27 (R1Bh) D7 - - - D6 - - - - D5 - - - - D4 - - - - D3 VSEL2 Specify the output voltage of the VS and - D1 VSEL0 VDH regulator. - D0 PGON Controls the VS and "0" : VS and VDH regulator off.		D0	FS0		
R27 (R1Bh) D6 - - - D5 - - - - D4 - - - - D3 VSEL2 Specify the output voltage of the VS and - D1 VSEL0 VDH regulator. - D0 PGON Controls the VS and "0" : VS and VDH regulator off.				Power Su	pply System Control Register 4
D5 - - - D4 - - - D3 VSEL2 Specify the output voltage of the VS and - "0A"h D1 VSEL0 VDH regulator. D0 PGON Controls the VS and "0" : VS and VDH regulator off.			-	-	-
D5 - - - D4 - - - D3 VSEL2 Specify the output voltage of the VS and - "0A"h D1 VSEL0 VDH regulator. D0 PGON Controls the VS and "0" : VS and VDH regulator off.	R27	D6	-	-	-
D4 - - D3 VSEL2 Specify the output voltage of the VS and - "0A"h D1 VSEL0 VDH regulator. D0 PGON Controls the VS and "0" : VS and VDH regulator off.			-	-	-
D3 VSEL2 Specify the output voltage of the VS and - "0A"h D1 VSEL0 VDH regulator. - D0 PGON Controls the VS and "0" : VS and VDH regulator off.			-	-	
default D2 VSEL1 voltage of the VS and - "0A"h D1 VSEL0 VDH regulator. - D0 PGON Controls the VS and "0" : VS and VDH regulator off.		D3			
"0A"h D1 VSEL0 VDH regulator. D0 PGON Controls the VS and "0" : VS and VDH regulator off.	default				
DO BGON Controls the VS and "0" : VS and VDH regulator off.					-
	UA II	U1	VSELU		
VDH regulator. "1" : VS and VDH regulator on.		D0	RGON		
		- •		VDH regulator.	1 "1" : VS and VDH regulator on.

			Dower Su	pply System Control Register 5
	D7	-	- Power su	-
	D6 D5	SAP2 SAP1		(SAP2, SAP1, SAP0) = "000": Halt (SAP2, SAP1, SAP0) = "001": 0.5(fixed) (SAP2, SAP4, SAP0) = "001": 0.75(fixed)
R28 (R1Ch)	D4	SAP0	Source driver circuit operating current control	(SAP2, SAP1, SAP0) = "010": 0.75(fixed) (SAP2, SAP1, SAP0) = "011": 1.0(fixed) (SAP2, SAP1, SAP0) = "100": 1.25(fixed) (SAP2, SAP1, SAP0) = "101": 1.5(fixed) (SAP2, SAP1, SAP0) = "110": 1.5(fixed) (SAP2, SAP1, SAP0) = "111": Setting disable
default	D3			
"33"h	D2	AP2		(AP2, AP1, AP0) = "000": Halt
	D1	AP1		(AP2, AP1, AP0) = "001": Setting disable
	D0	APO	Step-up circuit operating current control	(AP2, AP1, AP0) = "010": 0.5(fixed) (AP2, AP1, AP0) = "011": 0.75(fixed) (AP2, AP1, AP0) = "100": 1.0(fixed) (AP2, AP1, AP0) = "101": 1.25(fixed) (AP2, AP1, AP0) = "110": 1.5(fixed) (AP2, AP1, AP0) = "111": Setting disable
			Power Su	pply System Control Register 6
	D7	-	-	-
R29	D6	-	-	•
(R1Dh)	D5 D4	-	-	-
	04	-		-
default "03"h	D3	R/L	Specifies the gate scan direction.	-
~03~n	D2 D1	SCN2 SCN1	Specify gate scan	(SCN2, SCN1, SCN0) = "XX0" : MODE5
	DO	SCN0	mode.	(SCN2, SCN1, SCN0) = "011" : MODE2
	00	00140	Power Su	pply System Control Register 8
	D7	VCOMEN		and all and a subject of
	D6		Specify the VCOM1	
	D5	VCOMFX	operation.	-
R30	D4	VCOMHI		
(R1Eh)	D3	XVCOMG	VCOML output control	*0*: VCOML = GND *1*: VCOML is setting with VDV and VCM
default	D2	-	-	•
default "00"h	D1	-	-	-
	DO	DDVDHXON	Specifies whether to use or not to use the extra step-up circuit 1 for DDVDH.	"0" : Doesn't use the extra step-up circuit 1. "1" : Uses the extra step-up circuit 1.
	D -7		Power Su	pply System Control Register 9
R31	D7 D6	-	4	
(R1Fh)	D5	-	1	
	D4	VDV4	Specify the VCOM	
default	D3	VDV3	amplitude.	
"00"h	D2	VDV2		
	D1	VDV1	-	
	D0	VDV0	D 0	units Supreme Countral Dominton 40
	D7	-	Power Sup	pply System Control Register 10
R32	D6	-	1	
(R20h)	D5	-	1	
	D4	VCM4	Specify the VCOMH	
default	D3	VCM3	voltage level	
"00"h	D2	VCM2		
	D1	VCM1		
	D0	VCM0		

				ID code register 1			
		MCOD2		ID code register 1			
R49	D7	MCOD3					
(R31h)	D6	MCOD2	Manufacturer code.	-			
(,	D5	MCOD1					
	D4	MCOD0					
default	D3	VCOD3					
"10"h	D2	VCOD2		Demonds on the version of the number			
10 11	D1	VCOD1	The version of this LSI.	Depends on the version of the product.			
	DO	VCOD0	1				
		-	-	ID code register 2			
	D7	DCOD7	_				
R50	\vdash						
(R32h)	D6	DCOD6	-				
(,	D5	DCOD5					
	D4	DCOD4	Device code of this				
default	D3	DCOD3	LSI.				
"03"h	D2	DCOD2					
00 11	D1	DCOD1					
	D0	DCOD0	1				
	D7			N line inversion register			
R51	D6	NLINE6					
(R33h)	D5	NLINE5	1				
(13311)		NLINE4	Specify the number of				
	D4		Specify the number of	Set within the range of "01"h - "78"h.			
defect	D3	NLINE3	lines for N line	Refer to "7 Gate Line Driving Function".			
default	D2	NLINE2	inversion.				
"01"h	D1	NLINE1	1				
	D0	NLINE0					
				Partial gate register 1			
	D7	GSMLN7					
R52	D6	GSMLN6	1				
(R34h)	D5	GSMLN5	1				
	D4	GSMLN4	Specify the gate	"00"h : Doesn't scan the partial non-display area.			
	D3	GSMLN4 GSMLN3	scanning cycle of the	"01"h : Scans the partial non-display area every frame.			
default			non-display area	"02"h : Scans the partial non-display area every two frames.			
"01"h	D2	GSMLN2					
	D1	GSMLN1					
	D0	GSMLN0					
	L		1	Partial gate register 2			
	D7	-	-	-			
DE2	D6	-	-	-			
R53	D5	-	-	-			
(R35h)	D4	-	-	-			
	D3	-	-	-			
	D2	-	-	-			
default	D1	-	-				
"00"h		-		"0" : The partial non-display area is driven as that in the partial			
		PNFRM	Configures the driving				
	D0	FINERIV	method of the partial	display area.			
			non-display area.	"1" : The partial non-display area is driven by the frame inversion.			
				e scan selection register			
R55	D7	-	-	-			
(R37h)	D6	-	-				
(10/11)	D5	-	-	-			
	D4	-	-	-			
dofoult	D3	-	-				
default	D2	GSCAN2					
"00"h	D1	GSCAN1	Select the method of				
	D0	GSCANO	gate scanning.				
		GOUANU	C	e output control register			
			1	· · · · · · · · · · · · · · · · · · ·			
	D7	-	-	-			
R59	D6	-	-	-			
(R3Bh)	D5	-	-	-			
	D4	-	-	-			
	D3	-	-	-			
	001						
default		-	-	-			
default "00"h	D2		-	-			
	D2 D1	-	-	-			
	D2						

[Gamma control register 12							
R154	D6	-									
	D5	-									
	D4	ON14	Gamma adjustment								
	D3	ON13	register								
default [D2	ON12	0								
"00"h 📊	D1	ON11									
	DO	ON10									
			Exter	nd mode register							
	D7	-	-	-							
	D6	-	-	-							
	D5	MON_EN	Specify the V0 and	"0": V0 and V63 output monitor is disable.							
Ľ	03	MON_EN	V63 monitor function	"1": V0 and V63 output monitor is enable.							
	D4	MON SEL	V0 and V63 monitor	"0": V0 outputs at DS1 pin.							
R157	_		selection	"1": V63 outputs at DS1 pin							
(R9Dh)	D3	-	-	-							
· · /	D2	BPEN	Specify the Enable	"0": Enable control is available.							
Ľ		Di Ell	operation	"1": VBP/HBP control is enable							
	D1	EPL	Specify the Enable	"0": High active							
"00"h 🗕			polarity	"1": Low active							
		MSBF	NWRGB (R2:D0)="1"	"0" : 18-bit x 1transfer (BWS2="L"). RGB interface type "0" : 16-bit x 1transfer (BWS2="H"). RGB interface type							
			NWRGB (R2.D0)= 1	"1" : 6-bit x 3 transfer (BWS2= h). RGB interface type							
[D0		MSBF NWRGB (R2:D0)="0"	"0" : MPU5 mode A (use lower 6bits). MPU interface type							
				"1" : MPU5 mode B (use upper 6bits). MPU interface type							
			(12:20)	This bit is invalid in other modes.							
			Off	mode register							
				"0": Normal mode							
				"1": Off mode							
,	D7	OFFMOD	Specify the Off mode	In off mode, only OFFMOD bit can be updated. Other register and							
'	<i>U</i> ′	OFFINIOD	Specify the Off mode	the display RAM can not be updated. The display RAM data may							
R192				not be retained in off mode, and need to rewrite after off mode							
("C0"h)				canceling.							
	D6	-	-	-							
	D5	-	-	-							
default "00"h	D4	-	-	-							
	D3	-	-	-							
1	D2	-	-	-							
Γ	D1	-	-	-							
	D0	-	-	-							

9 Timing Characteristics

80-system Bus interface Timing Characteristics

Read / Write Characteristics (8080-series MPU)

Bus Timing Characteristics

Please refer to HX8312A specification

<<Normal Write Mode(HWM=0),IoVcc=1.65V-2.4V>>

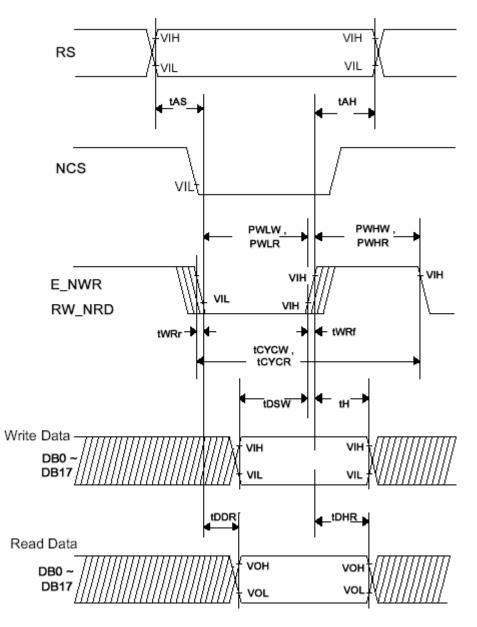
	İtem	Symbol	Unit	Min	Тур	Max
Bus cycle time	Write	t _{CYCW}	ns	125	-	-
Bus cycle unie	Read	t _{CYCR}	ns	300	-	-
Write low-level	PW _{LW}	ns	40	-	-	
Read low-level	PW_{LR}	ns	150	-	-	
Write high-level	PW _{HW}	ns	70	-	-	
Read high-level	pulse width	PW _{HR}	ns	150	-	-
Write/Read rise	Write/Read rise/fall time			-	-	25
	Set up time (RS to NCS,E_NWR)		ns	5	-	-
RS hold time	(NCS,NWR to RS)	t _{AH}	ns	5	-	-
Write data set u	t _{DSW}	ns	20	-	-	
Write data hold	t _H	ns	15	-	-	
Read data dela	t _{DDR}	ns	-	-	100	
Read data hold	time	t _{DHR}	ns	5	-	-

<<Normal Write Mode(HWM=0),IoVcc=2.4V-3.3V>>

	Item	Symbol	Unit	Min	Тур	Max
Bus cycle time	Write	t _{CYCW}	ns	200	-	-
Bus cycle time	Read	t _{CYCR}	ns	300	-	-
Write low-level	pulse width	PW_{LW}	ns	40	-	-
Read low-level	PW_{LR}	ns	150	-	-	
Write high-leve	PW _{HW}	ns	70	-	-	
Read high-leve	PW _{HR}	ns	150	-	-	
Write/Read rise	e/fall time	t _{WRr} ,t _{WRf}	ns	-	-	25
Set up time	Set up time (RS to NCS, E NWR)		ns	5	-	-
RS hold time	(NCS,NWR to RS)	t _{AH}	ns	5	-	-
Write data set u	up time	t _{DSW}	ns	20	-	-
Write data hold	t _H	ns	15	-	-	
Read data dela	t _{DDR}	ns	-	-	100	
Read data hold	time	t _{DHR}	ns	5	-	-

Reset Timing Characteristics

Item	Symbol	Unit	Min	Тур	Max
Reset"low"level width	t _{RES}	ms	1	-	-
Reset rise time	t _{rRES}	us	-	-	10



80-System Bus Timing

Note 1) PWEL is specified during the overlap period. (SC*="Low", WR* or RD*="Low") Note 2) When using 16-bit bus interface, parallel data can be transferred through DB17-10 pin and DB8-1 and DB0 must be fixed to "Vcc" or "GND".

10 QUALITY AND RELIABILITY

10.1 TEST CONDITIONS

Tests should be conducted under the following conditions : Ambient temperature : $25 \pm 5^{\circ}C$ Humidity : $60 \pm 25\%$ RH.

10.2 SAMPLING PLAN

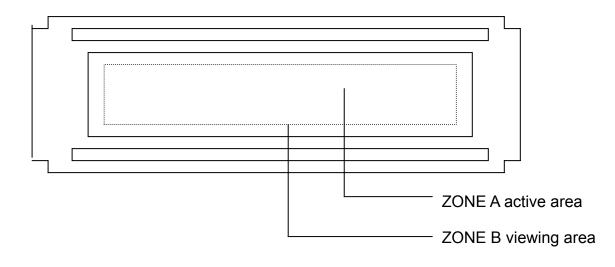
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

10.3 ACCEPTABLE QUALITY LEVEL

A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

10.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under fluorescent light. The inspection area of LCD panel shall be within the range of following limits.



10.5 INSPECTION QUALITY CRITERIA

No.	ltem	Criterion f	Defect type		
1	Non display	No non display is allowed	Major		
2	Irregular operation	No irregular operation is allo	Major		
3	Short	No short are allowed			Major
4	Open	Any segments or common are rejectable.	patte	rns that don't activate	Major
5	Black/White spot	Size D (mm) $D \leq 0.15$ $0.15 < D \leq 0.20$ $0.20 < D \leq 0.30$ $0.30 < D$	Aco	ceptable number Ignore 3 2 0	Minor
6	Black/White line	$\begin{tabular}{ c c c c c } \hline Length(mm) & Width (mm) \\ \hline 10 < L & 0.03 < W \le 0.04 \\ \hline 5.0 < L \le 10 & 0.04 < W \le 0.06 \\ \hline 1.0 < L \le 5.0 & 0.06 < W \le 0.07 \\ L < 1.0 & 0.07 < W < 0.09 \\ \hline \end{tabular}$		Acceptable number 5 3 2 1	Minor
7	Back Light	1. No Lighting is rejectable 2. Flickering and abnormal	lighting	g are rejectable	Major
		Bright dot Dark dot		$N\!\leq\!1$	Minor
8	dot defect			N≦3	
		Total dot defect (Bright dot + Dark dot)		N≦3	Winter
		Minimum distance between of dot and dark dot	dark	L \geq 5 mm	
9	Display pattern	$\frac{A+B}{2} \le 0.30 0 < C$ Note: 1. Acceptable up to 3 data 2. NG if there're to two o	Minor		

	-					
	Blemish & Foreign matters	Size D (mm) Acceptable number				
10	Foreign matters	$D \le 0.15$ Ignore		-		
	Size:	0.15 < D < 0.20			3	Minor
	A + B	0.20 < D < 0.30				
	$D = \frac{A+B}{2}$	0.30 < D 0				
	Scratch on	Width (mm)	· · · · · · · · · · · · · · · · · · ·		Acceptable number	
	Polarizer	W <u><</u> 0.03	Igno		Ignore	
11		0.03 <w<u><0.05</w<u>	L <u><</u> 2 L > 2		Ignore	Minor
	A	0.05 <w<u><0.08</w<u>	L>1		1	WIITIO
		0.00	L <u><</u> 1		Ignore	
		0.08 <w< td=""><td>Note</td><td></td><td>Note(1)</td><td></td></w<>	Note		Note(1)	
		Note(1) Regard				
				•		
	Dubble in	Size D (I	,	AC	ceptable number	
12	Bubble in				Ignore 3	Minor
	polarizer	0.20 < D <u><</u> 0.50 0.50 < D <u><</u> 0.80			2	
		0.80 < D	5		0	
	Stains on	Stains that as				
13	LCD panel	Stains that ca with a soft clot	Minor			
	surface	with a solt cior				
4.4	Duct in Decel	Duct which is	Minor			
14	Rust in Bezel	Rust which is	Minor			
	Defect of					
4 5	land surface					
15	contact (poor	Evident crevic	Minor			
	soldering)					
		1 Eciluro to m	Major			
16	Parts	 Failure to m Parts not in 	the specifi	cations a	are mounted	Major
10	mounting	3. Polarity, for	Major			
			Minor			
	Parts	1. LSI, IC lea outline.	WIITO			
17	alignment	2. Chip compo	Minor			
	angrinient	the leads i	WIIIO			
		1.0.45 < <i>φ</i>	.N≥1			Major
	Conductive	2. 0.30< φ <u><</u> 0.4	, —			Minor
18	foreign matter	natter				
	(Solder ball,	<i>⊈ .,</i> werug 3. 0.50 <l< td=""><td>,N≧1</td><td>0.001001</td><td></td><td>Minor</td></l<>	,N≧1	0.001001		Minor
	Solder chips)	L: Average				
		ulty PCB places are corrected per PCB			Minor	
19	Faulty PCB					
	correction	2. Short circuited part is cut, and no resist coating has				Minor
		been perfo	ormed.			

10.6 RELIABILITY

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=96 hrs	
Low Temperature Operation	-20±3°C , t=96 hrs	
High Temperature Storage	80±3°C , t=96 hrs	1,2
Low Temperature Storage	-30±3°C , t=96 hrs	1,2
Humidity Test	40°C , Humidity 90%, 96 hrs	1,2
Thermal Shock Test	-30°C ~ 25°C ~ 80°C 30 min. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Vibration Test (Packing)	Sweep frequency : 10~55~10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2
Static Electricity	150pF 330 ohm <u>+</u> 8kV, 10times air discharge	

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions

(15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

11 USE PRECAUTIONS

11.1 Handling precautions

- 1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
- 2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
- 3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
- 4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

11.2 Installing precautions

- 1) To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. $1M\Omega$ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
- 2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
- 3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
- 4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

11.3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between

0°C and 35°C and also the humidity under 60%.

- 2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
- 3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

11.4 Operating precautions

- 1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
- 2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
- The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
- 4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
- 5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
- 6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
- 7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.
- 8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk

occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

11.50ther

- 1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
- 2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.

12 OUTLINE DIMENSION

