SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	AM-240320JTNQW-00H-A
APPROVED BY	
DATE	

□.Approved For Specifications

☑ Approved For Specifications & Sample

APPROVED BY	CHECKED BY	ORGANIZED BY

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2006/6/30	-	New Release	Tony
2006/7/5	37	Modify Mechanic Drawing	Tony
2006/12/4	5~8	Modify Electric data	Tony
2007/3/21	6	Modify LED back light specification	Tony
2007/4/18	7,8,9	Modify LED back light specification	Tony
	25~27	and optical characteristics,	
		Timing Characteristics	
2007/7/6	30,31	Modify Inspection quality criteria	Tony
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	36	Modify the chapter 11.5	

1 Features

This single-display module is suitable for cellphone application. The Main-LCD adopts one backlight with High brightness 3-lamps white LED.

(1) Main LCD : 1.1 Amorphous-TFT 2.2 inch display, transmissive, Normally white type, 12 o'clock.

- 1.2 240(RGB) X 320 dots Matrix, 1/320 Duty.
- 1.3 Narrow-contact ledge technique.
- 1.4 Main LCD Driver IC: HX8312A
- 1.5 Real 262K colors display: 65K: Red-5bit, Green-6bit, Blue-5bit (8/16-bit interface)
 - 262K: Red-6bit, Green-6bit, Blue-6bit (9/18-bit interface)
- (2) Low cross talk by frame rate modulation
- (3) Direct data display with display RAM
- (4) Partial display function: You can save power by limiting the display space.
- (5) MPU interface: 8bit/16bit/18bit, 80Serial, parallel interface.
- (6) RGB interface:16bit/18bit parallel interface
- (7) Abundant command functions:
 - Area scroll function
 - Display direction switching function
 - Power saving function

Electric volume control function: you are able to program the temperature compensation function.

2 Mechanical specifications

Item	Specifications	Unit
shape dimensions	*66.4 (W) x 40.1 (H) x 3.65 (D) Max.	mm
Pixel pitch	0.1395 (W) x 0.1395(H)	mm
Active area	33.48 (W) x 44.64 (H)	mm
Viewing area	35.24 (W) x 46.92 (H)	mm
Weight	15	g
	Item shape dimensions Pixel pitch Active area Viewing area Weight	Item Specifications shape dimensions *66.4 (W) x 40.1 (H) x 3.65 (D) Max. Pixel pitch 0.1395 (W) x 0.1395(H) Active area 33.48 (W) x 44.64 (H) Viewing area 35.24 (W) x 46.92 (H) Weight 15

Dimensions and weight

*1. This specification is about External shape on shipment from AMPIRE.

3 Absolute max. ratings and environment

3-1 Absolute max. ratings

Ta=25°C GND=0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power voltage	VDD – GND	-0.3	+4.0	V	
Power voltage	LED A – LED K	-0.5	+12.8	V	
Input voltage	VIN	-0.5	VDD+0.5	V	

3-2 Environment

Item	Specifications	Remarks
Storage temperature	Max. +70 °C Min20 °C	Note 1: Non-condensing
Operating temperature	Max. +60 °C Min10 °C	Note 1: Non-condensing

Note 1 : Ta \leq +40 °C · · · Max.85%RH

Ta>+40 o C • • • • The max. humidity should not exceed the humidity with 40 o C 85%RH.

4 Electrical specifications

4-1 Electrical characteristics of LCM

				()	/ _{DD} =3.0V	, Ta=25 °	C)
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
IC power voltage	V _{DD}		2.4	3.0	3.3	V	
High-level input voltage	V _{IHC}		$0.8V_{DD}$		V_{DD}	V	Note 1,2,3
Low-level input voltage	V _{ILC}		0		$0.2V_{DD}$	V	
Consumption current of VDD	I _{DD}	LED OFF	-	4		mA	
Consumption current of LED	I _{LED}	V _{LED} =9.6V	-	15	20	mA	

※ 1. 1/320 duty.

2. Electronic Volumn value: (xxxxh) Decimal

3. Thermal Gradient: -0.05%/°C

4. Range of Electronic Volumn control : (xxxxH<u>+</u>3) Decimal

*Reference only.

(Note1) The Vci is the DC/DC converter power input. The limitation of the HX8312 are

DDVDH<5.6V , VGH-VGL < 32V.

(Note2) When VCI > 3.16V,

R27 Register: VR1SEL2-0 can not be set to 000 or 001 or 010. Otherwise the DDVDH > 5.6V.

R25 Register : BT3-0 can not be set to 0000,0001,0010,0011,0100,0101,0110,0111. Otherwise the VGH-VGL > 32V.

(Note 3) When VCI=3.4V .Recommend setting : VR1SEL2-0=100 , BT3-0=1000.



4-2 LED back light specification

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	V _f	I _f =15mA	9.3	9.8	-	V
Reverse voltage	Vr		-	-	12	V
Forward current	l _f	3-chip serial	12	15	20	mA
Power Consumption	P _{BL}	I _f =15mA	-	147	-	mW
Uniformity (with L/G)	-	l _f =15mA	80%*1	-	-	
Luminous color	White					
Chip connection	3 chip serial connection					

Bare LED measure position:



*1 Uniformity (LT):
$$\frac{Min(P1 \sim P9)}{Max(P1 \sim P9)} \times 100 \ge 80\%$$

5 Optical characteristics

Main LCD

5.1 Optical characteristics

(1/320 Duty in case except as specified elsewhere $Ta = 25^{\circ}C$)

Item	Symbol	Temp.	Min.	Std.	Max.	Unit	Conditions
Response	Tr	25 °C	NA	10	25		$\theta = 0^{\circ}$, $\varphi = 0^{\circ}$
time	Tf	25 °C	NA	20	40	1115	(Note 2)
Contrast ratio	CR	25 °C	150	200	-	-	$\theta = 0^{\circ}, \phi = 0^{\circ}$ LED:ON, LIGHT:OFF (Note 4)
Transmittance	Т	25 °C	-	5.5	-	%	
Visual angle range front and rear	θ	25 °C		(<i>θ</i> f) 35 (<i>θ</i> b) 15		De- gree	φ = 0°, CR \ge 10 LED:ON LIGHT:OFF (Note 3)
Visual angle range left and right	θ	25 °C		(<i>θ</i> I) 45 (<i>θ</i> r) 45		De- gree	φ =90°, CR \ge 10 LED:ON LIGHT:OFF (Note 3)
Visual angle direction priority				12:00			(Note 5)
Brightness			160*			Cd/ m2	V _{LED} =9.6V, 15mA Full White pattern

LED backlight transmissive module:

*This value is reference only, follow the limited samples.

$5.2 \text{ CHE}(\mathbf{x}, \mathbf{y}) \text{ chromaticity}(1/320 \text{ Duty ra} = 25 \text{ C})$							
			Tranm				
Item	Symbol		RGBV	V Range		Conditions	
		X1Y1	X2Y1	X1Y2	X2Y2		
Red	XR	0.55	0.55	0.65	0.65	$\theta = 0^{\circ} \cdot \varphi = 0^{\circ}$	
1.00	YR	0.31	0.41	0.31	0.41	о с ,,,	
Green	XG	0.30	0.30	0.40	0.40	$\theta = 0^{\circ} \cdot \phi = 0^{\circ}$	
0.001	YG	0.49	0.59	0.49	0.59		
Blue	Хв	0.09	0.09	0.19	0.19	$\theta = 0^{\circ}, \varphi = 0^{\circ}$	
	Yв	0.06	0.16	0.06	0.16		
White	Xw	0.26	0.26	0.36	0.36	$\theta = 0^{\circ}, \varphi = 0^{\circ}$	
	Yw	0.27	0.38	0.28	0.38	,,,-	

5.2 CIE	(x. v)	chromaticity	(1/320)	Duty Ta	= 25°C)
0.2 012	(Λ, \mathbf{y})	ornonnationty	(1/020	Duty iu	200)

***** The R G B W ranges are for reference, follow the limited samples.

LED Dice Bin Code

Color Coordinate @ I _f =20mA								
Rin Codo		1	2		3		4	
Bill Oode	Х	Y	Х	Y	X	Y	X	Y
Е	0.290	0.290	0.290	0.300	0.300	0.310	0.300	0.300
F	0.290	0.280	0.290	0.290	0.300	0.300	0.300	0.290
G	0.290	0.270	0.290	0.280	0.300	0.290	0.300	0.280

LED Part NO and IV Bin Code: Unity Opto LED Dice MSL- 518ZW U1B,U2A,U2B



NOTE 1: Optical characteristic measurement system

NOTE 2: Response tome definition









NOTE 5: Visual angle direction priority



6 Block Diagram

Block diagram (Main LCD)

Display format:A-Si TFT transmissive, Normally white type, 12 o'clock.Display composition:240 RGB x 320 dotsLCD Driver :HX8312ABack light:White LED x 3 (I_{LED}=15mA)



7 Interface specifications

Pin No.	Terminal	Functions
1	GND	Ground
2	GND	Ground
3	/CS	Chip Select Signal L : Select
1	/RS	Command/Display Data selection
4		0: Command , 1: Display Data
5	/WR	Serves As a Write Signal And Writes Data at The rising edge.
		M68 System:0:Write 1:Read.
6	(DD	I80 System: Serves as a Read Signal and Reads Data at the Low Level.
	/KD	M68 System:0:Write/Read Disable 1:Read.Write
7	RESET	Reset Signal L : Reset
8	D0	
9	D1	
10	D2	
11	D3	
12	D4	
13	D5	
14	D6	
15	D7	
16	D8	19 bit for Data Dua
17	D9	18-bit for Data Bus
18	D10	
19	D11	
20	D12	
21	D13	
22	D14	
23	D15	
24	D16	
25	D17	
26	DSV	The Parallel and Serial Bus Interface selection in system interface
20	FOX	circuit 0: Parallel Bus Interface, 1: Serial Bus Bus Interface.
27	BWS1	VCC Select Bit Length For CPU.
28	BWS0	VCC Select Bit Length For CPU.
29	DTX2	Ground 16BIT Parallel Data Transfer Method.
30	DTX1	Ground Select Data Length.
31	BWS2	Select Bit Length For RGB(VCC:16BIT GND:18BIT,6BIT)
32	SDI	Serial Data input Pin
33	VCL	Input for Serial Clock
34	VSYNC	Frame Synchronizing Signal
35	HSYNC	Line Synchronizing
36	DOTCLK	Dot Clock Signal

37	NC	No Connect
38	RGB/CPU	Gound switching For Data Bus 0:System Interface can be accessed. 1:System Interface can Not be accessed.
39	VCC	Power Supply
40	VCI	DC/DC Converter Power

• The Default FPC setting

BWS1	VCC
BWS0	VCC
DTX2	VCC
DTX1	VCC
BWS2	VCC

• Recommend Interface Type Setting :

Interface			Pin				Bit	Transferring	Transferring
Туре	PSX	BWS1	BWS0	DTX2	DTX1	Bus Width	number in a pixel	Method	Method of Command
MPU1	0	0	0	х	Х	18-bit parallel	18-bits	18-bit collective	
MPU2	0	1	0	0	1		19 bite	9-bit twice	16-bit
MPU3	0	1	0	1	1	16-bit parallel	10-0115	16-bit + 2-bit	collective
MPU4	0	1	0	0	0		16-bits	16-bit collective	
MPU5	0	1	1	0	1		19 hite	6-bit 3 times	
MPU6	0	1	1	1	1	8-bit parallel	TO-DILS	8-bit+8-bit+2-bit	8-bit twice
MPU7	0	1	1	1	0		16-bits	8-bit twice	
MPU8	1	0	1	х	х	18-bit serial	18-bits	18-bit serial	18-bit serial
MPU9	1	1	1	х	х	16-bit serial	16-bits	16-bit serial	16-bit serial

Connect the pin26 PSX to VCC . MPU9 interface type is selected.

The serial bus interface mode is enabled through the chip select input (NCS), and accessed via a three-wire control pin consisting of the serial input data (SDI), serial output data (SDO), and the serial transfer clock (SCL). The selection of read / write operation is made by R/W_nWR pin, and the RS pin specifies whether the access is to the register command or to the display data RAM.

7.1 Data format for 8-bit interface Data format for 16-bit SDI interface



Data format for SDI interface

7.2 **RGB interface** 16-bit RGB interface



7.3 Instruction Explanation

	Input Parts							
Signals	I/O	Pin Number	Connected with	Description				
BWS2	- 1	1	MPU	The bus width selection in RGB interface circuit. 0: 18-bit, 1: 16-bit				
BWS1-0		2	MPU	The bus width selection in system interface circuit. (see Table 2.1)				
PSX	I	1	MPU	The parallel and serial bus interface selection in system interface circuit. 0: Parallel bus interface, 1: Serial bus interface				
NCS	Т	1	MPU	Chip select signal. 0: chip can be accessed; 1: chip cannot be accessed.				
NRESET	I	1	MPU	Reset pin. Setting either pin low initializes the LSI. Must be reset the chop after power being supplied.				
NRD (E)	I	1	MPU	 I80 system: Serves as a read signal and reads data at the low level. M68 system: 0: Read/Write disable; 1: Read/Write enable Fix it to IOVCC or VSSD level when using serial buss interface. 				
NWR (RnW)	ı	1	MPU	Serves as a write signal and writes data at the rising edge. M68 system: 0: Write ; 1: Read Fix it to IOVCC or VSSD level when using serial bus interface.				
C86	I	1	MPU	MPU selection 0: i80 series MPU ; 1: M68 series MPU. Fix it to IOVCC or VSSD level when using serial bus interface.				
SI	I	1	MPU	Serial bus interface data input pin. Fix it to IOVCC or VSSD level when using parallel bus interface.				
SCL	I	1	MPU	Serial bus interface clock input pin Fix it to IOVCC or VSSD level when using parallel bus interface.				
RGB_nCPU	I	1	MPU	0: System interface can be accessed. 1: System interface can not be accessed.				
RS	I	1	MPU	Command/display Data Selection 0: Command, 1: Display data Connect to IOVCC or VSSD level when serial bus interface is selected.				
DTX2-1	I	2	MPU	Speciy the transferring method of one pixel data in system interface. (see Table 2.3)				
SCLEG1-0	I	1	MPU	Determine the effective edge operation of SCLK for SDI data latch and SDO data output. (see Table 2.6)				
VSYNC	I	1	MPU	Vertical synchronization signal input pin. Must be connected to IOVCC if not in use.				
HSYNC	I	1	MPU	Horizontal synchronization signal input pin. Must be connected to IOVCC if not in use.				
DOTCLK	I	1	MPU	Dot clock signal input used in the RGB interface circuit. Must be connected to IOVCC if not in use.				
ENABLE	I	1	MPU	Enable signal pin used in RGB interface circuit. 0: disable, 1: enable when EPL (D1 bit of R157) = 0. 0: enable, 1: disable when EPL (D1 bit of R157) = 1. Must be connected to IOVCC if not in use.				
VSEG	I	1	MPU	Valid VSYNC polarity selection pin 0: Start in the low level, 1: Start in the high level				
HSEG	I	1	MPU	Valid HSYNC polarity selection pin 0: Start in the low level, 1: Start in the high level.				
DCKEG	I	1	MPU	Valid DOTCLK polarity selection pin 0: falling edge latch, 1: rising edge latch				
DDS	I	1	MPU	Selection the position of dummy line (321th line). 0: the end of the frame, 1: the beginning of the frame				

	Output Part							
Signals	I/O	Pin Number	Connected with	Description				
SO	0	1	MPU	Serial bus interface data output pin. Keep it open while using parallel bus interface				
CSTB	0	1	MPU	Frame synchronization signal output pin. Keep it open if not in use.				
S1~S720	0	720	LCD	Source driver output pin. Output voltages to the liquid crystal.				
G1~G321	0	321	LCD	Output signals to panel gate lines. VGH: the level to select the gate lines VGL: the level not to select the gate lines				
VCOM1~4	0	4	LCD	VCOM output pin. They are short-circuited inside HX8312A.				

	Input/Output Part							
Signals	I/O	Pin Number	Connected with	Description				
DB17-0	I/O	18	MPU	Operates liked an 18-bit bi-directional data bus. Fix it to IOVCC or VSSD level when using serial bus interface. Don't set MPU output as Hi-Z when MPU has no output.				
OSC2-1	I/O	2	Oscillation Resistor	Connect an external resistor for generating internal clock by internal R-C oscillation. Or an external clock signal is supplied through OSC1 with OSC2 open.				
C11A , C11B CX11A , CX11B	I/O	4	Step up Capacitor	Connect to the step-up capacitors for step up circuit 1 operation. Leave this pin open if the internal step-up circuit is not used.				
C21A , C21B C22A , C22B C23A , C23B	I/O	6	Step up Capacitor	Connect to the step-up capacitors for step up circuit 2 operation. Leave this pin open if the internal step-up circuit is not used.				
C12A , C12B	I/O	2	Step up Capacitor	Connect to the step-up capacitors for step up circuit 3 operation. Leave this pin open if the internal step-up circuit is not used.				

Power Part							
Signals	I/O	Pin Number	Connected with	Description			
VCC		1	Power supply	A power supply for the internal logic circuit. VCC = 2.2 ~ 3.3V			
VCI	Ι	1	Power supply	A Power supply for step-up circuit and power supply circuit. VCI = $2.5 \sim 3.3V$			
IOVCC	-	1	Power supply	Power supply for I/O circuit. IOVCC = 1.65 ~ 3.3V			
V18	0	1	Bypass capacitor and VDDD, RVCC	 1.8V regulator output. V18, VDDD and RVCC must have the same voltage level. Connect to VDDD and RVCC on the FPC. 			
RVCC		1	V18 and VDDD	Power supply for RAM circuit.			
VDDD		1	V18 and RVCC	Power supply for logic circuit.			
VSSD		1	Power supply	Ground for digital circuit.			
VSSA		1	Power supply	Ground for analog circuit.			
VGH	0	1	Bypass Capacitor	A positive power supply for the gate line drive circuit.			
VGL	0	1	Bypass Capacitor Schottky Diode	A negative power supply for the gate line drive circuit. Insert a schottky diode in a forward direction to VSSA.			
ADDVDH	I	1	DDVDH	Power supply pins for VS and COMH regulators. Connected to DDVDH on FPC			
DDVDH	0	1	ADDVDH and Bypass Capacitor	Output supply pin. Connected to ADVDDH on FPC.			
VDH	0	1	Bypass Capacitor	Power supply for the source drive unit.			
VCL	0	1	Bypass Capacitor	The voltage of Vci x (-1) output			
VR2-1	0	2	Bypass Capacitor	Reference voltage output for the step-up circuit 2.			
VS	0	1	Bypass Capacitor	Power supply for the source drive unit.			
VGLDMY	0	1		A negative power supply for the gate line drive circuit.			

7.4 Register Description

Register	Bit	Symbol	Function	Configuration
			C	ontrol register 1
	D7	DISP1	Source output data selection.	All source output as "0" or "1" selection Refer to "10.2 " All "0" or "1" Source Output Display "
	D6	DISP0	Source output data selection.	All source output as "0" or "1" selection Refer to "10.2 " All "0" or "1" Source Output Display "
R0 (R00h)	D5	ADC	Specifies source output and display RAM address mapping.	Refer to 4.1 "Relation between the Display RAM Address and the Source Output Channel"
	D4	DTY	Specifies partial display mode.	"0" : Normal display mode. "1" : Partial display mode. Refer to "5. Partial Display Mode".
default "A0"h	D3	STBY	Specifies stand-by mode.	"0" : Normal operation. "1" : Stand-by mode.
	D2	COLOR	Specifies color mode.	"0" : 262,144 color mode. "1" : 8 color mode. Refer to "9 8-color Display Mode".
	D1	-	-	-
	D0	GSM	Gate scan selection in partial-off display areas.	 "0": Normal scan in non-display area "1": Configures the scanning cycle in non-display area by the number of the R52 register.
			C	ontrol register 2
	D7	ADX	RAM X address increment direction after one write or read operation .	"0" : From X0 to X239 Refer to "4.2. Display RAM Access" "1" : From X239 to X0 *Note : ADX = "1" setting is prohibited when RGB interface circuit is in use.
R1 (R01h)	D6	ADR	RAM Y address increment direction after one write or read operation .	"0" : Y0 to Y319 Refer to "4.2. Display RAM Access" "1" : Y319 to Y0 *Note : ADR = "1" setting is prohibited when RGB interface circuit is in use.
	D5	-	-	-
default	D4	-	-	-
"00"h	D3	-	-	-
	02	-	-	- "0" : 1ling period = tool
	D1	LTS	Specifies setting period of calibration.	"1" : 1 line period = tcal x 2 Refer to "3.3 Internal Clock Mode".
	D0	OSCST BY	Oscillation control.	"0" : Starts oscillation. "1" : Stops oscillation.
			RGB interf	ace register 2
	D7	-	-	-
	D6	-	-	-
	D5	-	-	- Befor to "Table 0.1"
	D4	VMODE	Vsync interface selection.	"1": Uses Vsync interface.
R2 (R02h)	D3	WNRGB	RGB interface writing mode selection.	"1" : Requires 1 frame data. "1" : Requires data only for the window area. Refer to "9.1.6 Restriction when using the RGB interface circuit".
	D2	RGBS	RGB interface writing mode selection.	"0" : Capture mode. Refer to "Table 9-1". "1" : Through mode.
default "00"h	D1	DISPCK	Specifies display timing at RGB interface circuit.	"0" : Internally synchronized display mode by SYSCLK. "1" : Externally synchronized display mode by Vsync and Hsync. Refer to "Table 9-1"
	DO	NWRGB	RGB interface pin control.	"0" : Writes to the display data RAM via the system interface circuit. "1" : Writes to the display data RAM via the RGB interface circuit. Refer to "Table 9-1".

	Reset register 1					
	D7	-	-	-		
R3	D6	-	-	-		
(R03h)	D5	-	-	-		
	D4	-	-	-		
	D3	-	-	-		
default	D2	-	-	-		
"00"h	D1	-	-	-		
		DEO	Reset command for the	"0" : Normal operation.		
	DU	RES	HX8312A	"1" : Reset Operation.		
			RA	M access control register		
	D7	-	-	-		
	D6	-	-	-		
	D5	-	-	-		
R5			Coopifico window orac	"0" : Normal writing mode.		
(R05h)	D4	WAS	Specifies window area	"1" : Window area access mode.		
			access mode.	Refer to "4.3. Window Area Access Mode".		
	D3	-				
default				"0" : X address increment, then Y address increment.		
"00"h	D2	AМ	Specifies the address	"1" : Y address increment, then X address increment,		
	02		increment direction.	*Note: This setting is invalid when RGB interface circuit is in use.		
				Refer to "4.2. Access to the Display Data RAM".		
	D1	-	-	-		
	D0	-	-	- Data vavana variatar		
	D7		1	Data reverse register		
D 0	D/	-	-	-		
R6 (Doch)	Db	-	-	-		
(R06N)	D5	-	-	-		
	D4	-	-	-		
default	D3 D2	-	-	-		
"00"h	D2	-	-	-		
		-	- Poverse the source	- "0": Data "0000"h: Source output: V63 at VCOMI		
	D0	REV	output data voltage	"1": Data "0000"h: Source output V0 at VCOML		
			Dis	splay size control register		
	D7	-	-	-		
R13	D6	-	-	-		
(R0Dh)	D5	-	-	-		
	D4	-	-	-		
al a 6 a 14	D3	-	-	-		
default	D2	NSO1	Specify source output	Refer to "4.1 Relation between the Display RAM Address and the		
-00-n	D1	NSO0	size.	Source Output Channel".		
	D0	-	-	-		
			Partial n	on-display area color register 1		
	D7	-	-	-		
	D6	-	-	-		
R14	D5	-	-	-		
(R0Eh)	D4	-	-	-		
	D3	-	-	-		
	D2	-	-	-		
default	D1	-	-	-		
"00"h			Specifies the color of	"0" : Displays the color specified in the R15 register.		
	DO	PSEI	the partial non-display	"1" : Displays the most significant bit of the display RAM data.		
	00	FJEL	area	Refer to "5.2 Display Color Selection and Gate Scan Method in		
			aiea	Partial Non-Display Areas".		

	Partial non-display area color register 2							
		-	-					
	D6	-	-					
R15	D5	-	-					
("0F"h)	D4	-	-	-				
(,	D3	-	-					
			Specifies display data	"0" · Displays "0"				
default	D2	PGR	for pixel R	"1" : Displays "1"				
"00"h	\vdash		Specifies display data	"0" : Displays "0"				
	D1	PGG	for pixel G	"1" : Displays "1"				
			Specifies display data	"0" : Displays "0"				
	D0	PGB	for pixel B.	"1" : Displays "1".				
	<u> </u>		First display	window area starting register 1, 2				
	D7	-	-	-				
R16	D6	-	-					
(R10h)	D5	-	-	-				
	D4	-	-	-				
4-6	D3	-	-	-				
default	D2	-	-	-				
-00-n	D1	-	-	-				
	D0	P1SL8						
	D7	P1SL7	1					
R17	D6	P1SL6	1					
(R11h)	D5	P1SL5	Specify the starting line					
(,	D4	P1SL4	number of the first	Set within the range of "000"h - "13F"h.				
	D3	P1SL3	display window area.					
default	D2	P1SL2						
"00"h	D1	P1SL1	1					
	D0	P1SL0						
	'		Second displa	ay window area starting register 1 , 2				
540	D7	-	-					
R18 (D40h)	D6	-	-	-				
(R12h)	D5	-	-	-				
	D4	-	-					
default	D3	-	-	-				
"00"h	D2	-	-	-				
	D1	-	-	-				
	D0	P2SL8						
	D7	P2SL7						
R19	D6	P2SL6						
(R13h)	D5	P2SL5	Specify the starting line					
	D4	P2SL4	number of the second	Set within the range of "000"h - "13F"h.				
	D3	P2SL3	display window area.					
default	D2	P2SL2						
n	D1	P2SL1						
	D0	P2SL0		laden en diaden llas muchand. A				
			First display w	/indow area display line number 1 , 2				
R20	D7	-	-	-				
(R14h)	D6	-	-	•				
(,	D5	-	-	•				
	D4	-	-	•				
default	D3	-	-	•				
"00"h	D2	-	-	•				
		-	-	-				
		P1AW8						
DOL		PIAW/						
R21	<u>D6</u>	P1AW6						
(R15h)		PIAW5	Specify the display line	Columbia the reason of "004"h				
		PIAW4	number of the first	Set within the range of "UUT"n - "140"h.				
dofoult	03	PIAW3	uispiay window area.					
"no"h		P1AW2						
~00~n		P1AW1						
	D0	P1AW0	1					

	Second display window area display line number 1 2						
			Second display	window area display line number 1, 2			
R22	D7	-	-	•			
(R16h)	D6	-	-	•			
. ,	D5	-	-	•			
	D4	-	-	•			
default	default D3		-	-			
"00"h	D2	-	-	-			
	D1	-	-	-			
	D0	P2AW8					
	D7	P2AW7					
P 23	D6	P2AW6					
(P17b)	D5	P2AW5	Specify the display line				
	D3	P2AWJ	specify the display line	Set within the range of 000"h "13E"h			
	D4 D2	P2AW4	display window area				
dofault	03	PZAVV3	display window area.				
"OO"h		PZAVVZ					
	D1	P2AW1					
	D0	P2AW0					
	<u> </u>		Power Su	pply System Control Register 1			
	70	VR2ON	Controls the VR2	"0" : VR2 regulator off.			
	Ľ,	11201	regulator.	"1" : VR2 regulator on.			
	D6	VR10N	Controls the VR1	"0" : VR1 regulator off.			
P 24	00	VICTOR	regulator.	"1" : VR1 regulator on.			
(P18b)	D5		Controls the step-up	"0" : VCL step-up circuit off.			
	05	VOLON	circuit 3 for VCL	"1" : VCL step-up circuit on.			
	БА	VCON	Controls the step-up	"0" : Step-up circuit 2 off.			
dofoult	04	VGON	circuit 2.	"1" : Step up circuit 2 on.			
"00"h	D3						
	D 2		Controls the step-up	"0" : DDVDH step-up circuit off.			
		DUVDHON	circuit 1 for DDVDH.	"1" : DDVDH step-up circuit on.			
	D1						
		DCON	Controls the DC/DC	"0" : DC/DC converter off.			
			converter.	"1" : DC/DC converter on.			
			Power Su	pply System Control Register 2			
	D7	VR2SEL2	Specify the output				
R25	D6	VR2SEL1	voltage of the VR2	-			
(R19h)	D5	VR2SEL0	regulator.				
	D4	VR1SEL2	Specify the output				
	D3	VR1SEL1	voltage of the VR1	-			
default	D2	VR1SEL0	regulator				
"00"h	D1	-	-				
		-	-	- -			
		_	Power Su	upply System Control Register 3			
	D7	-	-				
R26	De	-	-				
(R1Ah)	D5	-					
		-	-				
	D4	-	-	-			
default	03	F 53	orouit 2 and 2 from any	-			
"05"h	DZ	FS2	circuit 2and 3 frequency				
	D1	FS1	Specify the step-up	-			
	D0	FS0	circuit 1 frequency				
	L		Power Su	ipply System Control Register 4			
	D7	-	-	-			
R27	D6	-	-	-			
(R1Bh)	D5	-	-	-			
	D4	-	-	-			
	D3	VSEL2	Specify the output				
default	D2	VSEL1	voltage of the VS and	-			
"0A"h	D1	VSEL0	VDH regulator.				
	D	DOON	Controls the VS and	"0" : VS and VDH regulator off.			
		RGON	VDH regulator.	"1" : VS and VDH regulator on.			

Power Supply System Control Register 5					
	D7	-	-	•	
	D6	SAP2		(SAP2, SAP1, SAP0) = "000": Halt	
	D5	SAP1		(SAP2, SAP1, SAP0) = "001": 0.5(fixed)	
			Source driver circuit	(SAP2, SAP1, SAP0) = "010": 0.75(fixed)	
	_		operating current	(SAP2, SAP1, SAP0) = "011": 1.0(fixed)	
R28	D4	SAP0	control	(SAP2, SAP1, SAP0) = "100": 1.25(fixed)	
(R1Ch)	- I			(SAP2, SAP1, SAP0) = "101": 1.5(tixed)	
(it i on)				(SAP2, SAP1, SAP0) = 1101 1.5(lixed)	
	D3			(SAP2, SAP1, SAP0) = "111": Setting disable	
default	D2	AP2		- /ΔΡ2 ΔΡ1 ΔΡ0) = "000" Halt	
"33"h	h D1 AP1			(AP2, AP1, AP0) = "001": Setting disable	
	<u>⊢-</u>	- Au -	O (1)	(AP2, AP1, AP0) = "010"; 0.5(fixed)	
			Step-up circuit	(AP2, AP1, AP0) = "011": 0.75(fixed)	
	- DO	450	operating current	(AP2, AP1, AP0) = "100": 1.0(fixed)	
	00	APU	control	(AP2, AP1, AP0) = "101": 1.25(fixed)	
				(AP2, AP1, AP0) = "110": 1.5(fixed)	
				(AP2, AP1, AP0) = "111": Setting disable	
			Power Su	pply System Control Register 6	
	D7	-	-	•	
R29	D6	-	-	-	
(R1Dh)	(R1Dh) D5		-	-	
	D4	-	•	•	
default	D3	R/L	Specifies the gate		
#03#b	D2	POND.	scan direction.		
03 11	D2	SUNZ SCN4	Specify gate scan	(SCN2, SCN1, SCN0) = "XX0" : MODE5	
	00	SCNI	mode.	(SCN2, SCN1, SCN0) = "011" : MODE2	
	00	30140	Bower Su	ente Sustan Control Donistor 9	
	DZ	VCOMEN	Power ou	pply System control Register o	
	D6	VOOMEN	Specify the VCOM1		
	D5	VCOMFX	operation.		
R30	D4	VCOMHI			
(R1Eh)		No. COMO	traces - to tent and a	"0": VCOML = GND	
	03	XVCOMG	VCOME output control	"1": VCOML is setting with VDV and VCM	
	D2	-	-	•	
default	D1	-	-	•	
"00"h			Specifies whether to		
			use or not to	"0" : Doesn't use the extra step-up circuit 1.	
	D0	DDVDHXON	use the extra step-up	"1" : Uses the extra step-up circuit 1,	
			circuit 1 for		
			DDVDH. Bower Su	nul: Proton Canteal Desister 0	
	D7		Power su	oply System control Register 9	
R31	De		4		
(R1Fh)	D6	-	4		
	D4	VDV4	Specify the VCOM		
	D3	VDV3	amplitude.		
default	D2	VDV2	dirip.ita az.		
~00~n	D1	VDV1	4		
	DO	VDV0	1		
			Power Sur	pply System Control Register 10	
B 00	D7	-			
(D20h)	D6	-	7		
(R20h)	D5	-]		
	D4	VCM4	Specify the VCOMH		
default	D3	VCM3	voltage level	-	
"00"h	D2	VCM2]		
	D1	VCM1			
	D0	VCM0	7		

	ID code register 1						
	D7	MCOD3					
R49	D6	MCOD2					
(R31h)	D5	MCOD1	Manufacturer code.	-			
		MCOD0					
1.6	D3	VCOD3					
default	D2	VCOD2					
~10~n	D1	VCOD1	The version of this LSI.	Depends on the version of the product.			
		VCODO	-				
	00	VCOD0		ID code register 2			
			_	ib code register z			
R50							
(R32h)							
. ,	D5		Davias and of this				
	D4	DC0D4		-			
default	03	DCOD3					
"03"h		DCOD2					
		DCOD1					
	DU	DCODU					
				N line inversion register			
R51	D6	NLINE6					
(R33h)	D5	NLINE5					
	D4	NLINE4	Specify the number of	Set within the range of "01"h - "78"h.			
	D3	NLINE3	lines for N line	Refer to "7 Gate Line Driving Function".			
default	D2	NLINE2	inversion.				
"01"n	D1	NLINE1					
	D0	NLINE0					
	L		1	Partial gate register 1			
P52	D7	GSMLN7					
(R34b)	D6	GSMLN6					
(1(3411)	D5	GSMLN5	Specify the gate	"00"h : Doesn't scan the partial non-display area			
	D4	GSMLN4	scanning cycle of the	"01"h : Scans the partial non-display area every frame			
default	D3	GSMLN3	non-display area	"02"h : Scans the partial non-display area every two frames			
"01"h	D2	GSMLN2					
	D1	GSMLN1]				
	D0	GSMLN0					
				Partial gate register 2			
	D7	-	-	-			
R53	D6	-	-	-			
(R35h)	D5	-	-	-			
(110011)	D4	-	-	-			
	D3	-	-	•			
default	D2	-	-	-			
"00"h	D1	-	-	-			
			Configures the driving	"0" : The partial non-display area is driven as that in the partial			
	D0	PNFRM	method of the partial	display area.			
			non-display area.	"1": The partial non-display area is driven by the frame inversion.			
			Gat	e scan selection register			
R55	D/	-	-	-			
(R37h)	D6	-	-	-			
(,	D5	-	-	-			
	D4	-	-	-			
default	D3	-	-				
"00"h	D2	GSCAN2	Select the method of				
	D1	GSCAN1	gate scanning.	•			
	D0	GSCAN0	3				
			Gat	e output control register			
	D7	-	-	-			
R59	D6	-	-	-			
(R3Bh)	D5	-	-	-			
	D4	-	-	-			
4.0. 1	D3	-	-	-			
default	D2	-	-	-			
"00"h	D1	-	-	-			
	0	DISPTMG	Controls the gate	"0" : Fix all gate outputs to VGL level.			
-	1	2.3		"1" · Gate scanning normal operation			

			Gamma	control register 12
	D7	-		
R154	D6	-		
(R9Ah) D5 -				
	D4	ON14	Gamma adjustment	
D3 ON13 register			register	
default	D2	ON12		
"00"h	D1	ON11		
	D0	ON10	- .	
	D7		Exter	id mode register
		-	-	-
	00	-	- Specify the VO and	- "0": \/0 and \/62 autnut manitar is disable
	D5	MON_EN	V63 monitor function	"1": V0 and V63 output monitor is enable.
			V0 and V63 monitor	"0": V0 outputs at DS1 nin
	D4	MON_SEL	selection	"1": V63 outputs at DS1 pin
R157	D3	-	-	-
(R9Dh)	-	DDEN	Specify the Enable	"0": Enable control is available.
	D2	BPEN	operation	"1": VBP/HBP control is enable
default	D1	FPI	Specify the Enable	"0": High active
"00"h			polarity	"1": Low active
00 11		MSBF		"0" : 18-bit x 1transfer (BWS2="L"). RGB interface type
			NWRGB (R2:D0)="1"	"0" : 16-bit x 1transfer (BWS2="H"). RGB interface type
	D0			"0" : MPLI5 mode A (use lower 6bits) MPLL interface type
			NW/RGB (R2.D0)="0"	"1" : MPU5 mode B (use upper 6bits). MPU interface type
			1111100 (112.00) = 0	This bit is invalid in other modes.
			Off	mode register
				"0": Normal mode
				"1": Off mode
	ק	OFEMOD	Specify the Off mode	In off mode, only OFFMOD bit can be updated. Other register and
		OFTMOD	opecity the off mode	the display RAM can not be updated. The display RAM data may
R192				not be retained in off mode, and need to rewrite after off mode
("C0"h)	De			canceling.
	00	-	-	-
default	05	-	-	-
"00"h	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	-	-	-

8 Timing Characteristics

8.1Timing Characteristics



ltem		Symbol	Unit	Min.	Тур.	Max.	Test Condition
Sorial clock cycle time	Write (received)	t _{scyc}	ns	100	-	-	Figure 17.3
Serial Clock cycle tille	Read (transmitted)	t _{scyc}	ns	200	-	-	Figure 17.3
Serial clock high – level pulse	Write (received)	t _{SCH}	ns	40	-	-	Figure 17.3
width	Read (transmitted)	t _{SCH}	ns	150	-	-	Figure 17.3
Sevial cleak law, lawel wulse width	Write (received)	t _{SCL}	ns	40	-	-	Figure 17.3
Senal clock low – level pulse width	Read (transmitted)	t _{SCL}	ns	150	-	-	Figure 17.3
Serial clock rise / fal	l time	t _{scr} , t _{scf}	ns	-	I	20	Figure 17.3
Chip select (NCS) set	up time	tcs∪	ns	20	-	- (Figure 17.3
Chip select (NCS) ho	ld time	t _{сн}	ns	60			Figure 17.3
RS set up time		t _{RSU}	ns	10		(O)	Figure 17.3
RS hold time		t _{RSH}	ns	10			Figure 17.3
Read/write select (RNW) s	set up time	t _{WRU}	ns	10	$\langle \rangle$	2.	Figure 17.3
Read/write select (RNW)	hold time	t _{WRH}	ns	10			Figure 17.3
Read clock set up	time	t _{SCSR}	ns	10			Figure 17.3
Read clock hold time			ns	10			Figure 17.3
Serial input data set up time			ns	- 30	-	÷	Figure 17.3
Serial input data hold time			ns	30	V.	1	Figure 17.3
Serial output data delay time			ns	-		100	Figure 17.3
Serial output data ho	ld time	tsoн	ns	5			Figure 17.3

Serial Data Transfer Interface Timing Characteristics

Table 17. 6 (IOVCC=1.65~3.3V) / (VCC = 2.4V~3.3V)



			11			
ltem	Symbol	Unit	Min.	Тур.	Max.	Test Condition
VSYNC / HSYNC set up time	tsyncs	ns	10	-	<u> </u>	Figure 17.4
ENABLE set up time	tens	ns	10	6	1	Figure 17.4
ENABLE hold time	tenh	ns	10	6	1	Figure 17.4
DOTCLK "low" level pulse width	PWdl	ns	40		4	Figure 17.4
DOTCLK "high" level pulse width	PWDH	ns	40	Y	-	Figure 17.4
DOTCLK cycle time	toyop	ns	150	2	-	Figure 17.4
DATA set up time	tpds (ns	20	-	-	Figure 17.4
DATA hold time	tррн	ns	20	-	-	Figure 17.4
DOTCLK , VSYNC , HSYNC rising and falling time	trgbr , trgbf	ns	-	-	25	Figure 17.4

Table 17. 8 RGB interface mode, Normal Write Mode (IOVCC=2.4~3.3V) / (VCC = 2.4V~3.3V)



Reset Timing Characteristics

Item	Symbol	Unit	Min	Тур	Max
Reset"low"level width	tRES	ms	(1)	-	-
Reset rise time	trRES	us	-	-	(10)

9 SETUP FLOW OF POWER SUPPLY



Display ON Sequence

10 QUALITY AND RELIABILITY

10.1 TEST CONDITIONS

Tests should be conducted under the following conditions : Ambient temperature : $25 \pm 5^{\circ}C$ Humidity : $60 \pm 25\%$ RH.

10.2 SAMPLING PLAN

Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

10.3 ACCEPTABLE QUALITY LEVEL

A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

10.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under flourescent light. The inspection area of LCD panel shall be within the range of following limits.



10.5 INSPECTION QUALITY CRITERIA

No.	ltem	Criterion	Class of Defect	Accept able level	
1	Non display	No non display is allowed	Major	0.4	
2	Irregular operation	No irregular operation is al	lowed	Major	0.4
3	Short	No short are allowed		Major	0.4
4	Open	Any segments or commo are rejectable.	n patterns that don't activate	Major	0.4
5	Black/White spot (I)	Size D (mm)Acceptable number $D \le 0.1$ Ignore $0.1 < D \le 0.15$ 2 $\%1$ $0.15 < D$ 0		Minor	1.5
6	Dot Defect	Bright dot0Dark dotN \leq 2Total dot defect (Bright dot + Dark dot)N \leq 2Minimum distance between dark dot and dark dot0.1 < D \leq 0.3mm,N \leq 2Note: The phenomenon should follow the limit sample.		Minor	1.5
7	Back Light	 No Lighting is rejectable Flickering and abnormal lighting are rejectable Note: The phenomenon should follow the limit sample. 			0.4
8	Blemish & Foreign matters Size: $D = \frac{A+B}{2}$	Size D (mm)Acceptable number $D \le 0.15$ Ignore $0.15 < D \le 0.20$ 3 $0.20 < D \le 0.30$ 2 $0.30 < D$ 0		Minor	1.5

9	Scratch on Polarizer	Width (mm) W≤0.03 Note1: The dist Note2: With 30 no scratch sho	Width (mm)Length (mm)Acceptable number $W \le 0.03$ $L \le 2.0$ 2Note1: The distance of two defects must be more than 20mm.Note2: With 30cm from the LCD surface as testing distance, no scratch should be visible in 10secs as LCM was turned on.			
10	Bubble in polarizer	D <u><</u> 0.5 ,N <u><</u> 1 Note: Only one allowed. The phenomen	Minor	1.5		
11	Stains on LCD panel surface	Stains that cannot be removed even when wiped lightly with a soft cloth or similar cleaning too are rejectable.				1.5
12	Rust in Bezel	Rust which is visible in the bezel is rejectable.				1.5
13	Defect of land surface contact (poor soldering)	Evident crevices which is visible are rejectable.				1.5

Note: Please follow the above acceptable criteria before the limit samples collect completely.

RELIABILITY

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=96 hrs	
Low Temperature Operation	-20±3°C , t=96 hrs	
High Temperature Storage	80±3°C , t=96 hrs	1,2
Low Temperature Storage	-30±3°C , t=96 hrs	1,2
Humidity Test	40°C , Humidity 90%, 96 hrs	1,2
Thermal Shock Test	-30°C ~ 25°C ~ 80°C 30 min. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Vibration Test (Packing)	Sweep frequency : 10~55~10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2
Static Electricity	150pF 330 ohm ±8kV, 10times air discharge 150pF 330 ohm ±4kV, 10times contact discharge	

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions

(15-35°C, 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

Box Drop Test:

The module test on packing:

Falling body Height and Weight:

Totally Weight	Falling body Height
0 ~ 9 Kg	92 cm
9 ~ 25 Kg	76 cm
25 ~ 45 Kg	53 cm
45 ~ 68 Kg	46 cm
Over68 Kg	41 cm

The dropping test in turns :

- 1. Conner A
- 2. Edges of the planes : 1-4 , 1-6 , 4-6
- 3. Planes: 1, 2, 3, 4, 5, 6



11 USE PRECAUTIONS

11.1 Handling precautions

- 1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
- 2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
- 3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
- 4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

11.2 Installing precautions

- 1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. $1M\Omega$ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
- 2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
- 3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
- 4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

11.3 Storage precautions

- Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
- 2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
- 3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

11.4 Operating precautions

- 1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
- 2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
- The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
- 4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
- 5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
- 6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
- 7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that

they are shielded from light emissions.

8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

11.50ther

- 1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
- 2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.
- 3) AMIPRE will provide one year warranty for all products and three months warrantee for all repairing products.

12 Mechanic Drawing

