

A Brighter Solution

AMP DISPLAY INC.

SPECIFICATIONS

2.8 COLOR TFT MODULE W/TOUCH

CUSTOMER:	
CUSTOMER PART NO.	
AMP DISPLAY PART NO.	AM240320M8TNQW-T00H
APPROVED BY:	
DATE:	

☐

APPROVED FOR SPECIFICATIONS

☐

APPROVED FOR SPECIFICATION AND PROTOTYPES

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Revision Date	Page	Contents	Editor
2007/05/22	-	New Release	JACK

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1 Features

This single-display module is suitable for cell phone application. The Main-LCD adopts one backlight with High brightness 4-lamps white LED.

- (1) Construction: 2.8" a-Si color TFT-LCD, White LED Backlight, and FPCB.
 - (2) Main LCD :
 - 2.1 Amorphous-TFT 2.8 inch display, transmissive, Normally white type, 12 o'clock.
 - 2.2 240(RGB)X320 dots Matrix, 1/320 Duty.
 - 2.3 Narrow-contact ledge technique.
 - 2.4 Main LCD Driver IC: ILI9320
 - 2.5 Real 262K colors display:
 - 262K: Red-6bit, Green-6bit, Blue-6bit (9/18-bit interface)
 - Dithering 262K: Red-5bit, Green-6bit, Blue-5bit (8/16-bit interface)
 - (3) Low cross talk by frame rate modulation
 - (4) Direct data display with display RAM
 - (5) Partial display function: You can save power by limiting the display space.
 - (6) MPU interface: 8/16-bit 80-Series, parallel interface.
 - (7) Abundant command functions:
 - Area scroll function
 - Display direction switching function
 - Power saving function
- Electric volume control function: you are able to program the temperature compensation function.

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2 Mechanical specifications

Dimensions and weight

Item		Specifications	Unit
External shape dimensions		*1 50.0 (W) x 98.5 (H) .	mm
Main LCD	Pixel size	0.18 (W) x 0.18 (H)	mm
	Active area	43.2 (W) x 57.6 (H)	mm
	Number of Pixels	240(H)x320(V) pixels	mm
Weight		TBD	g

*1. This specification is about External shape on shipment from AMPIRE.

3 Absolute max. ratings and environment

3-1 Absolute max. ratings

Ta=25°C GND=0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power voltage	VDD – GND	-0.3	+3.3	V	
Power voltage	LED A – LED K	-0.5	+4.0	V	Parallel
Input voltage	VIN	-0.5	VDD	V	

3-2 Environment

Item	Specifications	Remarks
Storage temperature	Max. +70 °C Min. -20 °C	Note 1: Non-condensing
Operating temperature	Max. +60 °C Min. -10 °C	Note 1: Non-condensing

Note 1 : Ta ≤ +40 °C Max.85%RH

Ta > +40 °C The max. humidity should not exceed the humidity with 40 °C 85%RH.

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4 Electrical specifications

4-1 Electrical characteristics of LCM

($V_{DD}=3.0V$, $T_a=25^{\circ}C$)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IC power voltage	V_{DD}		2.6	2.8	3.3	V
High-level input voltage	V_{IHC}		$0.8V_{DD}$		V_{DD}	V
Low-level input voltage	V_{ILC}		0		$0.2V_{DD}$	V
Consumption current of VDD	I_{DD}	LED OFF	-	8	-	mA
Consumption current of LED	I_{LED_ON}	$V_{LED_ON}=3.6V$	-	80	-	mA

※ 1. 1/320 duty.

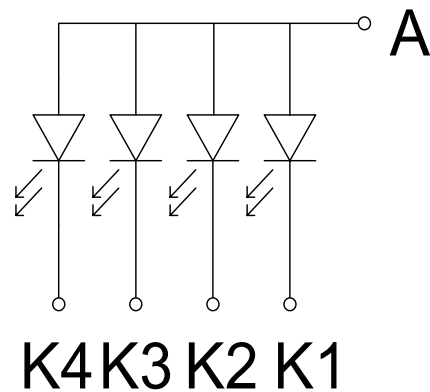
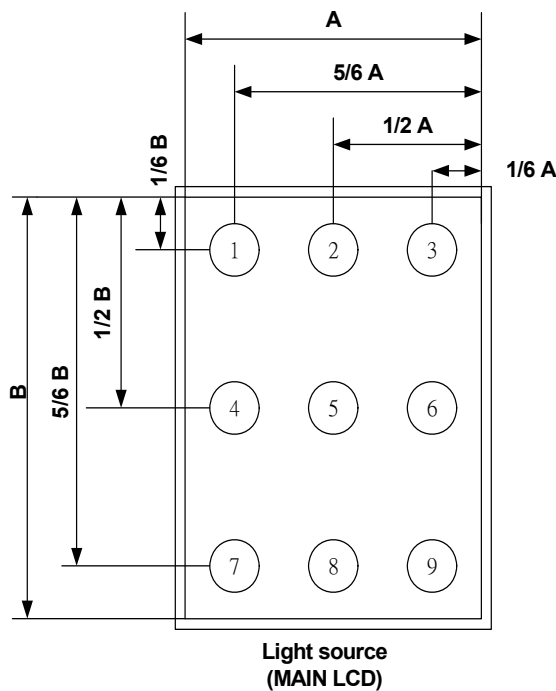
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4-2 LED back light specification

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	V_f	$I_f = 80\text{mA}$	3.4	3.6	3.8	V
Reverse voltage	V_r		-	-	12	V
Forward current	I_f	4-chip Parallel	75	80	85	mA
Power Consumption	P_{BL}	$I_f = 80\text{mA}$	-	288	-	mW
Uniformity (with L/G)	-	$I_f = 80\text{mA}$	80%*1	-	-	
Bare LED Luminous intensity	V_f I_f	3.6V 80mA	3000	-	-	cd/m ²
Luminous color	White					
Chip connection	4 chip parallel connection					

Bare LED measure position:



*1 Uniformity (LT): $\frac{\text{Min}(P1 \sim P9)}{\text{Max}(P1 \sim P9)} \times 100 \geq 80\%$

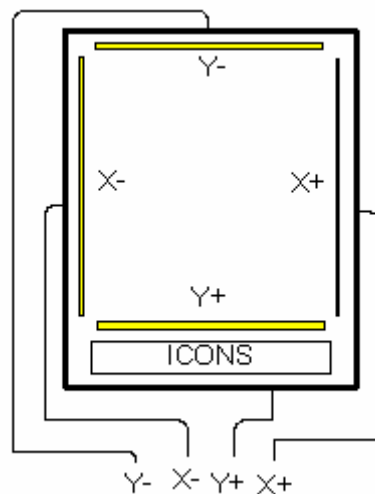
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4-3 Touch Panel Electrical Specification

Parameter	Condition	Standard Value
Terminal Resistance	X Axis	200 ~ 900 Ω
	Y Axis	200 ~ 900 Ω
Insulating Resistance	DC 25 V	More than 20M Ω
Linearity	--	± 1.5 %
Notes life by Pen	Note a	100,000 times(min)
Input life by finger	Note b	1,000,000 times (min)

	Symbol	Function
1	X+	Touch Panel Right Signal in X Axis
2	Y+	Touch Panel Bottom Signal in Y Axis
3	X-	Touch Panel Left Signal in X Axis
4	Y-	Touch Panel Top Signal in Y Axis



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5 Optical characteristics

Main LCD

5.1 Optical characteristics

(1/320 Duty in case except as specified elsewhere Ta = 25°C)

LED backlight transmissive module:

Item	Symbol	Temp.	Min.	Std.	Max.	Unit	Conditions
Response time	Tr	25 °C	--	15	--	ms	$\theta = 0^\circ$, $\varphi = 0^\circ$
	Tf	25 °C	--	35	--		(Note 2)
Contrast ratio	CR	25 °C	-	(250)	-	-	$\theta = 0^\circ$, $\varphi = 0^\circ$ LED:ON, LIGHT:OFF (Note 4)
Transmittance	T	25 °C	(5.0)	(5.5)	-	%	
Visual angle range front and rear	θ	25 °C	(θ f) 35 (θ b) 15			De- gree	$\varphi = 0^\circ$, CR \geq 10 LED:ON LIGHT:OFF (Note 3)
Visual angle range left and right	θ	25 °C	(θ l) 45 (θ r) 45			De- gree	$\varphi = 90^\circ$, CR \geq 10 LED:ON LIGHT:OFF (Note 3)
Visual angle direction priority			12:00				(Note 5)
Brightness			(180)	(200)	--	Cd/ m ²	V _{LED} =3.6V, 80mA Full White pattern

() is a default

5.2 CIE (x, y) chromaticity (1/320 Duty Ta = 25°C)

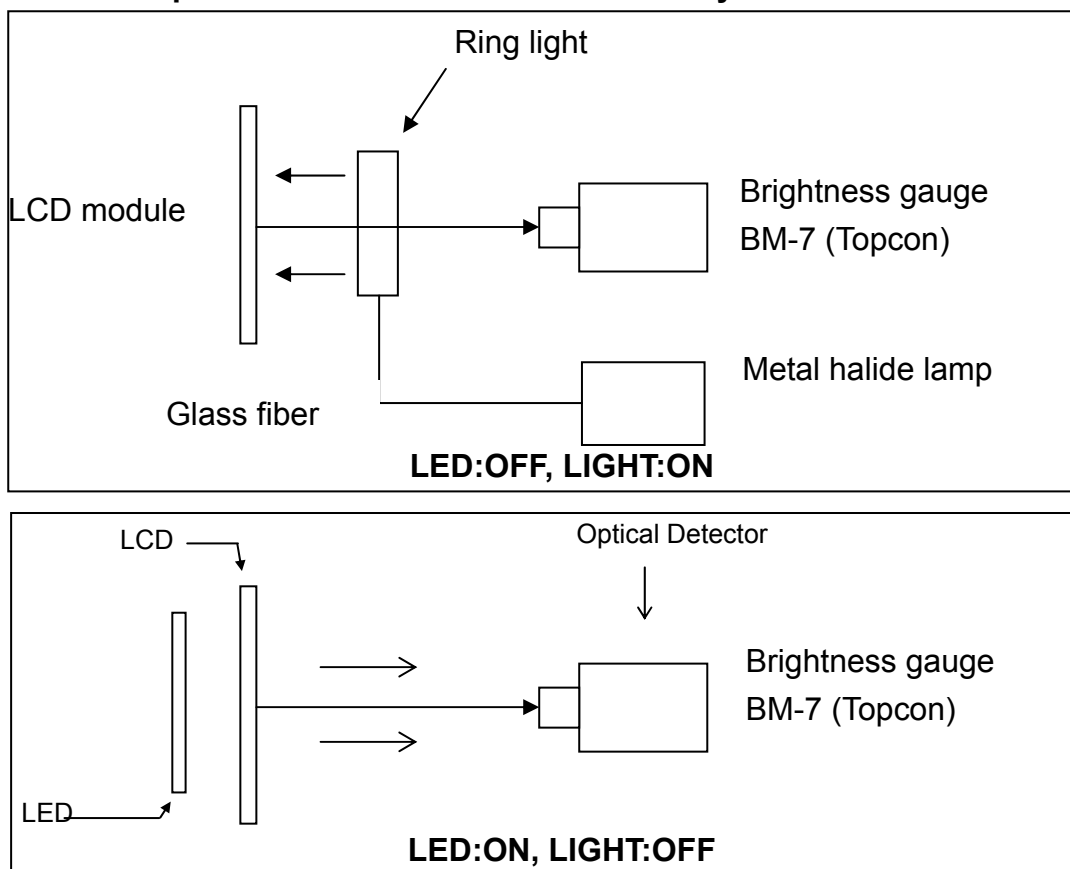
Item	Symbol	Transmissive			Conditions
		Min.	Typ.	Max.	
Red	X	(0.590)	(0.620)	(0.650)	$\theta = 0^\circ$, $\varphi = 0^\circ$
	Y	(0.310)	(0.340)	(0.370)	
Green	X	(0.303)	(0.333)	(0.363)	$\theta = 0^\circ$, $\varphi = 0^\circ$
	Y	(0.564)	(0.594)	(0.624)	
Blue	X	(0.132)	(0.152)	(0.182)	$\theta = 0^\circ$, $\varphi = 0^\circ$
	Y	(0.196)	(0.116)	(0.146)	
White	X	(0.275)	(0.305)	(0.335)	$\theta = 0^\circ$, $\varphi = 0^\circ$
	Y	(0.294)	(0.324)	(0.354)	

() is a default

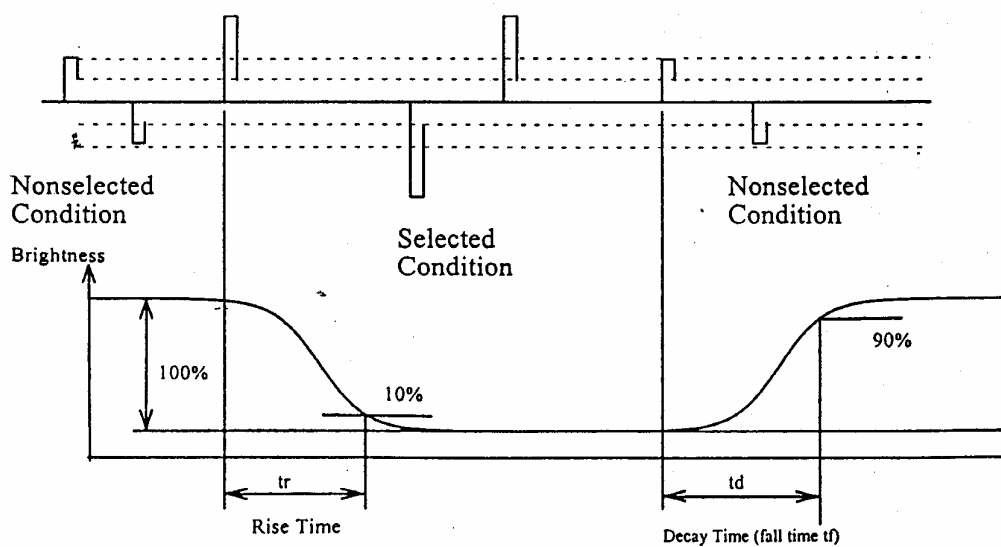
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NOTE 1: Optical characteristic measurement system



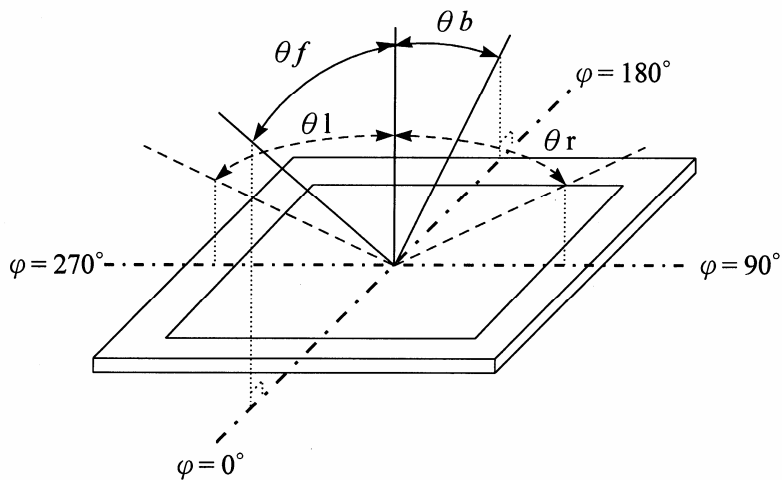
NOTE 2: Response time definition



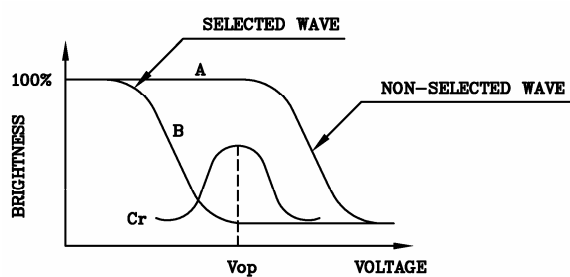
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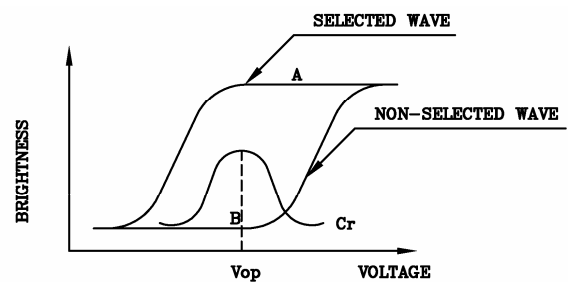
NOTE 3: φ 、 θ definition



NOTE 4: Contrast definition



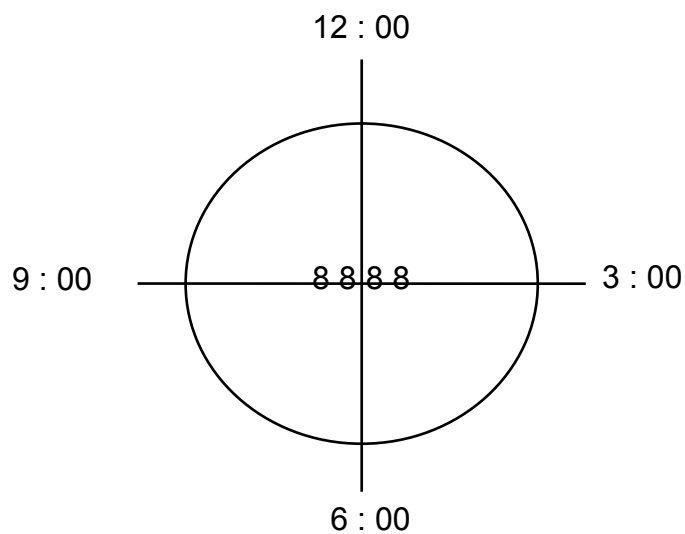
(positive type)



(negative type)

Contrast Ratio : $Cr=A/B$

NOTE 5: Visual angle direction priority



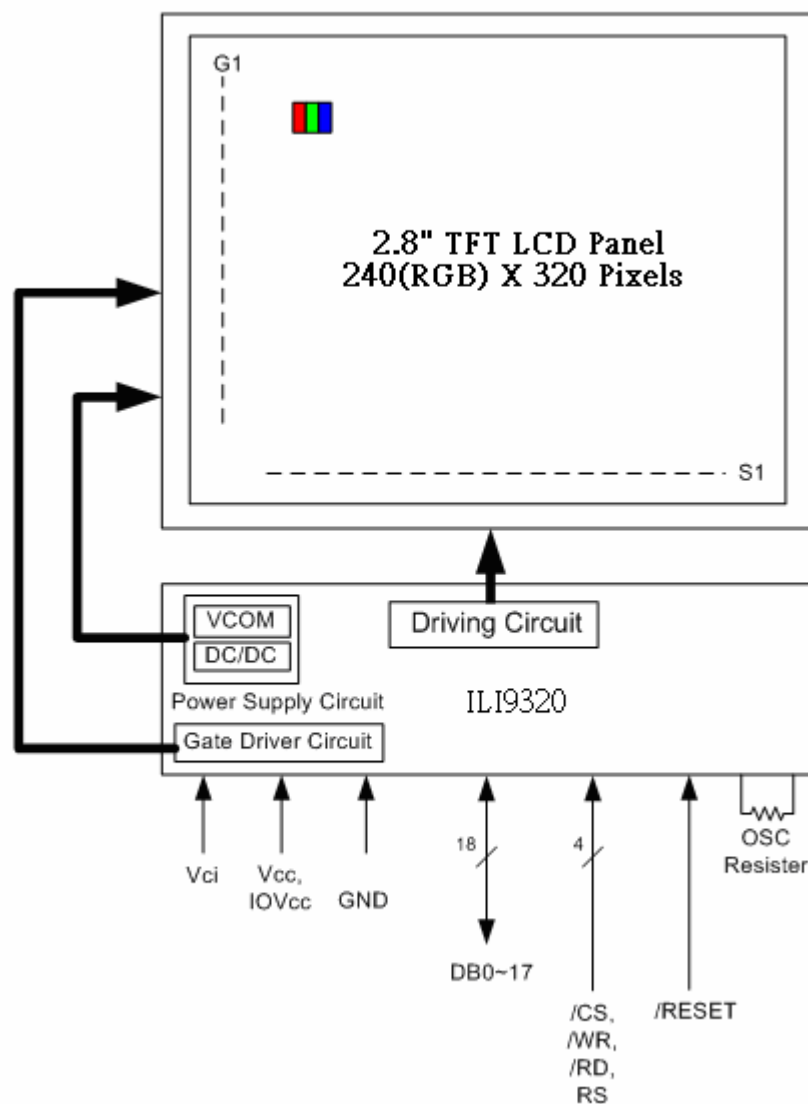
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6 Block Diagram

Block diagram (Main LCD)

Display format: A-Si TFT transmissive, Normally white type, 12 o'clock.
Display composition: 240 x RGB x 320 dots
LCD Driver : ILI9320
Back light: White LED x 4 ($I_{LED}=80mA$)



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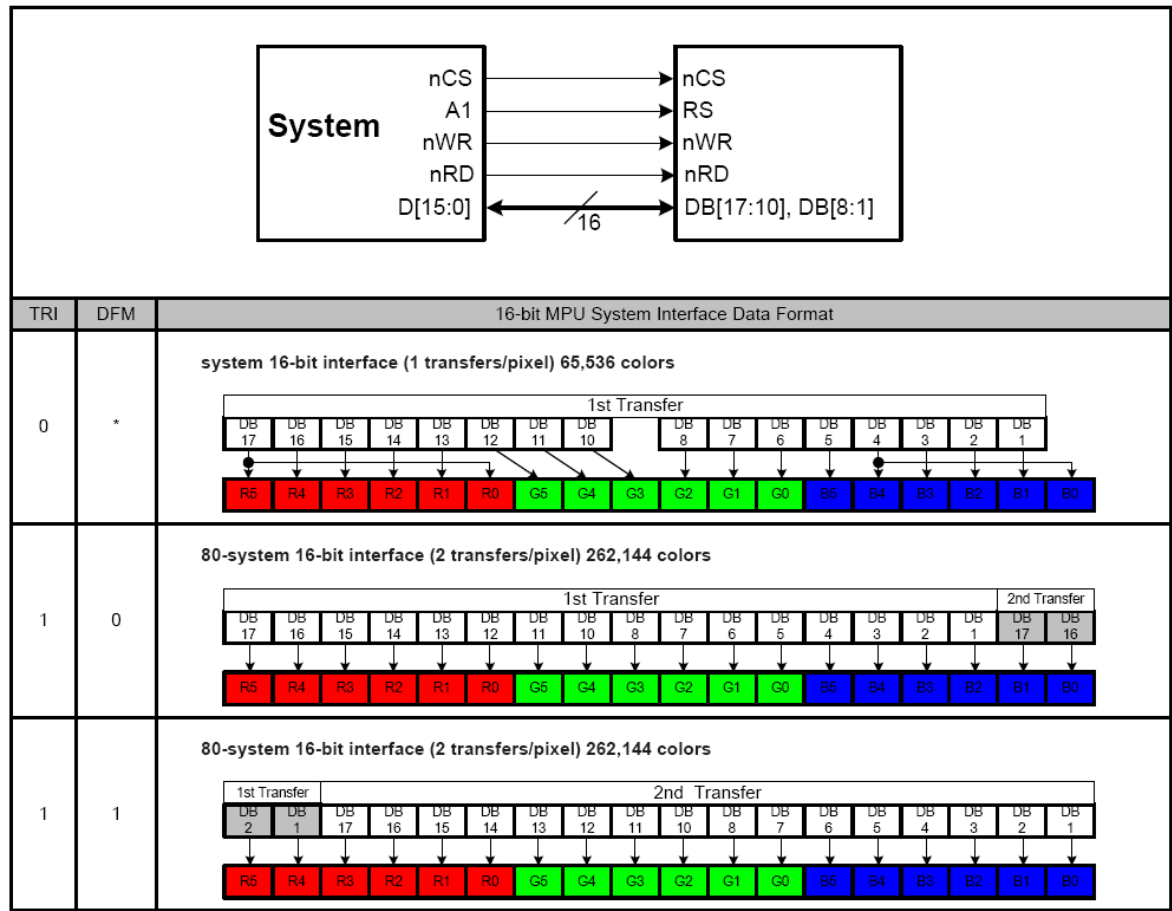
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7 Interface specifications

Pin No.	Terminal	Functions
1	DB0	Data Bus Bit 0 Contract to IC Data Bus Bit 1
2	DB1	Data Bus Bit 1 Contract to IC Data Bus Bit 2
3	DB2	Data Bus Bit 2 Contract to IC Data Bus Bit 3
4	DB3	Data Bus Bit 3 Contract to IC Data Bus Bit 4
5	GND	GND-terminal
6	VCC	Power supply for the internal logic circuit. (VCC=2.8~3.3V)
7	/CS	Chip select signal. Low : chip can be accessed; High : chip cannot be accessed.
8	RS	The signal for register index or register command select . Low: Register index or internal status (in read operation); High: Register command.
9	/WR	Write clock terminal , active "L" (80 series interface)
10	/RD	Read clock terminal , active "L" (80 series interface)
11	NC	Not connection (IM0)
12	X+	Touch panel X axis (RIGHT)
13	Y+	Touch panel Y axis (BOTTOM)
14	X-	Touch panel X axis (LEFT)
15	Y-	Touch panel Y axis (TOP)
16	LED A	LED Backlight A terminal
17	LED K1	LED Backlight K1 terminal
18	LED K2	LED Backlight K2 terminal
19	LED K3	LED Backlight K3 terminal
20	LED K4	LED Backlight K4 terminal
21	NC	Not connection (IM3)
22	DB4	Data Bus Bit 4 Contract to IC Data Bus Bit 4
23	DB8	Data Bus Bit 10 Contract to IC Data Bus Bit 8
24	DB9	Data Bus Bit 11 Contract to IC Data Bus Bit 9
25	DB10	Data Bus Bit 12 Contract to IC Data Bus Bit 10
26	DB11	Data Bus Bit 13 Contract to IC Data Bus Bit 11
27	DB12	Data Bus Bit 14 Contract to IC Data Bus Bit 12
28	DB13	Data Bus Bit 15 Contract to IC Data Bus Bit 13
29	DB14	Data Bus Bit 16 Contract to IC Data Bus Bit 14
30	DB15	Data Bus Bit 17 Contract to IC Data Bus Bit 15
31	/RESET	Reset pin. Setting either pin low initializes the LSI.
32	VCI	Power supply for Step-up circuit. (VCI=2.8~3.3V)
33	VCC2	Power supply for I/O circuit
34	GND	GND-terminal
35	DB5	Data Bus Bit 5 Contract to IC Data Bus Bit 5
36	DB6	Data Bus Bit 6 Contract to IC Data Bus Bit 6
37	DB7	Data Bus Bit 7 Contract to IC Data Bus Bit 7

7.1 80-system 16-bit interface

The i80/16-bit system interface is selected by setting the IM[3:0] as “0010” levels. The 262K or 65K color can be display through the 16-bit MPU interface. When the 262K color is displayed, two transfers (1st transfer: 2 bits, 2nd transfer: 16 bits or 1st transfer: 16 bits, 2nd transfer: 2 bits) are necessary for the 16-bit CPU interface.



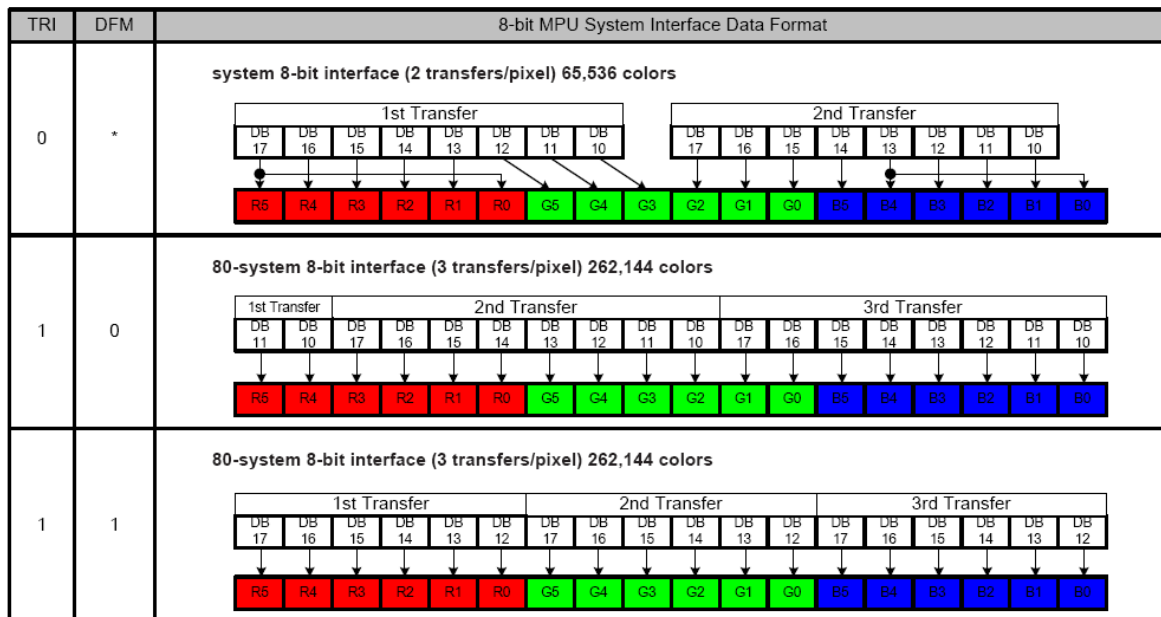
262,144color are available

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7.2 80-system 8-bit interface

The i80/8-bit system interface is selected by setting the IM[3:0] as "0011" and the DB17~DB10 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (8 bits) and lower byte, and the upper byte is transferred first. The written data is expanded into 18 bits internally (see the figure below) and then written into GRAM. The unused DB[9:0] pins must be tied to either Vcc or AGND.

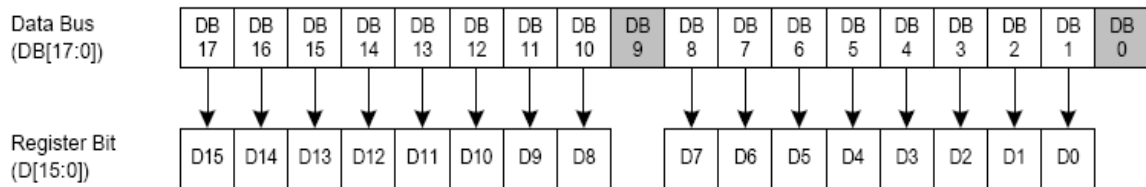


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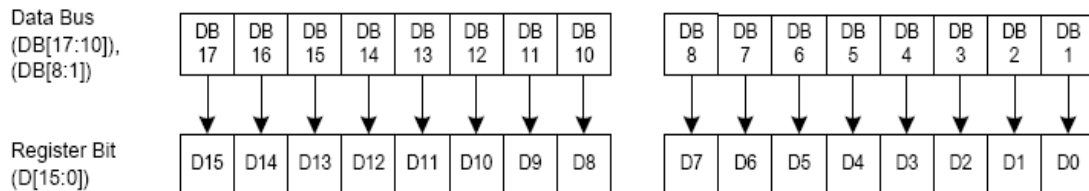
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7.3 Register setting with i80 System Interface

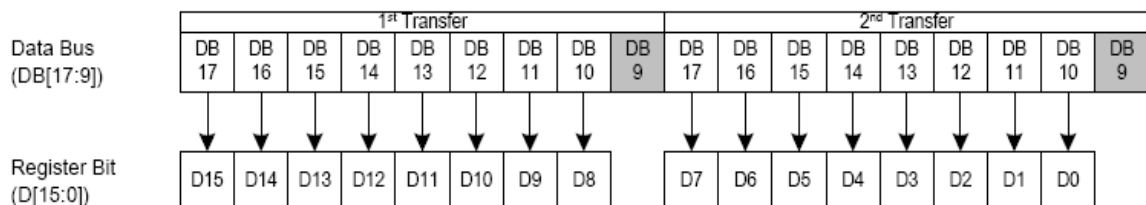
i80/M68 system 18-bit data bus interface



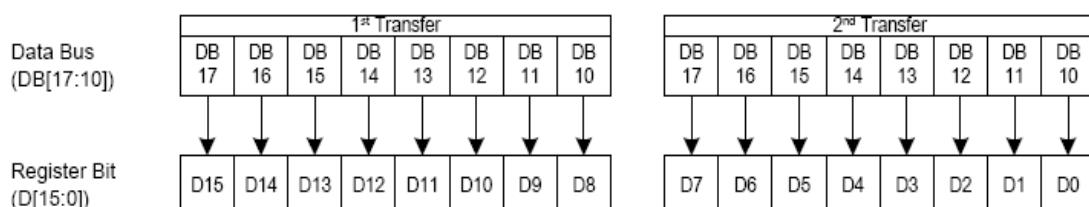
i80/M68 system 16-bit data bus interface



i80/M68 system 9-bit data bus interface



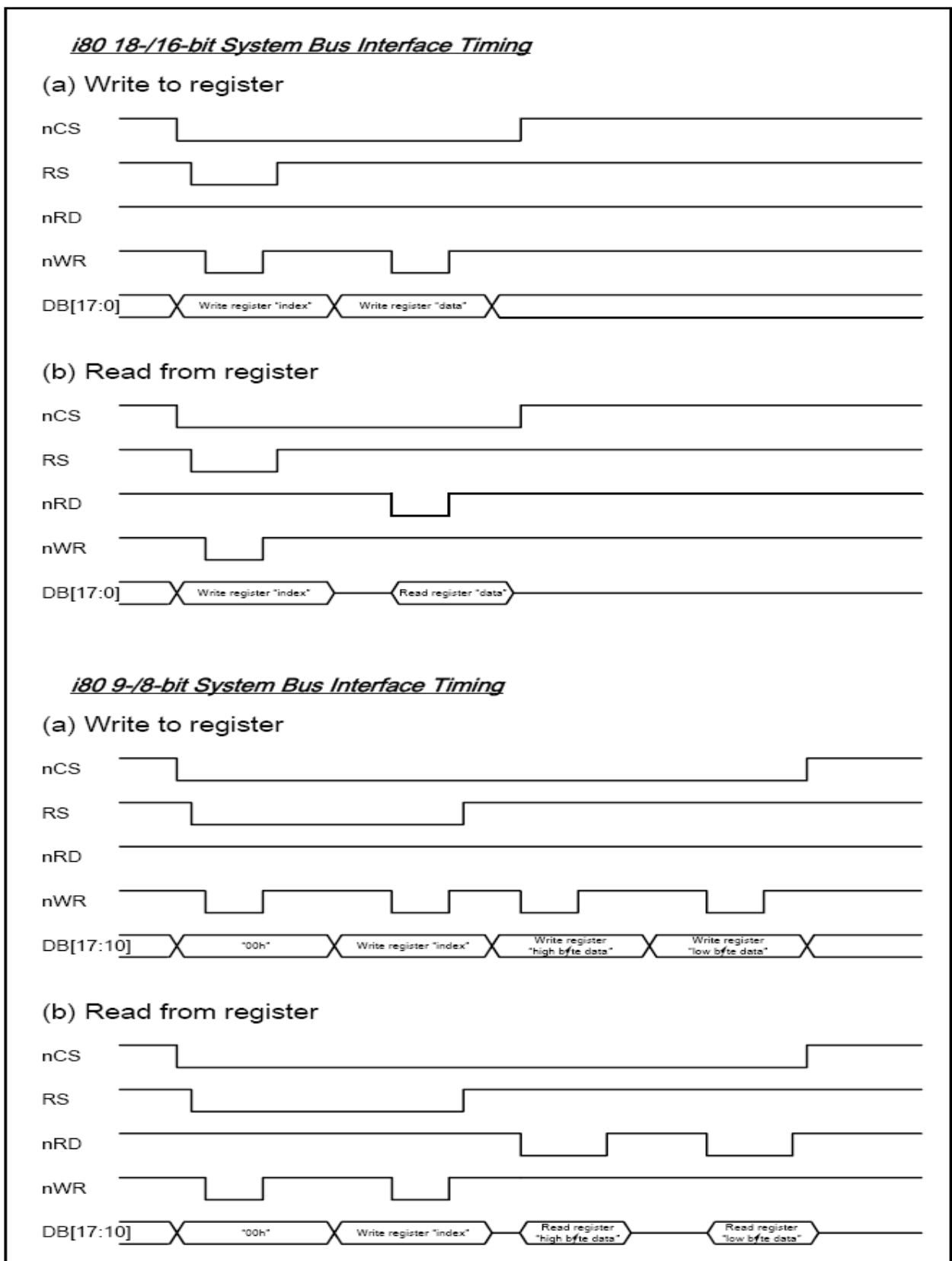
i80/M68 system 8-bit data bus interface/Serial peripheral interface (2/3 transmission)



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7.4 Register Read / Write Timing of i80 System Interface



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7.5 Instruction List

Main LCD Driver IC:ILI920

No.	Registers Name	RW	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status Read	R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
00h	Driver Code Read	R	1	1	0	0	1	0	0	1	0	0	0	1	0	0	0	1	0
00h	Start Oscillation	W	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	OSC
01h	Driver Output Control 1	W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
02h	LCD Driving Control	W	1	0	0	0	0	0	1	B/C	EOR	0	0	0	0	0	0	0	0
03h	Entry Mode	W	1	TRI	DFM	0	BGR	0	0	HWM	0	ORG	0	ID1	ID0	AM	0	0	0
04h	Resize Control	W	1	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0
07h	Display Control 1	W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
08h	Display Control 2	W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
09h	Display Control 3	W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
0Ah	Display Control 4	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FM12	FM11	FM10
0Ch	RGB Display Interface Control 1	W	1	ENC2	ENC1	ENC0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
0Dh	Frame Maker Position	W	1	0	0	0	0	0	0	0	FMF8	FMF7	FMF6	FMF5	FMF4	FMF3	FMF2	FMF1	FMF0
0Fh	RGB Display Interface Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	DPL	EPL
10h	Power Control 1	W	1	0	0	0	SAP	BT3	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	DS1B	SLP	0
11h	Power Control 2	W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
12h	Power Control 3	W	1	0	0	0	0	0	0	0	VCMR	0	0	0	PON	VRH3	VRH2	VRH1	VRH0
13h	Power Control 4	W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
20h	Horizontal GRAM Address Set	W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
21h	Vertical GRAM Address Set	W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
22h	Write Data to GRAM	W	1	RAM write data (WD17-0) / read data (RD17-0) bits are transferred via different data bus lines according to the selected interfaces.															
29h	Power Control 7	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2Bh	Frame Rate and Color Control	W	1	0	0	0	0	0	0	0	0	EXT_R	0	FR_SEL1	FR_SEL0	0	0	0	0
30h	Gamma Control 1	W	1	0	0	0	0	0	KP1[12]	KP1[11]	KP1[10]	0	0	0	0	0	KP0[12]	KP0[11]	KP0[10]
31h	Gamma Control 2	W	1	0	0	0	0	0	KP3[12]	KP3[11]	KP3[10]	0	0	0	0	0	KP2[12]	KP2[11]	KP2[10]
32h	Gamma Control 3	W	1	0	0	0	0	0	KP5[12]	KP5[11]	KP5[10]	0	0	0	0	0	KP4[12]	KP4[11]	KP4[10]
35h	Gamma Control 4	W	1	0	0	0	0	0	RP1[12]	RP1[11]	RP1[10]	0	0	0	0	0	RP0[12]	RP0[11]	RP0[10]
36h	Gamma Control 5	W	1	0	0	0	VRP1[14]	VRP1[13]	VRP1[12]	VRP1[11]	VRP1[10]	0	0	0	VRP0[14]	VRP0[13]	VRP0[12]	VRP0[11]	VRP0[10]
37h	Gamma Control 6	W	1	0	0	0	0	0	KN1[12]	KN1[11]	KN1[10]	0	0	0	0	0	KN0[12]	KN0[11]	KN0[10]
38h	Gamma Control 7	W	1	0	0	0	0	0	KN3[12]	KN3[11]	KN3[10]	0	0	0	0	0	KN2[12]	KN2[11]	KN2[10]
39h	Gamma Control 8	W	1	0	0	0	0	0	KN5[12]	KN5[11]	KN5[10]	0	0	0	0	0	KN4[12]	KN4[11]	KN4[10]
3Ch	Gamma Control 9	W	1	0	0	0	0	0	RN1[12]	RN1[11]	RN1[10]	0	0	0	0	0	RN0[12]	RN0[11]	RN0[10]

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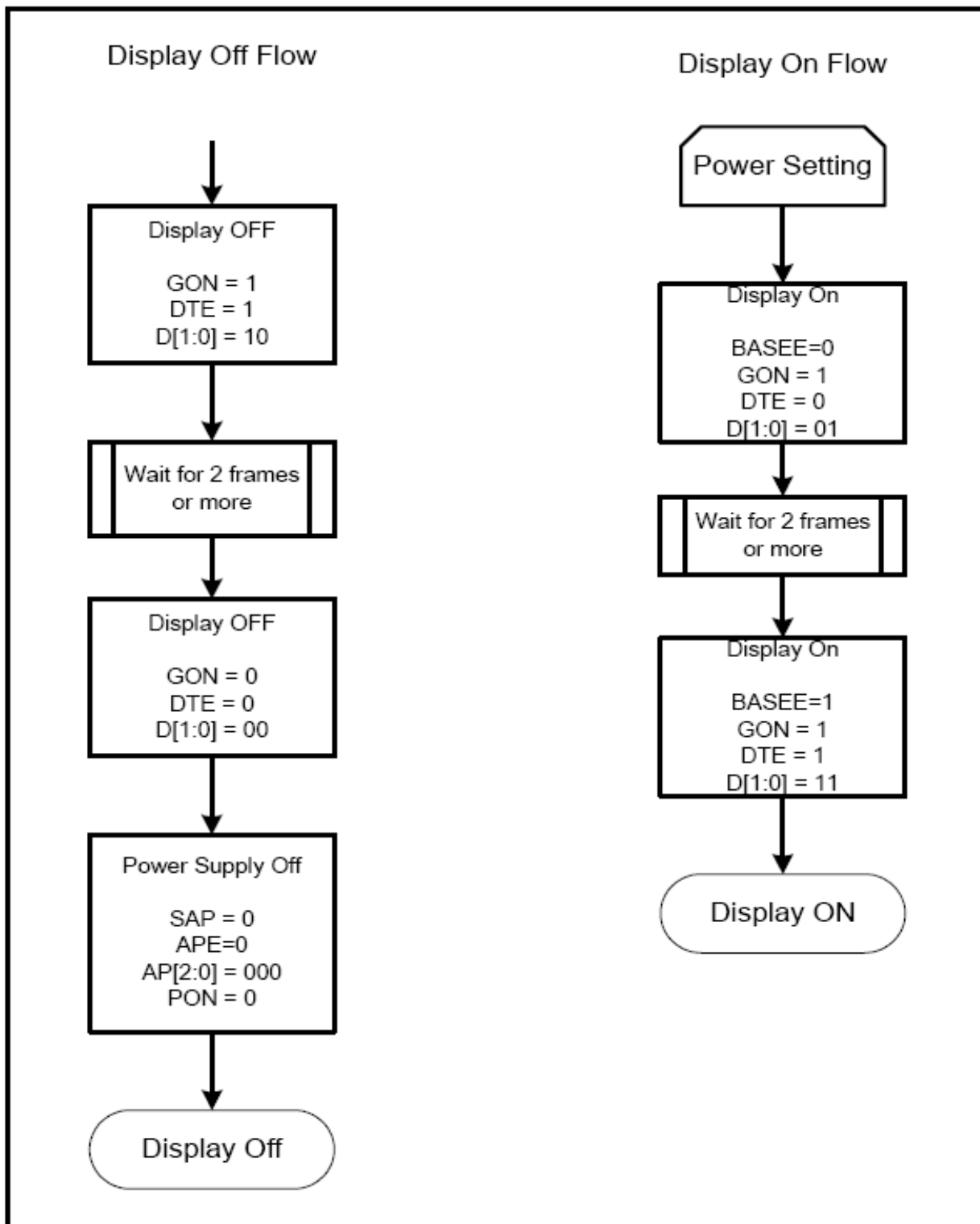
No.	Registers Name	RW	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
30h	Gamma Control 10	W	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	VRN04	VRN03	VRN02	VRN01	VRN00
50h	Horizontal Address Start Position	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
51h	Horizontal Address End Position	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
52h	Vertical Address Start Position	W	1	0	0	0	0	0	0	0	0	WSA8	WSA7	WSA6	WSA5	WSA4	WSA3	WSA2	WSA1
53h	Vertical Address End Position	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
60h	Driver Output Control 2	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
61h	Base Image Display Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
6Ah	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
80h	Partial Image 1 Display Position	W	1	0	0	0	0	0	0	0	PTDP08	PTDP07	PTDP06	PTDP05	PTDP04	PTDP03	PTDP02	PTDP01	PTDP00
81h	Partial Image 1 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA08	PTSA07	PTSA06	PTSA05	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00
82h	Partial Image 1 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA08	PTEA07	PTEA06	PTEA05	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00
83h	Partial Image 2 Display Position	W	1	0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10
84h	Partial Image 2 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10
85h	Partial Image 2 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10
90h	Panel Interface Control 1	W	1	0	0	0	0	0	0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0
92h	Panel Interface Control 2	W	1	0	0	0	0	0	NOM2	NOM1	NOM0	0	0	0	0	0	0	0	0
93h	Panel Interface Control 3	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPI2	MCPI1	MCPI0
95h	Panel Interface Control 4	W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0
97h	Panel Interface Control 5	W	1	0	0	0	0	NOME3	NOME2	NOME1	NOME0	0	0	0	0	0	0	0	0
98h	Panel Interface Control 6	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE2	MCPE1	MCPE0

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8. Application

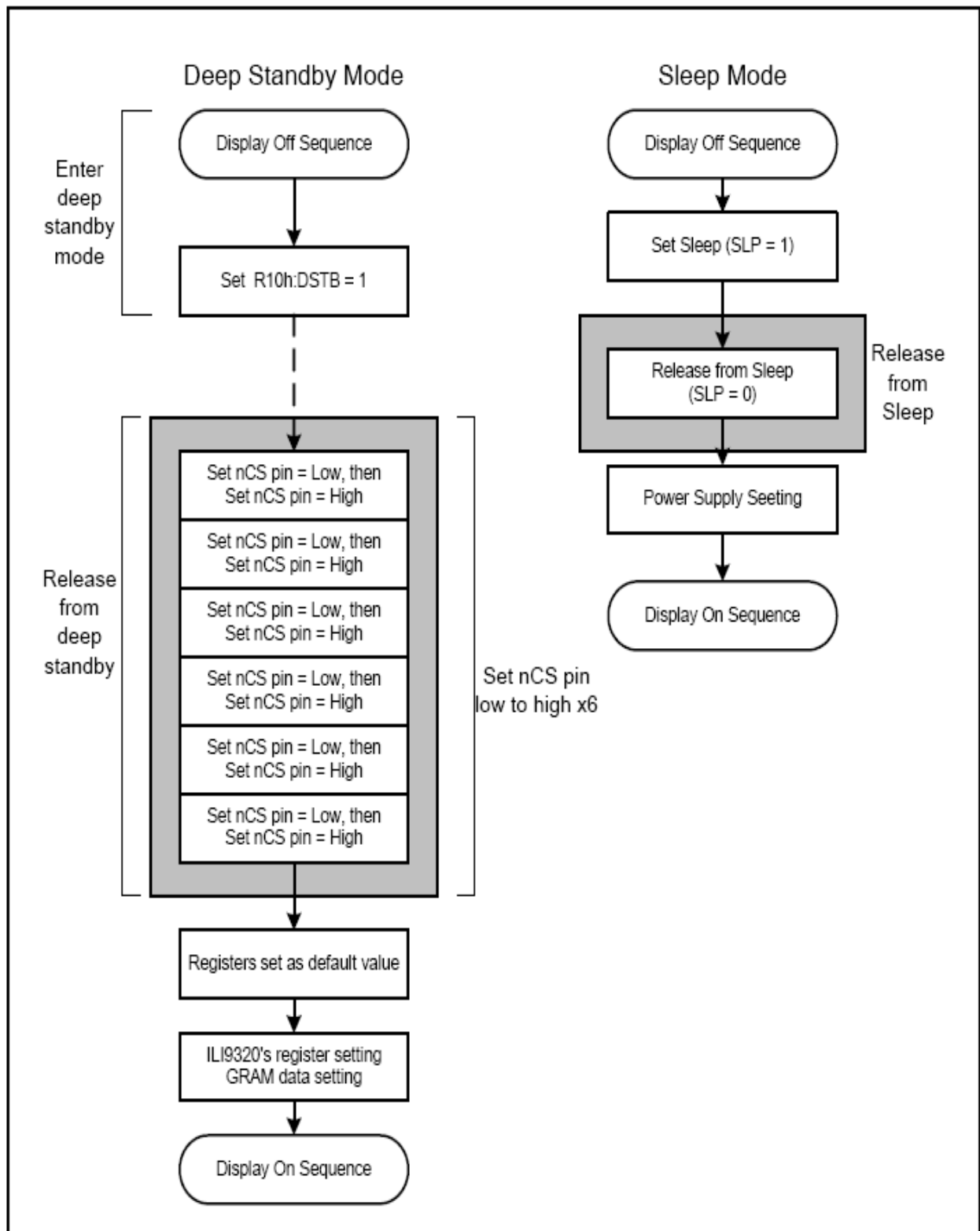
8.1 Display ON / OFF Sequence



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8.2 Deep Standby and Sleep Mode

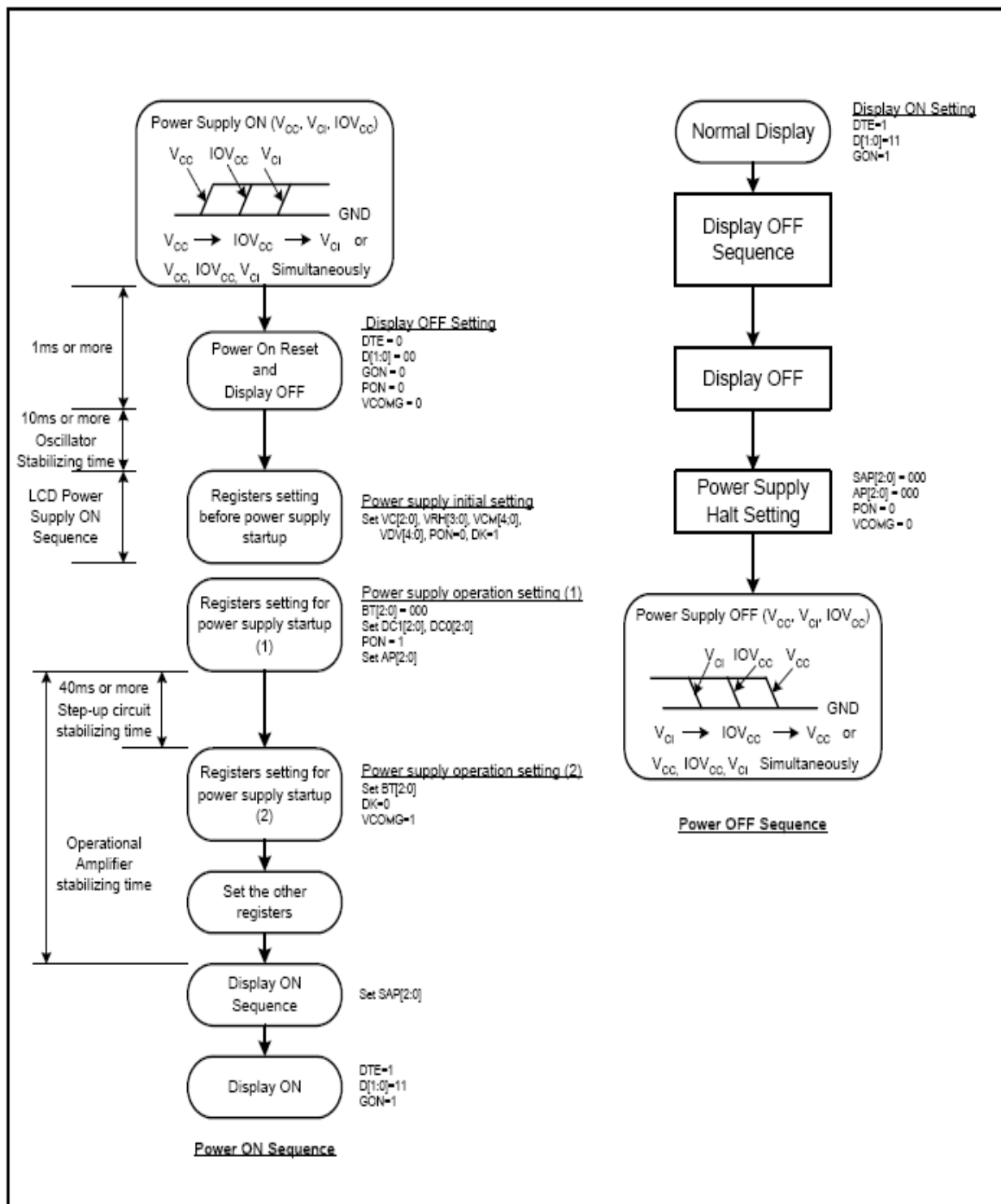


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8.3 Power Supply Configuration

When supplying and cutting off power, follow the sequence below. The setting time for oscillators, step-up circuits and operational amplifiers depends on external resistance and capacitance.



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9. Electrical Characteristics

9.1 Clock Characteristics

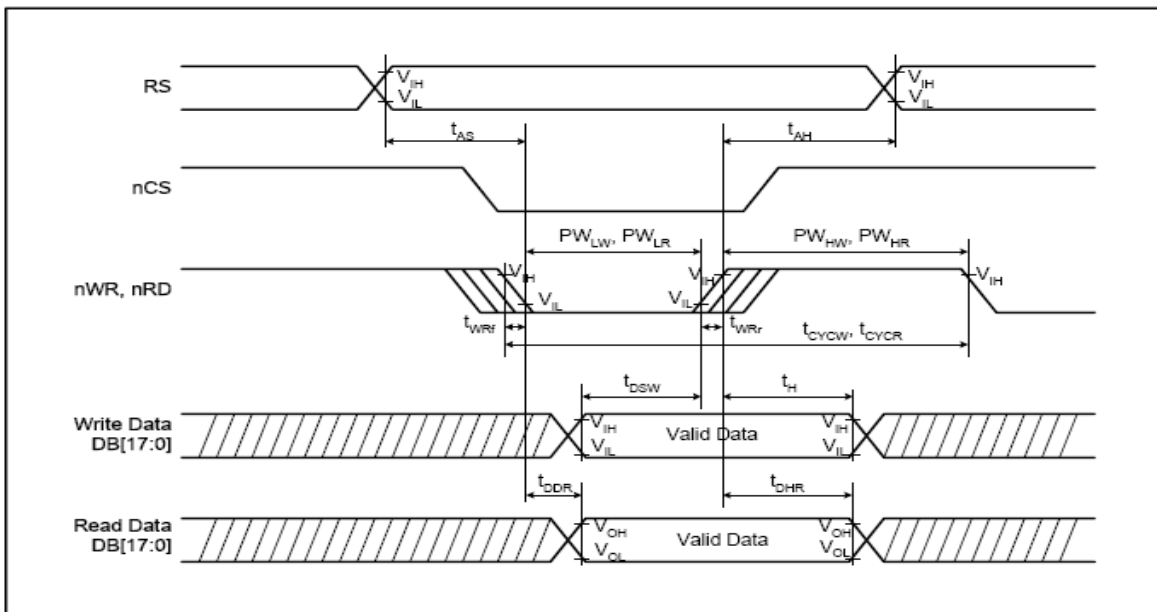
VCC = 2.40 ~ 3.30V, IOVCC = 1.65 ~ 3.30V

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
External Clock Frequency	f _{cp}	VCC = 2.4 ~ 3.3V	450	550	650	KHz
External Clock Duty	f _{duty}	VCC = 2.4 ~ 3.3V	45	50	55	
External Clock Rising Time	Trcp	VCC = 2.4 ~ 3.3V	-	-	0.2	μs
External Clock Falling Time	Tfcp	VCC = 2.4 ~ 3.3V	-	-	0.2	μs
RC oscillation clock	f _{osc}	Rf = 100KΩ, VCC = 2.8V	450	550	650	KHz

9.2 AC Characteristics (i80 – system Interface Timing Characteristics)

Normal Write Mode (IOVCC = 1.65~3.3V, VCC=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t _{CYCW}	ns	100	-	-
	Read	t _{CYCR}	ns	300	-	-
Write low-level pulse width	PW _{LW}	ns	50	-	500	-
Write high-level pulse width	PW _{HW}	ns	50	-	-	-
Read low-level pulse width	PW _{LR}	ns	150	-	-	-
Read high-level pulse width	PW _{HR}	ns	150	-	-	-
Write / Read rise / fall time	t _{WRP} /t _{WRF}	ns	-	-	25	-
Setup time	Write (RS to nCS, E/nWR)	t _{AS}	ns	10	-	-
	Read (RS to nCS, RW/nRD)					
Address hold time	t _{AH}	ns	5	-	-	-
Write data set up time	t _{DSW}	ns	10	-	-	-
Write data hold time	t _H	ns	15	-	-	-
Read data delay time	t _{DDR}	ns	-	-	100	-
Read data hold time	t _{DHR}	ns	5	-	-	-



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10.QUALITY AND RELIABILITY

10.1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : $25 \pm 5^{\circ}\text{C}$

Humidity : $60 \pm 25\% \text{ RH}$.

10.2 SAMPLING PLAN

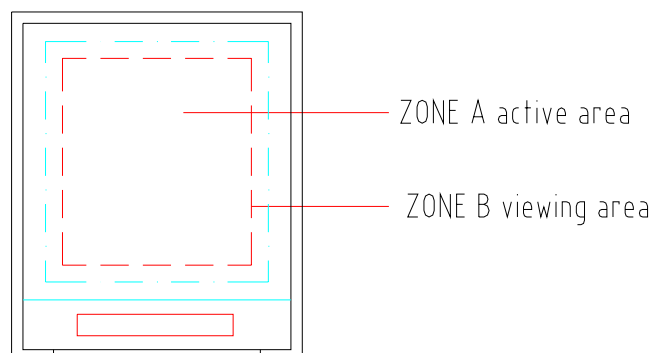
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

10.3 ACCEPTABLE QUALITY LEVEL

A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

10.4 APPEARANCE

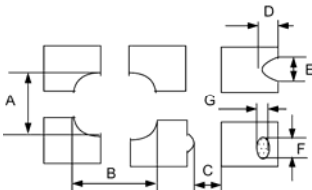
An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under florescent light. The inspection area of LCD panel shall be within the range of following limits.



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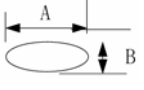
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11.5 INSPECTION QUALITY CRITERIA

No.	Item	Criterion for defects	Class of Defec	Acceptable level								
1	Non display	No non display is allowed	Major	0.65								
2	Scratch,Dent of Plastic Mold	Serious one is not allowed	Major	0.65								
3	Scratch on FPC	By limited sample	Major	0.65								
4	Dot Defect	<table><tr><th>Item</th><th>Number</th></tr><tr><td>Bright dot defect</td><td>$N \leq 0$</td></tr><tr><td>Black dot defect</td><td>$N \leq 2$</td></tr><tr><td>Total</td><td>$N \leq 2$</td></tr></table>	Item	Number	Bright dot defect	$N \leq 0$	Black dot defect	$N \leq 2$	Total	$N \leq 2$	Minor	1.5
Item	Number											
Bright dot defect	$N \leq 0$											
Black dot defect	$N \leq 2$											
Total	$N \leq 2$											
5	Line Defect	None	Minor	1.5								
6	Uneven Brightness : Line Shape	None	Major	0.65								
7	Uneven Brightness : Dot Shape	None	Major	0.65								
8	Display pattern	<div><p>Unit:mm</p><table><tr><td>$\frac{A+B}{2} \leq 0.30$</td><td>$0 < C$</td><td>$\frac{D+E}{2} \leq 0.25$</td><td>$\frac{F+G}{2} \leq 0.25$</td></tr></table><p>Note: 1. Acceptable up to 3 damages 2. NG if there're to two or more pinholes per dot</p></div>	$\frac{A+B}{2} \leq 0.30$	$0 < C$	$\frac{D+E}{2} \leq 0.25$	$\frac{F+G}{2} \leq 0.25$	Minor	1.5				
$\frac{A+B}{2} \leq 0.30$	$0 < C$	$\frac{D+E}{2} \leq 0.25$	$\frac{F+G}{2} \leq 0.25$									
9	Scratch of Polarizer :Dot Shapes Size: $D = \frac{A+B}{2}$	<table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>$D \leq 0.1$</td><td>Ignore</td></tr><tr><td>$0.1 < D \leq 0.3$</td><td>3</td></tr><tr><td>$0.3 < D$</td><td>0</td></tr></table>	Size D (mm)	Acceptable number	$D \leq 0.1$	Ignore	$0.1 < D \leq 0.3$	3	$0.3 < D$	0	Minor	1.5
Size D (mm)	Acceptable number											
$D \leq 0.1$	Ignore											
$0.1 < D \leq 0.3$	3											
$0.3 < D$	0											

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10	Scratch of Polarizer : Line Shape 	Width (mm)	Length (mm)	Acceptable number	Minor	1.5
		$W \leq 0.05$	$L \leq 0.3$	Ignore		
		$0.1 < W \leq 0.05$	$0.3 < L \leq 2.0$	$N \leq 3$		
		$0.1 < W$	-	See dot shape		
11	Bubble in polarizer	Size D (mm)		Acceptable number	Minor	1.5
		$D \leq 0.3$		Ignore		
		$0.30 < D \leq 0.50$		1		
		$0.50 < D$		0		
12	Stains inclusion : Line shape	Width (mm)	Length (mm)	Acceptable number	Minor	1.5
		$W \leq 0.04$	Ignore	Not Allowed		
		$0.04 < W \leq 0.06$	$L \leq 0.8$	Not Allowed		
		$0.06 < W$	-	Not Allowed		
13	Stains inclusion : dot shape	Size D (mm)		Acceptable number	Minor	1.5
		$D \leq 0.1$		Not Allowed		
		$0.1 < D \leq 0.2$		Not Allowed		
		$0.25 < D$		Not Allowed		

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11.6 RELIABILITY

Test Item	Test Conditions	Note
High Temperature Operation	60±3°C , t=72 hrs	
Low Temperature Operation	-10±3°C , t=72 hrs	
High Temperature Storage	70±3°C , t=72hrs	1,2
Low Temperature Storage	-20±3°C , t=72 hrs	1,2
Humidity Test	40°C , Humidity 90%, 72 hrs	1,2
Thermal Shock Test	-20°C ~ 25°C ~ 70°C 30 min. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Vibration Test (Packing)	Sweep frequency : 10~55~10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2
Static Electricity	150pF 330 ohm ±8kV, 10times air discharge ±5kV, 10times contact discharge	

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions (15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

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12 USE PRECAUTIONS

12.1 Handling precautions

- 1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
- 2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
- 3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
- 4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

12.2 Installing precautions

- 1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. $1M\Omega$ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
- 2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
- 3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
- 4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

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12.3 Storage precautions

- 1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
- 2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
- 3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

12.4 Operating precautions

- 1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
- 2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
- 3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC drive voltage.
- 4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
- 5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
- 6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
- 7) The characteristic of the semiconductor element changes when it is exposed to

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light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.

- 8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

12.5 Other

- 1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
- 2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.

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13. MECHANIC DRAWING

