Product Specifications

1.5″ COLOR TFT-LCD MODULE

Model Name：	A015AN05 V2
Planned Lifetime:	From 2009/Apr. to 2010/Aug.
Phase-out Control:	From 2010/Jun. to 2010/Aug.
EOL Schedule:	2010/Aug.

< > Preliminary Specification

< □ > Final Specification

Note: The content of this specification is subject to change without notice.

Record of Revision

Version	Revise Date	Page	Content
0.0	2009/04/22		First draft
0.1	2009/07/13	3	Update the weight of module
		15	Update viewing angle TYP spec of Bottom and add Min. spec.

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A. Physical Specifications

No.	Item	Specification	Remark
1	Display resolution (dot)	280 (W) ×220 (H)	
2	Active area (mm)	29.96 (W) ×22.66 (H)	
3	Screen size (inch)	1.48 (Diagonal)	
4	Dot pitch (mm)	0.107 (W) ×0.103 (H)	
5	Color configuration	R. G. B. delta	
6	Overall dimension (mm)	37.06 (W) ×34.0 (H) ×2.6(D)	Note 1
7	Weight (g)	5.5	
8	Panel surface treatment	Hard coating (3H)	

Note 1: Refer to Fig. 5

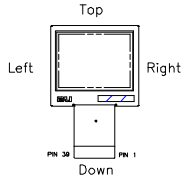
B. Electrical Specifications

1. Pin assignment (Note1)

Pin no.	Symbol	I/O	Description	Remark
1	VCOM	I	Common electrode driving signal	
2	V1	C	Power setting capacitor connect pin	
3	V2	C	Power setting capacitor connect pin	
4	V3	C	Power setting capacitor connect pin	
5	V4	C	Power setting capacitor connect pin	
6	VGH	C	Positive power for scan driver	
7	V5	C	Power setting capacitor connect pin	
8	V6	C	Power setting capacitor connect pin	
9	Vgoff_H	C	Negative power supply (High) for G1~G220 outputs	
10	Vgoff_L	C	Negative power supply (High) for G1~G220 outputs	
11	V7	C	Power setting capacitor connect pin	
12	V8	C	Power setting capacitor connect pin	
13	AVDD1	C	FRP level supply	
14	FRP	O	Frame polarity output for panel Vcom	
15	AGND	P	Ground pin for digital circuit	
16	VCP	P	Power supply for charge pump	
17	VLED+	P	LED power anode	
18	VLED-	P	LED power cathode	
19	VCC	P	Power supply for digital circuits	3.0V~3.6V
20	AGND	P	Ground pin for analog circuits	
21	AVDD	P	Power supply for analog circuits	
22	HSYNC	I	Horizontal sync input. Negative polarity	
23	VSYNC	I	Vertical sync input. Negative polarity	
24	DCLK	I	Clock signal; latch data onto line latches at the rising edge	
25	D5	I	Data input: MSB	
26	D4	I	Data input	
27	D3	I	Data input	
28	D2	I	Data input	
29	D1	I	Data input	
30	D0	I	Data input	
31	V9	C	Power setting capacitor connect pin	Note2
32	GRB	I	Global reset pin	
33	CS	I	Serial communication chip select	Note3
34	SDA	I	Serial communication data input	Note3
35	SCL	I	Serial communication clock input	Note3
36	VCC	P	Power supply for digital circuits	
37	DGND	P	Ground pin for digital circuits	
38	Dummy	-	Dummy pad	
39	Dummy	-	Dummy pad	

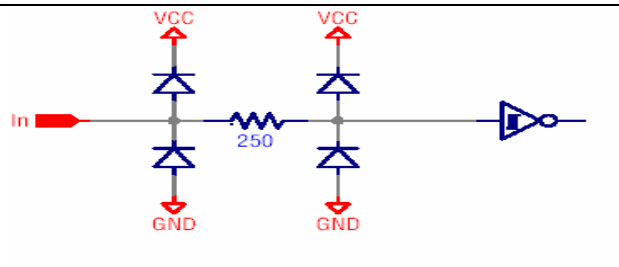
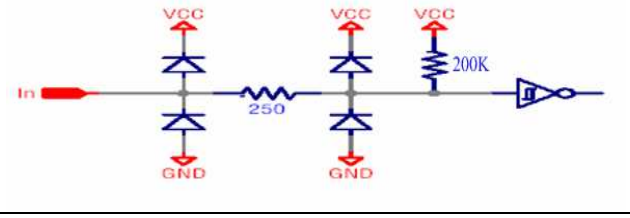
I: input; O: output, P: power

Note 1: For definition of scanning direction, please refer to figure as follows:



Note 2:The capacitor of V9(pin31) is needed.
Note 3: Please refer to application note for 3-wire serial communication setting.

2. Equivalent circuit of I/O

Pin no. & Pin name	Schematics
22.HSYNC 23.VSYNC 24.DCLK 25.D5 26.D4 27.D3 28.D2 29.D1 30.D0 33.CS 34.SDA 35.SCL	
32.GRB	

3. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Supply Voltage	VCC	GND=0V	-0.5	5	V	
	AVDD	AGND=0V	-0.5	5.5	V	
TFT-LCD Power Voltage	VGH	AGND=GND=0V	0	16	V	
	Vgoff_H	AGND=GND=0V	-10	0	V	
	Vgoff_L	AGND=GND=0V	-16	0	V	
Input Signal Voltage	CS,SDA,SCL,Vsync, Hsync,DCLK,D0~D7	AGND=GND=0V	-0.5	5	V	
VCOM AC Output Voltage	FRP	AGND=GND=0V	0	8	V	
VCOM AC Power Voltage	AVDD1	AGND=GND=0V	0	8	V	
VCOM DC Output Voltage	COMDC	AGND=GND=0V	0	5	V	
VCOM Input Voltage	VCOM	AGND=GND=0V	-2.9	5.6	V	
	V1	AGND=GND=0V	0	16	V	
	V2	AGND=GND=0V	0	8	V	
	V3	AGND=GND=0V	0	16	V	
	V4	AGND=GND=0V	-16	0	V	
Storage Temperature	Tstg	-	-25	80	℃	Ambient temperature
Operating Temperature	Topa	-	0	60	℃	Ambient temperature

4. Electrical characteristics

a. Typical operating conditions (GND = AGND = 0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		V_{CC}	3.0	3.3	3.6	V	
		AV_{DD}	3.0	3.3	3.6	V	
Output Signal voltage	H Level	V_{OH}	Vcc-0.4				
	L Level	V_{OL}	GND		GND+0.4		
Input Signal voltage	H Level	V_{IH}	$0.7V_{CC}$	-	V_{CC}	V	
	L Level	V_{IL}	GND	-	$0.3V_{CC}$	V	
Output current	H Level	IOH		10		uA	
	L Level	IOL		-10		uA	
Analog stand by current		Ist			200	uA	DCLK is stopped
VCOM Voltage		AVDD1	4.4	5.6	5.8	V	
		V_{CDC}	0.30	0.45	0.60	V	
Internal Voltage		VCP	6.5	-	8.8	V	
Positive Power Supply		VGH	12	13	14	V	
Negative Power supply (Low)		VGoff_L	-14	-13	-12	V	
Negative Power supply (High)		VGoff_H	-8.4	-7.4	-6.4	V	

b. Recommended Capacitance Values of External Capacitor

The recommended capacitance values of the external capacitor are shown below. These values should be finally determined only after performing sufficient evaluation on the module.

Pin name	Operating value of capacitors (μF)	Withstanding voltage (V)
VCC	1 to 10	6.3
AVDD	1 to 10	6.3
AVDD1	1 to 10	10
VGH	1 to 10	16
Vgoff_H, Vgoff_L	1 to 10	16
V1, V2	1 to 10	16
V3, V4	1 to 10	16
V5, V6	1 to 10	16
V7, V8	1 to 10	16
V9	4.7 to 10	6.3(Note1)
VCP	4.7 to 10	16
FRP	10	16

Note1: The capacitors of V9 (31pin) is needed.

Note2: Typical operating capacitors reference suggested reference application circuit

c. Current consumption (GND = AGND = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Current	I_{CC}	V_{CC} = 3.3V	-	2	2.5	mA	Note1 Note2
	I_{DD}	AV_{DD} = 3.3V	-	1.5	2.0	mA	

Note1:This power consumption doesn't include LED power consumption.

Note2:Test condition: 8colorbar+Grayscale pattern, UPS051 mode, DCLK=5.67MHz, frame rate:60Hz.

d. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
	$I_{LED\ anode}$	22	25	25.5	mA	Note1
LED voltage	V_L	3.0	3.3	3.6	*V*	Note2

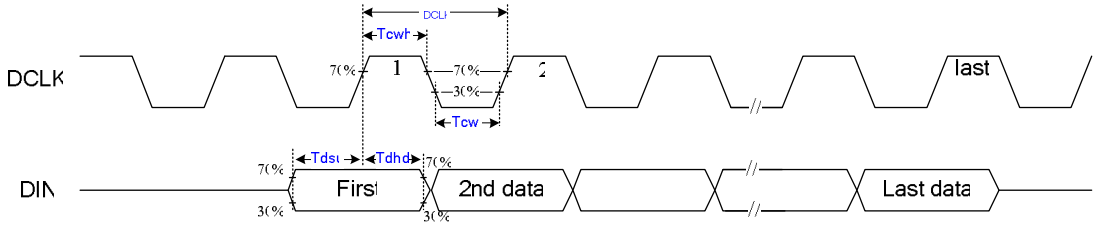
Note1: LED-.=0V

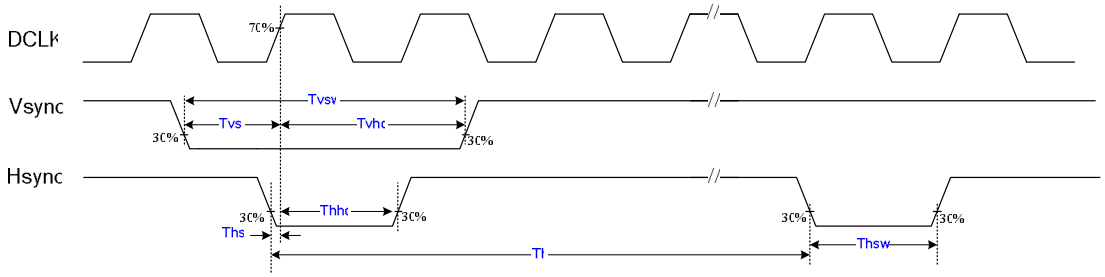
Note2: V_L = LED+ (PIN 17), LED Max. Voltage: 1pcs/3.6V, LED Min. Voltage: 1pcs/3.0V. @I_{LED}=25mA.

5. Input timing AC characteristic

(VCC=3.3V, AVDD=3.3V, AGND=GND=0V, TA=-25℃~85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK period time	t_{DCLK}	37	-	-	ns	
HSYNC period time	Th	60	63.56	67	us	
VSYNC setup time	Tvst	12	-	-	ns	
VSYNC hold time	Tvhd	12	-	-	ns	
HSYNC setup time	Thst	12	-	-	ns	
HSYNC hold time	Thhd	12	-	-	ns	
Data setup time	Thst	12	-	-	ns	
Data hold time	Thhd	12	-	-	ns	
HSYNC width	Thsw	1	1	96	t_{DCLK}	
VSYNC width	Tvsw	1 t_{DCLK}	1 t_{DCLK}	6Th		
DCLK duty cycle	Tcwh/Tcwl	40	50	60	%	





6. AC Timing

a. UPS051 Timing conditions

Note1: Horizontal display position:

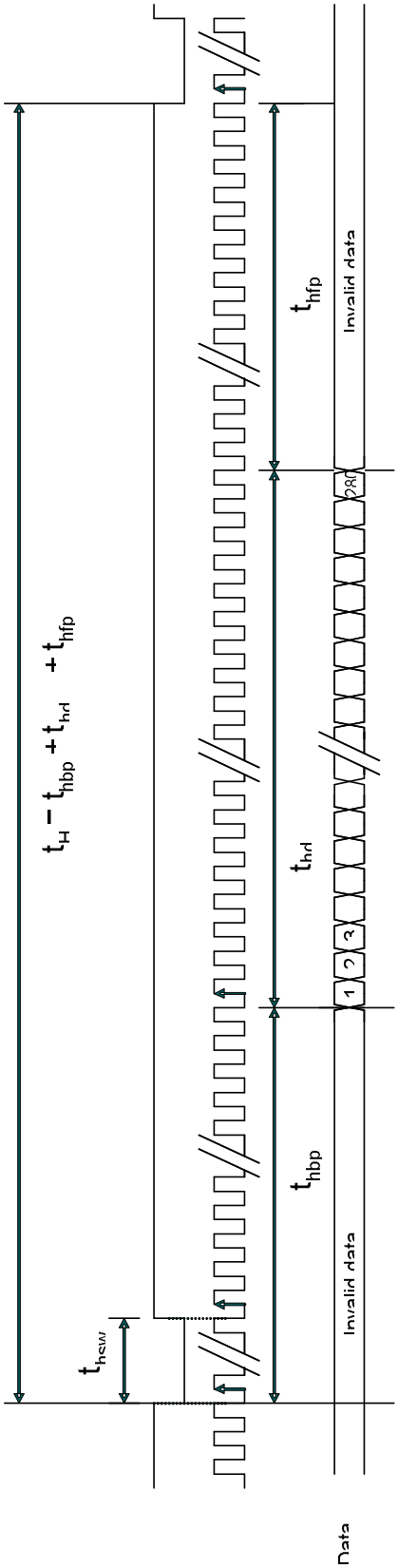
Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	5.62	5.67	12	MHz	
HSYNC	Period		t_H	360			t_{DCLK}	
	Display period		t_{hd}	280			t_{DCLK}	
	Back porch		t_{hbp}	61	62	64	t_{DCLK}	Note1
	Front porch		t_{hfp}	19	18	16	t_{DCLK}	
	Pulse width		t_{hsw}	1	25	56	t_{DCLK}	
VSYNC	Period	Odd	t_V	256	262.5	264	t_H	
		Even						
	Display period	Odd	t_{vd}	220			t_H	
		Even						
	Back porch	Odd	t_{vb}	23			t_H	
		Even		23.5				
	Front porch	Odd	t_{vf}	13	19.5	21	t_H	
		Even		12.5	19	20.5		
	Pulse width	Odd	t_{vsw}	1 t_{DCLK}	3 t_H	6 t_H	-	
		Even						

Available display starts from the data of 63 t_{DCLK} when back porch value (t_{hbp}) set 62.

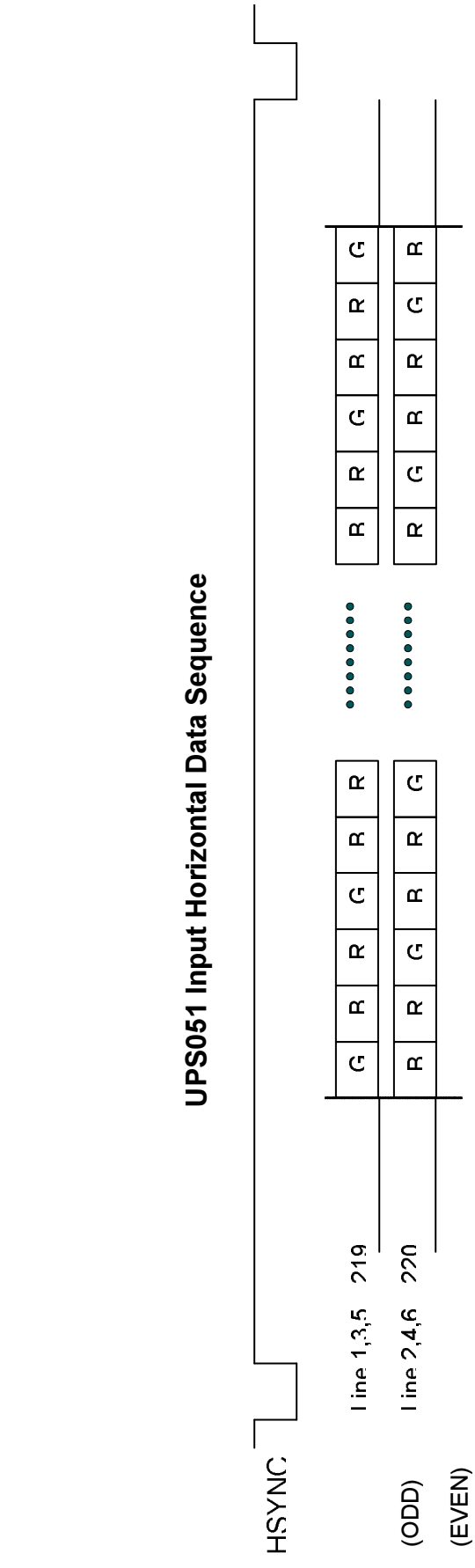
Note2: UPS051 support interlacing input format

Note3: UPS051 support non-interlacing input format. Odd field only or even field only

UPS051 Input Horizontal Timing Chart



UPS051 Input Horizontal Data Sequence



b. UPS052 Timing conditions

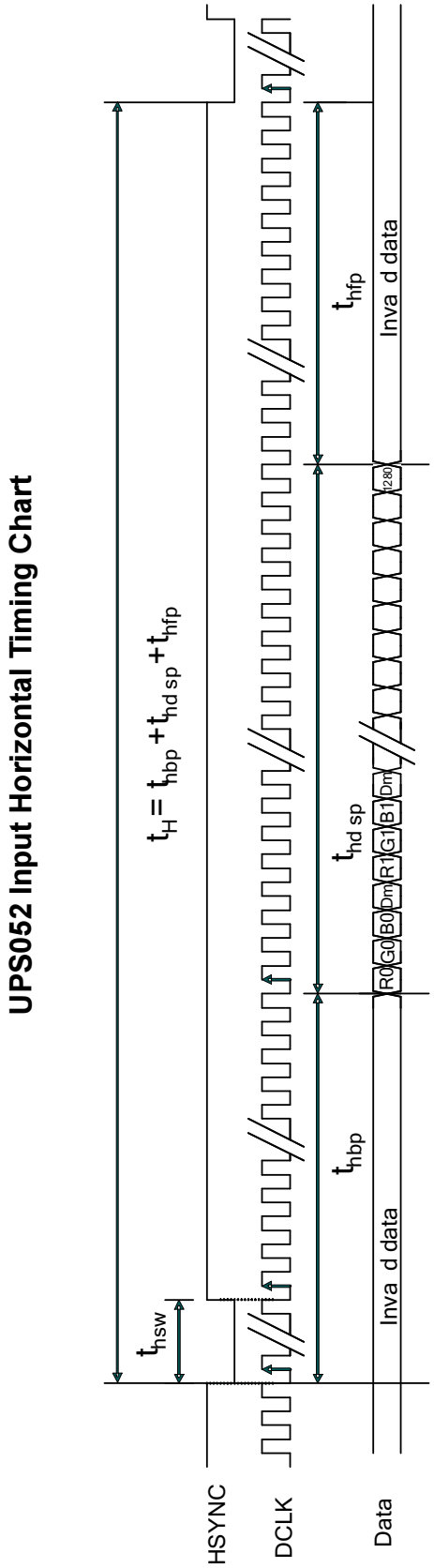
Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	23.3	24.54	25.7	MHz	
HSYNC	Period		t_H		1560		t_{DCLK}	Note1
	Display period		t_{hdisp}		1280		t_{DCLK}	
	Back porch		t_{hbp}	248	249	251	t_{DCLK}	
	Front porch		t_{hfp}	32	31	29	t_{DCLK}	
	Pulse width		t_{hsw}	1	25	56	t_{DCLK}	
VSYNC	Period	Odd	t_V	256	262.5	264	t_H	
		Even						
	Display period	Odd	t_{vdisp}		220		t_H	
		Even						
	Back porch	Odd	t_{vb}		23		t_H	Note2
		Even			23.5			
	Front porch	Odd	t_{vf}	13	19.5	21	t_H	
		Even		12.5	19	20.5		
	Pulse width	Odd	t_{vsw}	1 t_{DCLK}	3 t_H	6 t_H	-	
		Even						

Note1: Horizontal display position:

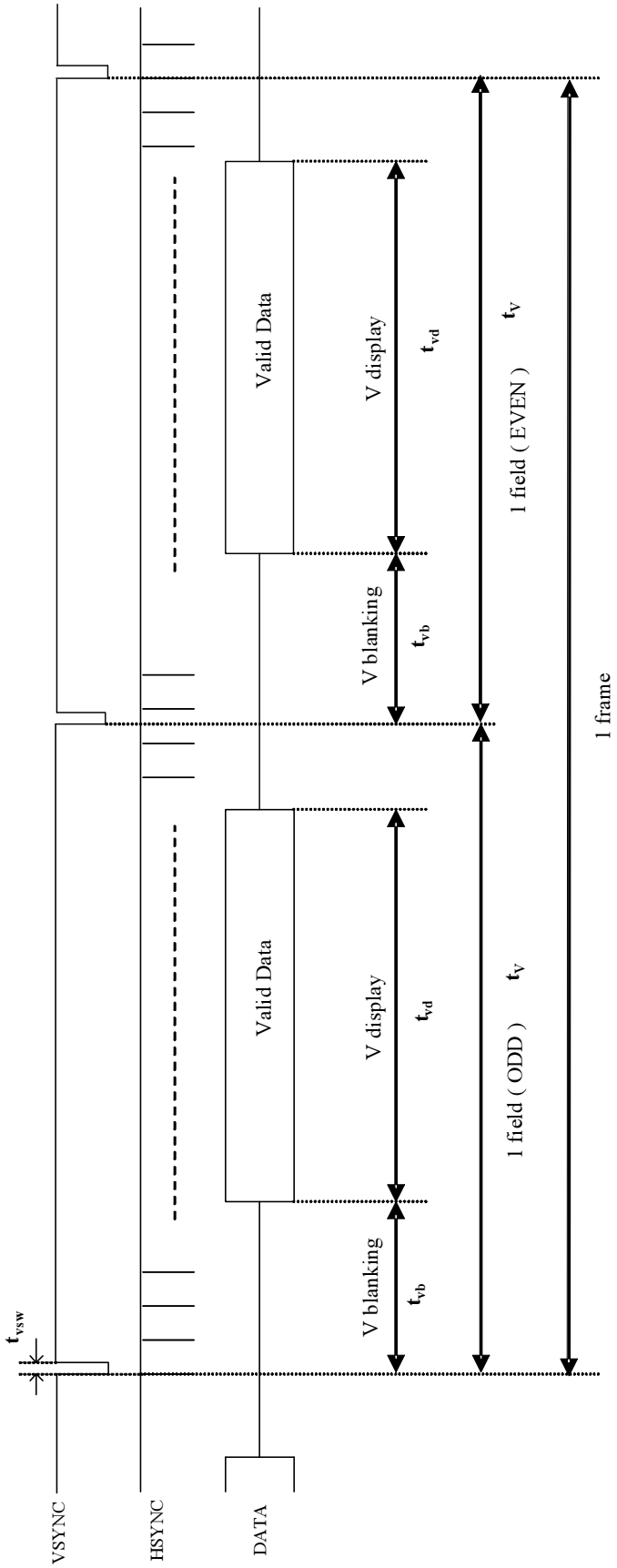
Available display starts from the data of 266 t_{DCLK} when back porch value (t_{hbp}) set 249.

Note2: UPS052 support interlacing input format

Note3: UPS052 support non-interlacing input format. Odd field only or even field only.



UPS052 Input Vertical Timing Chart



7. 3-wire serial communications

For 3-wire serial communication timing, it is shown in Fig.2. For register setting, please refer to application note.

8. DC-DC Converter Circuit

A015AN05 contains one high-power step-up DC-DC converte for active matrix TFT LCDs.

a. Charge Pump Block Diagram

The VCC Voltage is used for internal pump circuit to generate VCP/VGH/Vgoff_H/ Vgoff_L/Vcac for gate and VCOM used.

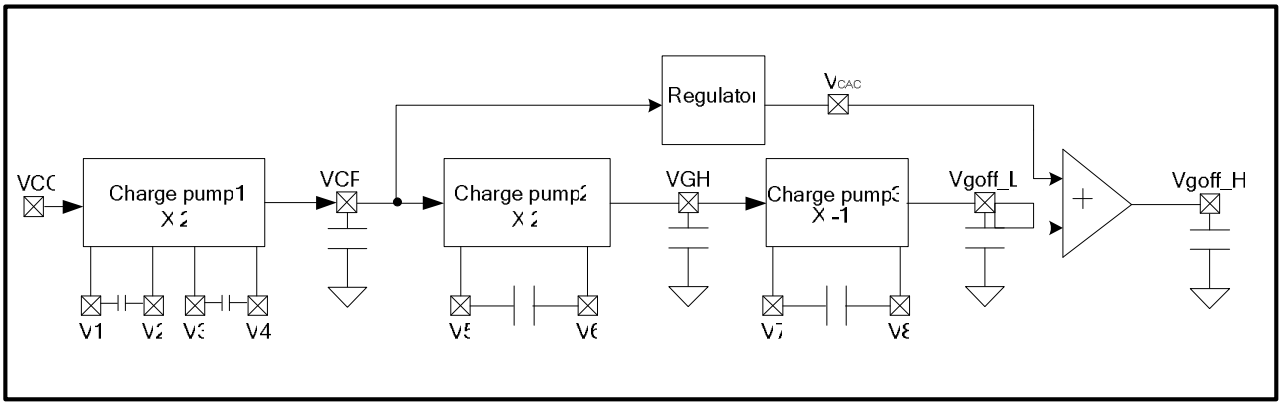


Fig. 1 charge pump diagram

C. Optical Specifications

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time Rise Fall	 Tr Tf	θ=0°	 - -	 25 30	 50 60	 ms ms	Note 4
Contrast ratio	CR	At optimized viewing angle	200	300	-		Note 5, 6
Viewing angle Top Bottom Left Right		CR□10	 40 45 50 50	 50 55 60 60	 - - - -	deg.	Note 7
Brightness (25mA)	Y_L	θ=0°	TBD	300	-	cd/m^2	Note 8
White chromaticity	X	θ=0°	TBD	(0.31)	TBD		
	y	θ=0°	TBD	(0.33)	TBD		

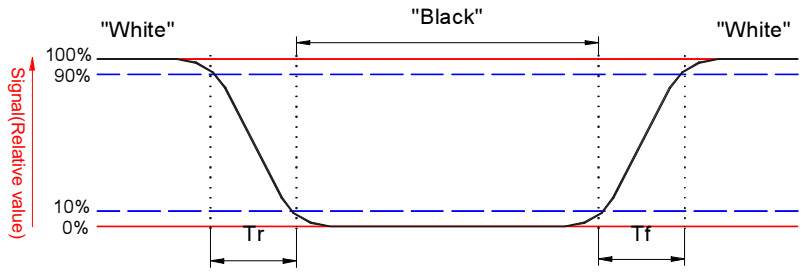
Note 1 Ambient temperature = 25□.

Note 2 Measured in the dark room

Note 3 Measured on the center area of panel with a field angle of 1° by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4 Definition of response time:

Output signals of photo detector are measured when the input signals are changed from “black” to “white” (falling time) and from “white” to “black” (rising time), respectively.



Response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to the figure as follows.

Note 5 Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6 White Vi = V_{i50} + 1.5V

Black Vi = V_{i50} ± 2.0V

“±” means that the analog input signal swings in phase with COM signal.

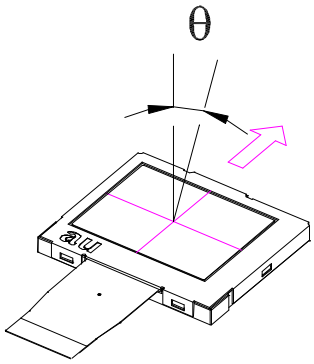
“∓” means that the analog input signal swings out of phase with COM signal.

V_{i50}: The analog input voltage when transmission is 50%

100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7 Definition of viewing angle:

Refer to the figure as follows.



Note 8 Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 9 Gray level inversion direction: 6 o'clock

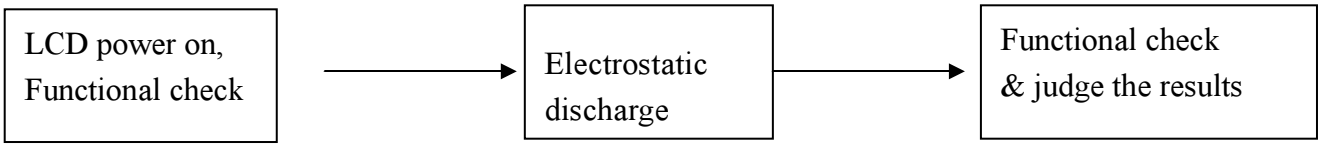
D. Reliability Test Items

No.	Test items	Conditions	Remark
1	High temperature storage	Ta = 80□ 240Hrs	
2	Low temperature storage	Ta = -25□ 240Hrs	
3	High temperature operation	Ta = 60□ 240Hrs	
4	Low temperature operation	Ta = 0□ 240Hrs	
5	High temperature and high humidity	Ta = 60□. 90% RH 240Hrs	Operation
6	Heat shock	-25□~80□, 50 cycles, 2Hrs/cycle	Non-operation
7	Electrostatic discharge	Air-mode : +/- 8kV Contact-mode : +/- 4kV	Note.2, 3
8	Vibration (with carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
9	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note1 Ta: Ambient temperature.

Make sure protection film(s) on top of polarizer or back of LCD module is/are removed before RA test.

Note2: ESD Testing Flow as the below,



Note 3. ESD testing method.

Ambient: 24~26℃, 56~65%RH

Instruments:NoisekenESS-2000,

Operation System: “CT30AA-A” and adapter “A015AN04 V5T0”

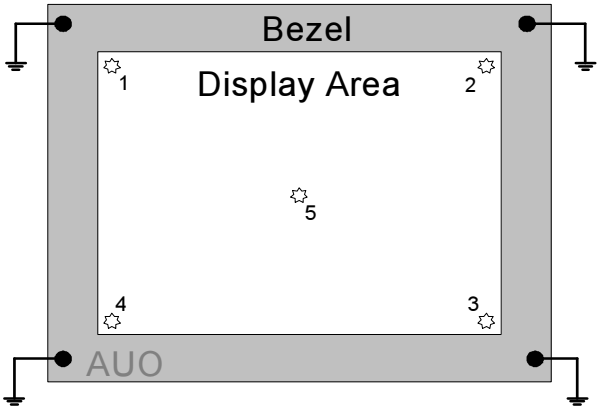
Test Mode: Operating mode, test pattern: colorbar+8Gray scale

Test Method:

Contact Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point

Air Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point

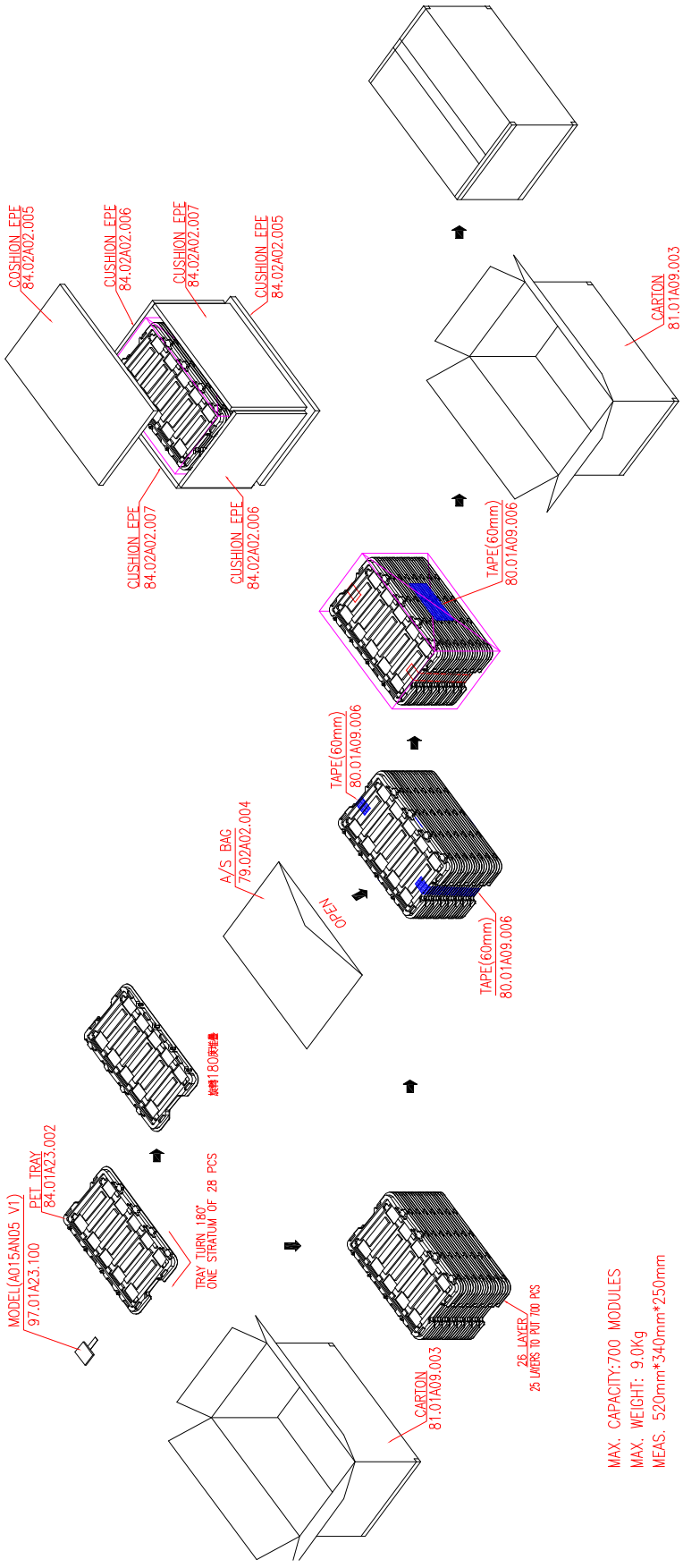
Test point:



The metal casing is connected to power supply ground (0V) at four corners.

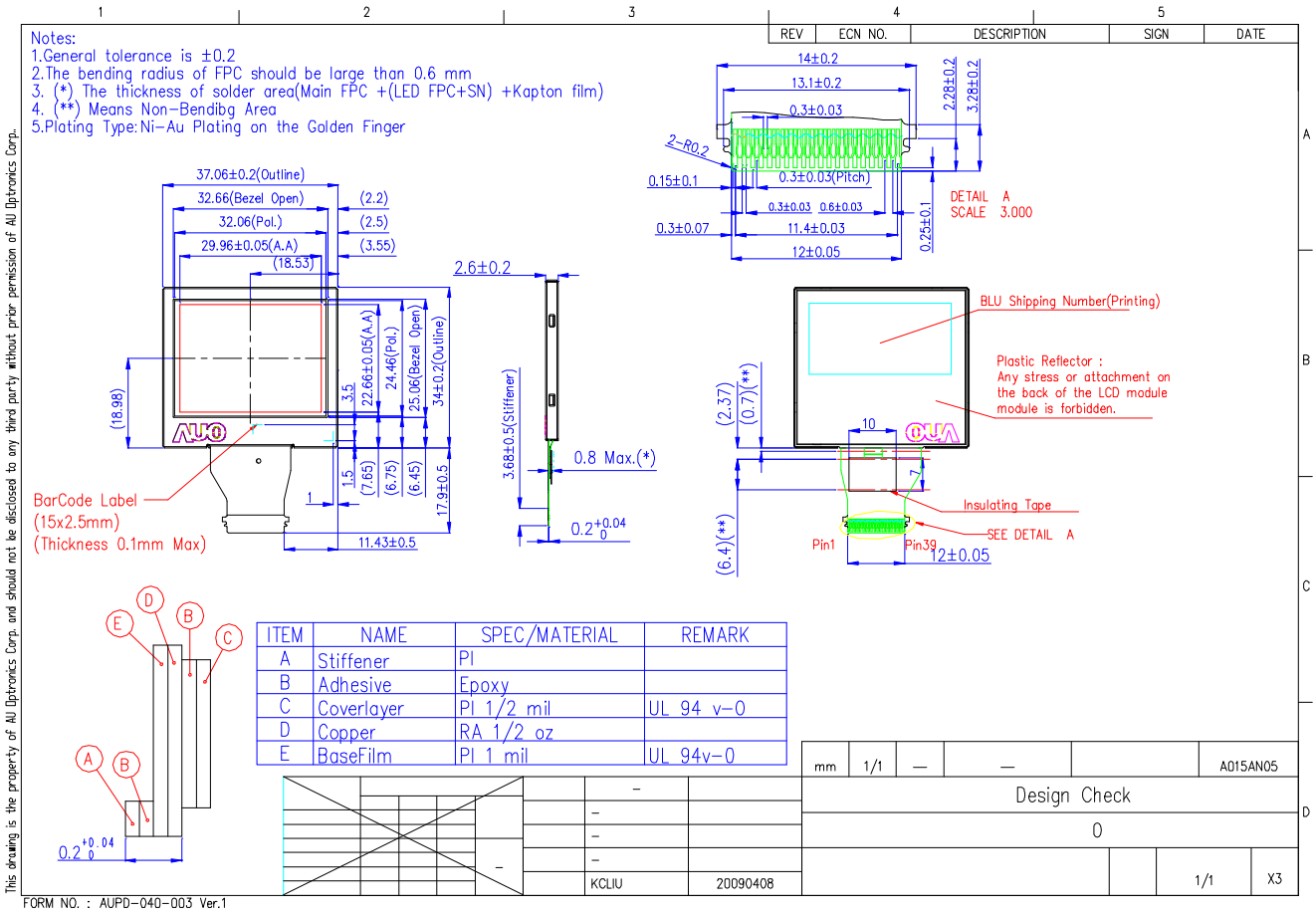
All register commands are repeating transfer.

E. Packing Form



F. Outline drawing

Note: Any stress or attachment on the back of the LCD module is forbidden.



G. Appendix

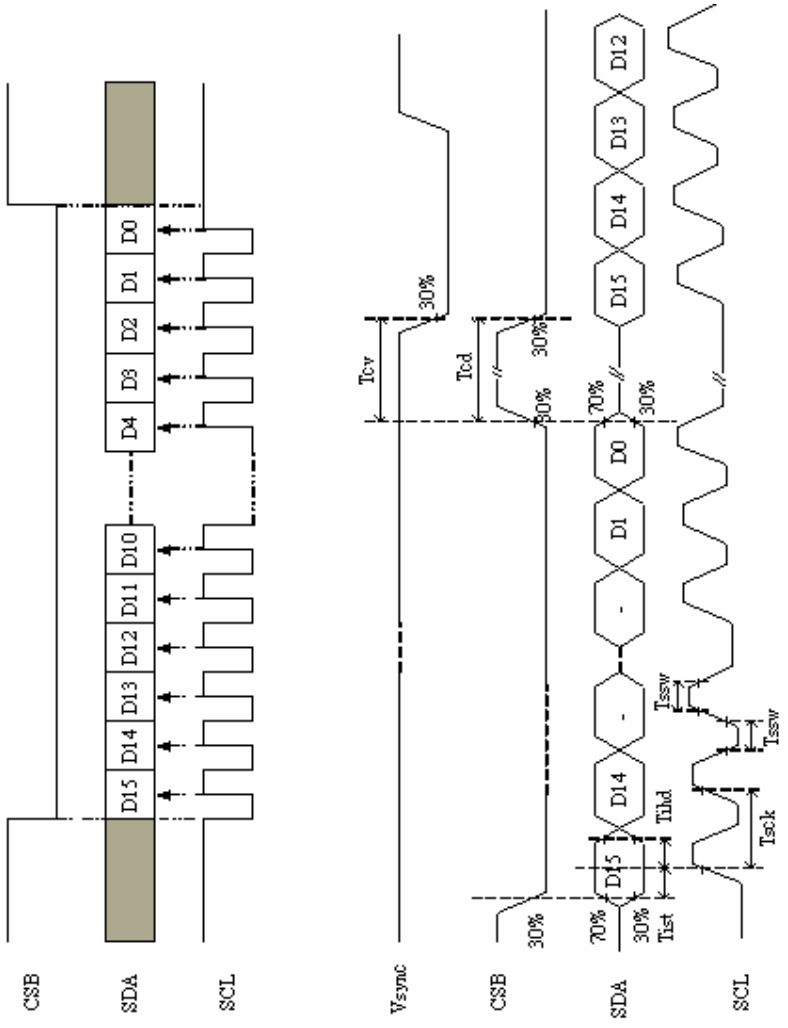


Fig. 2 3-wire programming function timing

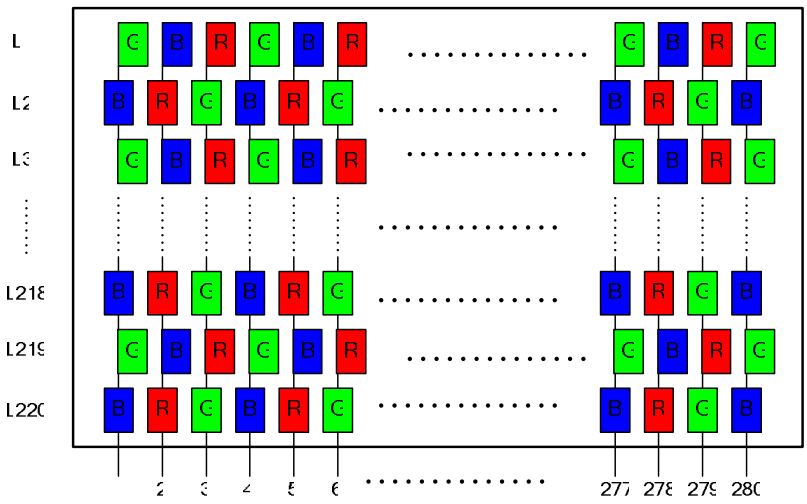


Fig. 5 Outline dimension of TFT-LCD module

Fig. 3 Panel color Filter Alignment

H. Suggested Application Note

A015AN05 is designed with smart integration advance (SIA) concept for DSC application. This panel integrated not only source driver & gate driver, but also built in power generator and embedded serial communication interface for the function setting.

A015AN05 is supported by two kinds of input timing format: UPS051 and UPS052. Customers can use 3-wire serial port for setting register and select different timing for their own design feature.

In this document, we list essential parameters for configuration. Please follow our recommend setting to achieve the best performance. In the last page, we provide application circuit to drive A015AN05.

For A015AN05 driving circuit design, you just need input one set of power 3.3V, because the charge-pump circuit inside the driver IC produces Vgh & Vgl. The external peripheral is very simple and good for saving BOM cost for customers.

1. 3-wire serial communication AC timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Serial clock	Tsck	320	-		ns
SCL pulse duty	Tscw	40	50	60	%
Serial data setup time	Tist	120	-	-	ns
Serial data hold time	Tiht	120	-	-	ns
Serial clock high/low	Tssw	120	-	-	ns
Chip select distinguish	Tcd	1	-	-	us
Time that the CSB to Vsync	Tcv	1	-	-	us

2. The configuration of serial data at SDA terminal is at below

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register address				DATA											

3. Recommend register table for UPS051 timing

		Address															
No.	Description	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	Scan direction	0	0	0	0	0	X	X	X	X	X	X	X	X	X	0	1
R1	Data setting	0	0	1	0	0	X	X	X	X	X	X	X	X	X	0	0
R2	Source IC setting	0	1	0	0	0	X	X	X	X	X	X	X	1	1	0	0
R3	Timing select	0	1	1	0	0	X	X	X	X	X	X	X	X	0	0	0
R4	VCAC level setting	1	0	0	0	0	X	X	X	X	X	X	X	X	1	1	0
R5	HBLK setting	1	0	1	0	0	X	X	X	X	X	X	X	X	X	0	0
T0	DRV setting	0	0	0	1	0	X	X	X	X	1	1	0	0	0	0	0

“X” =>Don’t care

4. Recommend register table for UPS052 timing

		Address															
No.	Description	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	Scan direction	0	0	0	0	0	X	X	X	X	X	X	X	X	X	0	1
R1	Data setting	0	0	1	0	0	X	X	X	X	X	X	X	X	X	0	1
R2	Source IC setting	0	1	0	0	0	X	X	X	X	X	X	X	1	1	0	0
R3	Timing select	0	1	1	0	0	X	X	X	X	X	X	X	X	0	0	1
R4	VCAC level setting	1	0	0	0	0	X	X	X	X	X	X	X	X	1	1	0
R5	HBLK setting	1	0	1	0	0	X	X	X	X	X	X	X	X	X	0	0
T0	DRV setting	0	0	0	1	0	X	X	X	X	1	1	0	0	0	0	0

“X”=>Don’t care

5. Register detail description

a. Register R0

Bit	Function
D0	Up/down scan direction: “0” => Down to up “1” => Up to down
D1	Left/Right scan direction: “0” => Left to right “1” =>Right to left

b. Register R1

Bit	Function
D0	“0” =>When UPS051 mode selected “1” =>When UPS052 mode selected
D1	Always fixed at “0”

c. Register R2

Bit	Function
D0	Always fixed at “0”
D1	Always fixed at “0”
D2	Standby mode setting: “0” => Turn off driver & DCDC “1” => Normal operating
D3	Global reset setting: “0” =>Driver control register is in reset state, all setting to default value. “1” =>Normal operating;

d. Register R3

Bit	Function
D0	“0” => To select UPS051 timing “1” => To select UPS052 timing
D1	Always fixed at “0”
D2	Always fixed at “0”

e. Register R4 ＊

Bit	Function
D0	Always fixed at “0”
D1	Always fixed at “1”
D2	Always fixed at “1”

＊ Set VCOM AC level = 5.6V (Amplitude)

f. Register R5

Bit	Function			
D1~D0	Select the horizontal input delay timing			
	DL1	DL0	NO.	Level
	0	0	+0	Unit: DCLK
	0	1	-1	
	1	0	+1	
	1	1	+2	

g. Register T0

Bit	Function
D4	PWM shutdown control circuit setting “0” => PWM control circuit will be shut down. “1” => PWM control circuit normal operation. (Default)
D5	Charge pump shutdown setting “0” => Charge pump will be shut down. “1” => Charge pump normal operation. (Default)
D6	Internal charge pump structure select “0” => Charge pump input voltage disable. (Default) “1” => Charge pump input voltage enable.

Suggested reference application circuit

External LED circuit

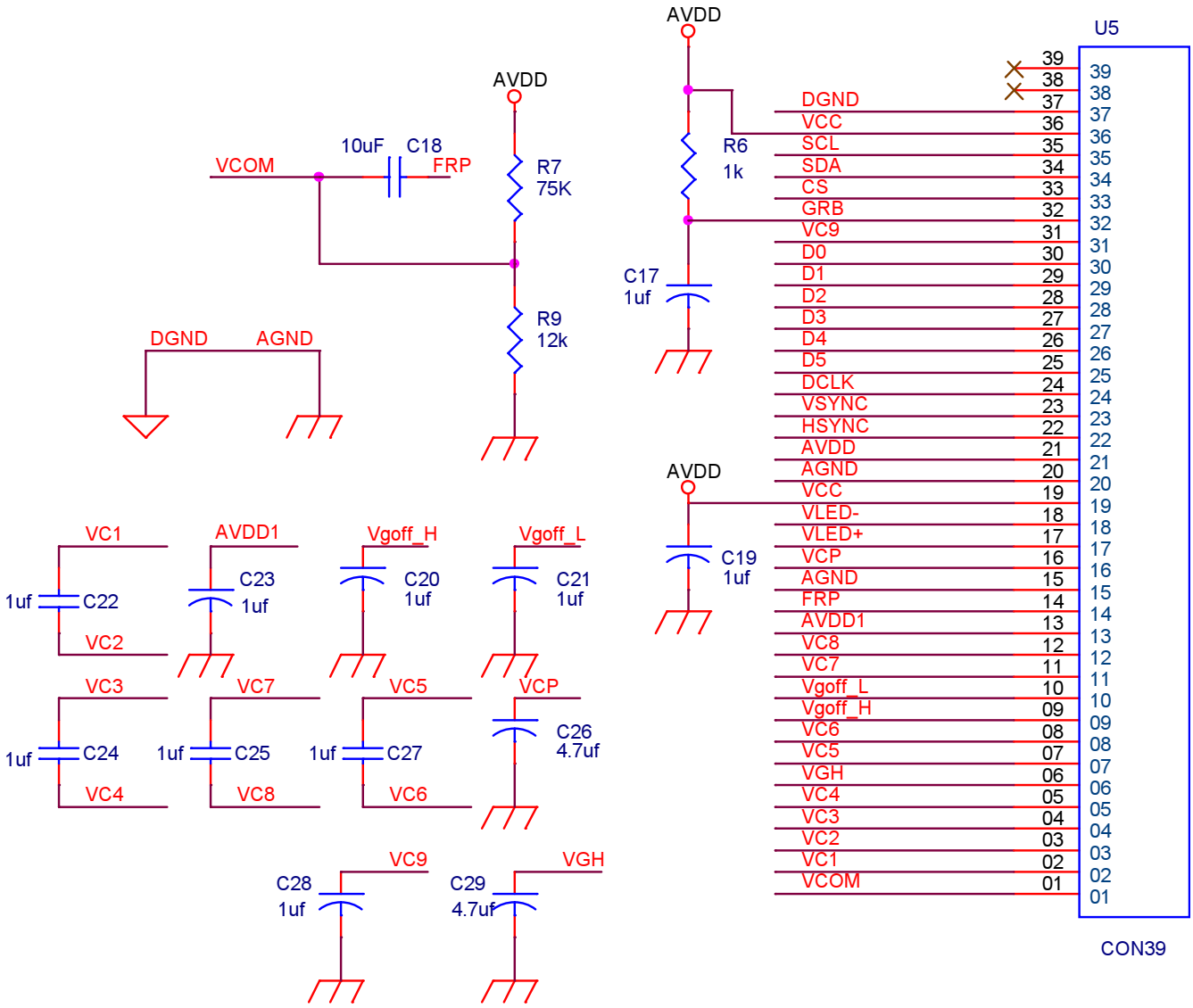


Fig. 9 External LED driver Circuit

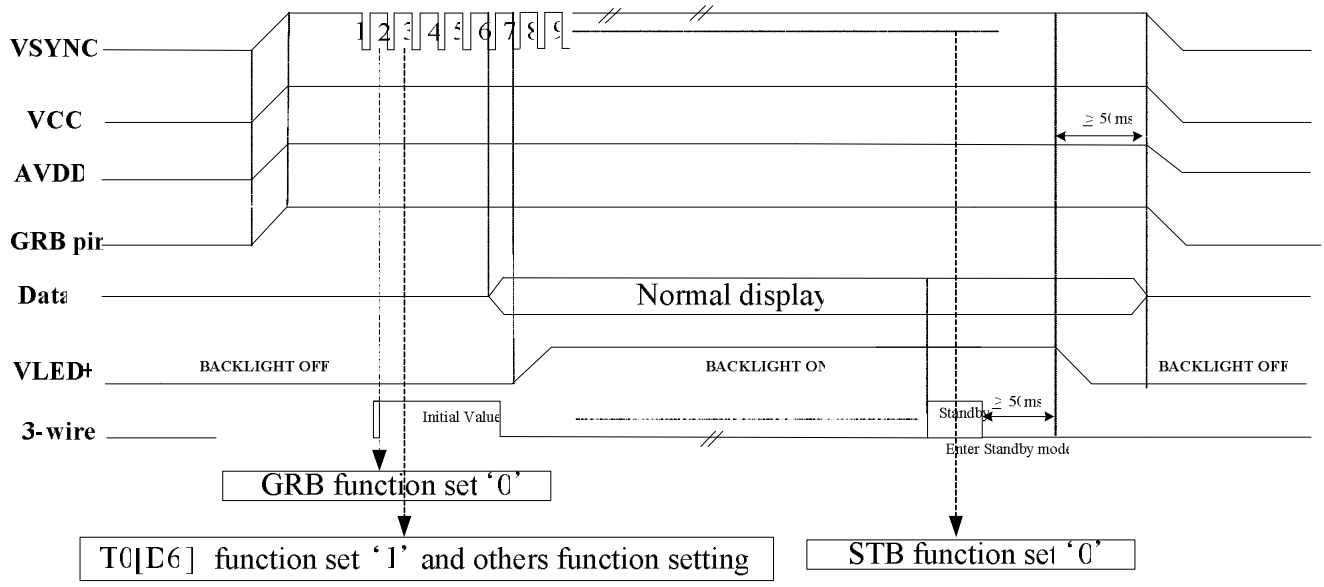
Note:

Please refer to suggestion power and standby on/off sequence.

Power supply VCC (typical 3.3V) and AVDD (typical 3.3V) are required to provide driver IC power and generate all necessary voltages for LCD related circuits.

We recommend the external LED driver circuit provide a constant 25mA for LED backlight unit.We suggest SPI setting must be turn off DRV signal.The capacitors of C28 will be used shrinkage IC.

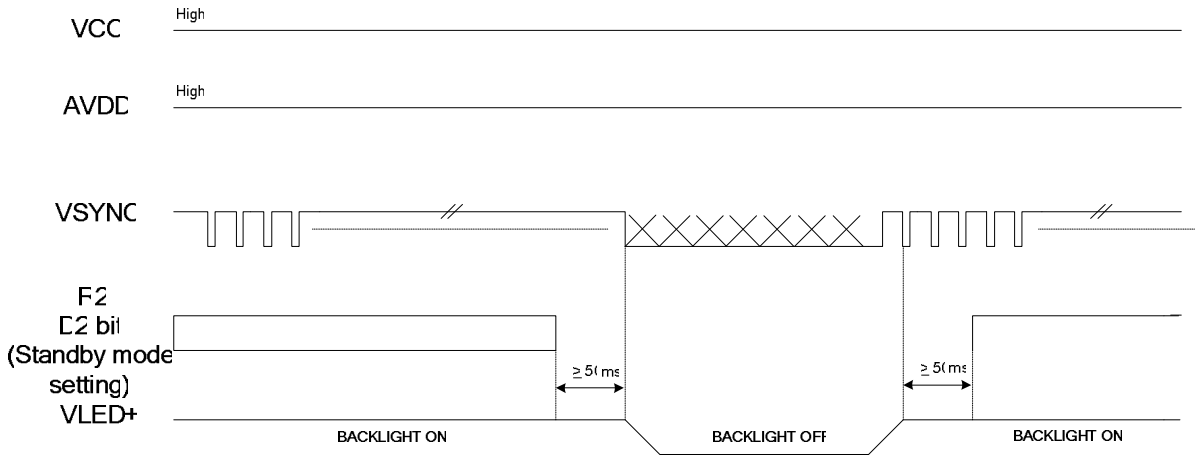
Suggestion power on/off sequence



We recommend power on/off sequence that base on application circuit to make sure power on/off function can work successfully in every time power on.

Note: In standby mode, VSYNC signal will don't care, but we suggestion VSYNC is disable.

Suggestion Standby on/off sequence



Note: xx means don't care this signal.

We recommend standby on/off sequence that base on application circuit to make sure function can work successfully.