Doc. version:	1.3
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Product Specification

2.36″ COLOR TFT-LCD MODULE

MODEL NAME: A024CN00 V2

< ◆ > Preliminary Specification

< > Final Specification

Note: The content of this specification is subject to change without prior notice.

Record of Revision

Version	Revise Date	Page	Content
1	AUG/31/2004		First draft
1.1	NOV/09/2004	4	N0.8 Panel surface treatment Revise AG to Glare
		21	Revise Viewing angle Left min from 45 to 40 Viewing angle Right min from 45 to 40
		24	Change E. Packing form
		25	Fig2 outline dimension of TFT_LCD module(add FPC UL mark)
		25	Notice for backlight design and assembly
1.2	NOV/23/2004	25	Fig2 outline dimension of TFT_LCD module update
1.3	JAN/11/2006	25	Update outline dimension of TFT_LCD module(revise FPC UL mark)

Contents:

A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution (dot)	480(W)×234(H)	
2	Active area (mm)	48.0 (W) × 35.685 (H)	
3	Screen size (inch)	2.36 (Diagonal)	
4	Dot pitch (mm)	0.10 (W) × 0.1525 (H)	
5	Color configuration	R. G. B. delta	
6	Overall dimension (mm)	52.9 (W) × 43.73 (H) × 1.54 (D)	Note 1
7	Weight (g)	TBD	
8	Panel surface treatment	Glare, Hard coating, LR(Low Reflection)	

Note 1: Refer to Fig. 1

B. Electrical specifications

1.Pin assignment (please note: the pin assignments are tentative, subject to change prior to

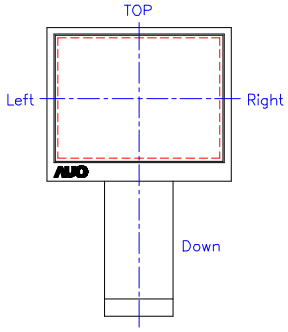
Pin no	Symbol	I/O	Description	Remark
1	DRV	VO	Power transistor gate signal for the boost converter	
2	FB	VI	Main boost regulator feedback input	
3	ADJ0	I	PLL adjustment Pin0	
4	ADJ1	I	PLL adjustment Pin1	
5	PVDD	P	Power supply for PLL circuits (3.3v)	
6	NC	D	No connection	
7	PGND	P	Ground pin for PLL circuits	
8	NC	D	No connection	
9	VA	I	Video R input signal	
10	VB	I	Video G input signal	
11	VC	I	Video B input signal	
12	SCL	I	Serial communication clock input	
13	SDA	I	Serial communication data input	
14	CSB	I	Serial communication chip select	
15	GRB	I	Global reset pin	
16	VSYNC	I	Vertical sync input. Negative polarity	
17	HSYNC	I	Horizontal sync input. Negative polarity	
18	DFRP	O	Digital Frame polarity output signal	
19	AGND	C	Ground pin for source driver	
20	NC	D	No connection	
21	VCI_OUT	C	Power supply for source driver	
22	VCC	P	System power (3.3v)	
23	NC	D	No connection	
24	GND	P	System ground	
25	C1+	C	Power setting capacitor connect pin	
26	C1-	C		
27	C12+	C		
28	C12-	C		
29	C8+	C		
30	C8-	C		

Pin no	Symbol	I/O	Description	Remark
31	V3	C	Power setting capacitor connect pin	
32	C31+	C		
33	C31-	C		
34	APOL	O	Frame polarity output signal for panel VCOM	
35	VCAC	C	APOL level supply	
36	VGH	C	VGH turn on voltage	
37	VGL	C	Power setting capacitor connect pin	
38	VGoffL	C	VGL turn off voltage	
39	VGoffH	C	VGL+VCOM	
40	VCOMR	I	Adjust VCOM DC voltage	

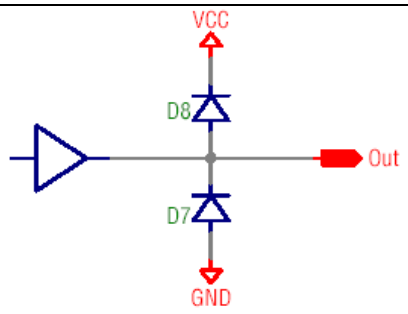
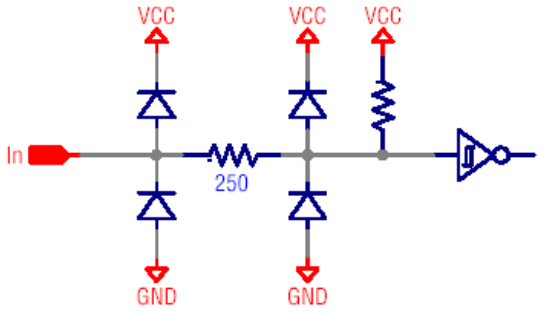
Illustration of I/O symbol

I: Input. O: Output. VI: voltage input. VO: voltage output. P: Power. C: Capacitor pin. D: Dummy.

Note 1: Please refer to figure below for the definition of scanning direction.



2. Equivalent circuit of I/O

Pin no & Pin name	Schematics
1.DRV	
15.GRB	

3. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	V_{CC}	GND=0	-0.5	5.	V	
	AV_{DD}	AV_{SS}=0	-0.5	5.5	V	
Input signal voltage	VCOM		-2.9	5.2	V	
Operating temperature	Topa		0	70	℃	Ambient temperature
Storage temperature	Tstg		-25	80	℃	Ambient temperature

4. Electrical characteristics

a. Typical operating conditions (GND=PGND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply	VCC	2.7	3.3	3.6	V	
	PVDD	2.7	3.3	3.6	V	
	VGH	11.5	14	15	V	Note1.
	VGL	-13,5	-12	-11.5	V	Note1.
	Vgoff_L	-13.5	-12	-11.5	V	Note1.
	Vgoff_H	-9.1	-6.4	-5.7	V	Note1.
	VCI_OUT	4.8	5	5.5	V	Note1.

Video signal Amplitude (VR,VG,VB)		ViA	0.2		5.0		
		ViAC		3			AC Component
		ViDC		2.5			DC Component
		VI_high			4.8		Note 2.
Output Signal voltage	H Level	V_{OH}	Vcc-0.4				
	L Level	V_{OL}	GND		GND+0.4		
Input Signal voltage	H Level	V_{IH}	$0.7V_{CC}$	-	V_{CC}	V	
	L Level	V_{IL}	GND	-	$0.3V_{CC}$	V	
Output current	H Level	IOH		10		uA	
	L Level	IOL		-10		uA	
Analog stand by current		Ist			200	uA	DCLK is stopped
VCOM		V_{CAC}	4.4	5.6	5.8	Vp-p	AC component
		V_{CDC}		1.1		V	DC component

Note 1. These voltages (VGH,VGL,VgoffH,VgoffL,VCI_OUT) are related to input voltage VCC.
Note 2. The R,G,B maximum input voltage can not higher than 4.8 volt.

b. Current consumption (GND=AVss=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
	I_{CC}	V_{CC}=3.3V	-	2	2.5	mA	
	I_{DD}	AV_{DD}=3.3V	-	1.5	2.0	mA	

5. AC Timing

a. NTSC:

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Clock period time	t_{OSC}	94	103	114	ns	
Hsync period time	T_{Hs}	61.5	63.5	65.5	**u**s	
Vsync pulse width	Twvs	1	-	260	Hs	
Vsync to Hsync timing	Tvshs	0			**ns**	Note1
Hsync to Vsync timing	Thsvs	0			**ns**	
Vsync to STV input time	Tvs	5	17	24	**Hs**	ref to Fig. 6
Horizontal lines per field		256	262.5	268	line	Note 2

b. PAL:

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Clock period time	t_{OSC}	94	103	114	ns	
Hsync period time	T_{Hs}	62	64	66	us	
Vsync pulse width	Twvs	1	-	260	Hs	
Vsync to Hsync timing	Tvshs	0			ns	Note1
Hsync to Vsync timing	Thsvs	0			ns	
Vsync to STV input time	Tvs	12	24	31	Hs	ref to Fig. 6
Horizontal lines per field		306	312.5	318	line	Note 2

Note 1: Vsync and Hsync both support rising edge or falling edge timing

Note 2: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

c. Horizontal Timing:

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Hsync frequency	Fhs	-	15.7k	-	**Hz**	
Hsync pulse width time	Twhs	5	44	600	Tclk	
Hsync to DFRP change time	Thsdfrp	-	40	-	Tclk	
Hsync to APOL change time	Thsapol	-	40	-	Tclk	

Refer to Figure 3.

d. 3-wire serial communication AC timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Serial clock	Tsck	300	1		ns
SCL pulse duty	Tscw	40	50	60	%
CSB hold time	Tcst	120			ns
Serial data setup time	Tist	120			ns
Serial data hold time	Tiht	120			ns
Serial clock high/low	Tssw	120			ns
Chip select distinguish	Tcd	1			us
CSB to Vsync Time	Tcv	1			us

Refer to Figure 5.

6. The configuration of serial data at SDA terminal is at below

	MSB															LSB		
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		
	Address			X	DATA													
No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description	default
R0	0	0	0	X	X	X	X	X	X	X	X	X	X	0	0	0	Select relationship between the inputs VA, VB, VC and outputs R, G, B.	V
				X	X	X	X	X	X	X	X	X	X	0	0	1		
				X	X	X	X	X	X	X	X	X	X	0	1	0		
				X	X	X	X	X	X	X	X	X	X	1	0	0		
R1	0	0	1	X	X	X	X	X	X	X	X	X	0	0	0	0	Up to down	V
				X	X	X	X	X	X	X	X	X	0	0	0	1	Down to up	
				X	X	X	X	X	X	X	X	X	0	0	0	0	Right to left	
				X	X	X	X	X	X	X	X	X	0	0	1	0	Left to right	V
				X	X	X	X	X	X	X	X	X	0	0	0	0	In reset state	
				X	X	X	X	X	X	X	X	X	0	1	0	0	Normal	V
				X	X	X	X	X	X	X	X	X	0	0	0	0	In standby mode	
				X	X	X	X	X	X	X	X	X	1	0	0	0	Normal	V
R2	0	1	0	X	X	X	X	X	X	X	X	0	0	0	0	0	Set horizontal position	V
				X	X	X	X	X	X	X	X	0	0	0	0	1		
				X	X	X	X	X	X	X	X	0	0	0	1	0		
				X	X	X	X	X	X	X	X	0	0	1	0	0		
				X	X	X	X	X	X	X	X	0	1	0	0	0		
				X	X	X	X	X	X	X	X	1	0	0	0	0		
R3	0	1	1	X	X	X	X	X	X	X	X	0	0	0	0	0	Set vertical position	V
				X	X	X	X	X	X	X	X	0	0	0	0	1		
				X	X	X	X	X	X	X	X	0	0	0	1	0		
				X	X	X	X	X	X	X	X	0	0	1	0	0		
				X	X	X	X	X	X	X	X	0	1	0	0	0		
				X	X	X	X	X	X	X	X	1	0	0	0	0		
R4	1	0	0	X	X	X	X	X	X	X	X	X	0	1	1	0	Adjust the VCOM AC level	V
				X	X	X	X	X	X	X	X	X	0	0	0	1		
				X	X	X	X	X	X	X	X	X	0	0	1	0		
				X	X	X	X	X	X	X	X	X	0	1	0	0		
				X	X	X	X	X	X	X	X	X	0	0	0	0	The APOL polarity, the same as DFRP.	V
				X	X	X	X	X	X	X	X	X	1	0	0	0	The APOL polarity will be inverted.	

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description	default
	Address			X	DATA													
R5	1	0	1	X	X	X	X	X	X	X	X	X	0	0	0	0	Data format selected by D1.	
				X	X	X	X	X	X	X	X	X	0	0	0	1	Data format auto selection.	v
				X	X	X	X	X	X	X	X	X	0	0	0	0	NTSC	v
				X	X	X	X	X	X	X	X	X	0	0	1	0	PAL	
				X	X	X	X	X	X	X	X	X	0	0	0	0	Normally display	v
				X	X	X	X	X	X	X	X	X	0	1	0	0	16:9 wide display	
				X	X	X	X	X	X	X	X	X	0	0	0	0	Hsync and Vsync input Positive polarity	v
				X	X	X	X	X	X	X	X	X	1	0	0	0	Hsync and Vsync input Negative polarity	
R6	1	1	0	X	X	X	X	X	X	X	X	0	0	0	0	0	PWM control circuit is shut down.	v
				X	X	X	X	X	X	X	X	0	0	0	0	1	PWM circuit is working.	
				X	X	X	X	X	X	X	X	0	0	0	0	0	PLL is working.	v
				X	X	X	X	X	X	X	X	0	0	0	1	0	PLL is disabled.	
				X	X	X	X	X	X	X	X	1	0	0	0	0	PLL freq. Selection: NTSC default (594 clk/line)	v
				X	X	X	X	X	X	X	X	0	1	1	0	0	PAL default (616 clk/line)	

"X" => Don't care.

Register detail description

Register **R0**:

Control and switch the relationship between the inputs VA, VB, VC and outputs R, G, B. This function is used to match different types of color filters.

D2	D1	D0	Output (n=1 to 160)			
			R	G	B	
0	0	0	R	G	B	Odd Line
			G	B	R	Even Line
0	0	1	G	B	R	Odd Line
			B	R	G	Even Line
0	1	X	B	R	G	Odd Line
			R	G	B	Even Line
1	0	0	R	G	B	Odd Line
			B	R	G	Even Line
1	0	1	G	B	R	Odd Line
			R	G	B	Even Line
1	1	X	B	R	G	Odd Line
			G	B	R	Even Line

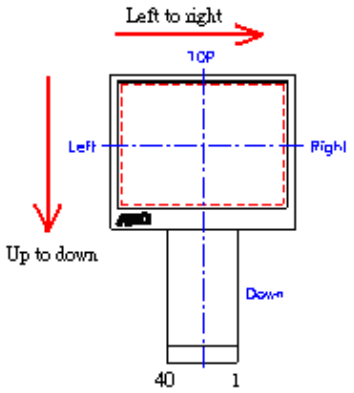
"X" => Regardless

Register **R1**:

Set the scan direction, reset, and standby mode.

Bit	Function
D0	Up/down scan direction. “1”=> Down to up. “0”=> Up to down (Default).
D1	Left/Right scan direction. “1”=> Left to right. (Default) “0”=>Right to left.
D2	Global reset pin, it should be connected to VCC in normal operation. IF connected to GND, the controller is in reset state, normally pulled high.
D3	Standby mode, active low. Normally pulled high.

Default scan direction is below:



Register **R2**:

Set the horizontal position adjustment timing.

D4	D3	D2	D1	D0	NO.	Unit
0	0	0	0	0	Default	DCLK
0	0	0	0	1	+1	
0	0	0	1	0	+2	
0	0	0	1	1	+3	
0	0	1	0	0	+4	
0	0	1	0	1	+5	
0	0	1	1	0	+6	
0	0	1	1	1	+7	
0	1	0	0	0	+8	
0	1	0	0	1	+9	
0	1	0	1	0	+10	
0	1	0	1	1	+11	
0	1	1	0	0	+12	
0	1	1	0	1	+13	
0	1	1	1	0	+14	
0	1	1	1	1	+15	
1	0	0	0	0	-16	
1	0	0	0	1	-15	
1	0	0	1	0	-14	
1	0	0	1	1	-13	
1	0	1	0	0	-12	
1	0	1	0	1	-11	
1	0	1	1	0	-10	
1	0	1	1	1	-9	
1	1	0	0	0	-8	
1	1	0	0	1	-7	
1	1	0	1	0	-6	
1	1	0	1	1	-5	
1	1	1	0	0	-4	
1	1	1	0	1	-3	
1	1	1	1	0	-2	
1	1	1	1	1	-1	

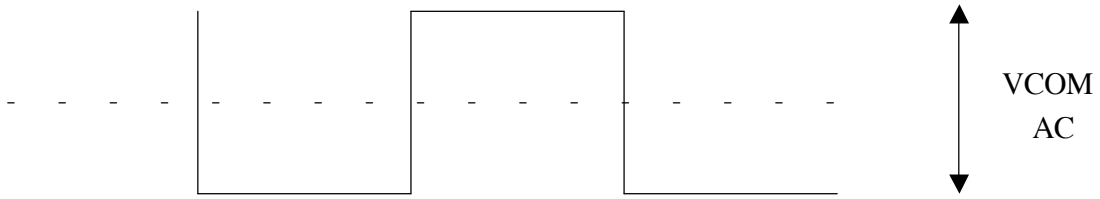
Register **R3**:

Set the vertical position adjustment timing.

D4	D3	D2	D1	D0	NO.	Unit
0	0	0	0	0	Default	H
0	0	0	0	1	+1	
0	0	0	1	0	+2	
0	0	0	1	1	+3	
0	0	1	0	0	+4	
0	0	1	0	1	+5	
0	0	1	1	0	+6	
0	0	1	1	1	+7	
0	1	0	0	0	X	
0	1	0	0	1	X	
0	1	0	1	0	X	
0	1	0	1	1	X	
0	1	1	0	0	X	
0	1	1	0	1	X	
0	1	1	1	0	X	
0	1	1	1	1	X	
1	0	0	0	0	X	
1	0	0	0	1	X	
1	0	0	1	0	X	
1	0	0	1	1	X	
1	0	1	0	0	-12	
1	0	1	0	1	-11	
1	0	1	1	0	-10	
1	0	1	1	1	-9	
1	1	0	0	0	-8	
1	1	0	0	1	-7	
1	1	0	1	0	-6	
1	1	0	1	1	-5	
1	1	1	0	0	-4	
1	1	1	0	1	-3	
1	1	1	1	0	-2	
1	1	1	1	1	-1	

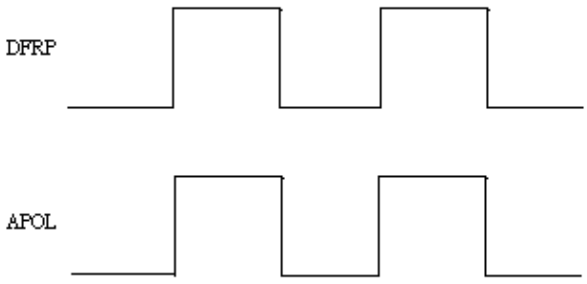
Register **R4**:

D0~D2: Adjust the VCOM AC level.

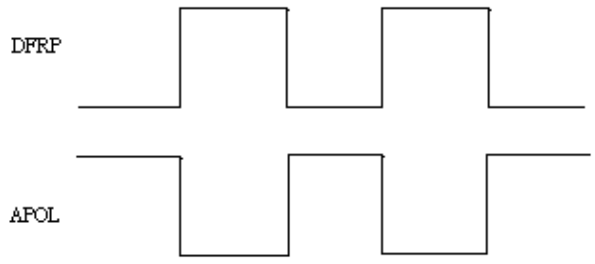


VCAC level setting (Unit: V)			
D2	D1	D0	Level
0	0	0	4.4
0	0	1	4.6
0	1	0	4.8
0	1	1	5.0
1	0	0	5.2
1	0	1	5.4
1	1	0	5.6(Default)
1	1	1	5.8

D3: Set the polarity of APOL. If D3=0, then the polarity of APOL is the same as the polarity of DFRP. As below:



If D3=1, then the polarity of APOL is inverted. As below:



D3	Control APOL are inverted or not, normally pulled low. '0'=>The APOL polarity, the same as DFRP, is negative at the first line. '1'=>The APOL polarity will be inverted.

Register **R5**:

In this register, the input format of NTSC/PAL is setting here. It would be set by AUTO-selection of external setting. Apart from this 4:3 mode to 16:9 mode is also setting be D2 bit. And the sync polarity could be set by positive and negative.

Bit	Function
D0	Data format auto selection pin, normally pulled high. '1'=>Data format is auto selection. '0'=>Data format is decided by D1.
D1	Data format selection pin, normally pulled low. '1'=>PAL. '0'=>NTSC.
D2	Wide display format selection pin, normally pulled low. '1'=>16:9 wide display. '0'=>Normally display.
D3	Horizontal and vertical sync edge selection, normally pulled low. '0'=>Horizontal and vertical sync input. Positive polarity. '1'=> Horizontal and vertical sync input. Negative polarity.

Register **R6**

In this register, PLL clock is generated by internal synchronize signal. And the PLL frequency can be set to adjust 4:3 circle ratio.

Bit	Function
D0	Shut down pin for PWM control circuit, normally pulled low. '1'=>PWM control circuit is working normally.. '0'=>PWM control circuit is shut down..
D1	Disable PLL pin, normally pulled low. '1'=>PLL is disabled and CLK must be input externally. '0'=>CLK is generated by PLL.
D2,D3,D4	PLL frequency selection. Note 3.

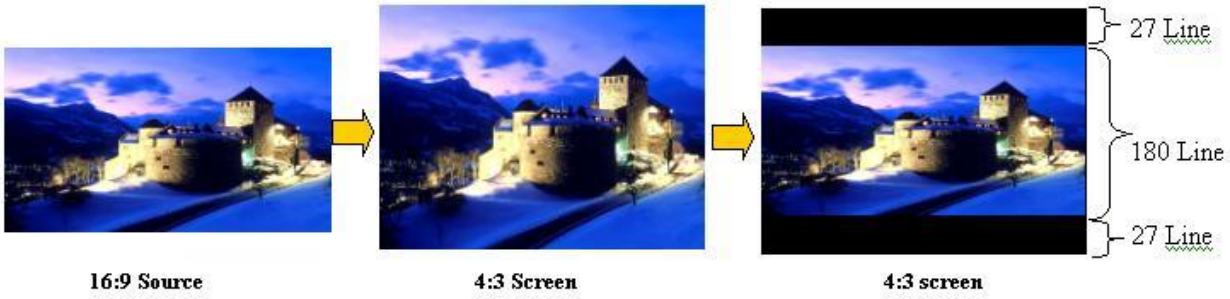
D4	D3	D2	clk/line	freq.	Unit	Condition
0	0	0	610	9.607	MHz	Hsync frequency 15.75kHz
0	0	1	612	9.639		
0	1	0	614	9.670		
0	1	1	616	9.702		
1	0	0	594 (default)	9.355		
1	0	1	597	9.402		
1	1	0	598	9.418		
1	1	1	600	9.450		

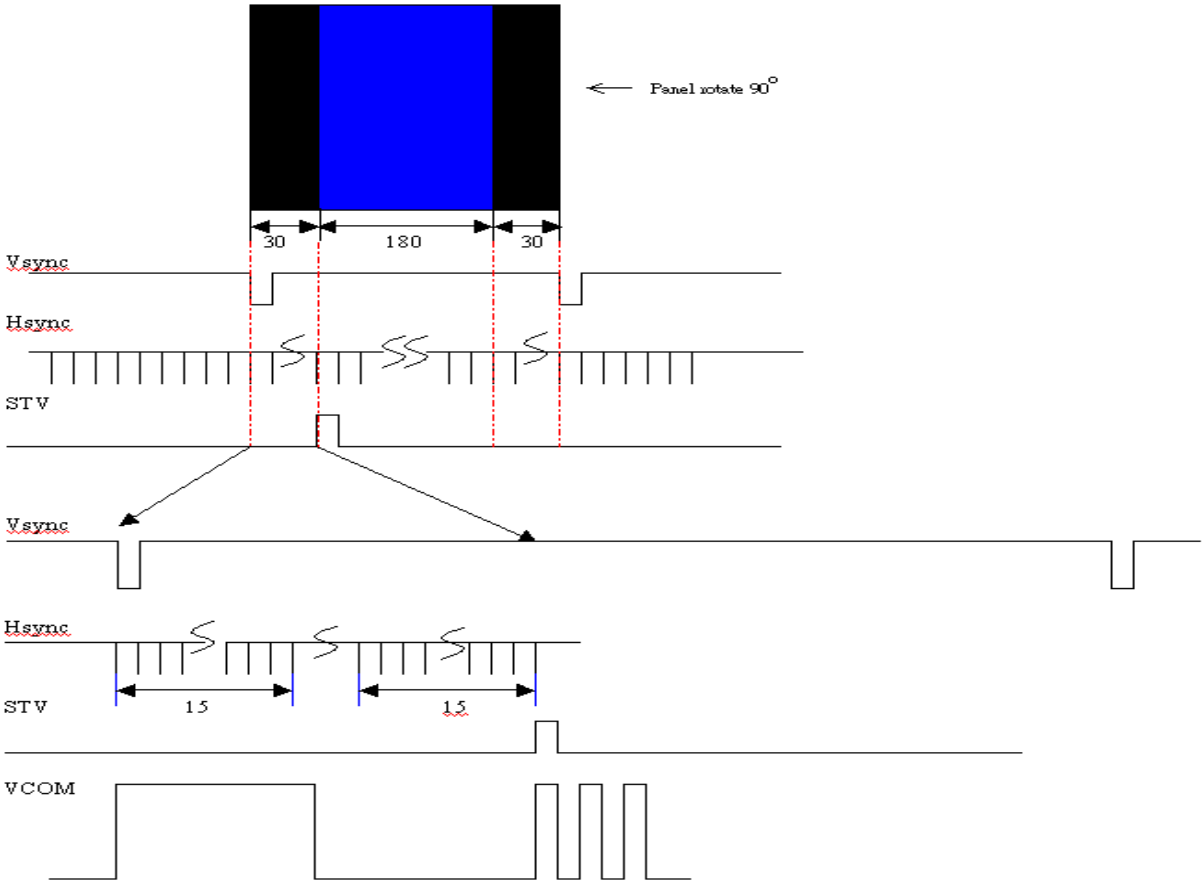
Note 3. NTSC default setting is 594.

PAL default setting is 616.

7.16:9 Wide display

Since the input signal is 240 valid lines. In order to keep 16:9 format, 1/4 lines will be cancelled on the input signal. So the valid lines is 240x0.75=180, Apart from this method, we will also write the black data to TFT. And the black lines are 60 lines where occupied on the up site and bottom site separately.





From above figure,we know that when in black region, We turn on the 15 gate pulses once and then turn on the other 15 gate pulses once. In display region, we show 180 lines normally. Last the black region will be showed and the method is the same as the first 30 lines.

8. DC-DC Converter Circuit

A024CN00 contains one high-power step-up DC-DC converter, and backplane drive circuitry for active matrix TFT LCDs. The output voltage of the main boost converter can be set from VCC to 22V with external resistors. A024CN00 design also include a precision 0.6V reference voltage, fault detection, and logic shutdown.

a .Boost Converter

A024CN00 main boost converter uses a boost PWM architecture to produce a positive regulated voltage, please refer to the below figures to see the block diagram.

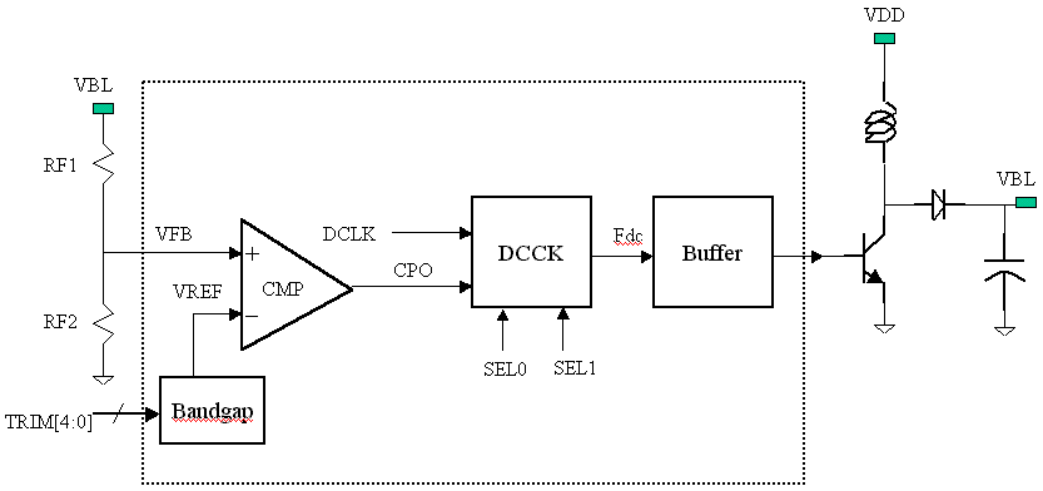


Fig 1 Dc-Dc converter block diagram

In the internal architecture of DC-DC converter. The feedback voltage(VFB) will connect to the triangle waveform comparator, and generates the output signal (CP0) which determines the duty cycle for (Fdc).

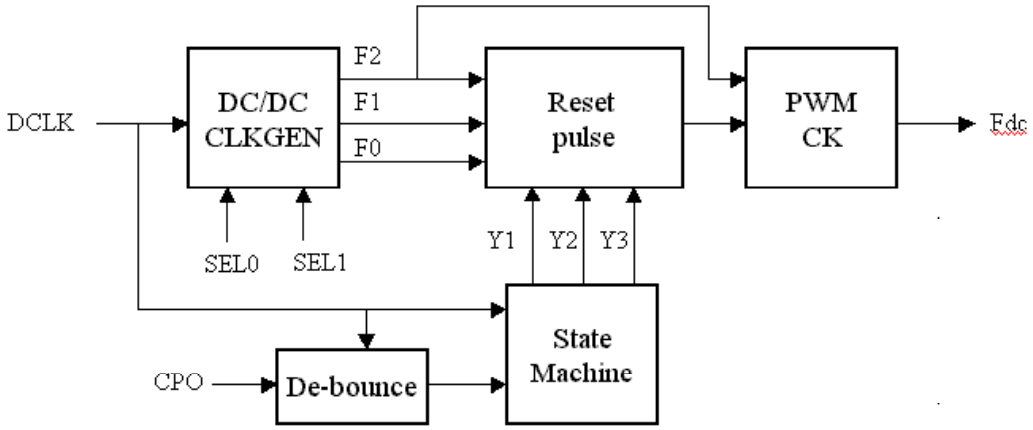


Fig 2 DC CK block diagram

To reduce the noise affect, CP0 will be processed by De-bounce circuit. State-machine will generate the duty cycle by CP0 signal. In order to make sure that VFB can reach default VREF quickly, State-machine's is designed with discrete step by step function (please refer to Fig 3). If CP0 is low, the duty cycle will work from 0% to 83% with the maximum duty ratio to 83%.

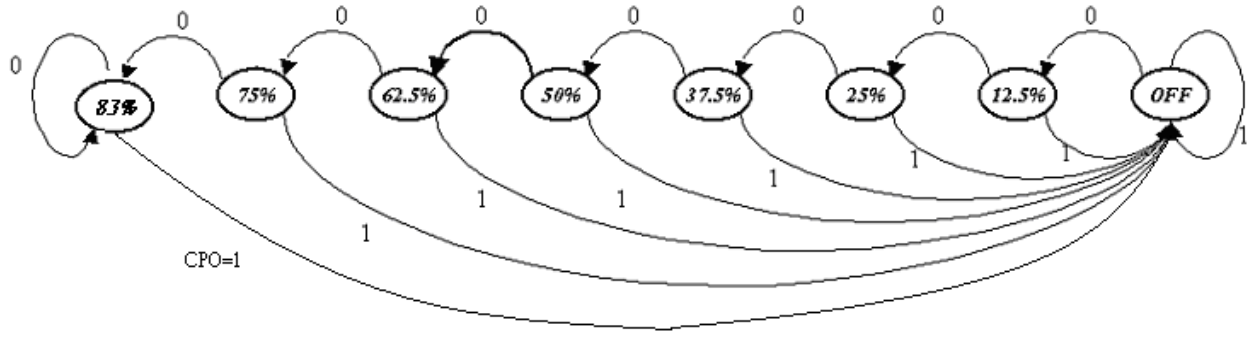
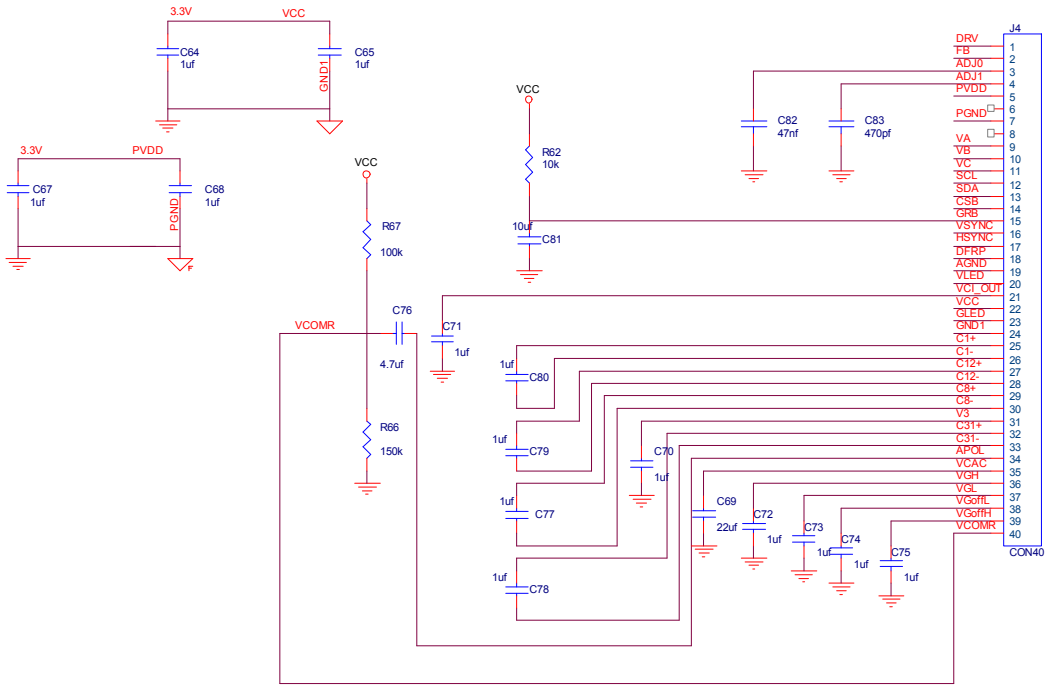


Fig 3 PWM Control state diagram

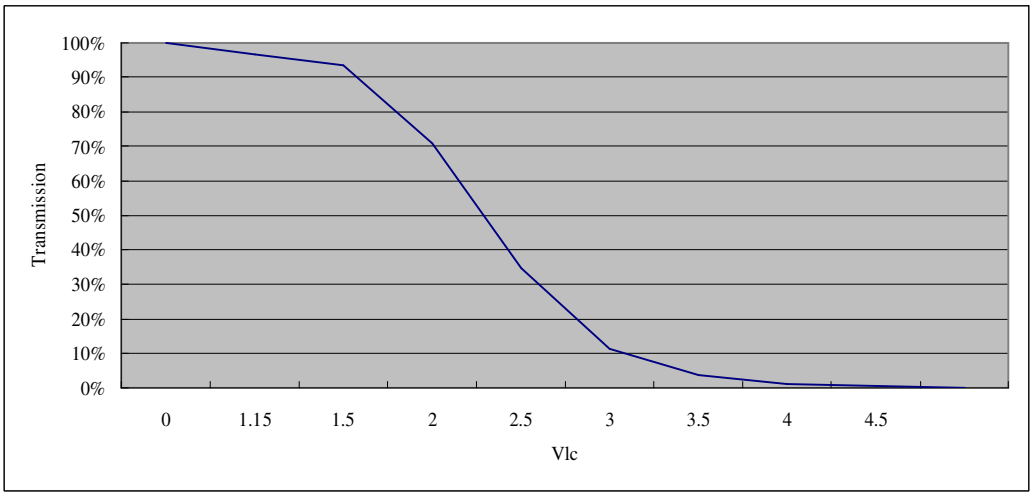
9. Reference Circuit



C. Optical specification (Note 1,Note 2, Note 3)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise	Tr	θ =0°	-	20	30	ms	Note 4, 6
	Fall	Tf		-	30	40	ms	
Contrast ratio		CR	At optimized viewing angle	100	150	-		Note 5, 6
Viewing angle	Top		CR≧10	10	-	-	deg.	Note 6, 7
	Bottom			30	-	-		
	Left			40	-	-		
	Right			40	-	-		
Transmission		Y_L	θ =0°	-	7.3	-	%	Note 8

V-T Curve:



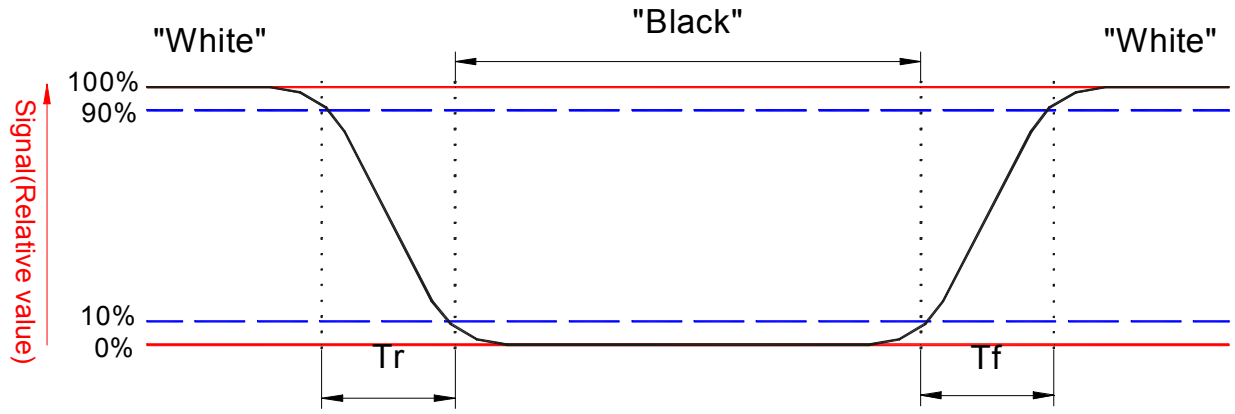
Transmission	Liquid Crystal Voltage (V)		
	Min.	Typ.	Max.
90%	1.5	1.8	2
50%	2.2	2.5	2.8
10%	2.9	3.25	3.5

Note 1. Ambient temperature =25℃.
Note 2. To be measured in the dark room.

Note 3.To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. White $Vi=V_{i50} \mp 1.5V$

Black $Vi=V_{i50} \pm 2.0V$

“±” Means that the analog input signal swings in phase with COM signal.

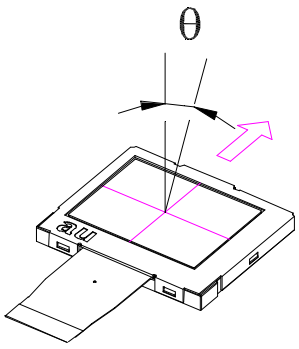
“$\mp$” Means that the analog input signal swings out of phase with COM signal.

V_{i50} : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle:

Refer to figure as below.



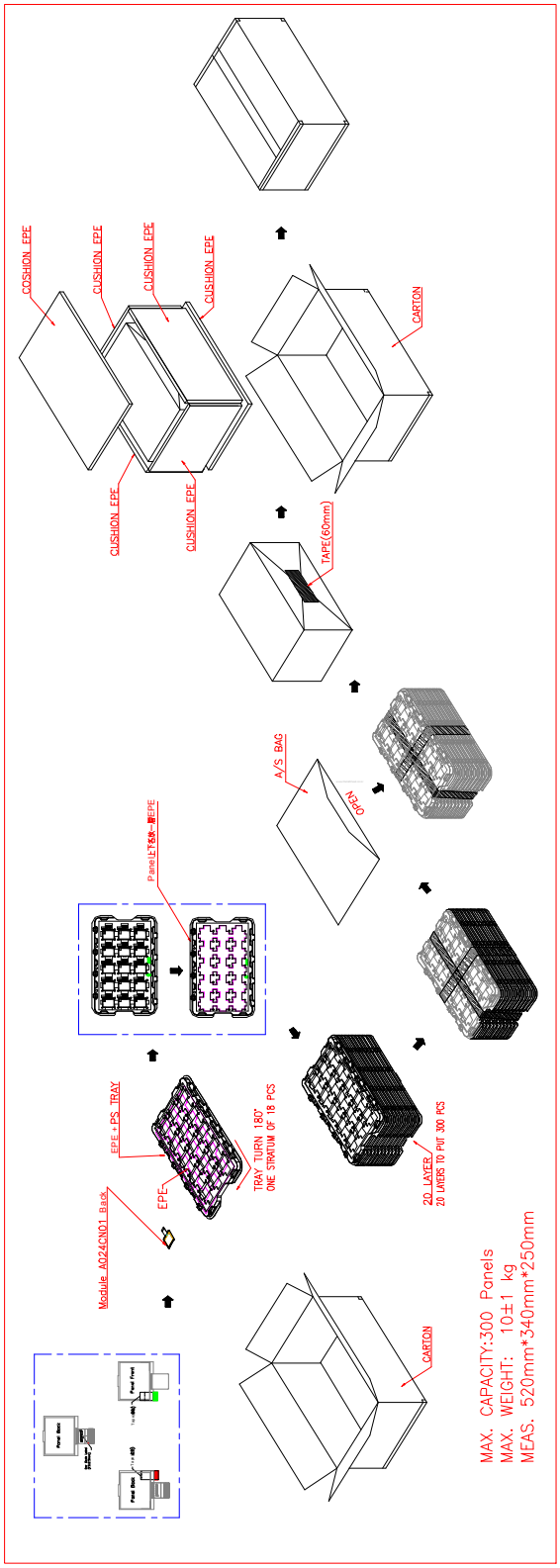
Note 8. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened without APCF (Light enhancement film).

D. Reliability test items:

No.	Test items	Conditions		Remark
1	High temperature storage	Ta= 80℃ 240Hrs		
2	Low temperature storage	Ta= -25℃ 240Hrs		
3	High temperature operation	Ta= 60℃ 240Hrs		
4	Low temperature operation	Ta= 0℃ 240Hrs		
5	High temperature and high humidity	Ta= 60℃. 90% RH 240Hrs		Operation
6	Heat shock	-25℃~80℃/50 cycle @ 2hrs/cycle		Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal		Non-operation
8	Vibration	Frequency range	: 10~55Hz	JIS C7021, A-10 condition A
		Stoke	: 1.5mm	
		Sweep	: 10~55Hz~10Hz	
		2 hours for each direction of X, Y, Z		
		(6 hours for total)		
9	Mechanical shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction		JIS C7021, A-7 condition C
10	Vibration (with carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz		IEC 68-34
11	Drop (with carton)	Height: 80cm 1 corner, 3 edges, 6 surfaces		
12	The copper's strength for FPC	The strength is larger 0.7 kg/cm		IPC TM650
13	The film's strength for FPC	The strength is larger 0.35 kg/cm		IPC TM650
14	Flexibility for FPC	1. curved radius: 2mm 2. Pulling force: 250g		MIT folm: Diagram of test set up for folding endurance

Note: Ta: Ambient temperature.

E. Packing form



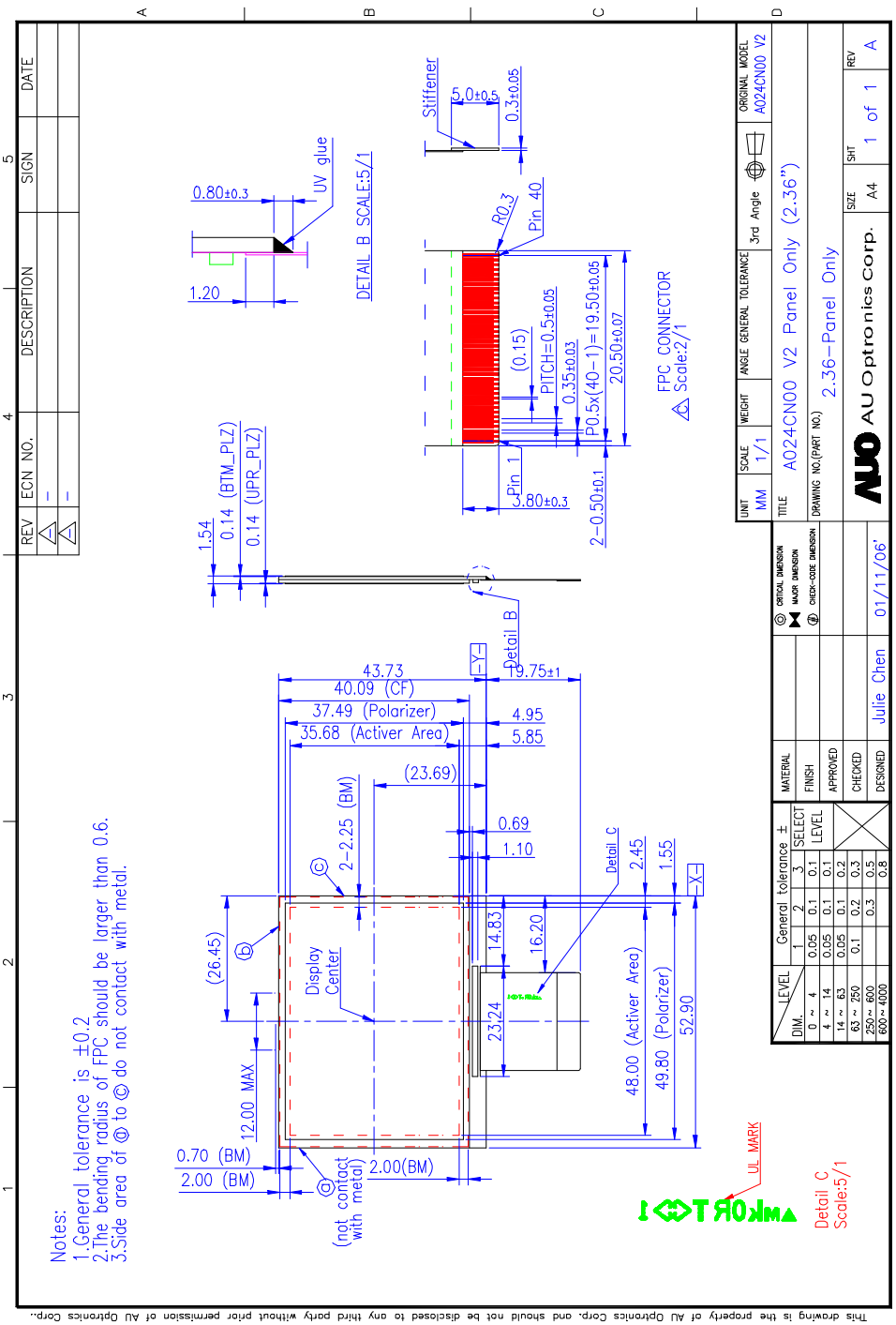


Fig. 2 Outline dimension of TFT-LCD module

Notice for backlight design and assembly:

This panel does not have side panel coating. To prevent VCOM or other electronic short, please avoid metal (i.e. bezel) contact with LC injection sealant located at central portion of upper glass side.

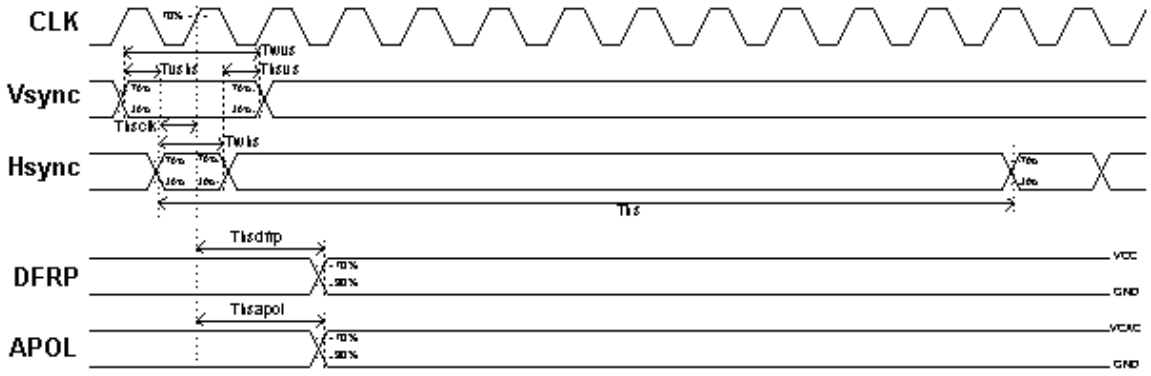


Fig .3 Horizontal Timing Diagram

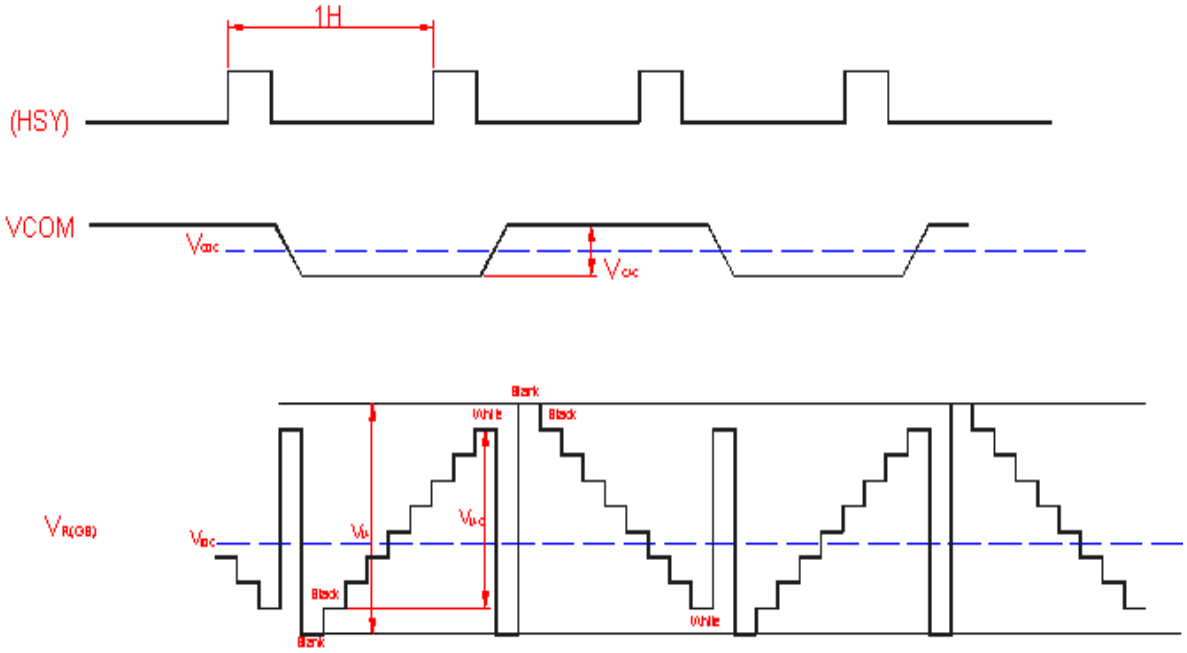


Fig. 4 Input Video signal

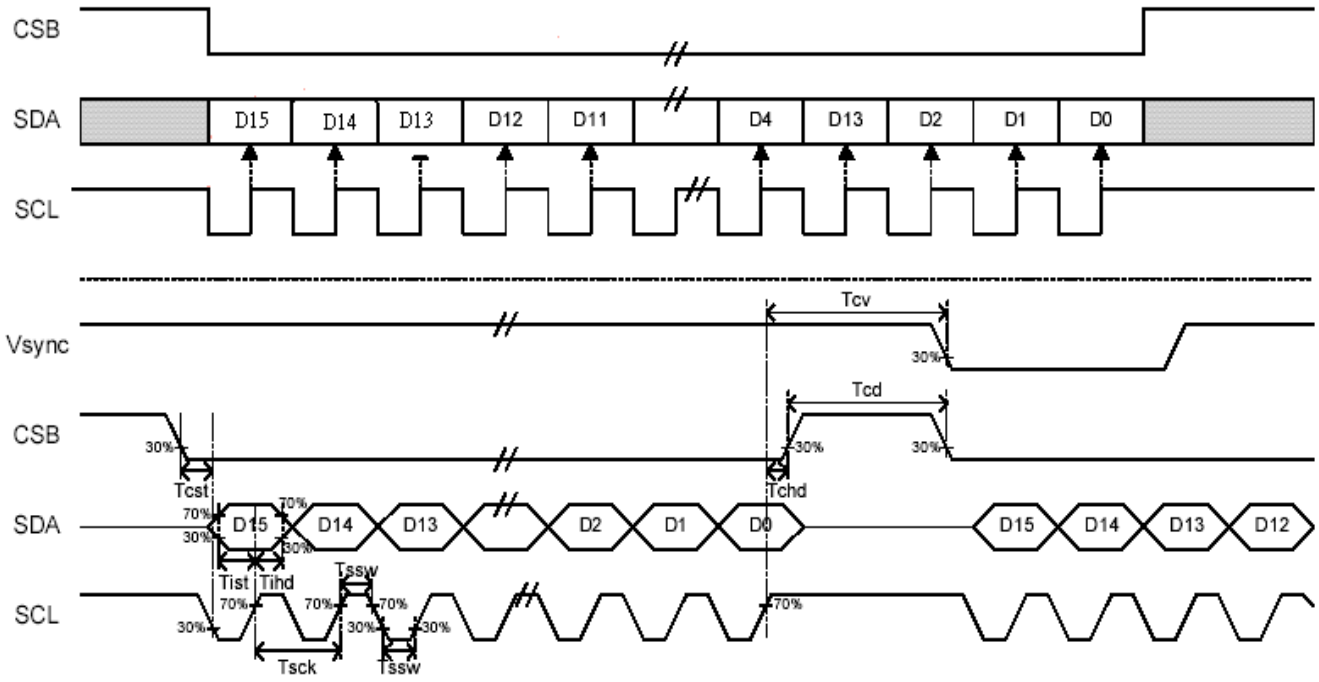


Fig. 5 3-wire programming function Timing

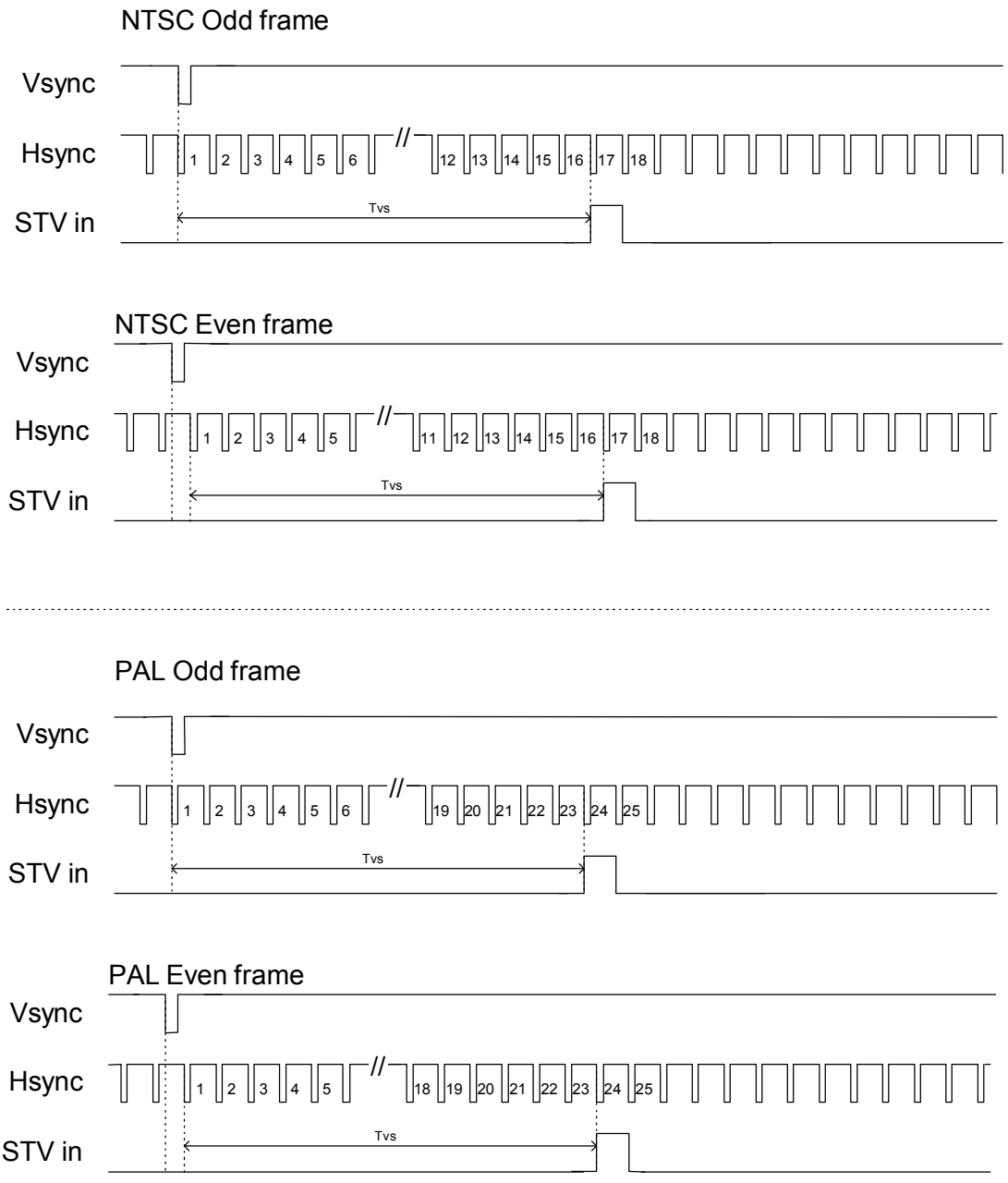


Fig. 6 Vertical Timing Diagram