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MODEL NAME: A030DL02 V1

< ◆ >Preliminary Specification

< > Final Specification

Note: The content of this specification is subject to change.

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Record of Revision

Version	Revise Date	Page	Content
0.1	SEP/16/2005		First draft
0.2	SEP/30/2005	27	Revise viewing angle to 55/55/40/55(L/R/U/D)
0.3	FEB/20/2006	4~5	Modify pin assignment
		7	Add backlight driving conditions
		22	Revise the description and setting range of register “VBLK”
		34~35	Modify typical application circuit description
		36	Revise power on/off sequence
		38	Add legal timing of global reset
0.4a	2006/05/08	7 27 30, 31 34,35	Revise Backlight driving conditions Revise viewing angle to 55/55/45/60 (L/R/U/D) Updated packing form and outline drawing Revise the description and figure of typical Application Circuit
0.4b	2006/05/23	4	Revise the typo of outline mimension
0.5	2006/06/13	8~9 18	Updated AC timing for UPS051 timing condition Updated serial control interface timing and serial settings

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D. Reliability test items **P30**

E. Packing format/outline drawing **P31**

F. Application Notes **P33**

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A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution (dot)	960(W)×240(H)	
2	Active area (mm)	65.76 (W) × 36.24 (H)	
3	Screen size (inch)	2.96 (Diagonal)	
4	Dot pitch (mm)	0.0685 (W) x 0.151 (H)	
5	Color configuration	R. G. B. delta	
6	Overall dimension (mm)	72.36 (W) × 46.15 (H) × 2.7 (D)	Note 1
7	Weight (g)	20.2	
8	Panel surface treatment	AG, Hard coating	

Note 1: Refer to Page 28 Fig. 9

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B. Electrical specifications

1. Pin assignment

Pin no	Symbol	I/O	Description	Remark
1	VCOM	I	Common voltage	
2	CS	I	Serial command enable signal	Note 1
3	SDA	I	Serial command data input	Note 1
4	SCL	I	Serial command clock input	Note 1
5	HSYNC	I	Horizontal sync input	
6	VSYNC	I	Vertical sync input	
7	DCLK	I	Input data clock	
8	D7	I	Data input; MSB	
9	D6	I	Data input	
10	D5	I	Data input	
11	D4	I	Data input	
12	D3	I	Data input	
13	D2	I	Data input	
14	D1	I	Data input	
15	D0	I	Data input; LSB	
16	DRV	O	VLED boost transistor driving signal	
17	VLED	P	LED power: anode	
18	FB	I / P	LED power: cathode	
19	AVDD	C	Power setting capacitor	
20	AGND	P	Ground for analog circuit	
21	GND	P	Ground for digital circuit	
22	VCCI	P	Power supply for digital interface	
23	VDC	P	Power supply for DC-DC circuit	
24	V1	C	Power setting capacitor	
25	V2	C	Power setting capacitor	
26	V3	C	Power setting capacitor	

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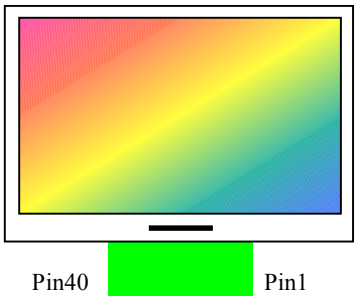
27	V4	C	Power setting capacitor	
28	V5	C	Power setting capacitor	
29	V6	C	Power setting capacitor	
30	V7	C	Power setting capacitor	
31	V8	C	Power setting capacitor	
32	V9	C	Power setting capacitor	
33	V10	C	Power setting capacitor	
34	FRP	O	VCOM driving signal	Note 2
35	VGL	C	Power setting capacitor	
36	VGH	C	Power setting capacitor	
37	VCOML	C	Power setting capacitor for VCOM	
38	VCOMH	C	Power setting capacitor for VCOM	
39	VCOM	I	Common voltage	
40	N.C.	-	Not connected	

I: Input; O: Output; P: Power; C: Capacitor.

Note 1: 3-wire serial control interface is operational after V_{CCI} power on reset, but execution of programmed commands is synchronized at front edge of next VSYNC pulse.

Note 2: FRP is the output of Vcom driver. It is the same phase and amplitude with common electrode driving signal (Vcom). The Vcom amplitude and DC level setting can be adjusted through serial control.



b. Backlight driving section

No.	Symbol	I/O	Description	Remark
Pin 17	VLED	I	LED Anode	
Pin 18	FB	-	LED Cathode	

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2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	V_{DC}	GND=0	-0.5	5	V	
Power voltage	V_{CCI}	GND=0	-0.5	5	V	
Operating temperature	Topa	-	0	60	℃	Ambient temperature
Storage temperature	Tstg	-	-25	80	℃	Ambient temperature

3. Electrical characteristics

a. Recommended operating conditions (GND=AGND=0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		V_{DC}	3.15	3.3	3.6	V	Note 1
		V_{CCI}	1.7	3.3	3.6	V	Note 2
Input Signal voltage	H Level	V_{IH}	0.8* V_{CCI}	-	V_{CCI}	V	
	L Level	V_{IL}	GND	-	0.2* V_{CCI}	V	

Note 1: A build-in power on reset circuit for V_{DC} and V_{CCI} is provided within the integrated LCD driver IC. The LCD module is in power save mode in default, and a standby releasing is required after V_{CCI} power on through serial control. Please refer to the register STB setting for detail.

Note 2: The power supply of digital interface , V_{CCI}, is for the 1.8V digital interface requirement in the future. These digital signals are DCLK, HSYNC, VSYNC, D7~D0, CS, SDA and SCL. If the digital interface is in the level of 3.3V, please short the power pin V_{DC} and V_{CCI} to 3.3V. In other words, no matter the voltage level of V_{CCI} is 1.8V or 3.3V, the voltage level of V_{DC} needs to be kept around 3.3V.

b. Electrical Characteristics (GND=AGND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input Current for V_{DC}	I_{DC}	V_{DC}=3.3V		22.5		mA	Note 1
				25			Note 2
	$I_{DC(STANDBY)}$	V_{DC}=3.3V		10		uA	Note 1,3
				10			Note 2,3
Input Current for V_{CCI}	I_{CCI}	V_{CCI}=3.3V		24		uA	Note 1
				45			Note 2
	$I_{CCI(STANDBY)}$	V_{CCI}=3.3V		10		uA	Note 1,3
				10			Note 2,3
DC-DC voltage	V_{GH}	V_{DC}=3.3V		10.5		V	Note 4
	V_{GL}	V_{DC}=3.3V		-3.7		V	Note 4

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VCOM voltage	V_{CAC}		5.0	5.6	6.4	Vp-p	AC component, Note 5
	V_{CDC}		1.75	2.4	3.5	V	DC component, Note 6
DRV output voltage	V_{DRV}		0	-	VDC	V	
DRV output current	I_{DRV}			-	10	mA	
Feedback voltage	V_{FB}		0.54	0.6	0.66	V	

Note 1:Test Condition: Black pattern, UPS051 mode, DCLK=24MHz, Frame rate:60Hz , other registers are default setting

Note 2:Test Condition: Black pattern,UPS052 320x240 mode, DCLK=24MHz, other registers are default setting

Note 3:In standby mode, digital signals DCLK, HSYNC, VSYNC, D7~D0, CS, SDA and SCL are stopped.

Note 4: V_{GH} and V_{GL} are output voltages of integrated LCD driver IC.

Note 5: The brightness of LCD panel could be adjusted by the adjustment of the AC component of VCOM

Note 6: V_{CDC} could be adjusted, so as to minimize flicker and maximum contrast on each module.

c. Recommended Capacitance Values of External Capacitor

The recommended capacitance values of the external capacitor are shown below. These valu should be finally determined only after performing sufficient evaluation on the module.

Pin name	Recommended value of capacitors (μF)	Withstanding voltage (V)
AVDD	4.7 to 10	16
VGH	4.7 to 10	16
VGL	4.7 to 10	16
VCOMH	4.7 to 10	16
V1, V2	2.2 to 10	16
V3, V4	2.2 to 10	16
V5, V6	2.2 to 10	16
V7, V8	2.2 to 10	16
V9, V10	2.2 to 10	16

d. Backlight driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	I_{LED}	-	25	30	mA	
LED voltage	V_{LED}	6.75	7.15	7.75	V	Note 1
LED Life Time	L_{LED}	10000	-	-	Hr	Note2,3

Note 1: Typical voltage:3.2V/pcs ,FB=0.75V. LED voltage: VLED=3.2*2+0.75=7.15V
Please refer to Fig.13 (P.34)

Note 2 : Ta. = 25℃, I_{LED} = 25mA

Note 3 : Brightness to be decreased to 50% of the initial value.

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4. AC Timing

a - 1. UPS051 (24MHz) Timing conditions (refer to Fig. 1, Fig. 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	22.93	24.535	27.19	MHz	
HSYNC	Period	t_H	1560	1560	1728	DCLK	Note 1
	Display period	t_{hdisp}		960		DCLK	
	Blanking	t_{hblk}	66	241	255	DCLK	
	Front porch	t_{hfp}	345	359	—	DCLK	
	Pulse width	t_{hsw}	1	1	t_{hblk} -1	DCLK	
VSYNC	Period	t_V	15.2	16.6	20	ms	Note 2
			245	262.5	265	t_H	
	Display period	t_{vdisp}		240		t_H	
	Blanking	t_{vblk}	3	21	31	t_H	
	Pulse width	t_{vsw}	1	1	t_{vblk} –1	DCLK	
Data set-up time		t_{ds}	12			ns	
Data hold time		t_{dh}	12			ns	
Vsync-to-Hsync set-up time		t_{vhs}	1			DCLK	

(*)when t_H = 68us, t_V=245t_H

Note 1: UPS051 Horizontal blanking time (t_{hblk}) is adjustable by setting register HBLK; requirement of minimum blanking time and minimum front porch time must be satisfied.

Note 2: UPS051 Vertical blanking time (t_{vblk}) is adjustable by setting register VBLK. UPS051 accepts both interlace and non-interlace vertical input timing.

a - 2. UPS051 (20MHz) Timing conditions (refer to Fig. 1, Fig. 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	19.43	20.00	22.93	MHz	
HSYNC	Period	t_H	1322	1360	1560	DCLK	Note 1,2
	Display period	t_{hdisp}		960		DCLK	
	Blanking	t_{hblk}	66	241	255	DCLK	
	Front porch	t_{hfp}	123	159	534	DCLK	
	Pulse width	t_{hsw}	1	1	t_{hblk} -1	DCLK	
VSYNC	Period	t_V	15.2	16.6	20	ms	Note 3
			245	245	265	t_H	
	Display period	t_{vdisp}		240		t_H	
	Blanking	t_{vblk}	3	4	24	t_H	
	Pulse width	t_{vsw}	1	1	t_{vblk} –1	DCLK	
Data set-up time		t_{ds}	12			ns	
Data hold time		t_{dh}	12			ns	
Vsync-to-Hsync set-up time		t_{vhs}	1			DCLK	

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Note 1: If the DCLK number of 1 Hsync period is less than 1560, please set series command **R133=29h & R134=AEh & R136=2Bh & R137=8Ch & R138=0Bh**.

Note 2: UPS051 Horizontal blanking time (t_{hblk}) is adjustable by setting register HBLK; requirement of minimum blanking time and minimum front porch time must be satisfied.

Note 3: UPS051 Vertical blanking time (t_{vblk}) is adjustable by setting register VBLK. UPS051 accepts both interlace and non-interlace vertical input timing.

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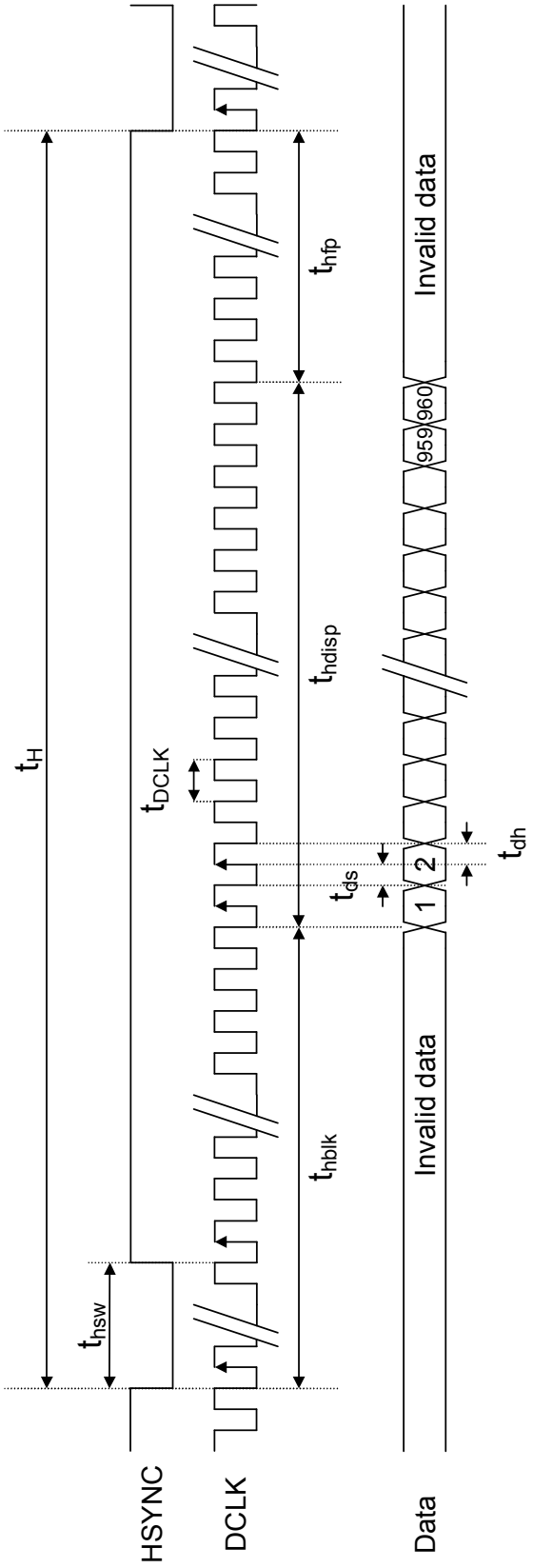

Fig.1 UPS051 Input Horizontal Signal

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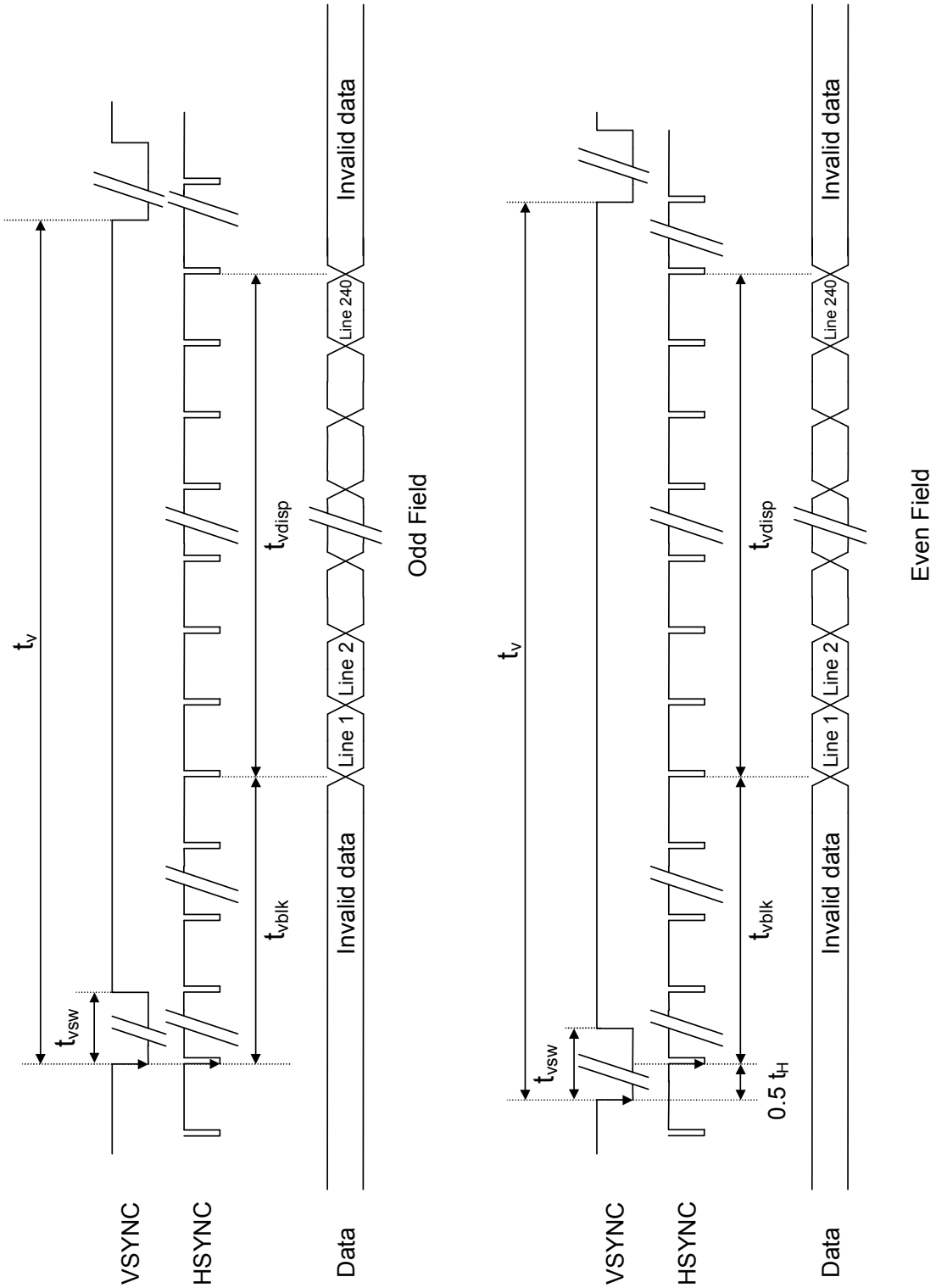

Fig.2 IIPS051 Input Vertical Signal

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b - 1. UPS052 (320 mode/NTSC/24.545MHz) timing specifications (refer to Fig. 3, Fig. 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	24	24.535	27	MHz	
HSYNC	Period	t_H		1560		t_{DCLK}	
	Display period	t_{hdisp}		1280		t_{DCLK}	
	Blanking	t_{hblk}		241		t_{DCLK}	
	Pulse width	t_{hsw}		1		t_{DCLK}	
VSYNC	Period	t_V		262.5		t_H	
	Display period	t_{vdisp}		240		t_H	
	Blanking	t_{vblk}		21		t_H	
	Pulse width	t_{vsw}		1		t_{DCLK}	

b - 2. UPS052 (320 mode/PAL/24.375MHz) timing specifications (refer to Fig. 3, Fig. 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	24	24.375	27	MHz	
HSYNC	Period	t_H		1560		t_{DCLK}	
	Display period	t_{hdisp}		1280		t_{DCLK}	
	Blanking	t_{hblk}		241		t_{DCLK}	
	Pulse width	t_{hsw}		1		t_{DCLK}	
VSYNC	Period	t_V		312.5		t_H	
	Display period	t_{vdisp}		288		t_H	
	Blanking	t_{vbp}		24		t_H	
	Pulse width	t_{vsw}		1		t_{DCLK}	

c - 1. UPS052 (360 mode/NTSC/27MHz) timing specifications (refer to Fig. 3, Fig. 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	24	27	28	MHz	
HSYNC	Period	t_H		1716		t_{DCLK}	
	Display period	t_{hdisp}		1440		t_{DCLK}	
	Blanking	t_{hblk}		241		t_{DCLK}	
	Pulse width	t_{hsw}		1		t_{DCLK}	
VSYNC	Period	t_V		262.5		t_H	
	Display period	t_{vdisp}		240		t_H	
	Blanking	t_{vblk}		21		t_H	
	Pulse width	t_{vsw}		1		t_{DCLK}	

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c - 2. UPS052 (360 mode/PAL/27MHz) timing specifications (refer to Fig. 3, Fig. 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	24	27	28	MHz	
HSYNC	Period	t_H		1728		t_{DCLK}	
	Display period	t_{hdisp}		1440		t_{DCLK}	
	Blanking	t_{hblk}		241		t_{DCLK}	
	Pulse width	t_{hsw}		1		t_{DCLK}	
VSYNC	Period	t_V		312.5		t_H	
	Display period	t_{vdisp}		288		t_H	
	Blanking	t_{vbp}		24		t_H	
	Pulse width	t_{vsw}		1		t_{DCLK}	

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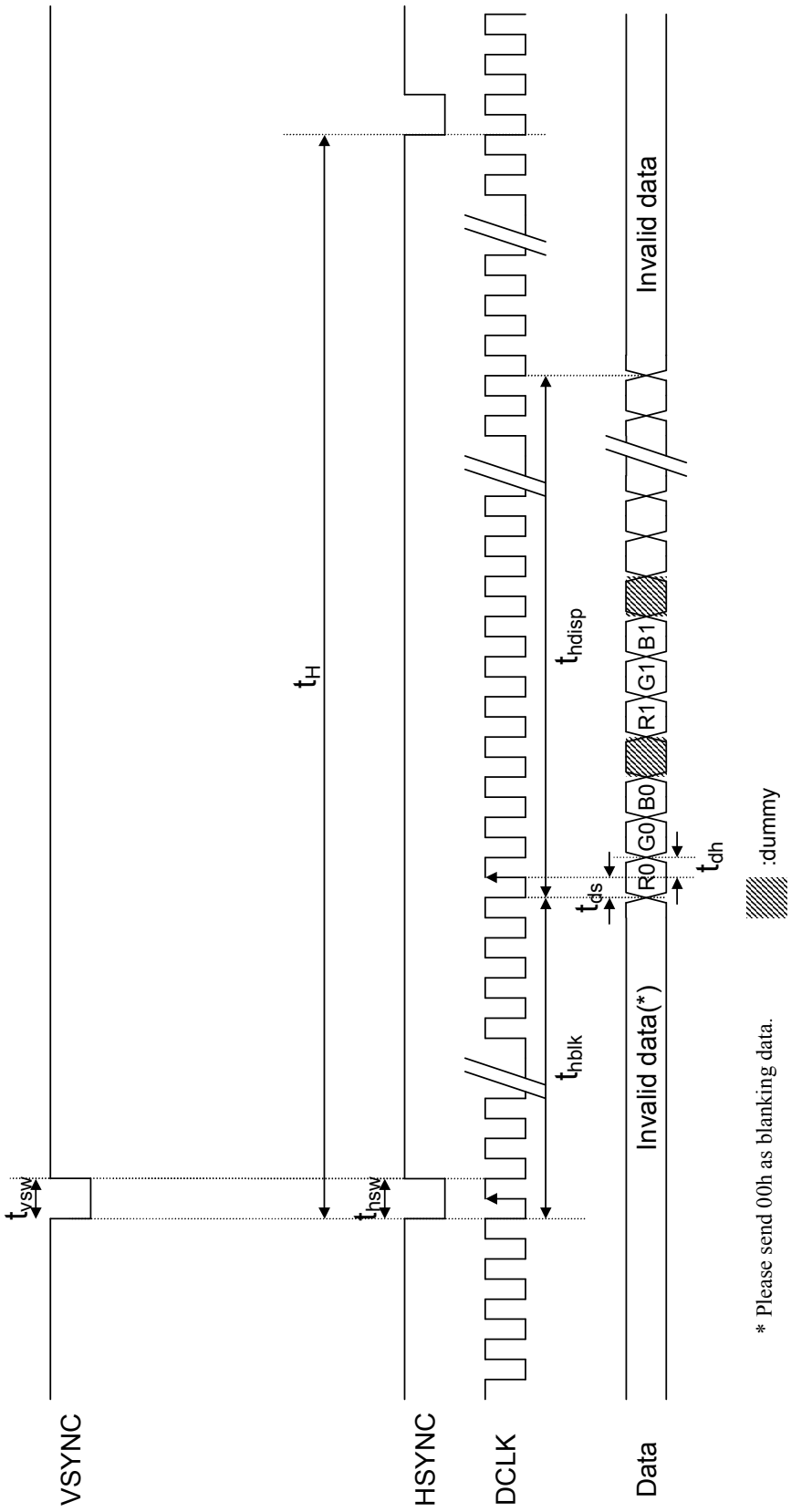

Fig. 3 UPS052 Input Horizontal Signal

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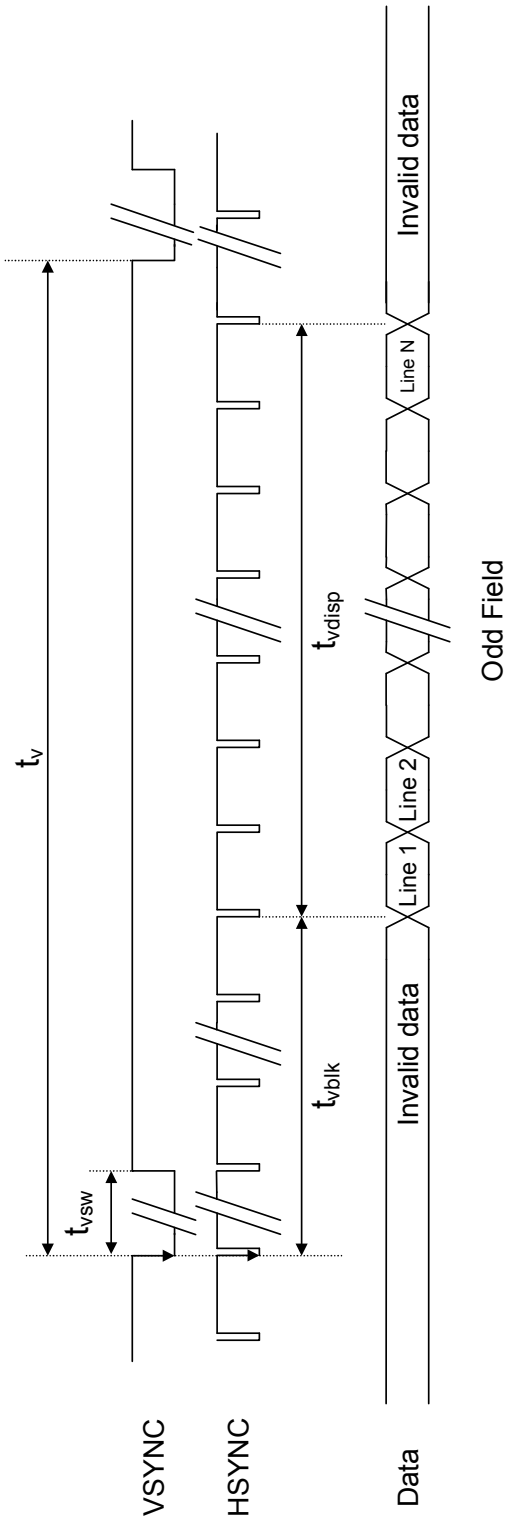

Fig.4 UPS052 Input Vertical Signal

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d- 1. CCIR656 Timing chart

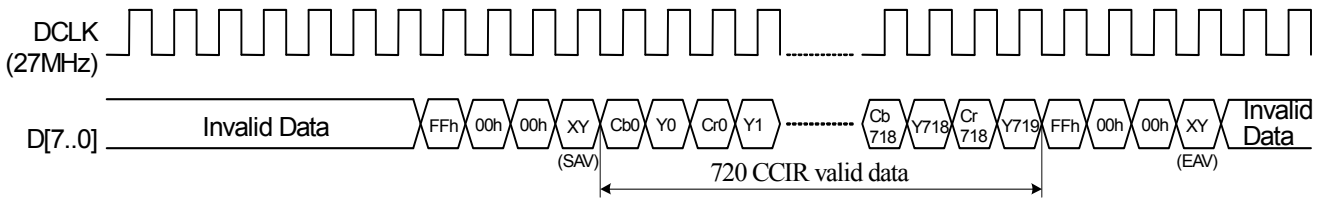

Fig. 5: CCIR656 Data input format

d- 2. CCIR656 decoding

FF 00 00 XY signals are involved with HSYNC,VSYNC and Field

XY encode following bits:

F=field select

V=indicate vertical blanking

H=1 if EAV else 0 for SAV

P3-P0=protection bits

P3=V⊕H P2=F⊕H P1=F⊕V P0=F⊕V⊕H

⊕represents the exclusive-OR function.

Control is provided through “End of Video” (EAV) and “Start of Video” (SAV) timing references.

Horizontal blanking section consists of repeating pattern 80 10 80 10

XY							
D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	F	V	H	P3	P2	P1	P0

d- 3. CCIR656 to RGB conversion

R=Y +1.371*(Cr-128)

G=Y -0.698(Cr-128)-0.336(Cb-128)

B=Y +1.732(Cb-128)

Where Y:16~235 Cr:16~240 Cb:16~240

In CCIR656 mode , please set series command **R3=2Eh & R13=4Bh** for the better contrast .

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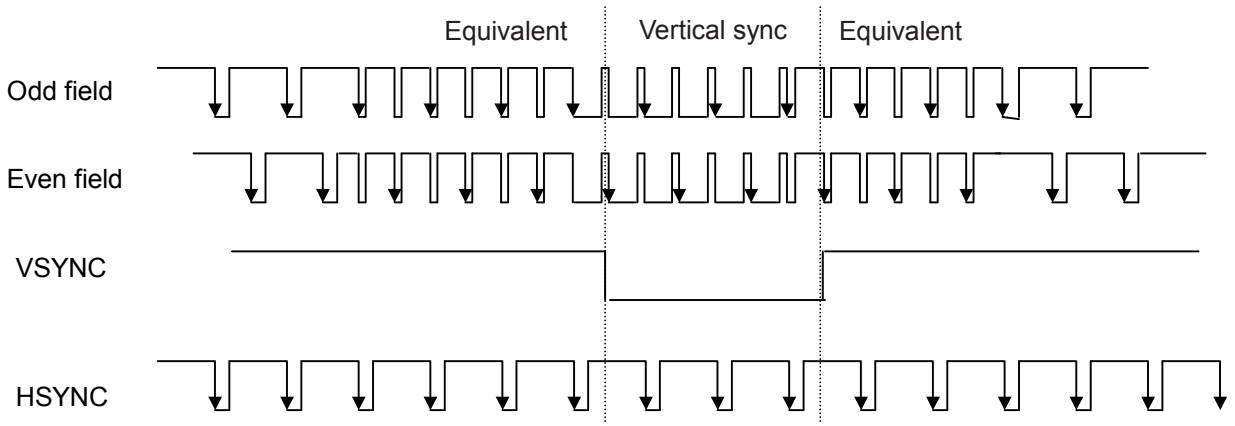
e. CSYNC Timing chart

NTSC mode



PAL mode

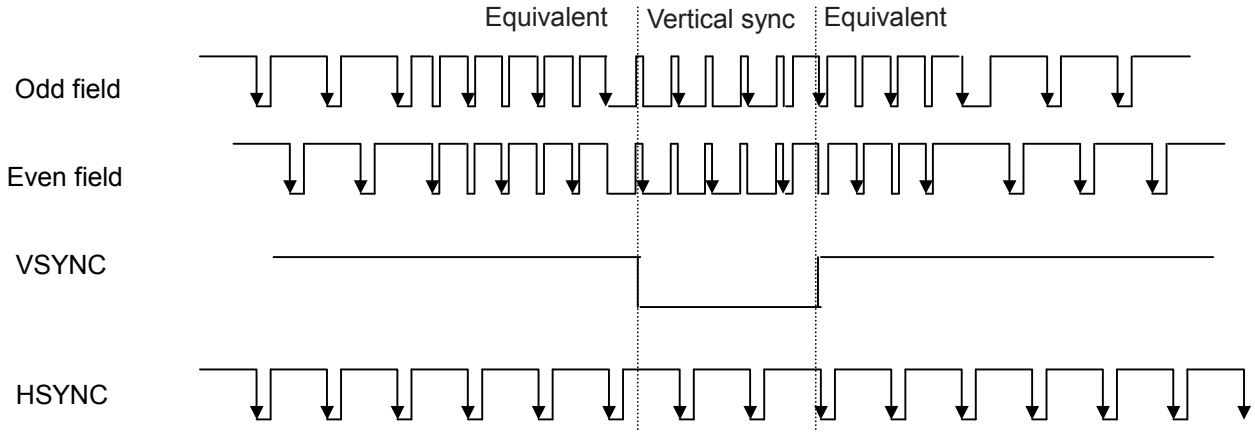


Fig. 6: CSYNC Data input format

Item	Min	Typ	Max
HYSNC width	20 clk	4.7us	6us
Equivalent pulse width	20 clk	2.35us	3us
Serrated pulse width (inside VSYNC)	20 clk	4.7us	6us
VSYNC width	2.3H	NTSC:3H PAL:2.5H	10H

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5. Serial Control Interface

a. Timing condition (refer to Fig. 7)

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Serial load input setup time	t_{s0}	100			ns	
Serial load input hold time	t_{h0}	100			ns	
Serial data input setup time	t_{s1}	100			ns	
Serial data input hold time	t_{h1}	100			ns	
SCL pulse width	t_{w1L}	200			ns	
	t_{w1H}	200			ns	
CS pulse width	T_{w2}	600			ns	

b. Serial setting map

No	Register Address								Register Data (Default setting)							
	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
R0	0	0	0	0	0	0	0	0	×	×	×	×	×	VCOM_AC (011)		
R1	0	0	0	0	0	0	0	1	×	FLK (0)	VCOM_DC (18h)					
R3	0	0	0	0	0	0	1	1	BRIGHTNESS(40h)							
R4	0	0	0	0	0	1	0	0	×	YUV (0)	SEL (00)		NTSC/PAL (10)		VDIR (1)	HDIR (1)
R5	0	0	0	0	0	1	0	1	DRV_FREQ (0)	GRB (1)	×	PWM_DUTY(10)		SHDB2 (1)	SHDB1 (1)	STB (0)
R6	0	0	0	0	0	1	1	0	×	LED_CURRENT (00)	VBLK (15h)					
R7	0	0	0	0	0	1	1	1	HBLK (1Eh)							
R8	0	0	0	0	1	0	0	0	BL_DRV (00)	×	×		×	×	×	×
R12	0	0	0	0	1	1	0	0	PAIR(00)	CSYNC (1)	CbCr (0)		×	VDpol (1)	HDpol (1)	DCLKpol (0)
R13	0	0	0	0	1	1	0	1	CONTRAST(40h)							
R14	0	0	0	0	1	1	1	0	×	SUB-CONTRAST_R(40h)						
R15	0	0	0	0	1	1	1	1	×	SUB-BRIGHTNESS_R(40h)						
R16	0	0	0	1	0	0	0	0	×	SUB-CONTRAST_B(40h)						
R17	0	0	0	1	0	0	0	1	×	SUB-BRIGHTNESS_B(40h)						
R18	0	0	0	1	0	0	1	0	Gamma_VR2(8h)				Gamma_VR1(8h)			
R19	0	0	0	1	0	0	1	1	Gamma_VR4(8h)				Gamma_VR3(8h)			
R133	1	0	0	0	0	1	0	1	Reserved register for IC Test Mode							
R134	1	0	0	0	0	1	1	0	Reserved register for IC Test Mode							
R136	1	0	0	0	1	0	0	0	Reserved register for IC Test Mode							
R137	1	0	0	0	1	0	0	1	Reserved register for IC Test Mode							
R138	1	0	0	0	1	0	1	0	Reserved register for IC Test Mode							

× : reserved, please set to **'0'**

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c. Description of Serial Control Operations

- Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL
- Command loading operation starts from the falling edge of CS and is completed at the next rising edge
- The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid. Please refer to Fig. 8.
- If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.
- If 16 bits or more of SCL are input while CS is low, the first 16 bits of transferred data before the rising edge of CS pulse are valid data.
- Serial block operates with the SCL clock and serial data can be accepted in the power save mode

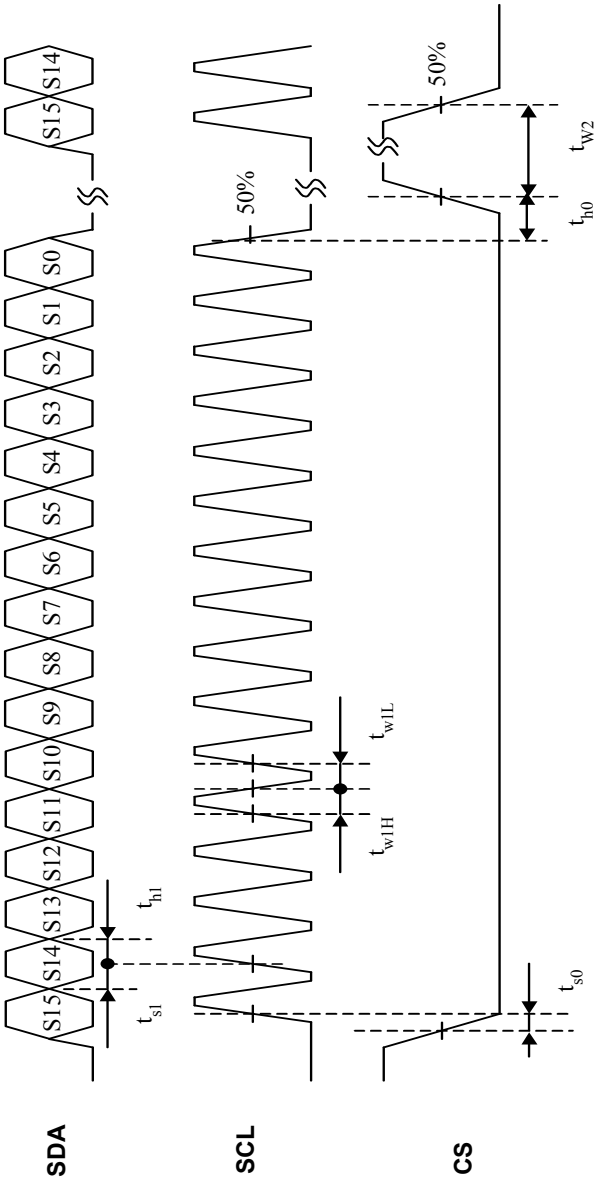

Fig. 7 Serial Control Timing

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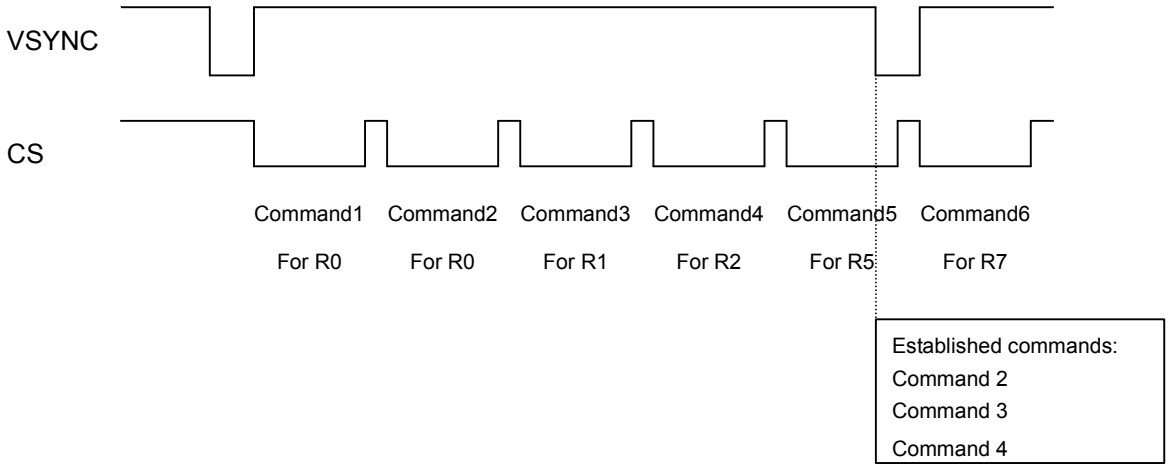
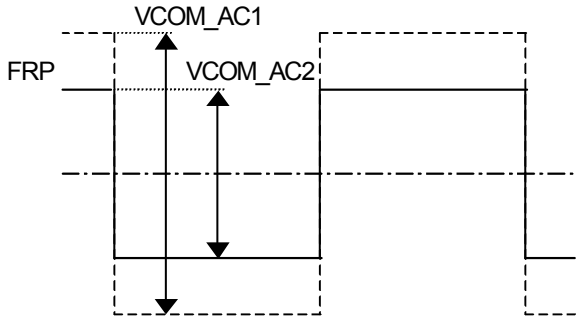


Fig. 8 Illustration of Serial Command Operation

d. Description of serial control data

(1) VCOM_AC: Common voltage AC level selection; 3 bit setting, 0.2V / LSB (deviation ±4%)

(MSB – LSB)	VCOM AC LEVEL	UNIT
000	5.0	V
001	5.2	
010	5.4	
011	5.6 (Default)	
100	5.8	
101	6.0	
110	6.2	
111	6.4	



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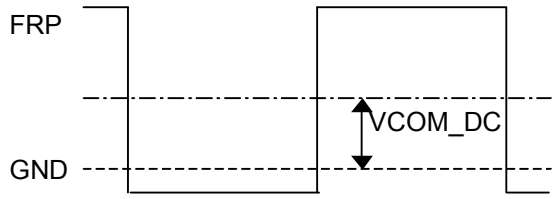
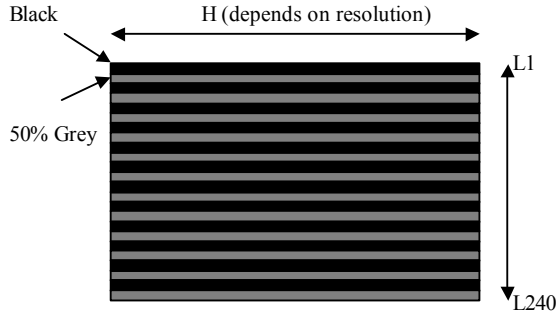
(2) VCOM_DC : Common voltage DC level selection; 6 bit setting, 27.8mV / LSB

(MSB – LSB)	VCOM AC LEVEL	UNIT
00h	1.75	V
18h	2.4(Default)	
3Fh	3.5	



(3) FLK : flicker pattern output

FLK	Function
0	Normal operation (Default)
1	Flicker patttern output



(4) BRIGHTNESS : RGB bright level setting; 8-bit setting

(MSB-LSB)	Function
00h	Dark
40h	Center (Default)
FFh	Bright

(5) HDIR : Horizontal scan direction setting

HDIR	Function
0	Right-to-left scan
1	Left-to-right scan (Default)

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(6) VDIR : Vertical scan direction setting

VDIR	Function
0	Down-to-up scan
1	Up-to-down scan (Default)

(7) NTSC/PAL : NTSC or PAL mode selection (for UPS052 input timing)

(MSB-LSB)	Function
00	PAL mode
01	NTSC mode
1X	Auto-detection mode (Default)

(8) SEL : Input data timing format selection; please refer to AC timing section for detail specifications.

(MSB-LSB)	Input Timing Format
00	UPS051 (Default)
01	UPS052: 320x240
1X	UPS052: 360x240

(9) YUV : YUV(CCIR656) or RGB input selection

YUV	Function
0	RGB input (Default)
1	CCIR656 input(*)

When this command is sent to ASIC,it will be executed immediately.

When CSYNC =‘0’, CSYNC input from HSYNC pin,If YUV=‘1’ & CSYNC=‘0’ ,YUV is the input signal.

(*)for CCIR656 input interface, SEL has to be set as “**11**”

(10) Narrow : This setting is for WIDE scale panel to switch display mode between Wide mode display(16:9) and Narrow mode display (4:3).

Narrow	Function
0	Wide display(16:9) Default
1	Narrow display(4:3)

The function Narrow applies to UPS052 320x240, UPS052 360x240 and CCIR656 interfaces.

(11) STB : Standby (power saving) mode setting

STB	Function
0	Standby mode (Default)
1	Normal operation

(12)SHDB1: Shut-down for back light power converter

SHDB1	Function
0	The black power converter is off
1	The black power converter is controlled by build-in on/off sequence (Default)

(13) SHDB2: Shut-down for VGH/VGL charge pump

SHDB	Function
0	The VGH/VGL charge pump is off
1	The VGH/VGL charge pump is controlled by build-in on/off sequence (Default)

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(14) PWM_DUTY: PWM duty cycle selection for back light power converter

(MSB-LSB)	Function(PWM duty cycle)
00	50%
01	60%
10	65%(Default)
11	70%

(15) GRB: Register reset setting

GRB	Function
0	Reset all registers to default values
1	Normal operation (Default)

(16) DRV_FREQ: DRV signal frequency setting

Mode	DRV_FREQ='0' (default)	DRV_FREQ='1'
UPS051 960x240	DCLK/64	DCLK/32
UPS052	DCLK/64	DCLK/32

Note: For better efficiency, the setting DRV_FREQ='1' and BL_DRV="11" are recommended.

(17) VBLK: Vertical blanking setting for UPS051, UPS052 and CCIR656 ; 5-bit setting, 1 line/LSB

For UPS051and UPS052 NTSC mode ; 5-bit setting, 1 line/LSB

(MSB-LSB)	V-blanking t_{vblk}	UNIT
03h	3	line
15h	21 (Default)	
1Fh	31	

For CCIR656 NTSC mode ; 5-bit setting, 1 line/LSB

(MSB-LSB)	V-blanking t_{vblk}	UNIT
03h	3	line
16h	22	
1Fh	31	

Under CCIR656 PAL mode; Vertical blanking+3, as the following table ; 5-bit setting, 1 line/LSB

(MSB-LSB)	V-blanking t_{vblk}	UNIT
03h	6	line
15h	24	
1Fh	34	

Note1:V-blanking must be adjusted based on the input data.

(18)LED_CURRENT: Adjust LED current

DC-DC feedback voltage

(MSB-LSB)	Function
00	0.6 V(default, 20mA)
01	0.75V (25mA)
10	0.45V (15mA)
11	0.3V (10mA)

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(19) HBLK: Horizontal blanking setting for UPS051; 8-bit setting, 1 DCLK/LSB

(MSB-LSB)	H-blanking t_{hblk}	UNIT
00h	0	DCLK
1Eh	30 (Default)	
FFh	255	

(20) BL_DRV: Backlight driving capability setting

D7	D6	BL_DRV capability
0	0	Normal capability (Default)
0	1	2 times the Normal capability
1	0	4 times the Normal capability
1	1	8 times the Normal capability

Note: For better efficiency, the setting DRV_FREQ='1' and BL_DRV="11" are recommended.

(21) DCLKpol : DCLK polarity selection

DCLKpol	Function
0	Positive polarity (Default)
1	Negative polarity

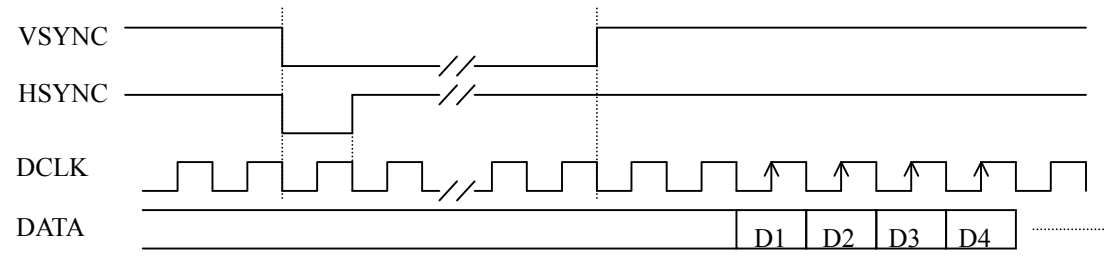
(22) HDpol : HSYNC polarity selection

HDpol	Function
0	Positive polarity
1	Negative polarity (Default)

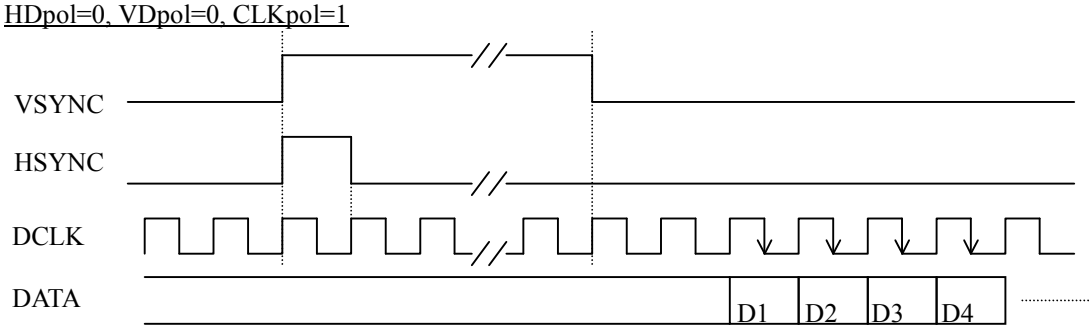
(23) VDpol : VSYNC polarity selection

VDpol	Function
0	Positive polarity
1	Negative polarity (Default)

HDpol=1, VDpol=1, CLKpol=0



HDpol=0, VDpol=0, CLKpol=1



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(24)CbCr: CbCr: Cb & Cr exchange position

CbCr='0'		Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3
CbCr='1'		Cr0	Y0	Cb0	Y1	Cr2	Y2	Cb2	Y3

(25) CSYNC : Separate SYNC or CSYNC input selection

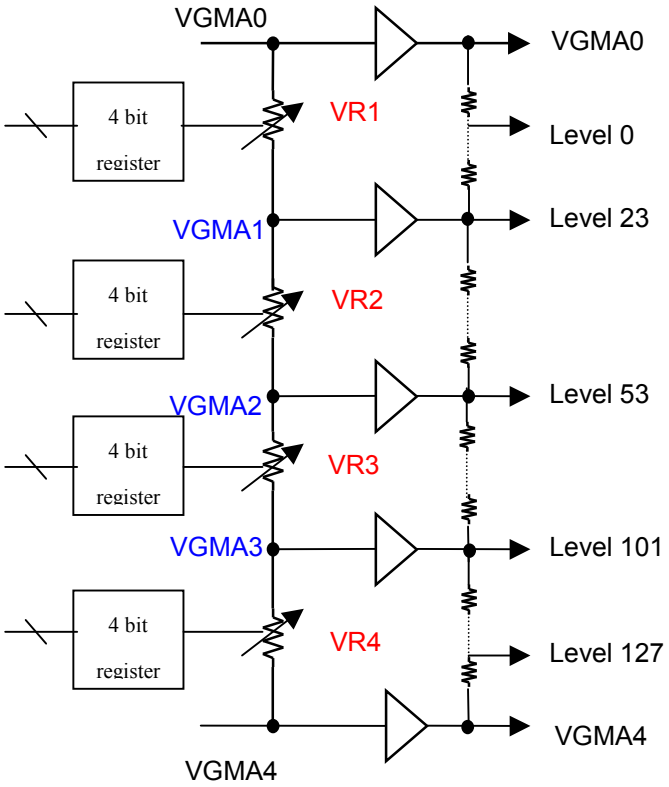
CSYNC	Function
0	CSYNC input
1	Separate SYNC input (Default)

When CSYNC ='0', CSYNC input from HSYNC pin

If YUV='1' & CSYNC='0' ,YUV is the input signal(VSYNC needs to pull high).

(26)Gamma_VR1, Gamma_VR2 , Gamma_VR3 , Gamma_VR4 : resistor range 8K(0000)~23K(1111)

(MSB-LSB)	Function
0000	8K
1000	16K (Default)
1111	23K



1, VGMA1,VGMA2,VGMA3 are generated within driver IC and adjustable through serial register setting

2. VR1,VR2,VR3,VR4 are adjustable through 4 bit registers

3. When FRP=L (Positive Polarity) VGMA0=3.7V,VGMA4=0V

4. When FRP=H (Negative Polarity) VGMA0=0V,VGMA4=3.7V

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(27)CONTRAST: RGB Contrast level setting, the gain changes (1/64)/bit

(MSB-LSB)	Function
00h	0
40h	1 (Default)
FFh	3.984

(28) SUB-CONTRAST : RB sub-contrast level setting, the gain changes (1/256) / bit

(MSB-LSB)	Function
00h	0.75
40h	1 (Default)
7Fh	1.246

(29) SUB-BRIGHTNESS : RB sub-bright level setting, setting accuracy: 1 step / bit

(MSB-LSB)	Function
00h	Dark (-64)
40h	Center (0) (Default)
7Fh	Bright (+63)

(30) PAIR : PAIR :Vertical start time setting for Odd/Even frame

UPS051 / UPS052 NTSC / UPS052 PAL(*)

PAIR(1:0)		VBLK ODD / EVEN	UNIT
X	0	21/21(default)	H
X	1	21/20	

CCIR656 NTSC/PAL(**)

PAIR(1:0)		VBLK ODD / EVEN	UNIT
0	0	22/22	H
0	1	22/23	
1	0	23/22	
1	1	23/23	

(*)The typical value of VBLK of UPS052 PAL(24 H) is different than UPS051/UPS052 NTSC(21H).

(**) The typical value of VBLK of CCIR656 PAL(24 H) is different than CCIR656 NTSC(22H).

Note :V-blanking must be adjusted based on the input data.

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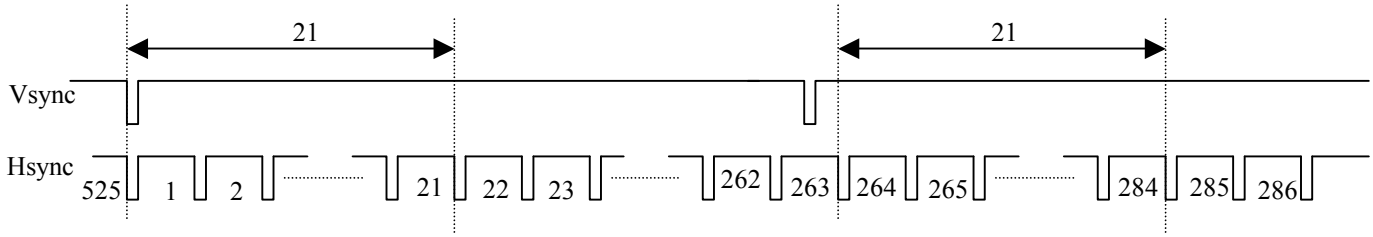

Field \ Line	PAIR=0		PAIR=1	
	START	END	START	END
ODD	22	261	22	261
EVEN	285	524	284	523

This table is based on VBLK=21.

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C. Optical specification (Note 1,Note 2, Note 3)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise	Tr	θ =0°	-	15	25	ms	Note 4, 6
	Fall	Tf		-	20	30	ms	
Contrast ratio		CR	At optimized viewing angle	120	300	-		Note 5, 6
Viewing angle	Top		CR≧10	-	45	-	deg.	Note 6, 7
	Bottom			-	60	-		
	Left			-	55	-		
	Right			-	55	-		
White Chromaticity		x	θ =0°	0.28	0.33	0.38		
		y	θ =0°	0.30	0.35	0.40		
Brightness		Y	θ =0°		250			Note 8

Note 1. Ambient temperature =25℃.

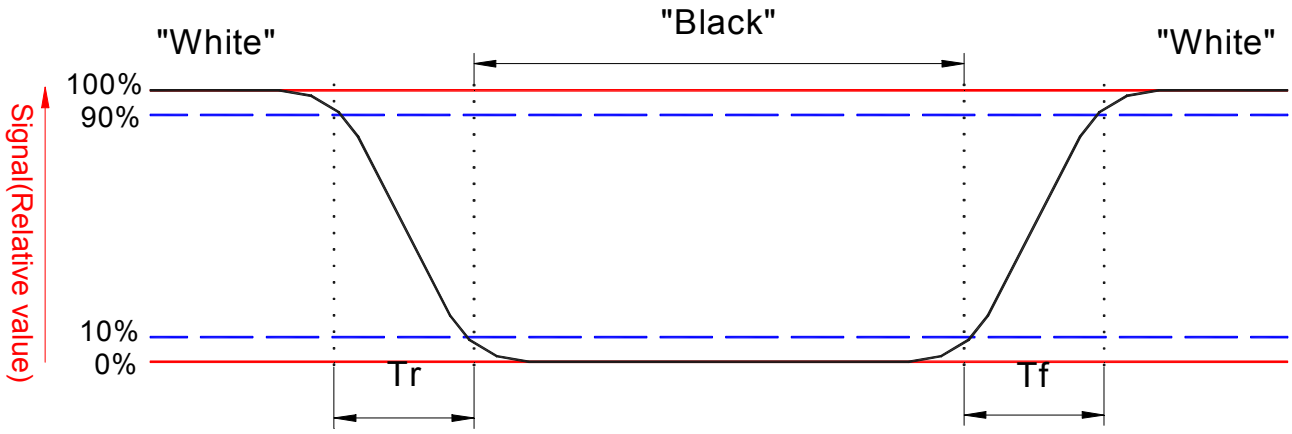
Note 2. To be measured in the dark room.

Note 3.To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. White $Vi=V_{i50} \pm 1.5V$

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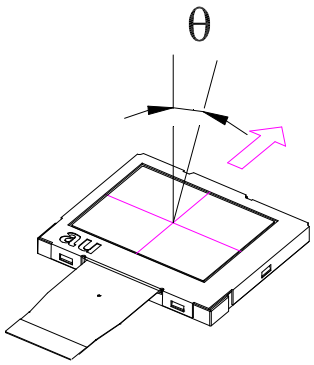
Black Vi=V_{i50} ± 2.0V
"±" Means that the analog input signal swings in phase with COM signal.

" ∓" Means that the analog input signal swings out of phase with COM signal.
V_{i50} : The analog input voltage when transmission is 50%
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle:
Refer to figure as below.



Note 8. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

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D. Reliability test items:

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 80℃ 240Hrs	
2	Low temperature storage	Ta= -25℃ 240Hrs	
3	High temperature operation	Ta= 60℃ 240Hrs	
4	Low temperature operation	Ta= 0℃ 240Hrs	
5	High temperature and high humidity	Ta= 60℃. 90% RH 240Hrs	Operation
6	Heat shock	-25℃~80℃/50 cycle 2Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration (with carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
9	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note: Ta: Ambient temperature.

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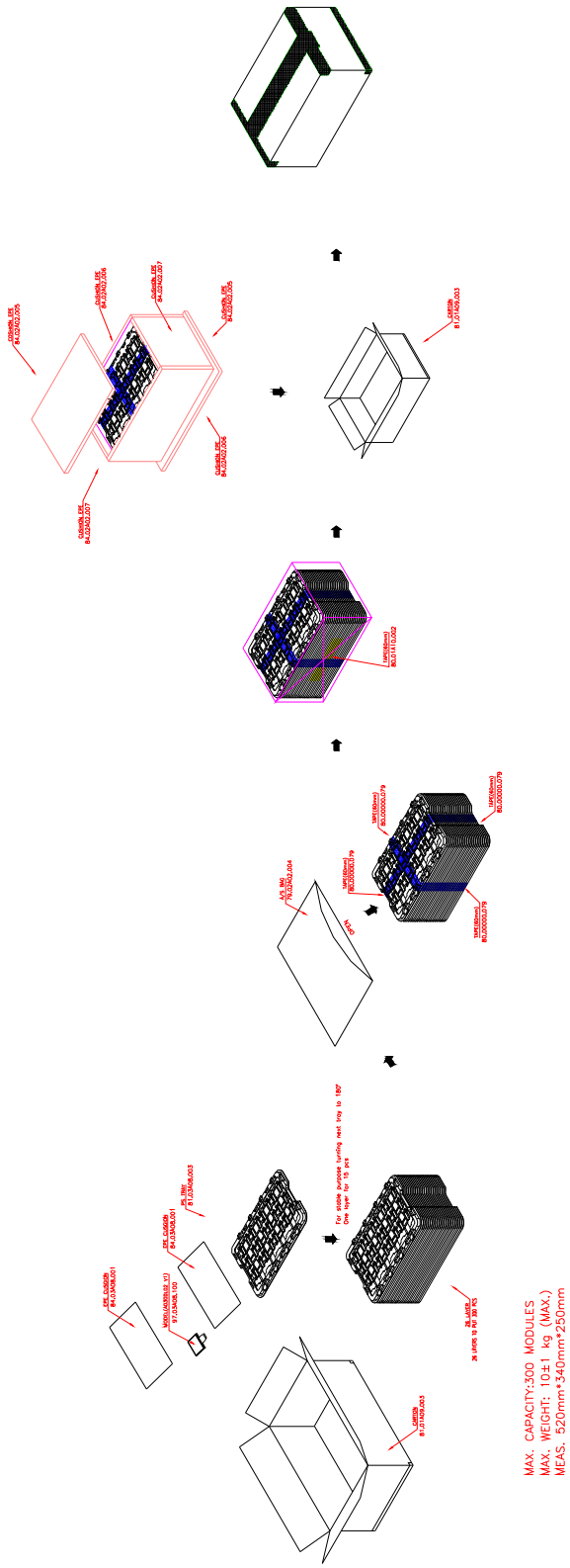
E. Packing form



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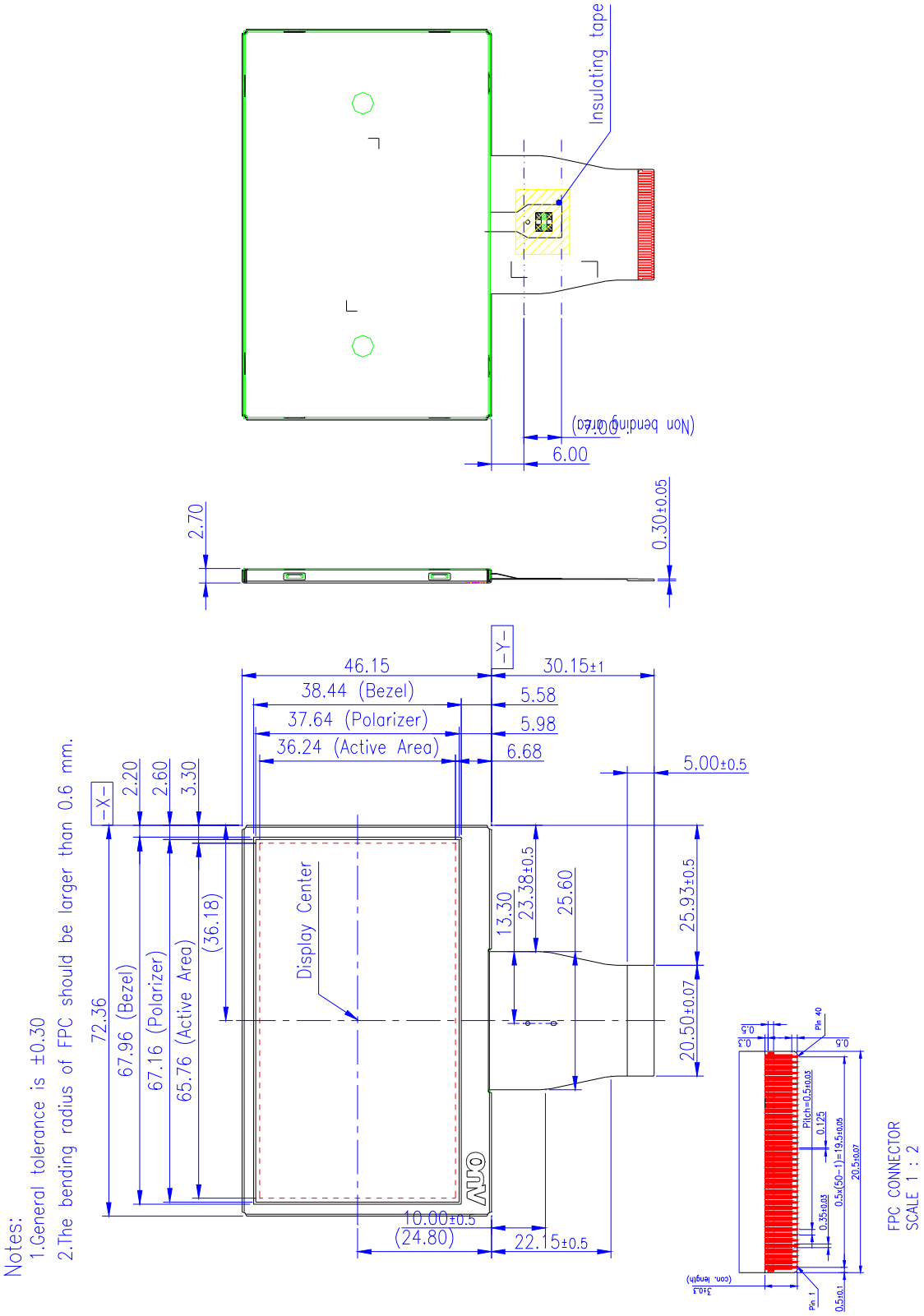

Fig. 9 Outline dimension of TFT-LCD module

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F. Application Notes

This LTPS TFT LCD module is designed for digital still camera application. A COG type LCD driver IC is integrated within this module, makes it much easier to design and cost-effective. The main features of integrated driver are:

- Accepting digital serial R, G, B 8-bit signal, fewer adjustment, fewer design effort, and lower power consumption compared to other analog LTPS solution.
- Integrated timing controller for UPS051 and UPS052 input timing formats. For UPS052 input timing, the input signal is always the same for different panel resolution.
- Integrated LED power converter controller, DC-DC charge pump, and Vcom driver. A design requires less peripheral components and reduces the total system cost.

1. Input Data Timing

Two kinds of input timing format are supported: UPS051 and UPS052. In UPS051 input format, the conversion of image data to display dots is controled by the user. In UPS052 input format, the mapping of incoming data to display dots is take cared by built in scaling function of driver IC.

For UPS051 timing, the module accpet one dot video data at the rising edge of DCLK, and display them one dot by one dot. Therefore the input data timing is different according to different panel resolutions and scan directions. Refer to the AC Timing of UPS051 part, you can use the typ. value for a typical case, or you can use the min. value to lower down the power consumption and EMI.

Because of delta color filter arrangement, the RGB data sequence for even and odd lines are different based on scan direction. For the definition of even and odd lines, see Fig. 10.

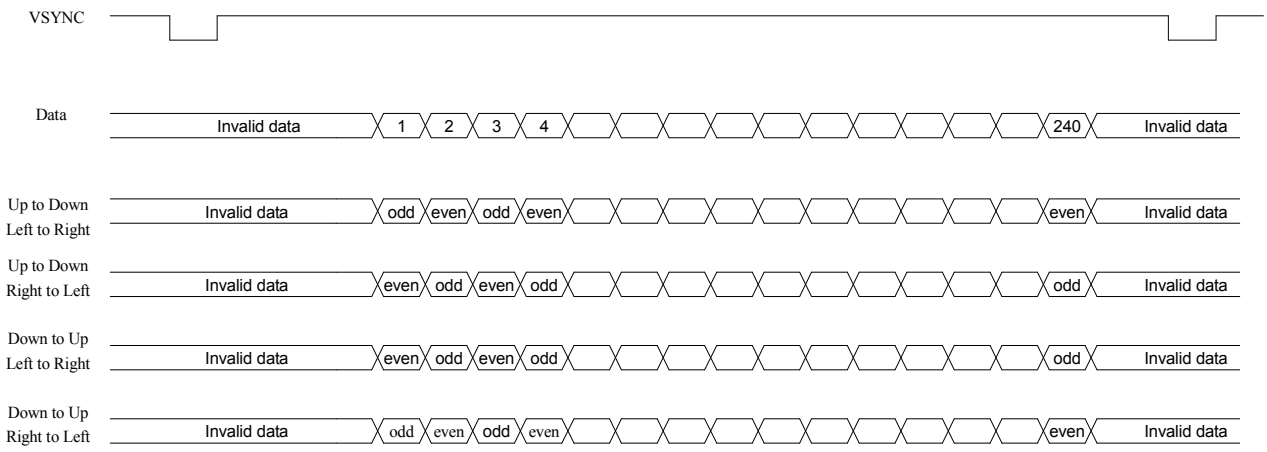

Fig 10. UPS051 even and odd lines definition

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For the RGB sequence, see Fig. 11.

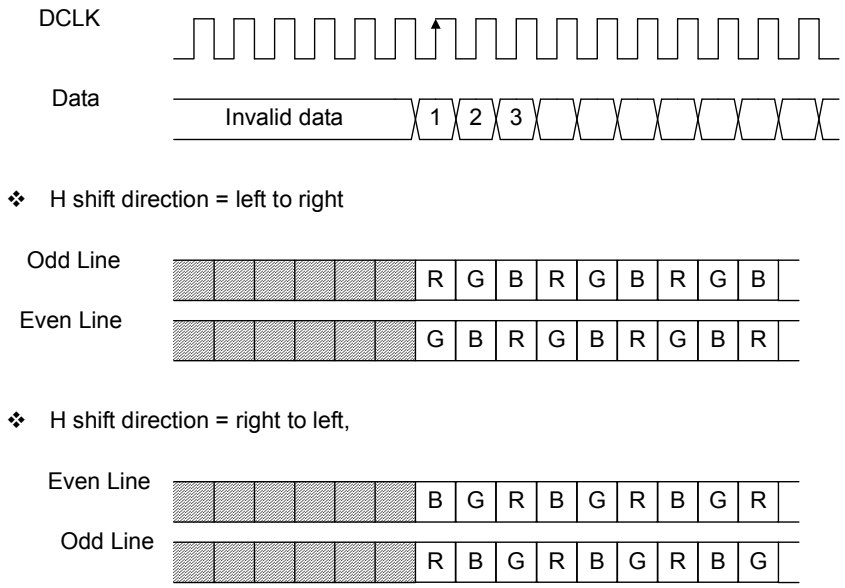

Fig. 11 UPS051 Input RGB sequence for 960x240 resolution

For the color filter arrangement, see Fig. 12.

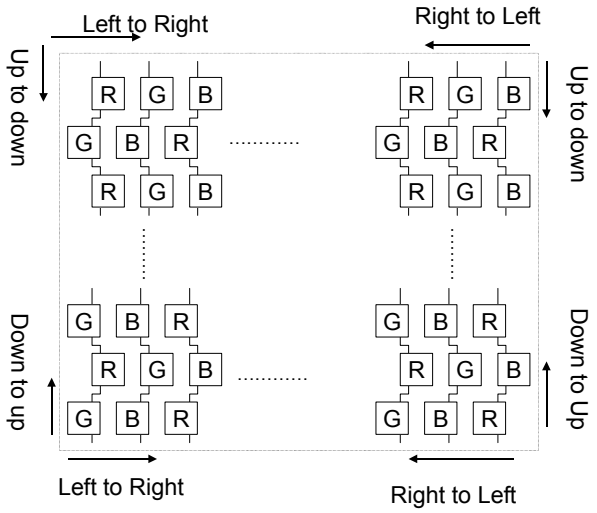

Fig. 12 Color filter arrangement for 960x240 resolution

For UPS052 timing, there are two input RGB data modes to choose from: 320xRGB and 360xRGB. Input data is processed and mapped to display dots by integrated driver IC according to panel resolution and scan direction settings. UPS052 input format saves the effort of data scaling for users and keeps a consistent interface for different display resolutions, in the cost of higher input data rate and less image processing elasticity. An additional NTSC/PAL auto-detection function is provided for UPS052 input format. When the function is active, the HSYNC and VSYNC inputs are monitored. If there are more than 288 HSYNC in a VSYNC period, it is detected as the PAL mode (288 active lines). On the other hand, if there are less than 288 HSYNC in a

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VSYNC period, it is asserted as the NTSC mode (240 active lines). Please refer to the serial control setting for more details.

For vertical input timing, both UPS051 and UPS052 accept odd / even field switching or single field only input.

For detail timing spec., please refer to Fig 2 and Fig 4.

2. Typical Application Circuit

2-1. Internal LED booster circuit

The integrated driver IC provides build-in LED booster controller, DC-DC charge pump, and Vcom driver. See Fig. 13 for the application circuit.

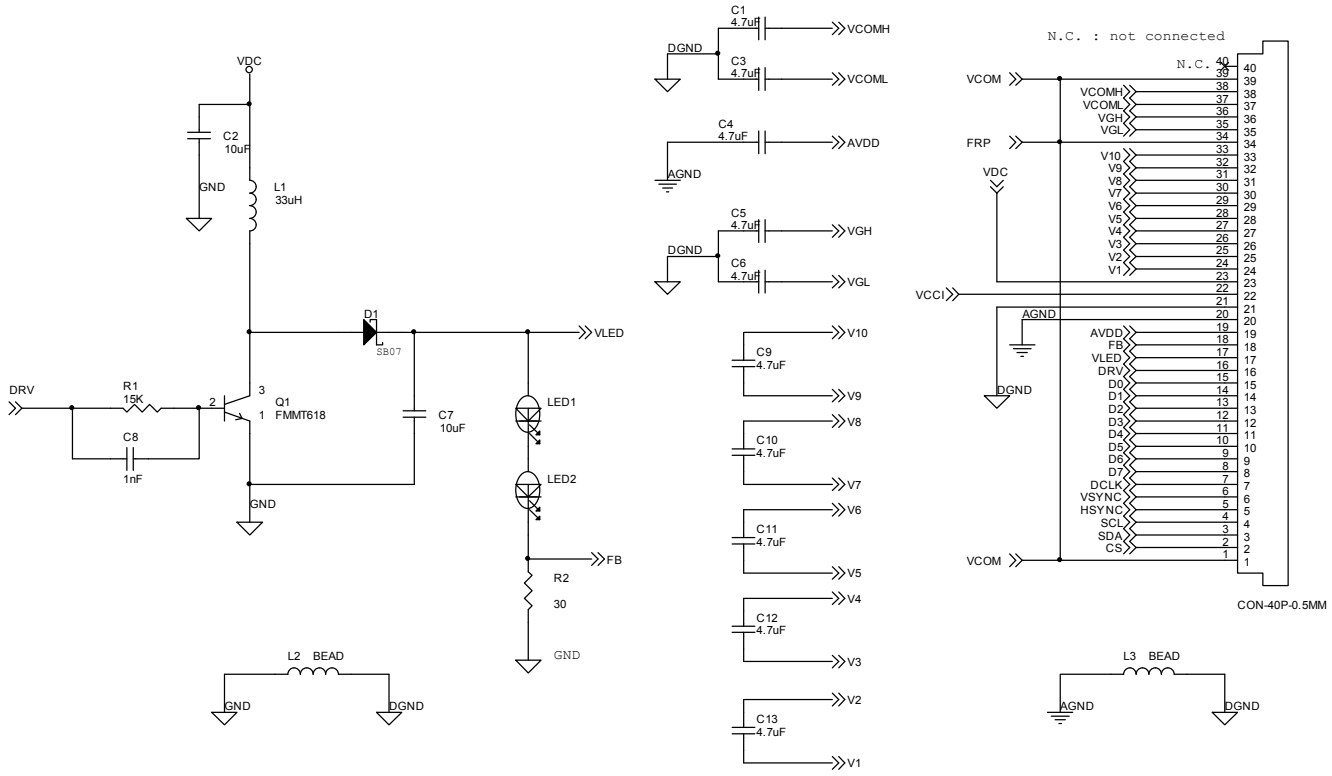

Fig.13 Typical Application Circuit

Power supply VDC (typical 3.3V) and VCCI (typical 3.3V) are required to provide driver IC power and generate all necessary voltages for LCD related circuits.

According to Fig. 13, the L1, Q1, D1,and C7 together form the LED boost converter. The converter with 0.75V feedback (FB) and R2 provide a constant 25mA current for LED backlight unit. The boost converter switching signal DRV is generated base on divided frequency of DCLK. Therefore the DCLK input is required for LED driver operation, and the absent of DCLK signal during normal operation will set the driver IC into standby mode. A low ESR capacitor for C7 is recommended in order to reduce voltage ripple of VLED. The build-in LED boost controller is default active, and it is able to be turned off by setting the register SHDB1 to low.

The positive (VGH) and negtive (VGL) power supplies for LCD are generated through build-in DC-DC charge pump circuit, an elegant design with only seven passive power-setting capacitors are required.

The LED booster circuit may cause the wave like phenomenon, In order to reduce the phenomenon ,AGND and DGND (system GND) and LED booster circuit GND must be separated.

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If user wants higher DC-DC charge pump efficiency or to fine-tune the LED current , using external LED driver circuit is an alternative choice.

<Note> : The charge pump frequency is about 7~8KHz, which can be heard by human. To prevent this signal from being amplified by microphone or other audio recorder, C9~C13 are suggested to be kept as far away as possible from these devices.

2-2. External LED driver circuit

See Fig. 14 for the application circuit.

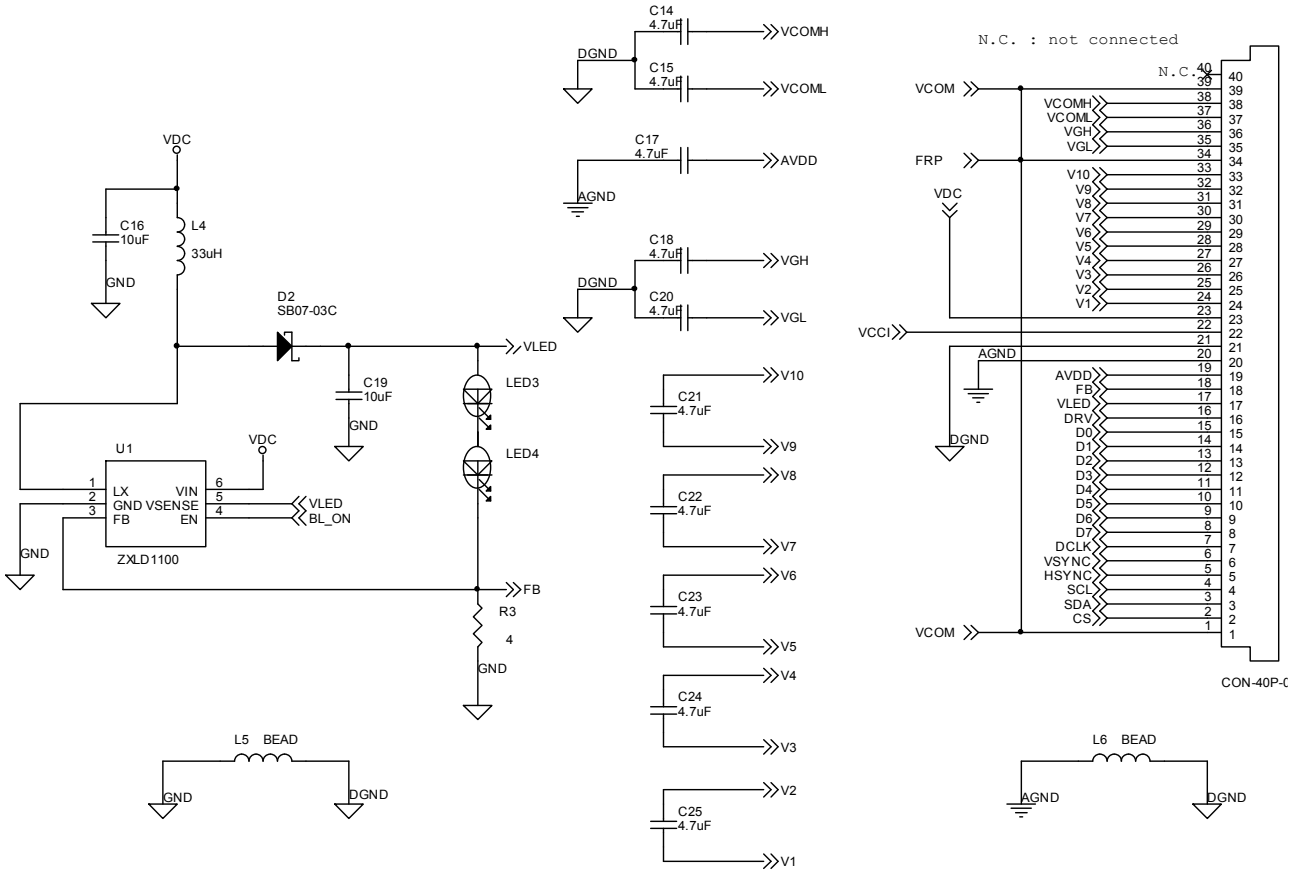

Fig.14 External LED driver Circuit

Power supply VDC (typical 3.3V) and VCCI (typical 3.3V) are required to provide driver IC power a generate all necessary voltages for LCD related circuits.

According to Fig. 14, the LED driver(ZXLD1100) and R3(4 ohm) with 0.1V feedback (FB) can provid constant 25mA current for LED backlight unit. To control the back light on/off timing, user should create a cor signal BL_ON (please refer to the ZXLD1100 date sheet). The LCD driver output DRV signal can also be used to drive BL_ON.

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<Note> : The charge pump frequency is about 7~8KHz, which can be heard by human. To prevent this signal from being amplified by microphone or other audio recorder, C21~C25 are suggested to be kept as far away as possible from these devices.

3. Power ON/OFF Sequence

The register setting of standby mode disabling / enabling is used to control the build-in power on / off sequence.

3-1 Power On (Global Reset and Standby Disabling)

After V_{DC}/V_{CCI} power on reset, VSYNC/HSYNC/DCLK/DATA can be input, and serial control interface is also operational. To ensure that panel can be lighted on successfully, the first step is setting global reset (register #5 "16(hex)") as the timing in Fig. 16. Then the LCD driver is in default standby mode after V_{DC}/V_{CCI} power-on, and setting register #5 bit #0 to high (STB=1) to disable the standby mode is required for normal operation. When the standby mode is disabled, a build-in power on sequence is started. The driver IC analog power AVDD is turned on first, and then the LCD positive and negative power supplies VGH/VGL are pumped, and followed by the LED power VLED. Since we recommend using external LED driver, the BL_ON signal (see Fig.15) should be provided at this time. Please refer to Fig.15 and Fig. 16 for the detail timing of power on/off sequence, especially the global reset timing in Fig. 16.

3-2 Power Off (Standby Enabling)

When the register #5 bit #0 is set to low (STB=0) to enable standby mode, a build-in power off sequence is started. Please refer to Fig.15 for the detail timing. No serial command programming is allowed right after standby mode is enabled, for a time period of minimum 5 fields (1 field: NTSC=16.6msec / PAL=20msec).

3-3 Clock Stop Reset

The DCLK signal is required for normal operation. When the DCLK is stopped for more than 5.6μsec (or DCLK frequency < 140KHz) during normal operation, the driver IC will be reset and operated in standby mode. This DCLK stop reset does not affect the serial interface settings.

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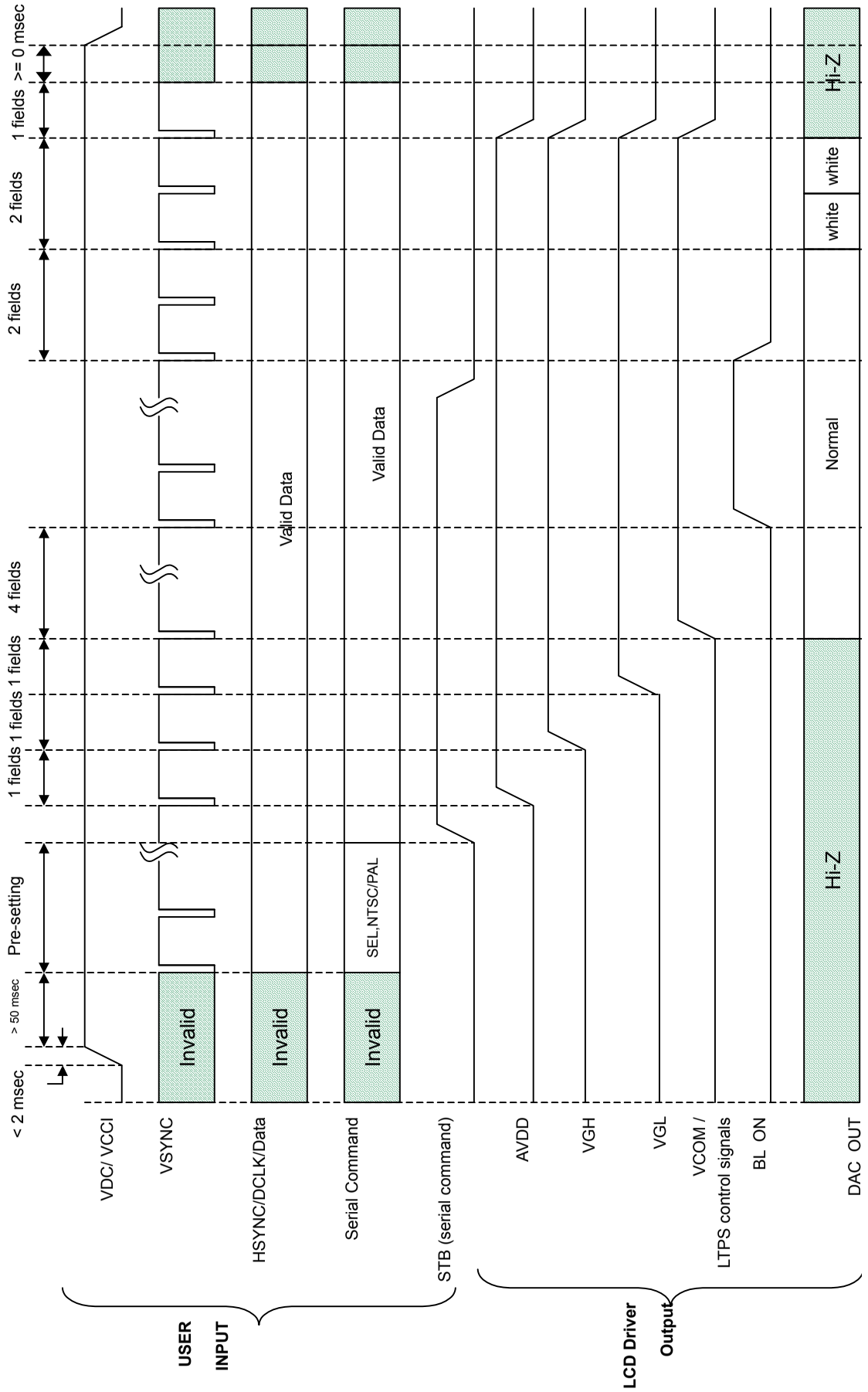

Fig.15 Power ON / OFF Sequence

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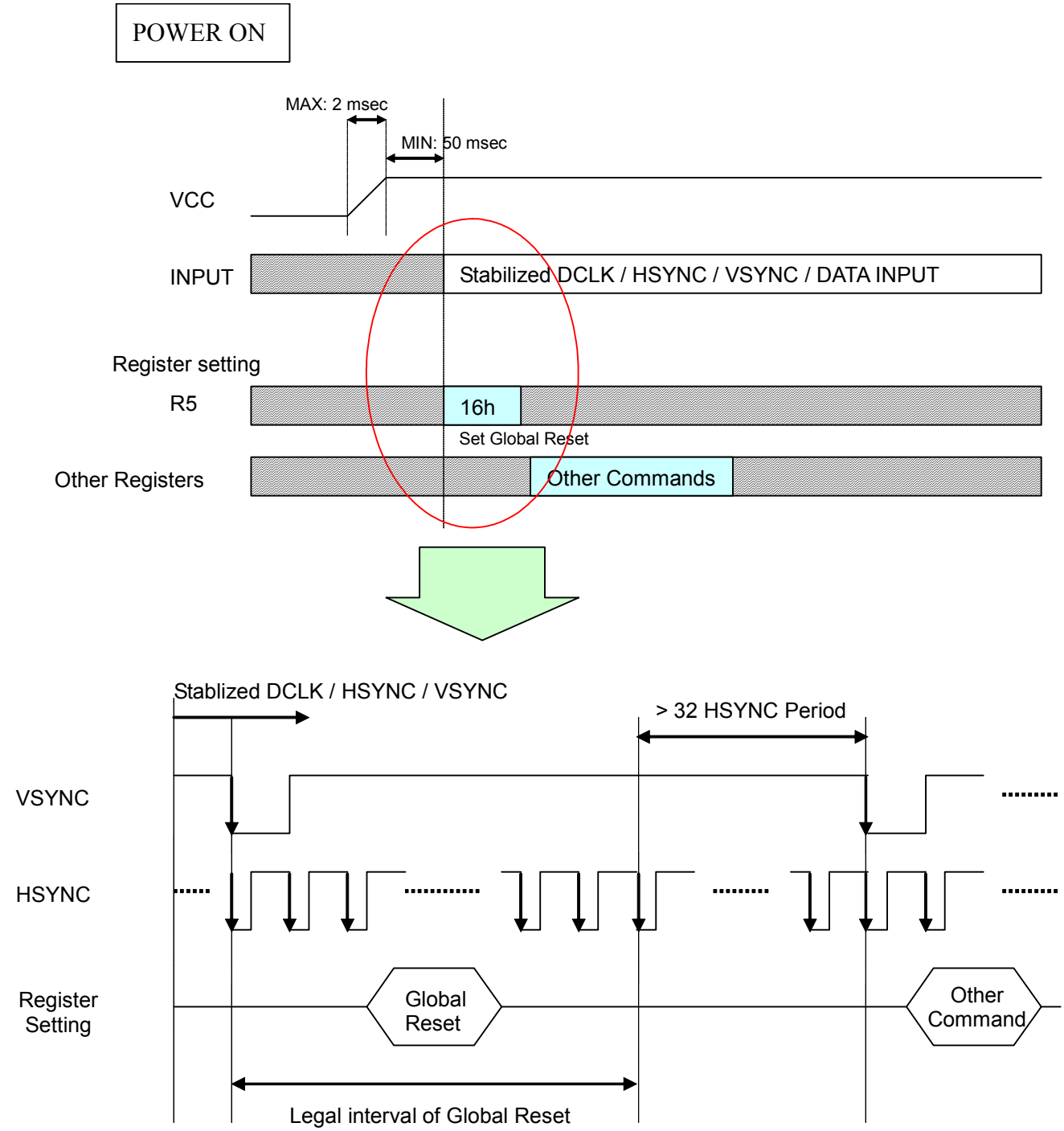

Fig.16 Legal Timing of Global Reset

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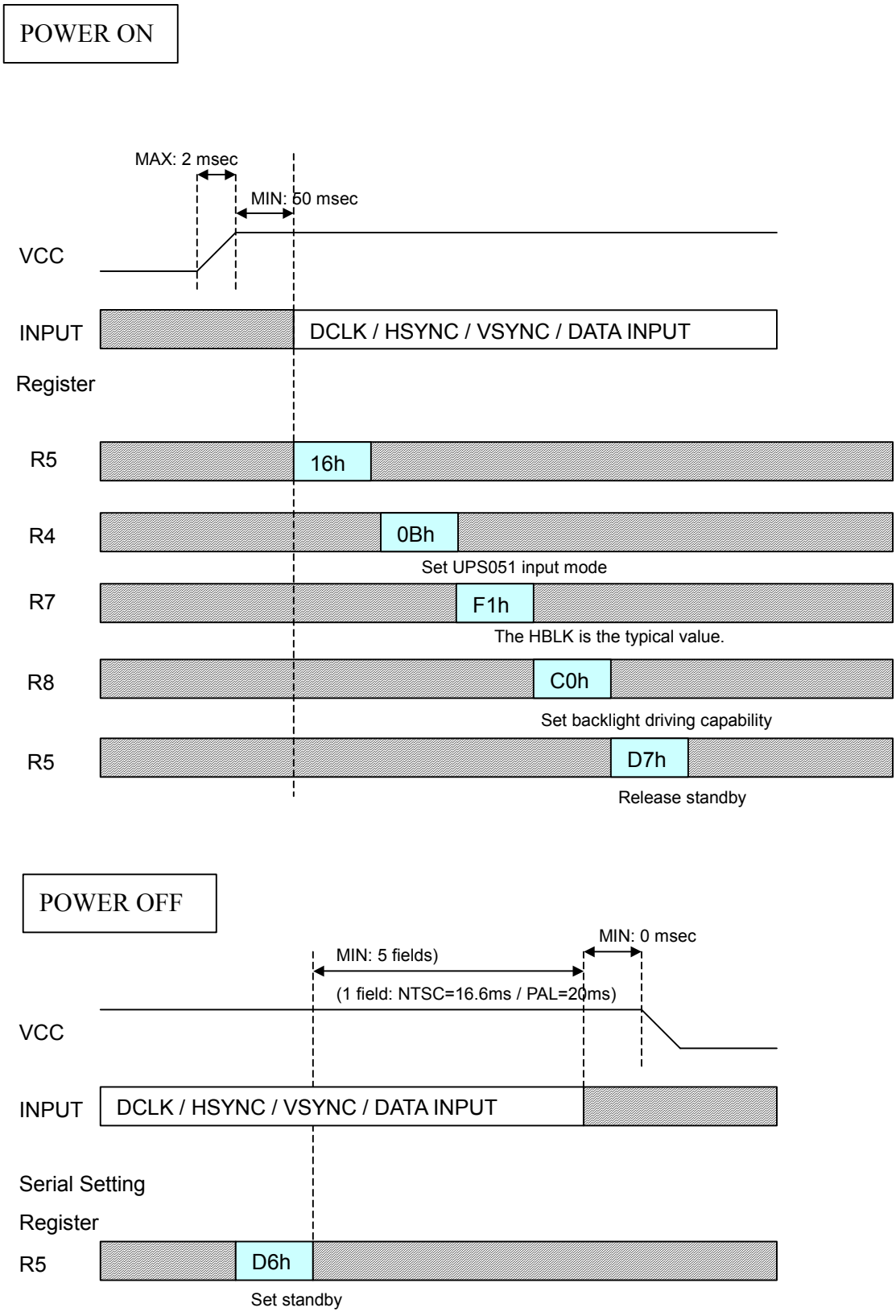

Fig.17 Recommend serial command settings for UPS051

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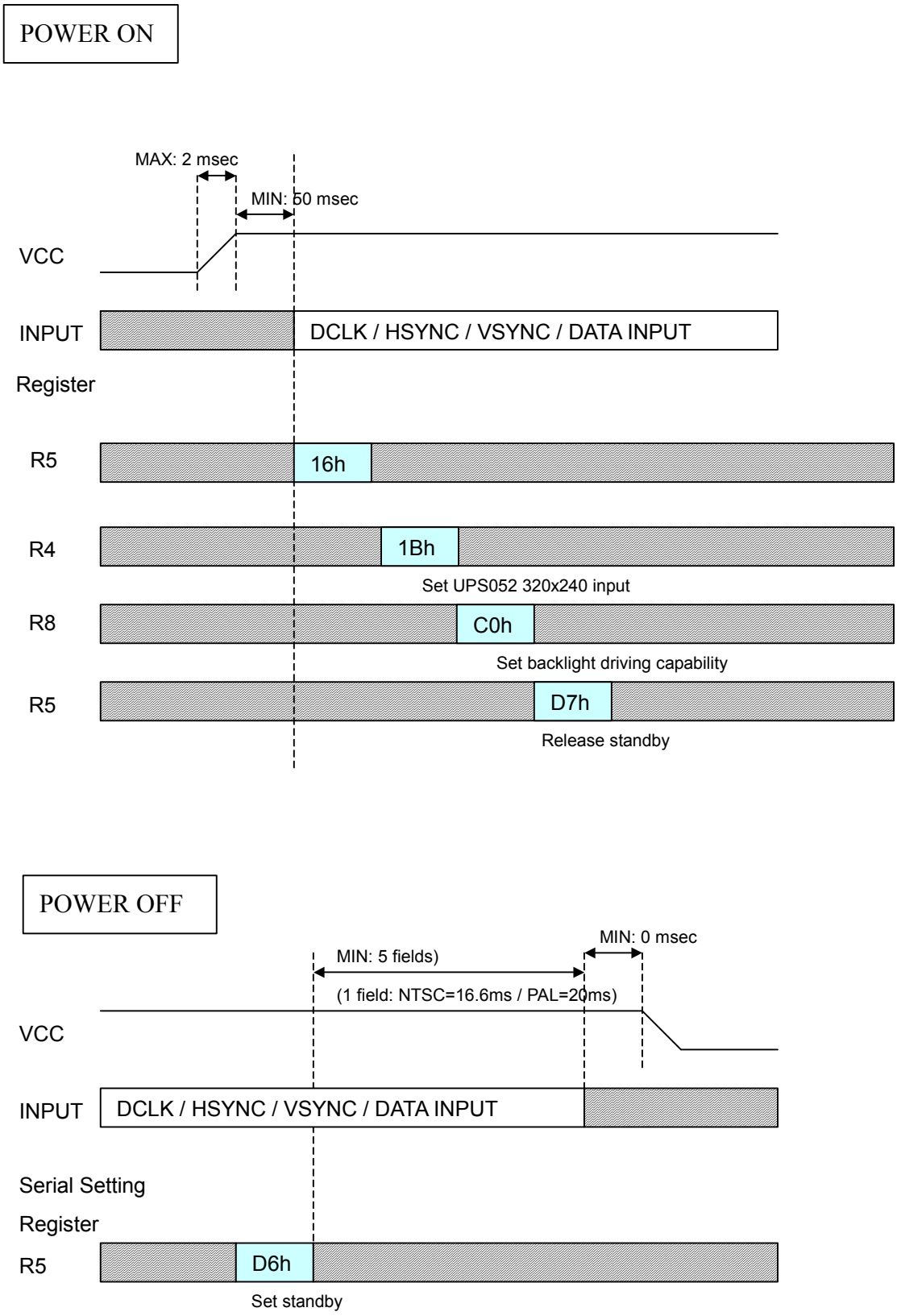

Fig.18 Recommend serial command settings for UPS052 320x240

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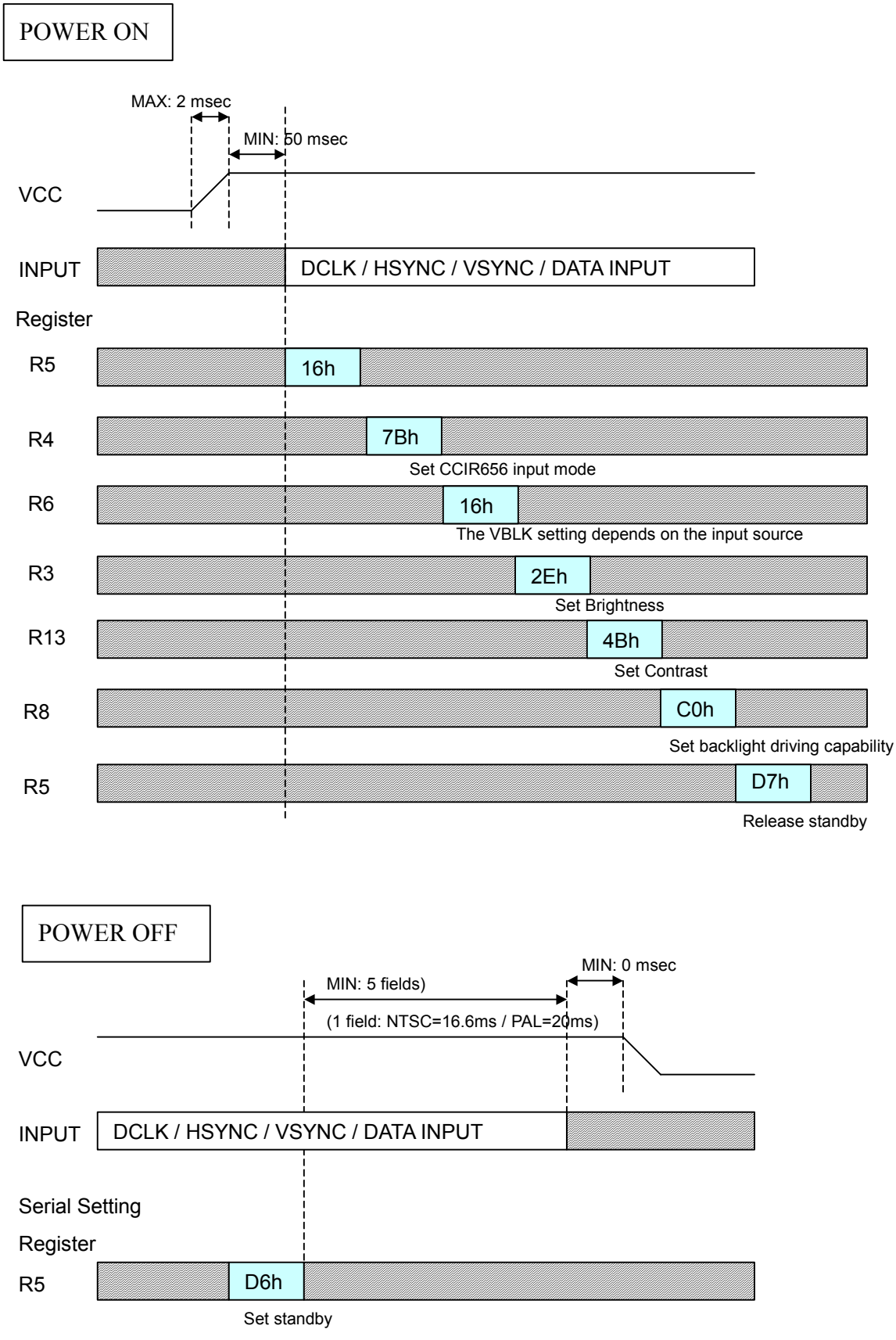

Fig.19 Recommend serial command settings for CCIR656

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