Doc. Version	1.2
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Date	2007/11/12

Product Specification

3.5” COLOR TFT-LCD MODULE

MODEL NAME: A035QN01 V4

(compatible for both 97.03A09.400 and 97.03A09.4S0)

< > Preliminary Specification

< ◆ > Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.1	2006/10/04	5	Modify outline dimension
		7	Correct the note of pin assignment
		10	Revise the timming condition
		16	Add luminance uniformity in to optical spec.
0.2	2006/11/16	23	Add application circuit
0.3	2006/11/17	7	Add note 1, 2 & 4
		8	Correct the LED limit curve
		9	Modify note 1
0.4		6, 7	POL & ENB voltage range VDD/GND
		8	Remove note 4, POL & VCOM phase
0.5	2006/12/22	5	Revise outline drawing
		6	Revise pin description 8 to 11
		8	Revise electrical characteristics (AVDD)
		9	Revise electrical characteristics and note 2
		20	Revise FPC pin assignment description
		24-26	Revise diagrams and circuits
0.6	2007/01/12	4	Add Color Gamut
		11-13	Add timing condition
		14-17	Revise command register R3
		18	Add R, G, B color coordinate
		25	Revise power on/off sequence
0.7	2007/01/30	11-13	Revise Vsync setup time and hold time definition
		18	Revise Contrast Ratio and Gamma value
		22	Add T/P Maker and Haze percentage
		26	Add power on/off sequence notice
0.8	2007/2/12	5	Modify outline dimension
		6-7	Modify pin assignment remark
		11-12	Add ENB signal illustration and revise timing condition
0.9	2007/5/28	9	Add cuurent consumption of electrical characteristics.
1.0	2007/5/31	5	Add Mylar tape position on the drawing
1.1	2007/7/24	11	Revise AC timing condition
1.2	2007/11/12	5	Modify outline dimension

Contents:

A. General Description

A035QN01 V4 is an amorphous transmissive type Thin Film Transistor Liquid crystal Display (TFT-LCD). This model is composed of a TFT-LCD, drive and gate IC's, an FPC (flexible printed circuit), a backlight unit and a touch panel.

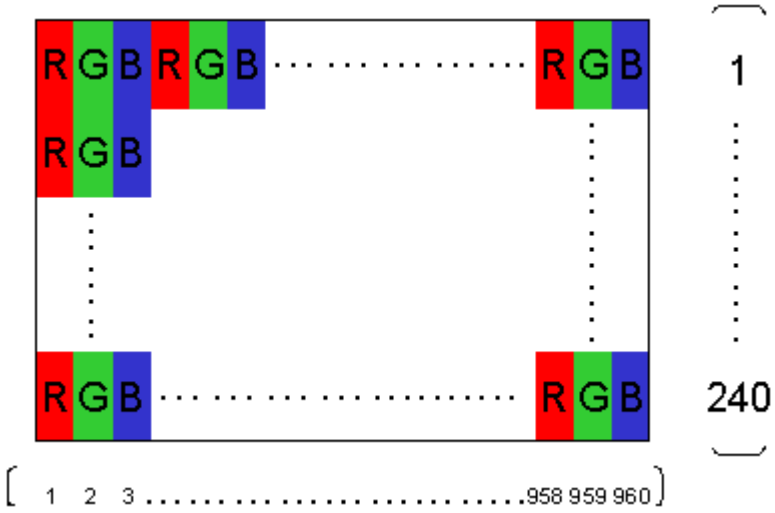
B. Features

- 3.5-inch display size with touch panel
- QVGA resolution in RGB stripe dot arrangement
- High brightness
- 3-wire register setting
- Interfaces: parallel RGB 24-bit
- 3-in-1 FPC for LCD signals, backlight LED power and touch panel
- Wide viewing angle
- Integrated touch screen panel (resistance type)
- Green design

C. Physical Specifications

NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	320 RGB (H)×240(V)	
2	Active Area	mm	70.08(H)×52.56(V)	
3	Screen Size	inch	3.5(Diagonal)	
4	Dot Pitch	mm	0.073(H)×0.219(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	16.7M Colors	Note 2
7	Overall Dimension	mm	76.9(H) × 63.9(V) × 4.23(T)	Note 3
8	Weight	g	42.9	
9	Panel surface treatment	--	Hard coating 3H	
10	Display Mode	--	Normally White	
11	Color Gamut	%	60	

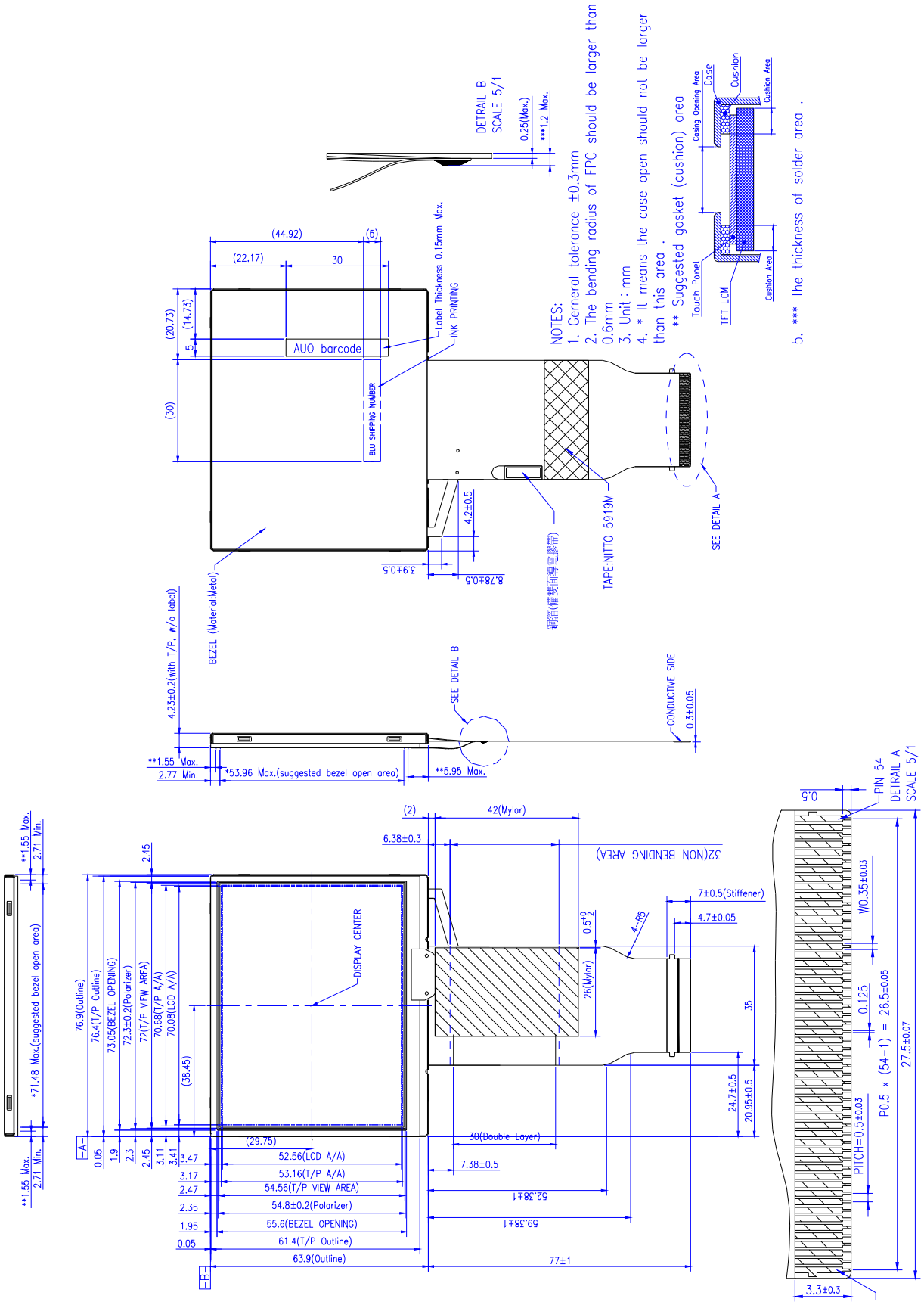
Note 1: Below figure shows dot stripe arrangement.



Note 2: The full color display depends on 8-bit data signal (pin12~35).

Note 3: Not include FPC. Refer to the next page for further information.

D. Outline Dimension



E. Electrical Specifications

1. Pin Assignment

No.	Pin Name	I/O	Description	Remarks
1	LED_Cathode	I	Backlight LED Cathode	
2	LED_Cathode	I	Backlight LED Cathode	
3	LED_Anode	I	Backlight LED Anode	
4	LED_Anode	I	Backlight LED Anode	
5	NC	-	Not Connected	
6	RESET	-	Reset	
7	POL	O	The Signal to Generate VCOM	Note 1
8	Y1	I/O	Touch Panel Top Electrode	
9	X1	I/O	Touch Panel Right Electrode	
10	Y2	I/O	Touch Panel Bottom Electrode	
11	X2	I/O	Touch Panel Left Electrode	
12	B0	I	Blue Data Bit 0	
13	B1	I	Blue Data Bit 1	
14	B2	I	Blue Data Bit 2	
15	B3	I	Blue Data Bit 3	
16	B4	I	Blue Data Bit 4	
17	B5	I	Blue Data Bit 5	
18	B6	I	Blue Data Bit 6	
19	B7	I	Blue Data Bit 7	
20	G0	I	Green Data Bit 0	
21	G1	I	Green Data Bit 1	
22	G2	I	Green Data Bit 2	
23	G3	I	Green Data Bit 3	
24	G4	I	Green Data Bit 4	
25	G5	I	Green Data Bit 5	
26	G6	I	Green Data Bit 6	
27	G7	I	Green Data Bit 7	
28	R0	I	Red Data Bit 0	
29	R1	I	Red Data Bit 1	
30	R2	I	Red Data Bit 2	
31	R3	I	Red Data Bit 3	
32	R4	I	Red Data Bit 4	
33	R5	I	Red Data Bit 5	

34	R6	I	Red Data Bit 6	
35	R7	I	Red Data Bit 7	
36	HSYNC	I	Horizontal Sync Input	
37	VSYNC	I	Vertical Sync Input	
38	DCLK	I	Dot Data Clock	
39	AVDD	I	Analog Power	
40	AVDD	I	Analog Power	
41	VDD	I	Digital Power	
42	VDD	I	Digital Power	
43	SPENA	I	SPI Interface Data Enable Signal	Note 3
44	NC	-	Not Connected	
45	VGL	I	Gate Off Power	
46	NC	-	Not Connected	
47	VGH	I	Gate On Power	
48	NC	-	Not Connected	
49	SPCLK	I	SPI Interface Clock	Note 3
50	SPDAT	I	SPI Interface Data	
51	VCOM	I	Driving Input	Note 1
52	ENB	I	Data Enable Input	Note 2
53	GND	I	Ground	
54	GND	I	Ground	

I: Input pin; O: Output pin

Note 1. The polarity of VCOM should be generated from POL through driving circuit. The H/L voltage level of POL is VDD/GND. Hence, it cannot be used as Vcom signal directly. The phase shift from POL to Vcom can be set as either 0° or 180° by 3-wire SPI interface.

Note 2. For digital RGB input data format, both SYNC mode and DE+SYNC mode are supported. If ENB signal is fixed low, SYNC mode is used. Otherwise, DE+SYNC mode is used.

Note 3. SPENA、SPCLK are usually pulled high.

2. Absolute Maximum Ratings

Items	Symbol	Values		Unit	Condition
		Min.	Typ.		
Power Voltage	AVDD	-0.3	7.0	V	AVSS=0
	VDD	-0.3	7.0	V	GND=0
	VGH	-0.3	32.0	V	GND=0
	VGL	-22.0	+0.3	V	GND=0
	VGH-VGL	-0.3	+45	V	GND=0
Input Signal Voltage	Vi	-0.3	AVDD+0.3	V	
	VI	-0.3	VDD+0.3	V	
LED Reverse Voltage	Vr	-	3.6	V	One LED
LED Forward Current	If	-	28	mA	One LED, Note 4
Storage Temperature	T_{ST}	-10	70	˚C	Note 2
Operating Temperature (Ta)	T_{OP}	-0	60	˚C	Note 2, Note 3

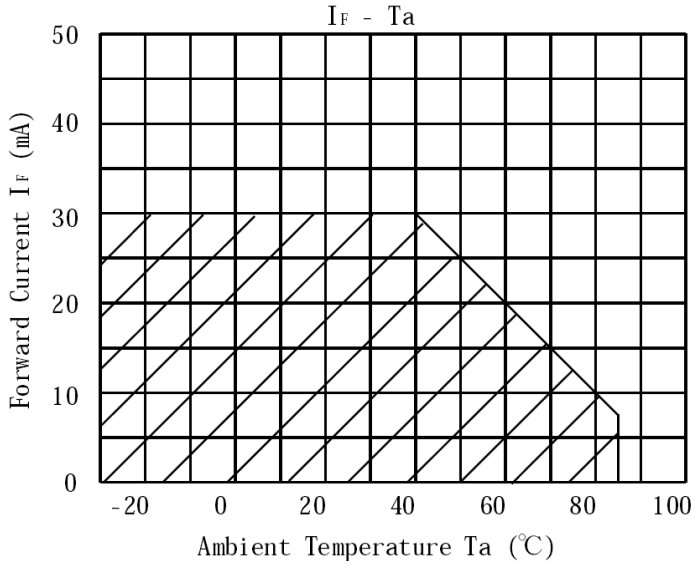
Note 1.If the operating condition exceeds the absolute maximum ratings, the TFT-LCD module may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, its reliability may drop.

Note 2. Temp. ≤60˚C, 90% RH MAX

Temp. >60˚C, Absolute humidity shall be less than 90% RH at 60˚C

Note 3. The LCD module operating temperature, excluding touch panel, is from -10 to 70˚C

Note 4. If LED current exceeds the limit curve, the lifetime will drop dramatically.



3. Electrical Characteristics

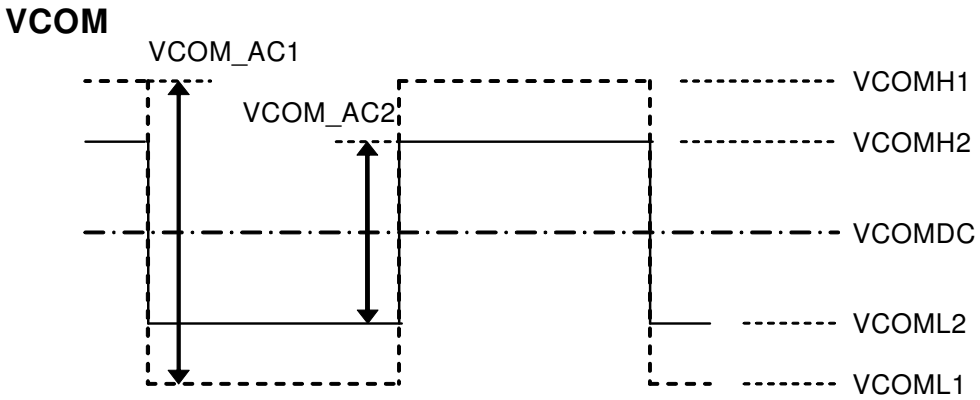
The following items are measured under stable condition and suggested application circuit.

a. TFT- LCD Panel (GND=0V)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Digital Power Supply	VDD	3	3.3	3.6	V	
Input Current for VDD	I_{VDD}	-	1	2	mA	Note 4
Analog Power Supply	AVDD	4.65	5	5.2	V	
Input Current for AVDD	I_{AVDD}	-	5.4	8	mA	Note 4
Gate On Voltage	V_{GH}	14	16	18	V	
Input Current for VGH	I_{VGH}	-	50	100	uA	Note 4
Gate Off Voltage	V_{GL}	-11	-10	-8	V	
Input Current for VGL	I_{VGL}	-	50	100	uA	Note 4
VCOM AC Amplitude	$V_{COM}AC$	4.65	5.0	5.35	V	Note 1, 4
VCOM DC Voltage	$V_{COM}DC$	1.81	1.89	1.97	V	Note 1, 4
Frame Frequency	f_{Frame}	55	60	70	Hz	
Dot Data Clock	DCLK	-	6.4	7.0	MHz	

Note 1. Vcom AC=VCOMH - VCOML: Adjust the color with gamma data.

Note 2. Vcom DC=1.89+0.025*(26-(V_{GH}-V_{GL}))



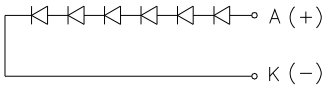
Note 3. Panel surface temperature should be kept less than content of section 3.2. “Absolute maximum ratings"

Note 4. Based on VDD=3.3V, AVDD=5.0V, VGH=16V, VGL=-10V, VCOMAC=5V, White pattern and application circuit in the page 27.

b. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Current	I_L	---	20	28	mA	single serial
LED Voltage	V_L	---	19.2	21.6	V	single serial
LED Life Time	L_L	10,000	---	---	Hr	Note 2, 3

Note 1: LED backlight is six LEDs serial type.



Note 2: The ”LED Supply Voltage” is defined by the number of LED at Ta=25°C, If=20mA. In the case of 6 pcs LED, V_{LED}=3.2*6=19.2V

Note 3: The ”LED life time” is defined as the time for the module brightness to decrease to 50% of the initial value at Ta=25°C, If=20mA

Note 4: The LED lifetime could be decreased if operating I_L is larger than 25mA

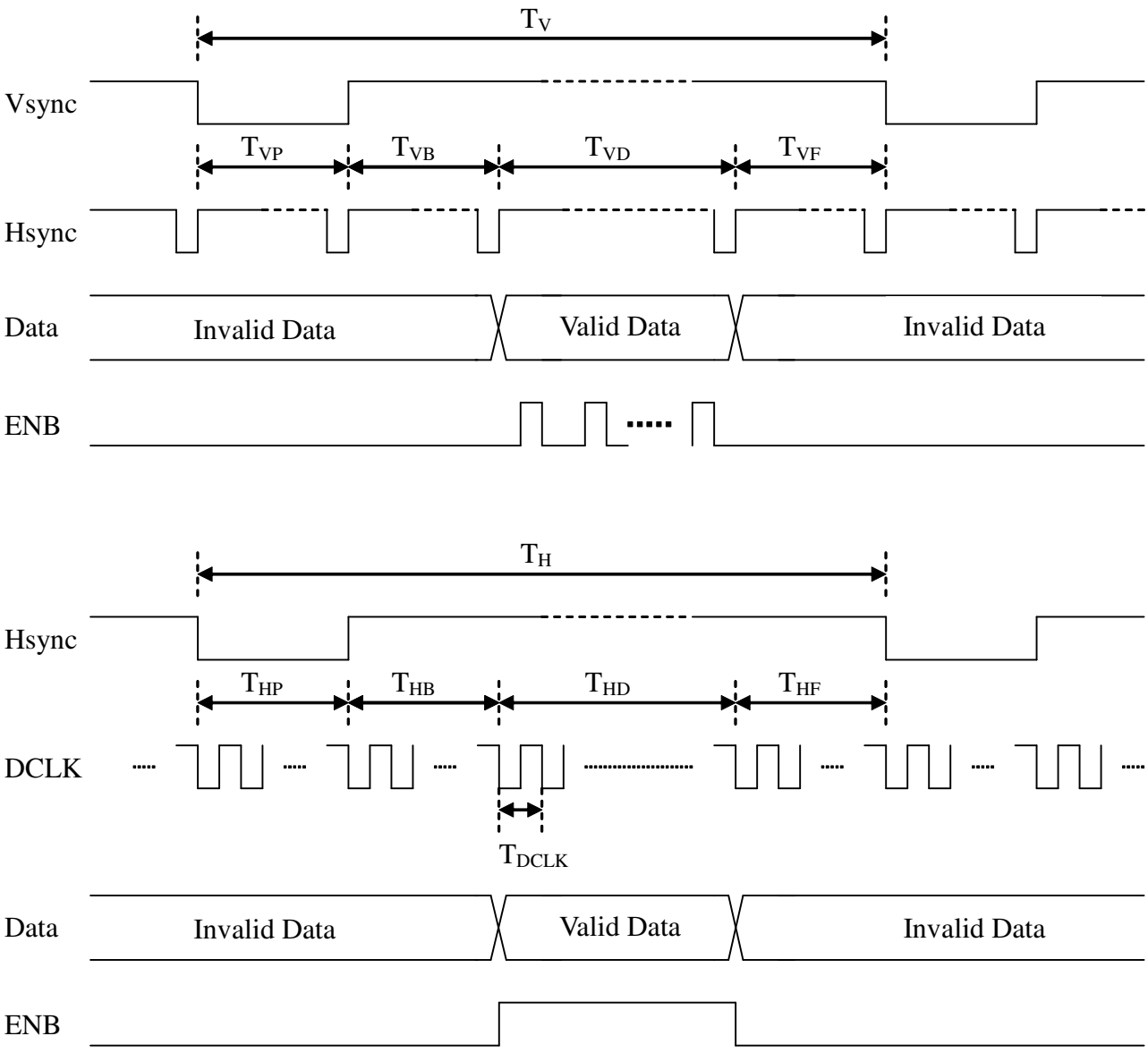
4. AC Timing

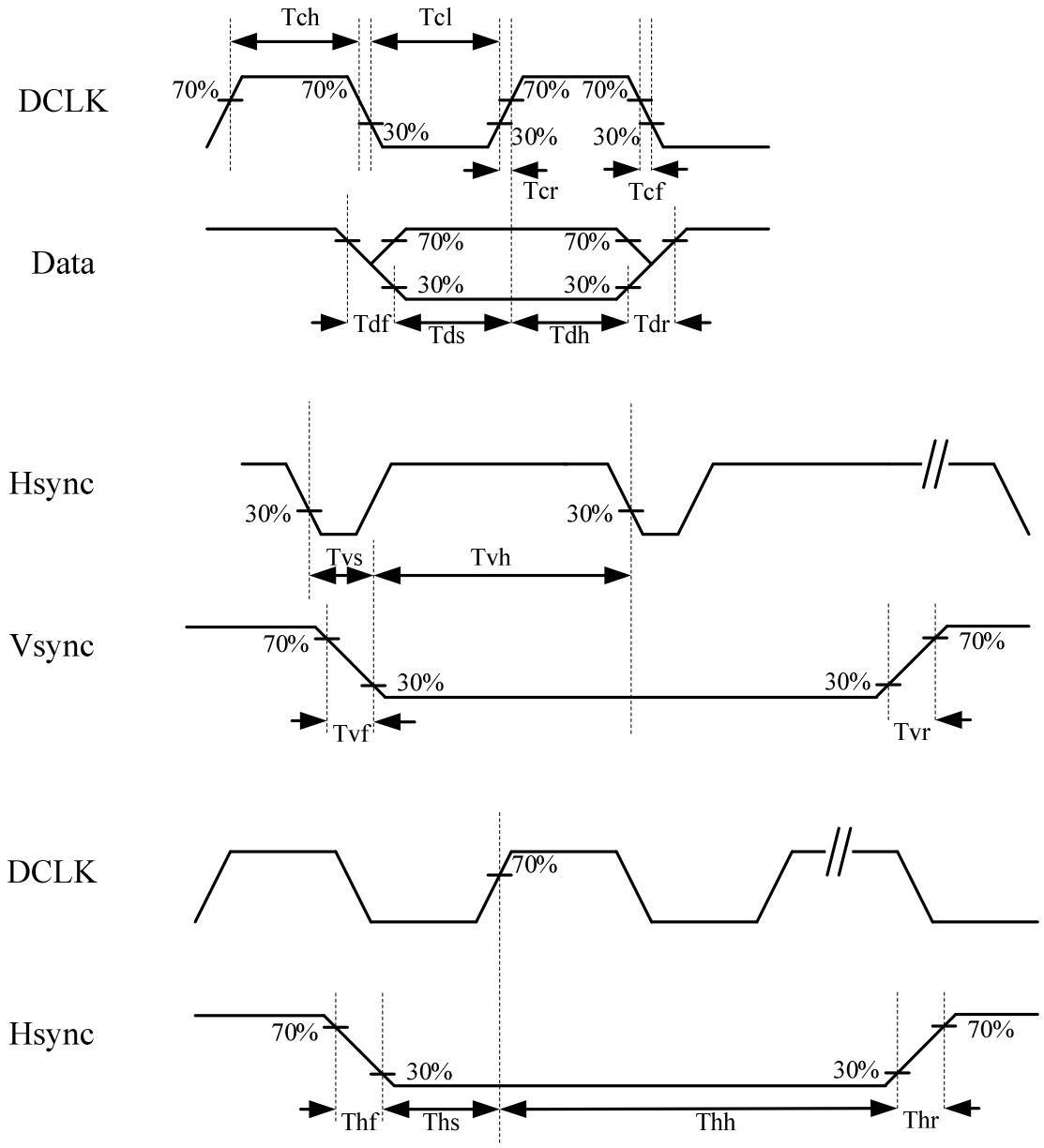
a. Timing Condition

Signal	Item		Symbol	Min	Typ	Max	Unit
DCLK	Frequency		f_{Dclk}	6	6.4		MHz
	High Time		Tch		78	80	ns
	Low Time		Tcl		78	80	ns
	Rising Time		Tcr			25	ns
	Falling Time		Tcf			25	ns
Data	Rising Time		Tdr			20	ns
	Falling Time		Tdf			20	ns
	Setup Time		Tds	12			ns
	Hold Time		Tdh	12			ns
HSYNC	Period		T_H		408	432	DCLK
	Pulse Width		T_{HP}	5	30		DCLK
	Back-Porch		T_{HB}		38		DCLK
	Display Period		T_{HD}		320		DCLK
	Front-Porch		T_{HF}		20		DCLK
	Rising Time		Thr		200	700	ns
	Falling Time		Thf		200	300	ns
	Setup Time		Ths	12			ns
	Hold Time		Thh	12			ns
VSYNC	Period	NTSC	T_V		262.5		TH
		PAL			312.5		
	Pulse Width		T_{VP}	1	3		TH
	Back-Porch	NTSC	T_{VB}		15		TH
		PAL			23		
	Display Period		T_{VD}		240		TH
	Front-Porch	NTSC	T_{VF}		4.5		TH
		PAL			46.5		
	Rising Time		Tvr		500	700	ns
	Falling Time		Tvf			1.5	us
	Setup Time		Tvs	12			ns
	Hold Time		Tvh	12			ns
VSYNC-ENB Time		NTSC	$T_{VSE}=T_{VP}+T_{VB}$		18		TH
		PAL			26		TH
HSYNC-ENB Time			$T_{HE=}T_{HP}+T_{HB}$		68		DCLK
ENB Pulse Width			T_{EP}		320		DCLK

b. Timing Diagram

Based on default register settings, the definitions of above timing symbols in the previous page are shown as below.





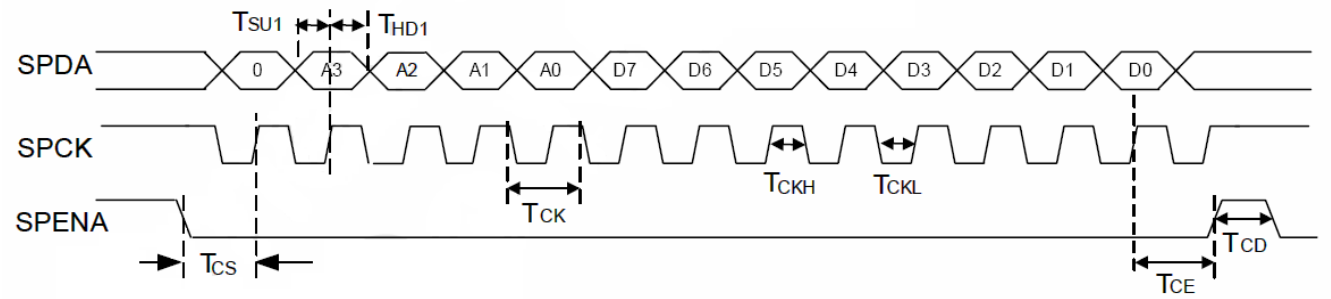
5. Command register map

a. Command timing : Serial Peripheral Interface

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SPCK period	T_{CK}	60	-	-	ns
SPCK high width	T_{CKH}	30	-	-	ns
SPCK low width	T_{CKL}	30	-	-	ns
Data setup time	T_{SU1}	12	-	-	ns
Data hold time	T_{HD1}	12	-	-	ns
SPENA to SPCK setup time	T_{CS}	20	-	-	ns
SPENA to SPDA hold time	T_{CE}	20	-	-	ns
SPENA high pulse width	T_{CD}	50	-	-	ns

b. Serial setting map

No.	Address				Register Data (default setting)							
	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	Reserved(0)	Reserved(0)	Reserved(0)	STHP(00h)				
R1	0	0	0	1	STVP(0h)				STVNT(00)		STVPAL(00)	
R2	0	0	1	0	Reserved(1)	RGBVPOL(0)	Reserved(1)	Reserved(0)	Reserved(1)	HS_POL(0)	NPC_IN(1)	NPC_SET(0)
R3	0	0	1	1	Reserved(1)	Reserved(0)	Reserved(01)		Reserved(0)	POL_OUT(0)	DE_POL(0)	DE_SEL(0)



c. Description of serial control data

c-1. R0

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0
R0	**0h**	Reserved(0)	Reserved(0)	Reserved(0)	STHP(00h)				

STHP [4:0]: adjust start pulse position by pixel

STHP [4:0]	STH position adjust by pixel
10h	-16
18h	-8
1Fh	-1
00h	0
08h	+8
0Fh	+15

c-2. R1

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0
R1	1h	STVP (0h)				STVNT (00)		STVPAL (00)	

STVP [3:0]: adjust first line position by line

STVP [3:0]	STV position adjust by line
8h	-8
Ch	-4
Fh	-1
0h	0
4h	+4
7h	+7

STVNT[1:0]: Adjust the relationship of first line of active video in Odd/Even Field in NTSC mode.

STVNT [1:0]	Function description
00	The first line of active video in Even Field = The first line of activevideo in Odd Field
01	The first line of active video in Even Field = The first line of active video in Odd Field + 1
10	No Use
11	The first line of active video in Even Field = The first line of active video in Odd Field – 1

STVPAL[1:0]: Adjust the relationship of first line of active video in Odd/Even Field in PAL mode.

STVPAL [1:0]	Function description
00	The first line of active video in Even Field = The first line of activevideo in Odd Field
01	The first line of active video in Even Field = The first line of active video in Odd Field + 1
10	No Use
11	The first line of active video in Even Field = The first line of active video in Odd Field – 1

c-3. R2

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0
R2	2h	Reserved(1)	RGBVPOL(0)	Reserved(1)	Reserved(0)	Reserved(1)	HS_POL(0)	NPC_IN(1)	NPC_SET(0)

RGBVPOL: VS polarity setting for Serial/Parallel RGB

RGBVPOL =”L”, negative polarity.

RGBVPOL =”H”, positive polarity

HS_POL: HS polarity setting for CCIR601 and Serial/Parallel RGB.

HS_POL=L, negative polarity.

HS_POL=H, positive polarity.

NPC_IN: Define the NTSC/PAL mode by SPI.

NPC_IN=L, PAL.

NPC_IN=H, NTSC.

NPC_SET: Set the NTSC/PAL auto detection or define by NPC_IN.

NPC_SET=L, auto detection.

NPC_SET=H, define by NPC_IN.

c-4. R3

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0
R3	3h	Reserved(1)	Reserved(0)	Reserved(01)		Reserved(0)	POL_OUT(0)	DE_POL(0)	DE_SEL(0)

POL_OUT: POL phase select

POL_OUT=L, POL and VCOM are in phase.

POL_OUT=H, POL and VCOM are reverse.

DE_POL: DE signal polarity setting.

When DE_SEL=L:

DE_POL =L, positive polarity.

DE_POL =H, negative polarity.

When DE_SEL=H:

DE_POL =L, negative polarity.

DE_POL =H, positive polarity.

DE_SEL: DE mode select.

DE_SEL=L, DE signal with HS and VS signal

DE_SEL=H, DE signal only

F. Optical specifications (Note 1, 2)

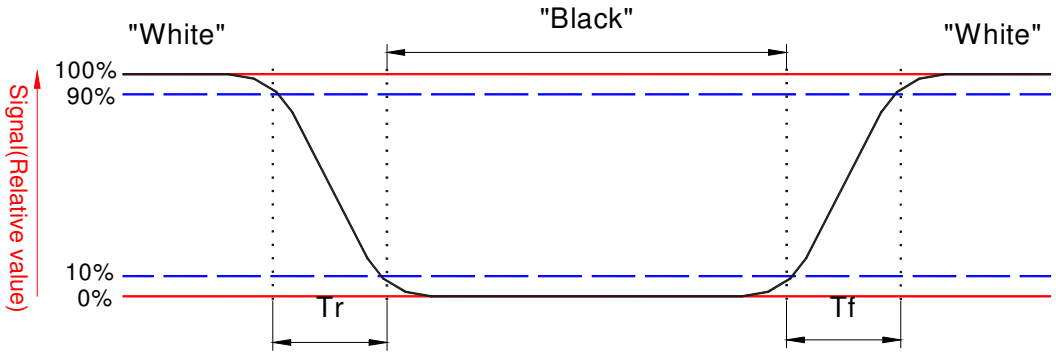
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time							
Rise	Tr	θ =0°	-	10	20	ms	Note 3, 4
Fall	Tf		-	15	25	ms	
Contrast ratio	CR	At optimized viewing angle	300	350	-		Note 5, 6
Viewing Angle							
Top			35	50	-		
Bottom		CR≧10	40	55	-	deg.	Note 7, 8
Left			45	60	-		
Right			45	60	-		
Brightness	Y_L	θ =0°	300	350	-	cd/m^2	
Color Chromaticity	Wx	θ =0°	0.26	0.31	0.36		
	Wy		0.28	0.33	0.38		
	Rx		0.57	0.62	0.67		
	Ry		0.30	0.35	0.40		
	Gx		0.29	0.34	0.39		
	Gy		0.53	0.58	0.63		
	Bx		0.10	0.15	0.20		
	By		0.03	0.08	0.13		
Gamma			1.7	2.2	2.4		Note 9
Luminance Uniformity			75	80		%	Note 10

Note 1: Measurement should be performed in the dark room, optical ambient temperature =25°C, and backlight current I_L=20 mA

Note 2: To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.



Note 4. From liquid crystal characteristics, response time will become slower and the color of panel will become darker when ambient temperature is below 25℃.

$$\text{Contrastratio} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 5. Contrast ratio is calculated with the following formula.

Note 6. White Vi=Vi50 $\overline{+}$ 1.5V

Black Vi=Vi50 ± 2.0V

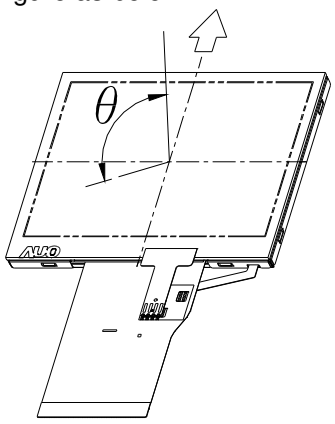
"±" means that the analog input signal swings in phase with COM signal.

"$\overline{+}$" means that the analog input signal swings out of phase with COM signal.

Vi50 :The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle: refer to figure as below.

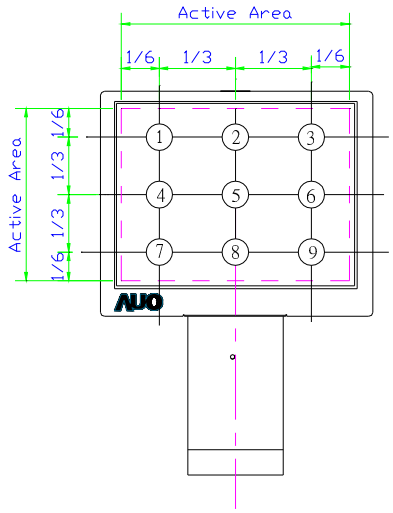


Note 8. The viewing angles are measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 9. Gamma value is measureed under the typical timing condition.

Note 10. Definition of luminance uniformity

$$\text{Luminance Uniformity} = \frac{\text{Min. Brightness of nine point}}{\text{Max. Brightness of nine point}}$$



G. Reliability Test Items

No.	Test items	Conditions		Remark
1	High Temperature Storage	Ta= 70℃	240Hrs	
2	Low Temperature Storage	Ta= -10℃	240Hrs	
3	High Temperature Operation	Ta= 60℃	240Hrs	
4	Low Temperature Operation	Ta= 0℃	240Hrs	
5	High Temperature & High Humidity	Ta= 60℃. 90% RH	240Hrs	Operation
6	Heat Shock	-25℃~70℃, 50 cycle, 2Hrs/cycle		Non-operation
7	Electrostatic Discharge	±200V,200pF(0Ω), once for each terminal		Non-operation
8	Vibration (With Carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz		IEC 68-34
9	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces		

Note : Ta: Ambient temperature.

H. Touch Screen Panel Specifications (Touch Panel Maker is TTI, Haze=10%)

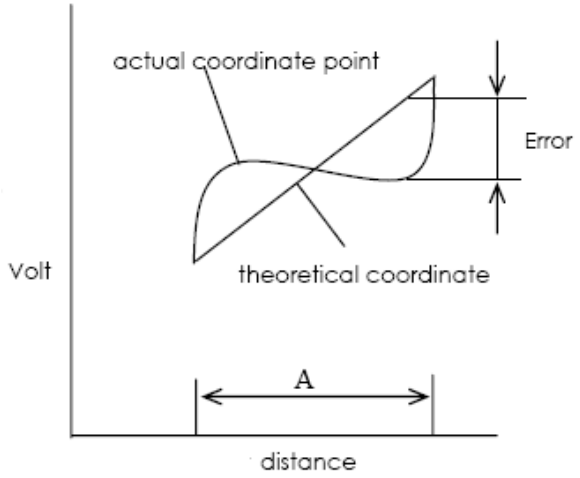
1. FPC Pin Assignment

Pin No.	Symbol	I/O
8	Top	I/O
9	Right	I/O
10	Bottom	I/O
11	Left	I/O

2. Electrical Characteristics

Item		Min.	Max.	Unit	Remark
Rate DC Voltage			7	V	
Resistance	X (Film)	350	950	Ω	At connector
	Y (Glass)	150	800		
Linearity		-1.5%	1.5%	--	Note 1, test by 250 gf
Chattering			20	ms	At connector pin
Insulation Resistance		10M		Ω	DC 25V

Note 1: Measurement condition of Linearity: difference between actual voltage & theoretical voltage is an error at any points. Linearity is the value max. error voltage divided by voltage difference on active area.



3. Mechanical Characteristics

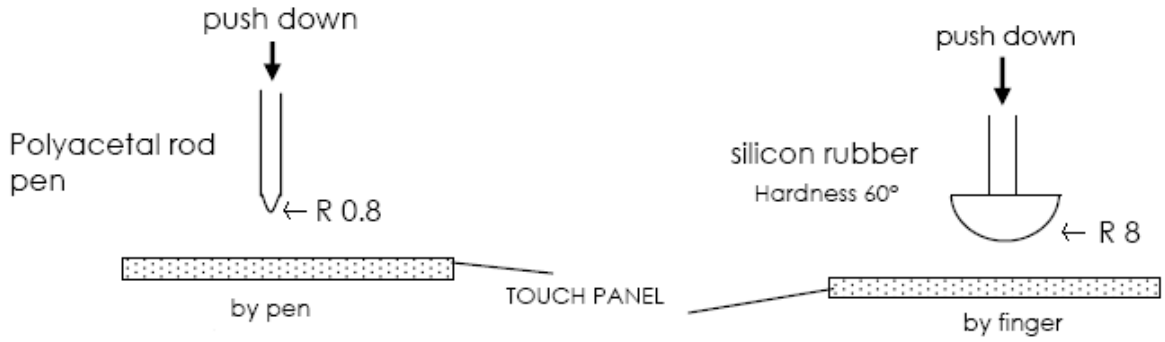
Item	Min.	Max.	Unit	Remark
Hardness of Surface	3	--	H	JIS K-5400
Operation Force (Pen or Finger)	--	80	gf	Note 1

Note 1: Within ”guaranteed active area”, but not on the edge and dot-spacer.

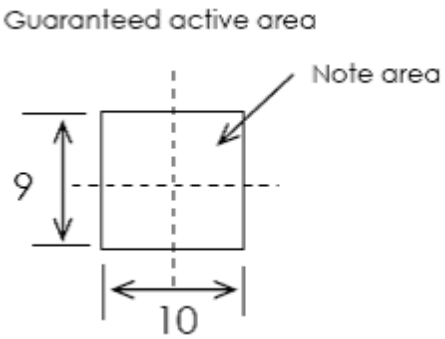
4. Life test Condition

Item	Min.	Max.	Unit	Remark
Notes Life	10^5	--	words	Note 1, 2
Input Life	10^6	--	times	Note 1, 3

Note 1: Measurement condition of Operation Force: Within ”guaranteed active area” under normal (NTP) condition. When user pushes down on the film, resistance between X & Y axis must be equal or lower than 2kΩ. Below is test figure.



Note 2: Notes Life test condition (by pen): Notes area for pen notes life test is 10×9 mm. Size of word is 7.5×6.75mm. Word is any A.B.C….. letter. Writing speed is 60mm/s. Center of each word is changed at random in notes area.

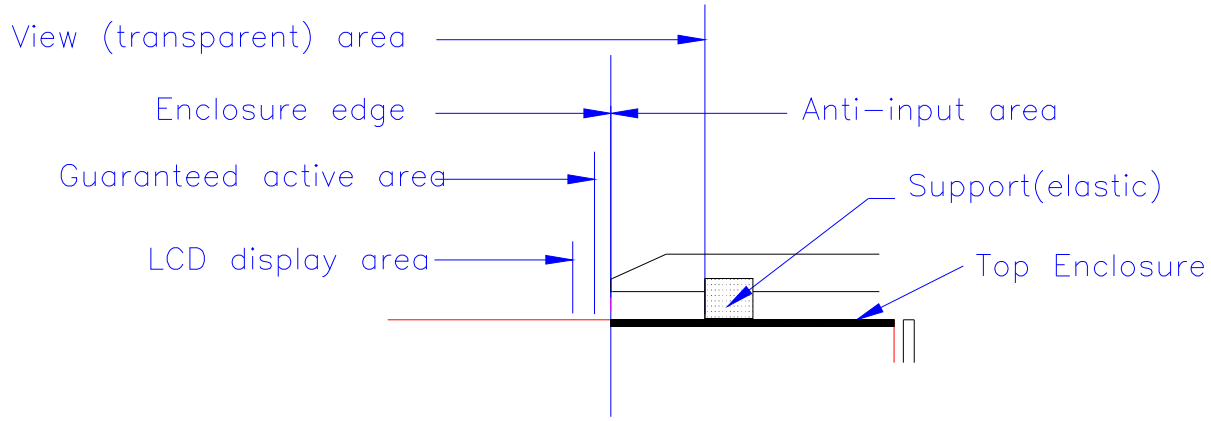


Note 3: Input Life test condition(by finger): By silicone rubber tapping at same point. Tapping Load is 200g, and tapping frequency is 5Hz.

5. Attention

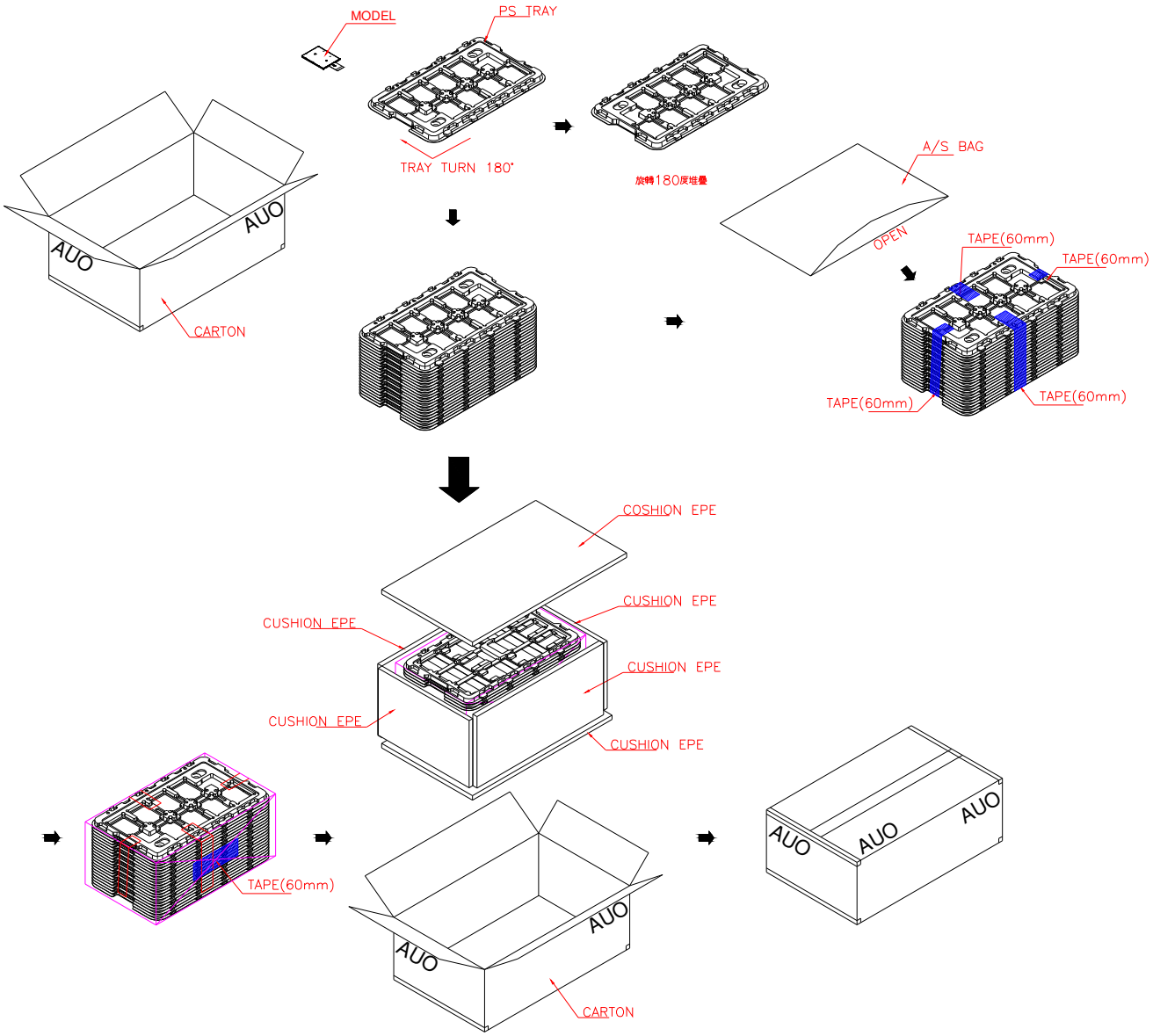
Please pay attention for below matters at mounting design of touch panel of LCD module.

1. Do not design enclosure pressing the view area to prevent from miss input.
2. Enclosure support must not touch with view area.
3. Use elastic or non-conductive material to enclosure touch panel.
4. Do not bond film of touch panel with enclosure.
5. The touch panel edge is conductive. Do not touch it with any conductive part after mounting.
6. If user wants to cleaning touch panel by air gun, pressure 2kg/cm2 below is suggested. Not to blow glass from FPC site to prevent FPC peeled off.



7. Do not put a heavy shock or stress on touch panel and film surface. Ex. Don't lift the panel by film face with vacuum.
8. Do not lift LCD module by FPC.
9. Please use dry cloth or soft cloth with neutral detergent (after wring dry) or one with ethanol at cleaning. Do not use any organic solvent, acid or alkali liquor.
10. Do not pile touch panel. Do not put heavy goods on touch panel.

I. Packing Form

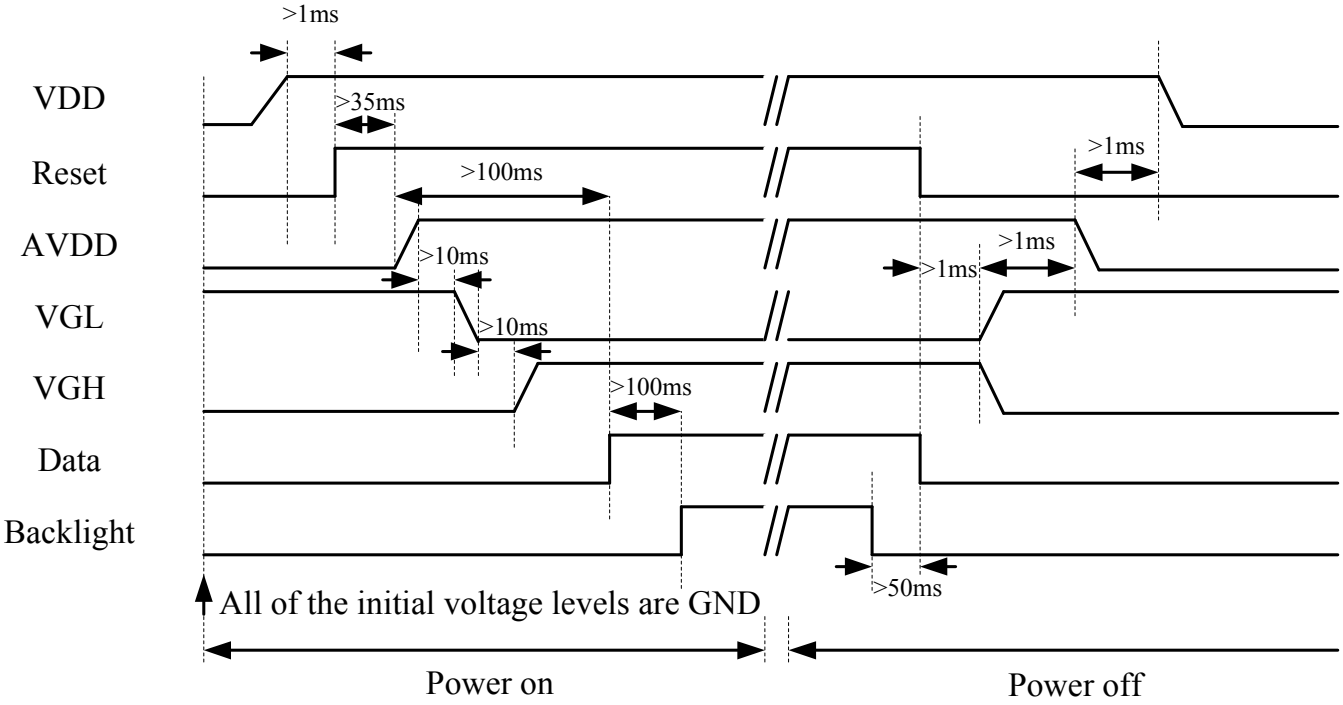


MAX. CAPACITY:160 MODULES
MAX. WEIGHT: 12Kg
MEAS. 520mm*340mm*250mm

J. Application Note

i.Power on/off sequence

The LCD panel adopts high voltage driver ICs, so it could be permanently damaged if a wrong power on/off sequence is used. When powering on the LCD, VDD should go up firstly, and then turn on VGL and AVDD, and finally VGH. Turn off the LCD panel with reversed order or shut off all the power supplies simultaneously.

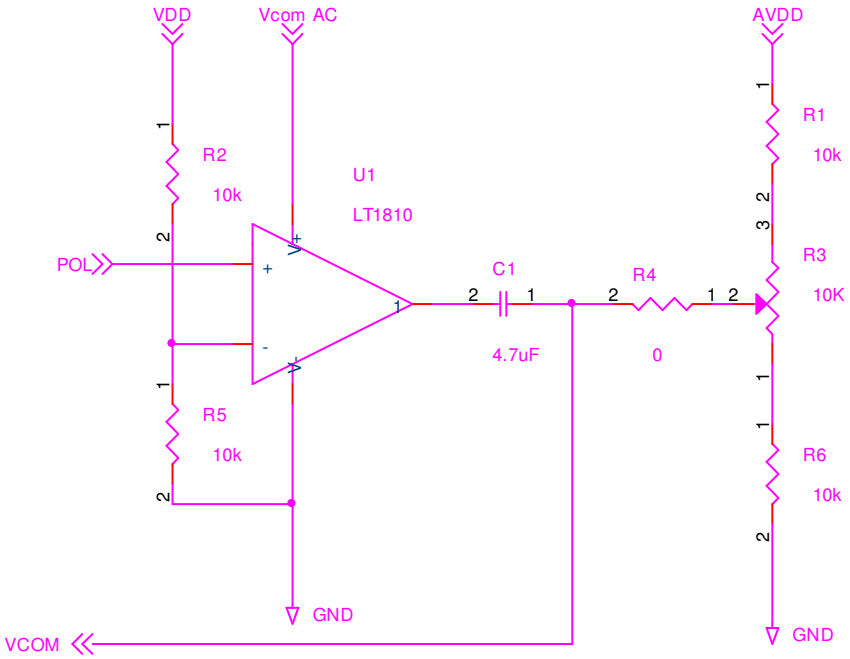


<Note>：The power-on intervals between AVDD and VGL/VGH can be less than 10ms. However, following the recommended power on sequence can eliminate the random start up display issue.

ii. Application Notes – Vcom driving circuit

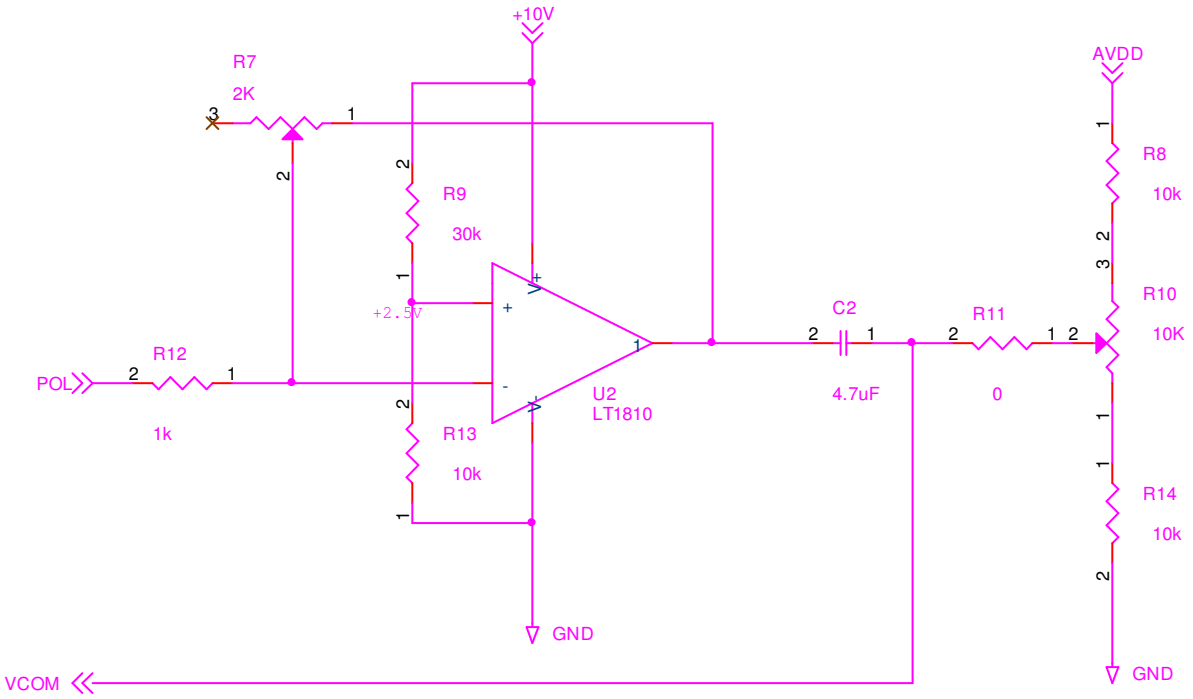
POL which is a digital output signal from LCM is used to generate Vcom signal. According to register R3, when POL_OUT is 'L', POL and Vcom are in phase. Otherwise, POL and Vcom are reverse. Below application circuits are for POL_OUT='L' and POL_OUT='H', respectively. In the typical condition, Vcom AC is equal to 5V.

a. POL and Vcom are in phase (POL_OUT='L')



<Note>：The resistors R1, R3 and R6 are used to optimizing flicker by adjusting VcomDC value which equals to $\frac{1}{2}(VcomH + VcomL)$.

b. POL and Vcom are reversed



Base on above circuit Vcom AC are following the equations as below

$$Vcom\ AC = VDD * \frac{R_7}{R_{12}}$$

<Note>：The resistors R8, R10 and R14 are used to optimizing flicker by adjusting VcomDC value which equals to $\frac{1}{2}(VcomH + VcomL)$.