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# **Product Specification**

## **3.6" COLOR TFT-LCD MODULE**

MODEL NAME: A036QN01 V0

<◆>Preliminary Specification

< > Final Specification

Note: The content of this specification is subject to change.

©

## Record of Revision

Version	Revise Date	Page	Content
0	12/Feb/2004		First draft.
0.1	25/Feb/2004	11	Add a note "DCLK Tr and Tf is defined at 10%~90%" and a refer figure
0.2	1/Mar/2004	7	Correct Note4 text from "SEL0=Low, SEL1=High, SEL0=Low" to "SEL0=Low, SEL1=High, SEL2=Low"
0.3	4/May/2004	5-6 23-25	1) Point out optional $V_{GH}$ , $V_{GL}$ and LED backlight driving circuit in FPC pin assignment. 2) Provide suggested application circuit for private power supply of $V_{GH}$ , $V_{GL}$ and LED backlight driving
		7	Provide definition and suggestion of select pin in Note 4 and Note 5.
0.4	19/May/2004	4	Correct dot pitch.
0.5	18/Jun/2004	7 10 23-26	Modify "SEL2" setting in Note 4, from "Low (or 0)" to N/C Modify "Current consumption" table. Modify application circuits. (it is effective after 07/15/2004Y)

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## A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution(dot)	960(W) x240(H)	
2	Active area(mm)	72.96(W)x54.72(H)	
3	Screen size(inch)	3.59(Diagonal)	
4	Dot pitch(mm)	0.076(W)x0.228(H)	
5	Color configuration	R. G. B. stripe	
6	Overall dimension(mm)	84.3(W) x 66.42(H) x 3.2(D)	Note 1
7	Weight(g)	38 (typ)	
8	Panel surface treatment	Anti-Glare	

## B. Electrical specifications

### 1. Pin assignment

#### a. TFT-LCD panel driving section

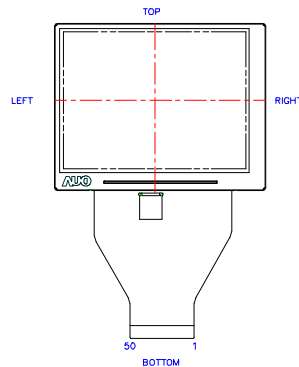
Pin no	Symbol	I/O	Description	Remark
1	VSCL2	I	VCAC level Selection	Note 6
2	VSCL1	I	VCAC level Selection	Note 6
3	VSCL0	I	VCAC level Selection	Note 6
4	GND	P	Digital ground for gate	
5	VCC	PI	Digital Power for gate (+3.3V)	
6	VCAC	PS	VCOM level supply	
7	VGoff_H	PS	Negative power supply (High) for gate	
8	VCOM	SO	Frame polarity output for panel VCOM	
9	VGoff_L	PS	Negative power supply (Low) for gate	
10	C3M	C	Power setting capacitor connect pin	
11	C3P	C	Power setting capacitor connect pin	
12	VGH	PI	Positive power supply for gate (+15V)	Option Note 7
13	GND	-	Ground	
14	FB_G	FI	Main boost regulator feedback input. FB threshold is 0.6V	
15	GND	-	Ground	
16	DRV_G	O	Power transistor gate signal for the boost converter	
17	GLED1	PI	LED module 1 Cathode	
18	VLED1	-	LED module 1 Anode	Option Note 7
19	VLED2		LED module 2 Anode	Option Note 7
20	GLED2		LED module 2 Cathode	
21	DRV_S	O	Power transistor gate signal for the boost converter	
22	FB_S	FI	Main boost regulator feedback input. FB threshold is 0.6V	
23	GND	P	Digital ground for source	
24	SHL	I	Selects left or right shift (Default="H")	Note 1
25	STB	I	Standby mode (Normal operation="H", Default setting)	Note 2
26	VCC	PI	Digital power supply for source (+3.3V)	
27	SHDB	I	Shutdown input (SHDB="L" DRV_S is off, Default="L")	Note 3

28	AVDD	PI	Analog power supply (+3.3V)	
29	AGND	P	Analog ground	
30	VSYNC	I	Vertical sync input (Negative polarity)	
31	HSYNC	I	Horizontal sync input (Negative polarity)	
32	GND	-	Ground	
33	DCLK	I	Clock Signal	
34	DND	-	Ground	
35	D07	I	Data input (MSB)	
36	D06	I	Data input	
37	D05	I	Data input	
38	D04	I	Data input	
39	D03	I	Data input	
40	D02	I	Data input	
41	D01	I	Data input	
42	D00	I	Data input (LSB)	
43	GND	-	Ground	
44	RSTB	I	Global reset pin (Default="H", Normal operation)	Note 5
45	SEL0	I	Data format selection (Default="L")	Note 4
46	SEL1	I	Data format selection (Default="L")	Note 4
47	SEL2	I	Data format selection (Default="L")	Note 4
48	U/D	I	Shift up or down control. (Default="H")	Note 1
49	Q1H	O	Data sequence control. Data sequence information	
50	VCOM_O	SI	VCOM Output	

Note 1: Selection of scanning mode

Mode	Setting of scan control input		Scanning direction
	U/D	SHL	
Normal mode	L	H	From up to down, and from left to right.
Reverse mode	H	L	From down to up, and from right to left.

Refer to figure as below:



Note 2: Stand by mode (STB). If STB high, it is normal operation.

If it is low, it is standby function. Normally pulled high.

Note 3: Shutdown input (SHDB). Active low, DC-DC converter for White LED is off when SHDB is low, normally pulled low.

Note 4: Interface select pin, Pull "SEL0=Low, SEL1=High, SEL2=N/C" for A036QN01 V0 Model.

Note 5: RSTB="L", the controller is reset.

RSTB="H", normal operation (RSTB should be connected to VCC). Default setting.

SEL2	SEL1	SEL0	Data input format	Operating frequency
N/C	1	0	UPS051 path, special data format : DDX , 8-bits	19.4MHz (NTSC)
N/C	1	1	UPS051 path, special data format : DDX , 8-bits	19.4MHz (PAL)



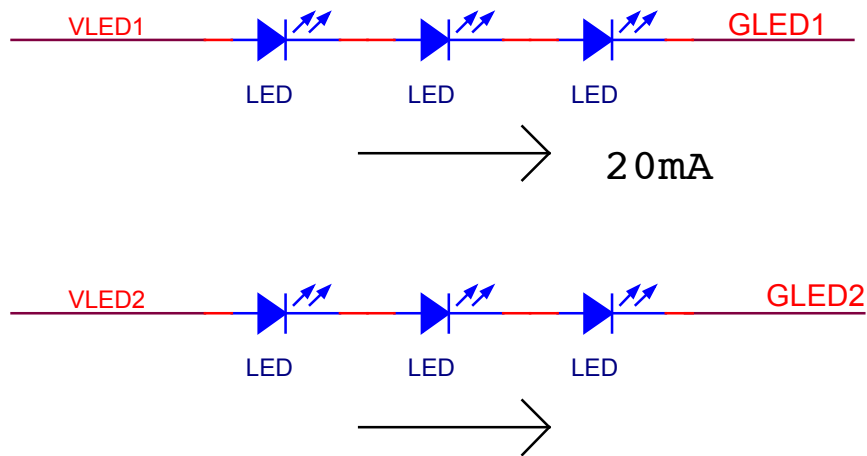
Note 6: Selection of VCAC level

VCSL2	VCSL1	VCSL0	Level (unit: V)
0	0	0	4.4
0	0	1	4.6
0	1	0	4.8
0	1	1	5.0
1	0	0	5.2
1	0	1	5.4
1	1	0	5.6(Default)
1	1	1	5.8

b. LED driving section

No.	Symbol	I/O	Description	Remark
Pin 17	GLED1	-	LED Cathode	
Pin 18	VLED1	-	LED Anode	
Pin 19	VLED2	-	LED Anode	
Pin 20	GLED2	-	LED Cathode	

Please refer to the below figure.



## 2. Equivalent circuit of I/O

Pin no & Pin name	Schematics
21.DRV_S	TBD
22.FB_S 24.SHL 25.STB 27.SHDB 30.HSYNC 31.VSYNC 33.DCLK 35.D07 36.D06 37.D05 38.D04 39.D03 40.D02 41.D01 42.D00 44.RSTB 45.SEL0 46.SEL1 47.SEL2 48.U/D	TBD

## 3. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	V <sub>CC</sub>	GND=0	-0.5	5	V	
	AV <sub>DD</sub>	AV <sub>SS</sub> =0	-0.5	7	V	
	V <sub>GH</sub>	GND=0	13	17	V	
Operating temperature	Topa		0	60	°C	Ambient temperature
Storage temperature	Tstg		-25	80	°C	Ambient temperature

## 4. Electrical characteristics

### a. Typical operating conditions (GND=AVss=0V)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply	V <sub>CC</sub>	2.7	3.3	3.6	V	
	AV <sub>DD</sub>	3.0	3.3	5	V	
	V <sub>GH</sub>	14	15	16	V	
	VGoff_H	---	-10+VCAC	---	Vp-p	

	VGoff_L	---	-10	---	V	
VCOM	V <sub>CAC</sub>	4.4		5.8	V <sub>p-p</sub>	AC component, Note 1
	V <sub>CDC</sub>	-	TBD	-	V	Note 2
Output Signal voltage	H Level	V <sub>OH</sub>	V <sub>CC</sub> -0.4		V	
	L Level	V <sub>OL</sub>	GND	GND+0.4	V	
Input Signal voltage	H Level	V <sub>IH</sub>	0.8V <sub>CC</sub>	-	V <sub>CC</sub>	V
	L Level	V <sub>IL</sub>	GND	-	0.2V <sub>CC</sub>	V
DRV output voltage	V <sub>DRV</sub>	0		V <sub>CC</sub>	V	
DRV output	IDRV			10	mA	
Feedback voltage	V <sub>FB</sub>	0.55	0.6	0.65	V	
Output current	H Level	I <sub>OH</sub>		10	uA	
	L Level	I <sub>OL</sub>		-10	uA	
Analog stand by current	I <sub>st</sub>			200	uA	DCLK is stopped
FRP output current	H Level	I <sub>OHF</sub>		20	mA	For Vcom circuits.
	L Level	I <sub>OLF</sub>		20	mA	

Note 1: The brightness of LCD panel could be adjusted by the adjustment of the AC component of VCOM.

Note 2: V<sub>CDC</sub> could be adjusted so as to minimize vertical straight line, flicker and maximum contrast on each module.

b. Current consumption (GND=AVss=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Current for source driver	I <sub>CC</sub>	V <sub>CC</sub> =3.3V	---	4.0	---	mA	
	I <sub>DD</sub>	AV <sub>DD</sub> =3.3V	---	2.0	2.5	mA	
Current for gate driver	I <sub>GH</sub>	V <sub>GH</sub> =15V	---	1	2.5	mA	
	I <sub>CC</sub>	V <sub>CC</sub> =3.3V	---	0.5	1	mA	

c. LED driving conditions

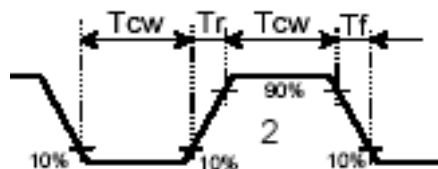
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current			20		mA	Single Series
LED voltage	V <sub>L</sub>			12	V	Single Series
LED Life Time	L <sub>L</sub>	10000			Hr	Note 1,2

### 5. AC Timing

#### a. Timing conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK	Frequency	1/Tvc	-	19.4	-	MHz	
	Duty cycle	Tcw	40	50	60	%	
	Rising time	t <sub>r</sub>	-		10	ns	Note 1
	Falling time	t <sub>f</sub>	-		10	ns	Note 1
HSYNC	Period	TH	60	63.56	67	us	Note 2
				1235		DCLK	
	Display period	THd		49.4		us	
	Pulse width	THp	5	91		DCLK	
HSYNC-Clk timing		THc	20		Tvc-20	ns	
Hsync setup time		Thst	12			ns	
Hsync hold time		Thhd	12			ns	
Horizontal lines per field		t <sub>v</sub>	256	262	268	t <sub>H</sub>	
VSYNC	Period	TV		16.6		ms	Note 2
					262		
	Display period	TVd		14.83		ms	
	Pulse width	TVp	1			DCLK	
			3		TH		
Vsync setup time		Tvst	12			ns	
Vsync hold time		Tvhd	12			ns	
DATA D00~D07	DCLK-DATA timing	Tds	12	-	-	ns	
	DATA-CLK timing	Tdh	12	-	-	ns	
	Rising time Falling time	Tdrf	-	-	10	ns	

Note 1 DCLK Tr and Tf is defined at 10%~90%. Refer to figure as below:



B. Vertical display position

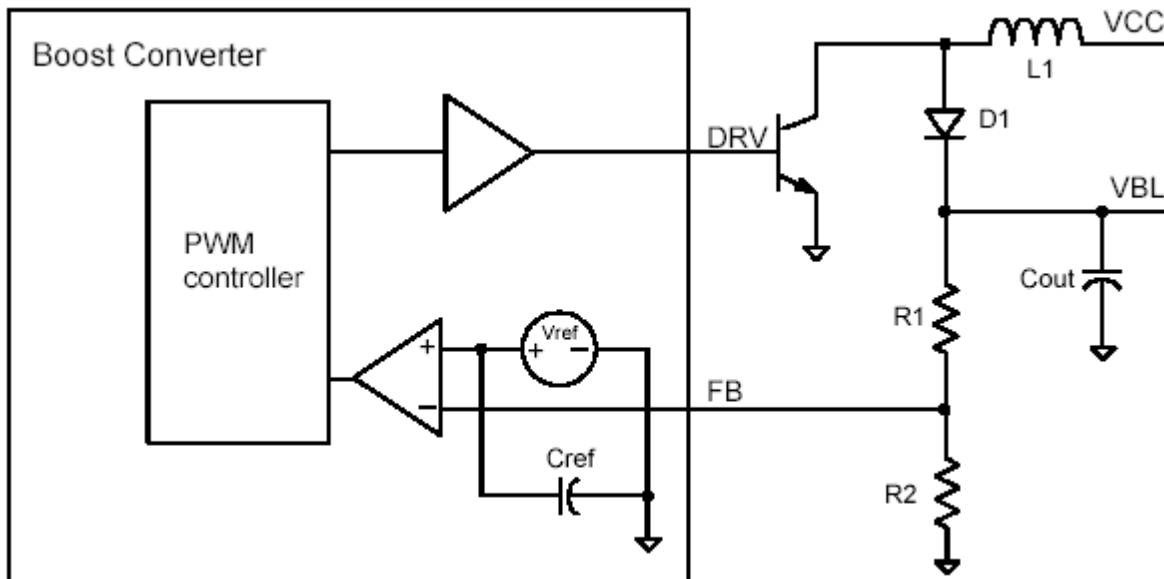
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical display position	TVS		18		TH	NTSC

b. Timing diagram

Please refer to the attached drawing, from Fig.5 to Fig.8.

6. Boost Converter

A036QN01 V0 main boost converter uses a boost PWM architecture to produce a positive regulated voltage, Please refer to the below figures to see the block diagram.



### C. Optical specification (Note 1, Note 2, Note 3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise	$\theta = 0^\circ$	-	25	50	ms	Note 4
	Fall		-	30	60	ms	
Contrast ratio	CR	At optimized viewing angle	100	150	-		Note 5,6
Viewing angle	Top	$CR \geq 10$	10	-	-	deg.	Note 7
	Bottom		30	-	-		
	Left		45	-	-		
	Right		45	-	-		
Brightness	$Y_L$	$\theta = 0^\circ$	200	230	-	$cd/m^2$	Note 8
White chromaticity	X	$\theta = 0^\circ$		TBD			
	y	$\theta = 0^\circ$		TBD			

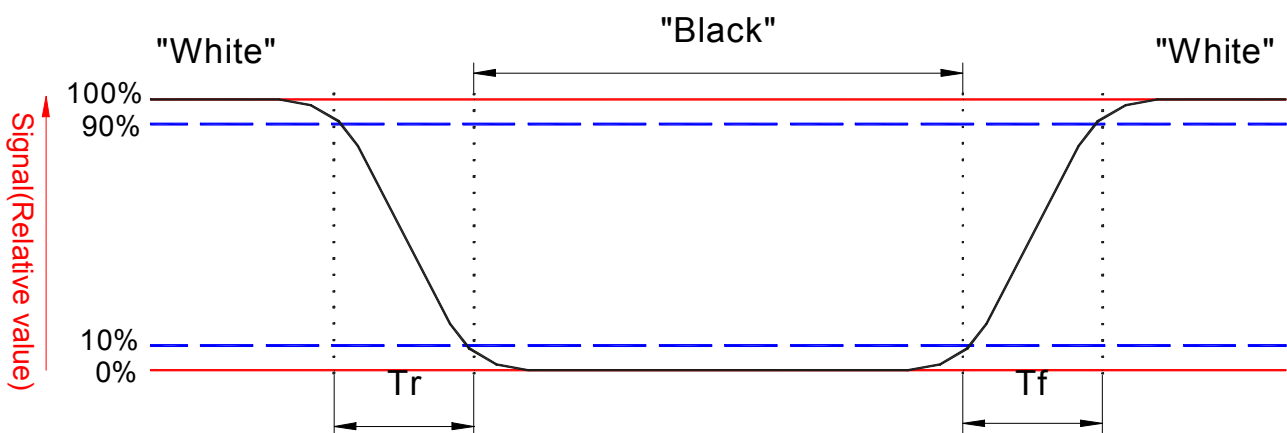
Note 1. Ambient temperature = 25°C. And backlight current  $I_L = 20\text{ mA}$

Note 2. To be measured in the dark room.

Note 3. To be measured on the center area of panel with a field angle of 1° by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (falling time) and from "white" to "black" (rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 6. White  $V_i = V_{i50} \mp 1.5V$

Black  $V_i = V_{i50} \pm 2.0V$

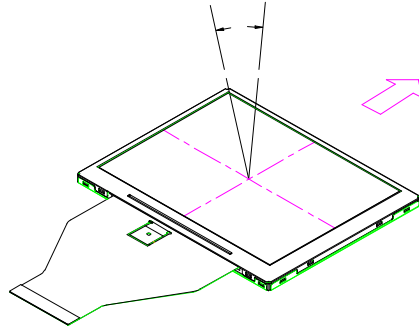
"±" Means that the analog input signal swings in phase with COM signal.

“ $\frac{-}{+}$ ” Means that the analog input signal swings out of phase with COM signal.

$V_{i50}$ : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle:, refer to figure as below.



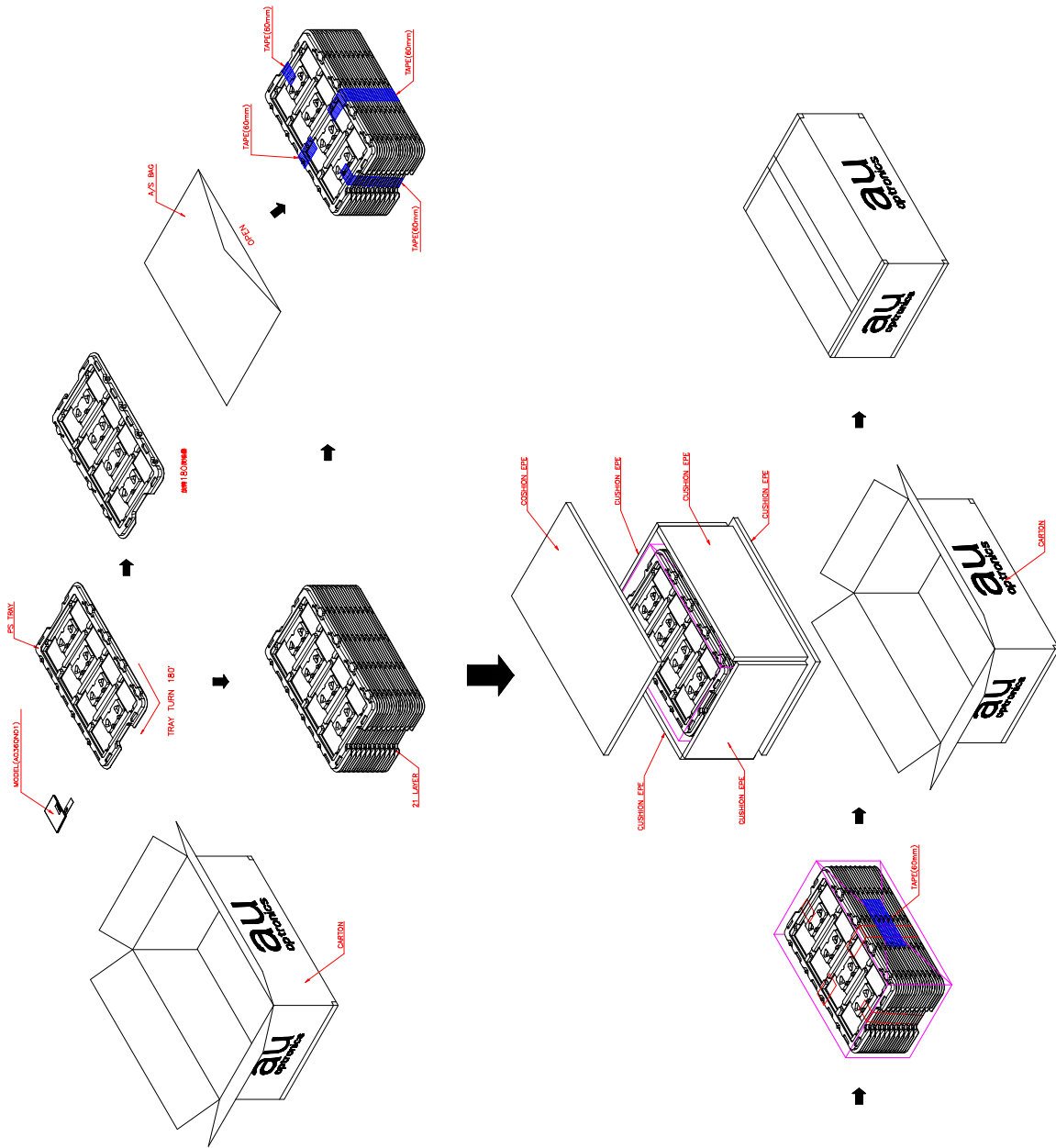
Note 8. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

#### D. Reliability test items:

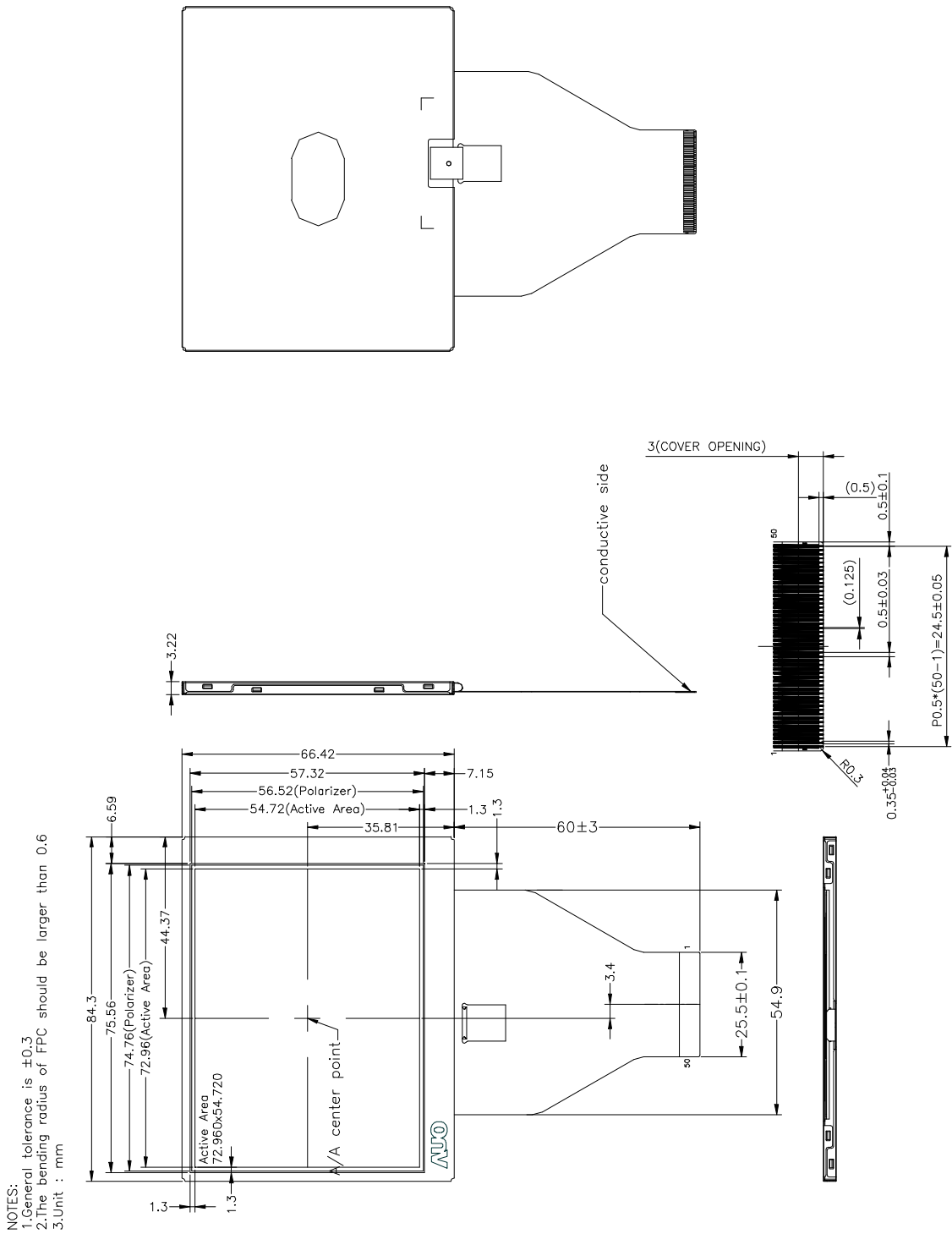
No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 80°C                      240Hrs	
2	Low temperature storage	Ta= -25°C                      240Hrs	
3	High temperature operation	Ta= 60°C                      240Hrs	
4	Low temperature operation	Ta= 0°C                      240Hrs	
5	High temperature and high humidity	Ta= 60°C . 90% RH              240Hrs	Operation
6	Heat shock	-25°C~80°C, 50 cycle, 2Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
9	Mechanical shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
10	Vibration (with carton)	Random vibration: 0.015G <sup>2</sup> /Hz from 5~200Hz -6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	



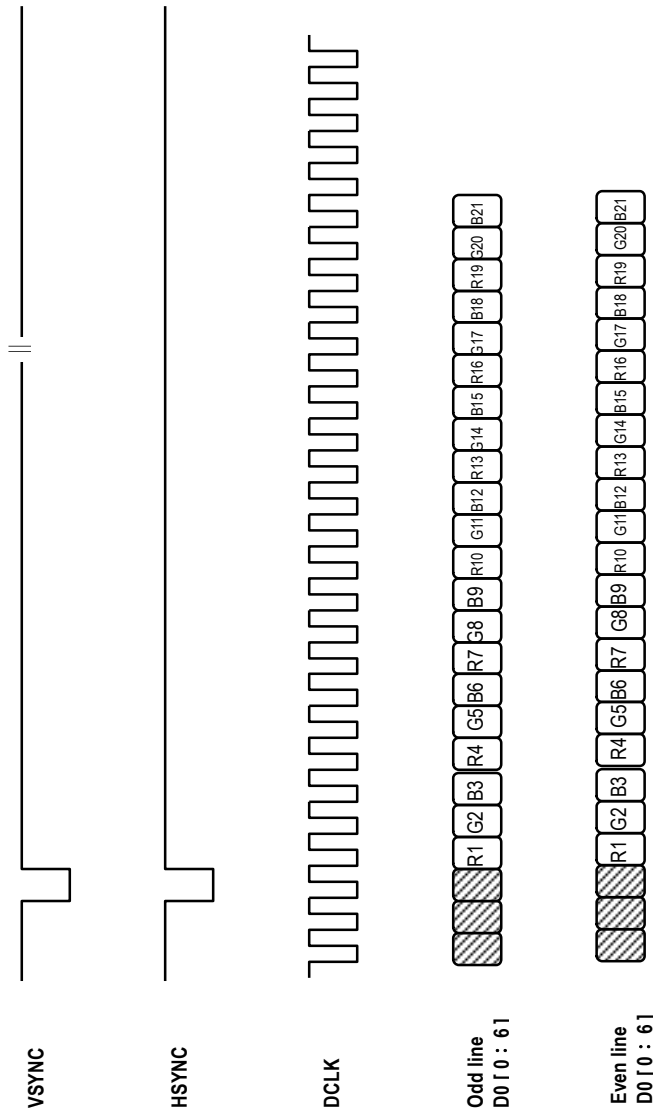
**E. Packing form**



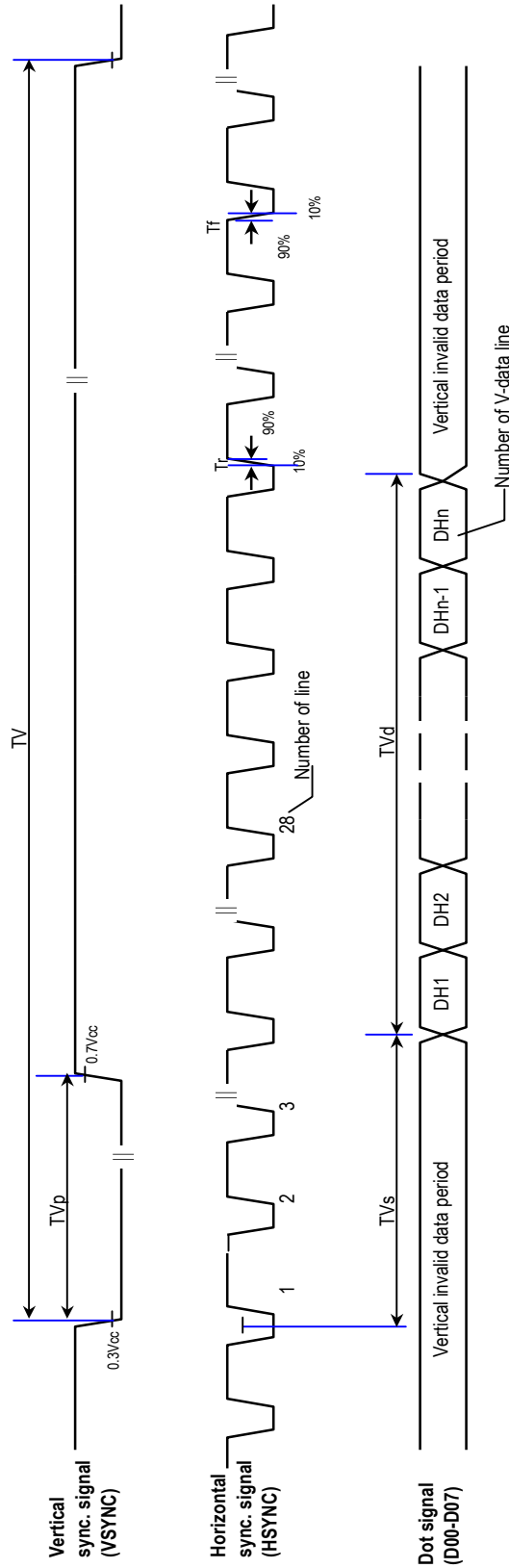
MAX. CAPACITY: 160 MODULES  
MAX. WEIGHT: 9 g  
MEAS. 520mm\*340mm\*250mm



**Fig. 4 outline dimension of TFT-LCD module**



**Fig. 5 Input signals timing relationship**



**Fig. 6 Input Vertical Timing**

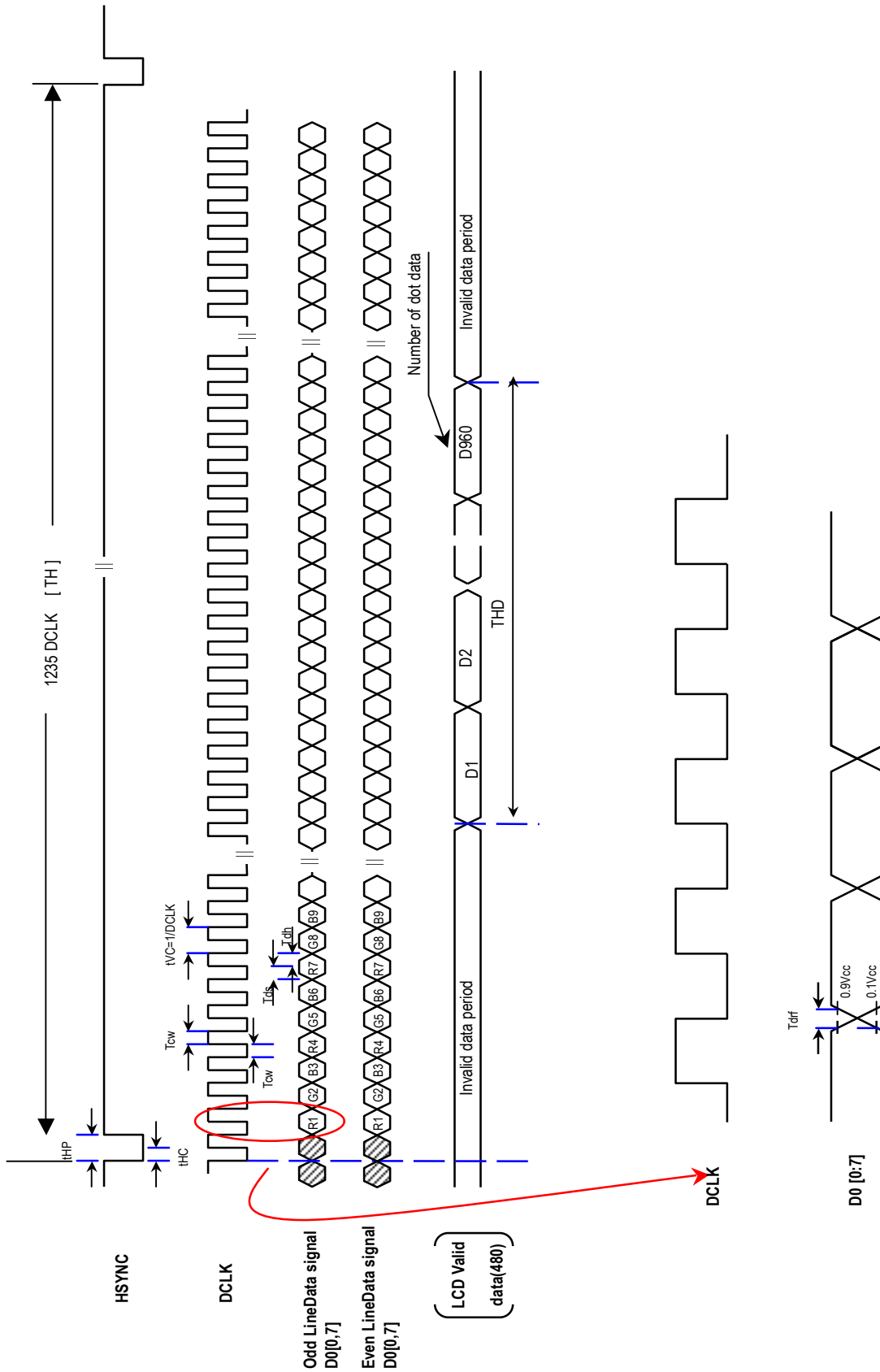
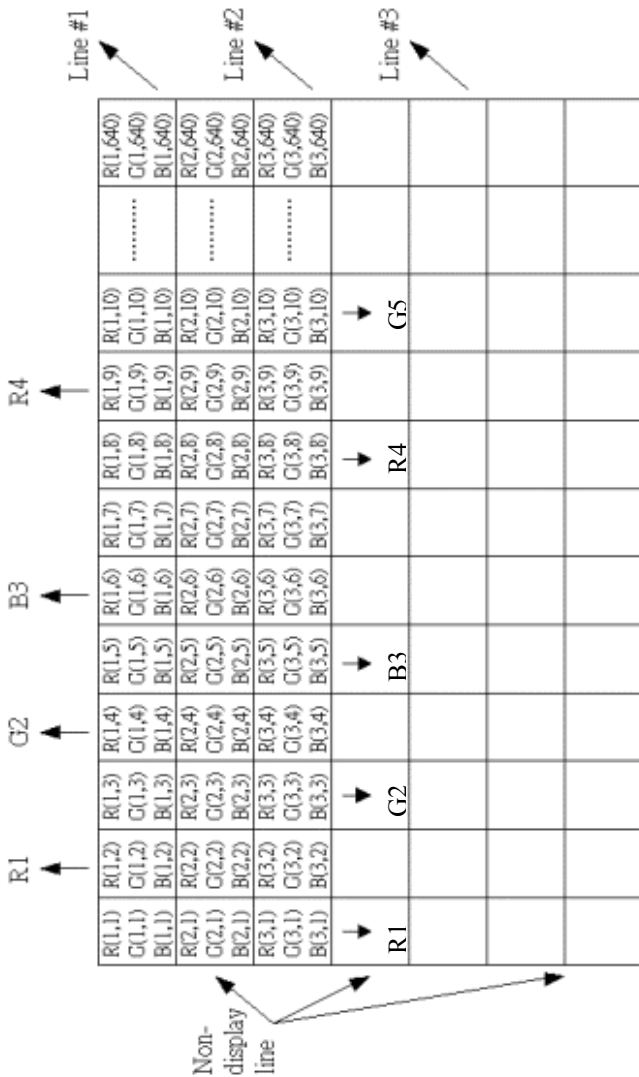
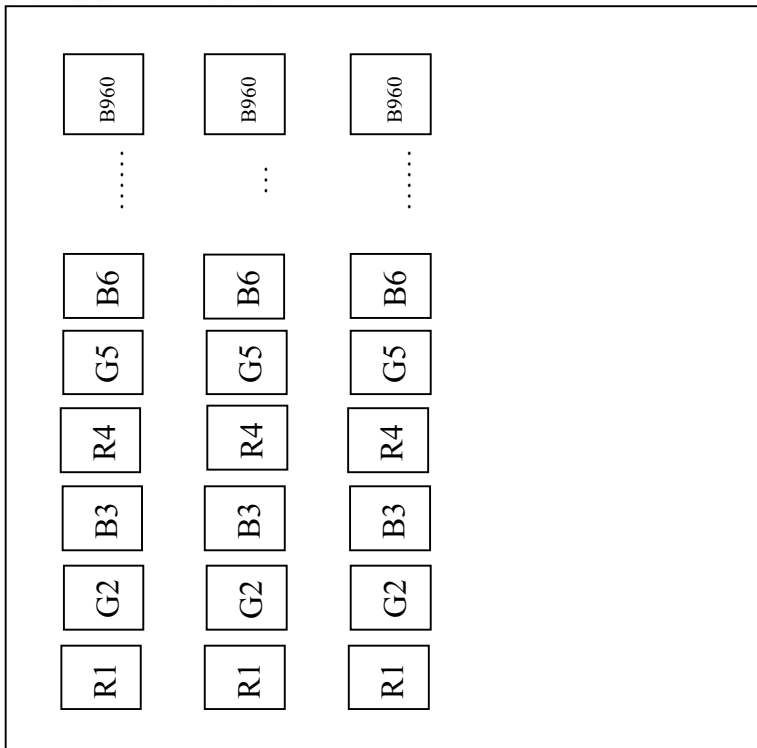


Fig. 7 Horizontal Input Timing)



VGA Memory

Fig. 8 Extraction of display data from memory to panel

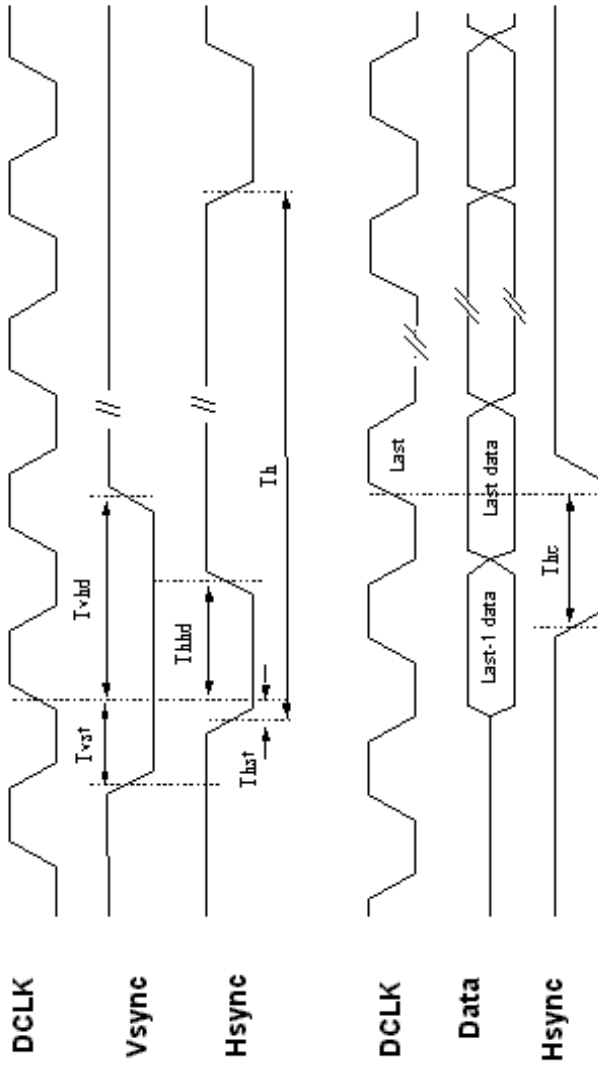
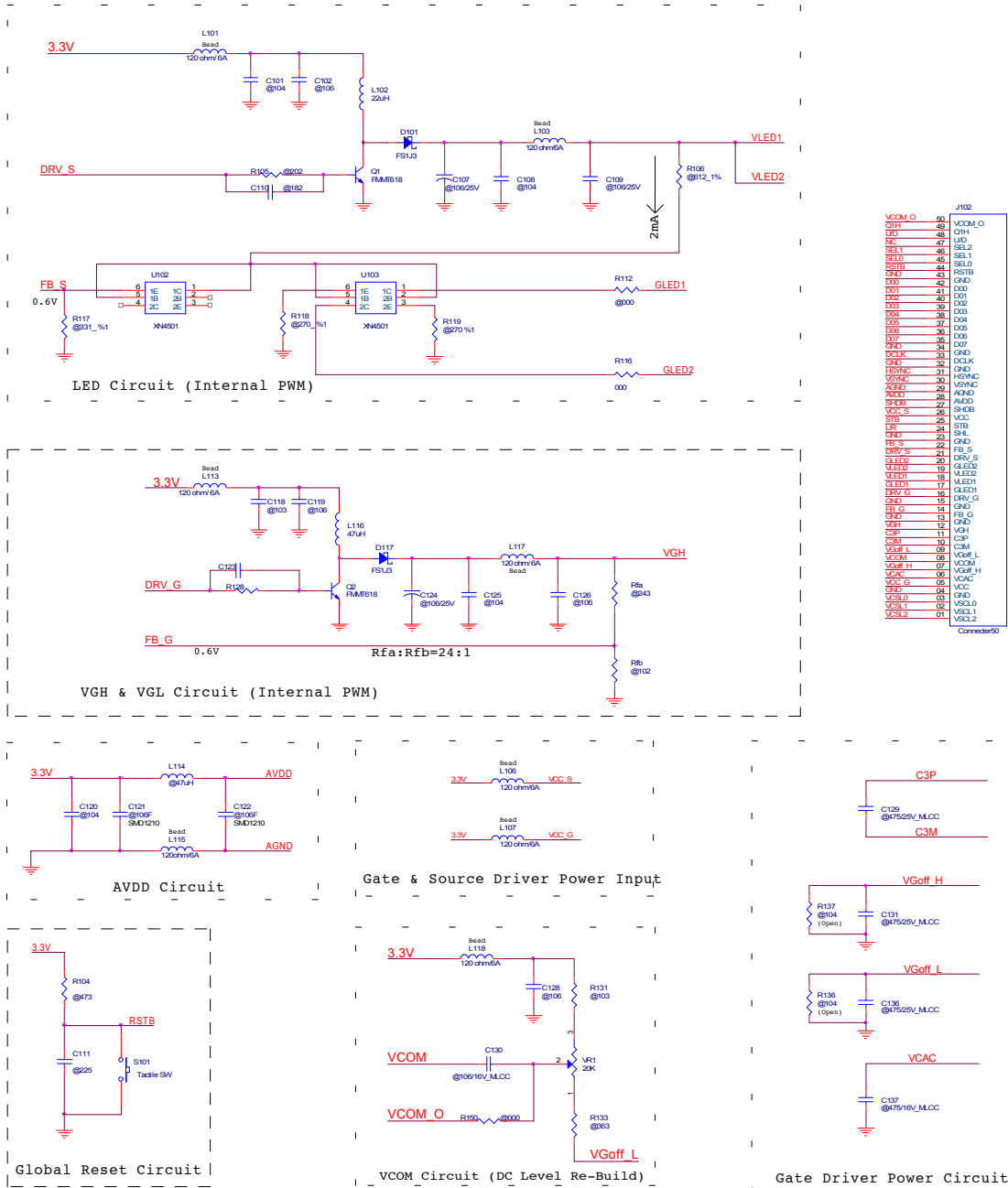


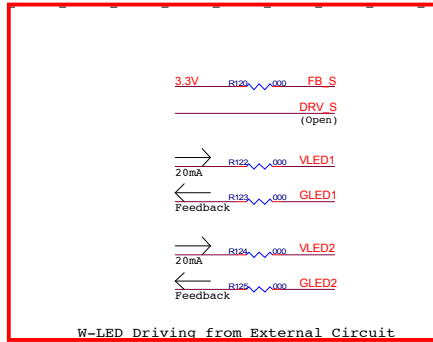
Fig. 9 Hsync, Vsync, Data, DCLK re



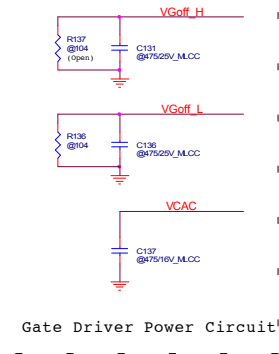
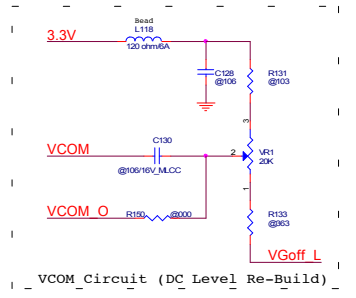
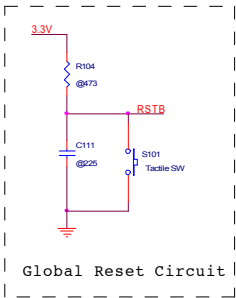
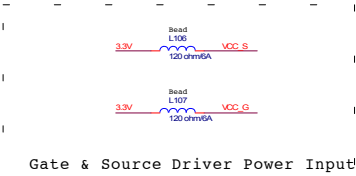
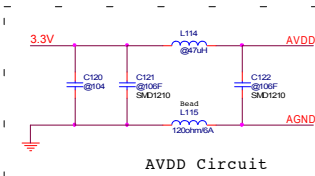
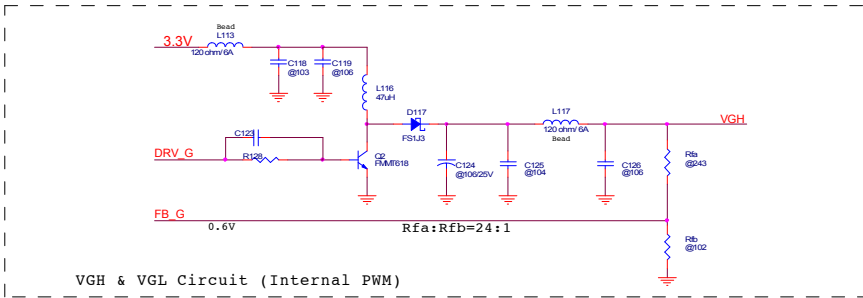
Note: Application circuit for using internal V<sub>GH</sub> & V<sub>GL</sub>, LED backlight driving function of drive IC

Fig. 10 Typical application circuit



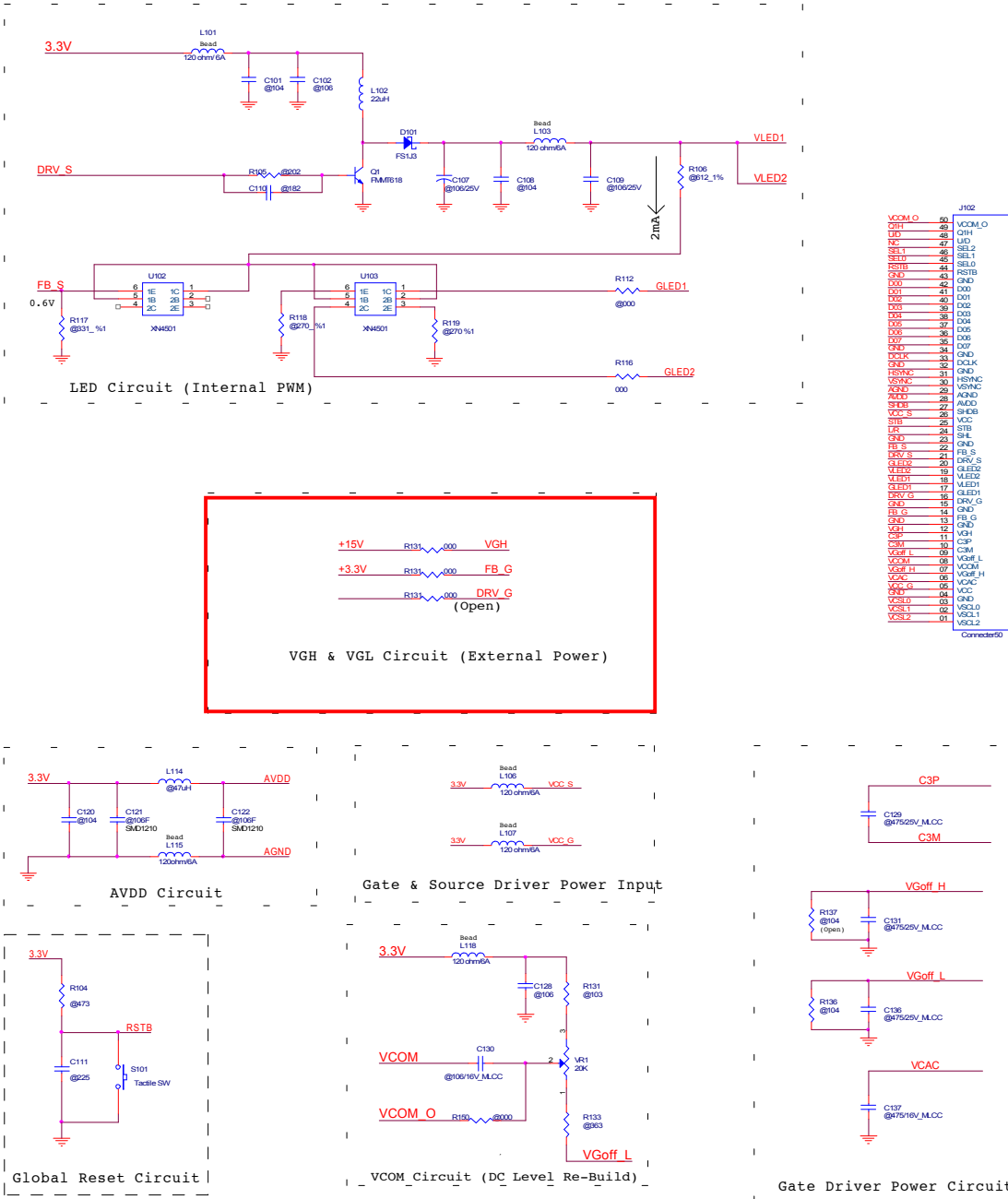


VCOM_O	50	J102
G1H	49	VCOM_O
UID	48	G1H
SEL2	47	UID
SEL1	46	SEL2
SEL0	45	SEL1
RS1B	44	SEL0
RS1A	43	RS1B
D00	42	RS1A
D01	41	D00
D02	40	D01
D03	39	D02
D04	38	D03
D05	37	D04
D06	36	D05
D07	35	D06
D08	34	D07
D09	33	D08
D10	32	D09
HSYNC	31	D10
VSYNC	30	HSYNC
VCOM	29	VSYNC
AGND	28	VCOM
AVDD	27	AGND
VCC_S	26	AVDD
VCC	25	VCC_S
VBI	24	VCC
VBL	23	VBI
FB_S	22	VBL
FB_G	21	FB_S
GLED2	20	FB_G
GLED1	19	GLED2
VLED2	18	GLED1
VLED1	17	VLED2
DRV_S	16	VLED1
DRV_G	15	DRV_S
GND	14	DRV_G
GND	13	GND
VGH	12	GND
VGL	11	VGH
CSP	10	VGL
C3M	9	CSP
VCOM_L	8	C3M
VCOM_H	7	VCOM_L
VCOM	6	VCOM_H
VCAC	5	VCOM
VCC	4	VCAC
GND	3	VCC
VCOM_O	2	GND
VCOM	1	VCOM_O
VCOM2	0	VCOM



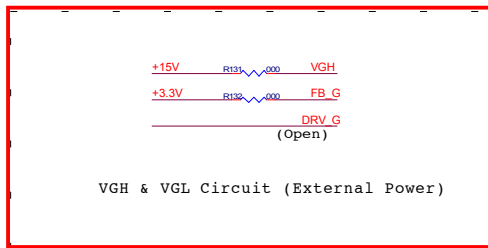
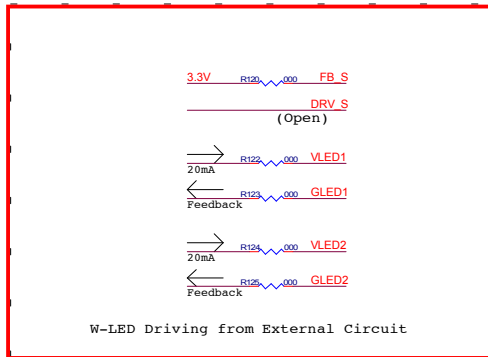
Note: Application circuit for only using internal V<sub>GH</sub> & V<sub>GL</sub> driving function of drive IC. Customer provides private LED driving circuit.

**Fig. 11 Application circuit for LED driving circuit unused**



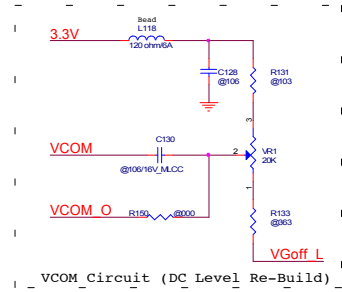
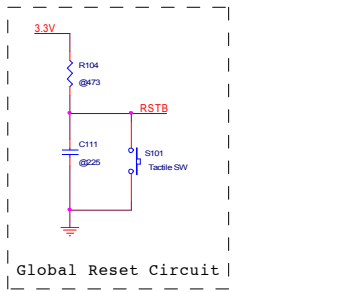
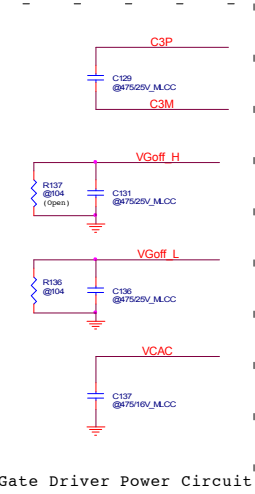
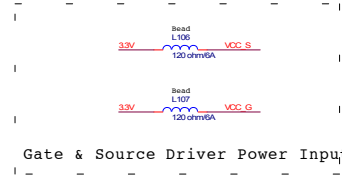
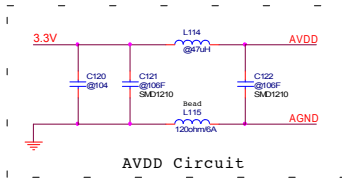
Note: Application circuit for only using internal LED driving function of drive IC. Customer provides private  $V_{GH}$  &  $V_{GL}$  driving circuit.

**Fig. 12 Application circuit for  $V_{GH}$  &  $V_{GL}$  driving circuit unused**



VCOM_O	60	J102
G1H	49	VCOM_O
G1H	48	G1H
U10	47	U10
SEL1	46	SEL1
SEL2	45	SEL2
SEL3	44	SEL3
RSTB	43	RSTB
DO0	42	DO0
DO1	41	DO1
DO2	40	DO2
DO3	39	DO3
DO4	38	DO4
DO5	37	DO5
DO6	36	DO6
DO7	35	DO7
GND	34	GND
DO8	33	DO8
DO9	32	DO9
DO10	31	DO10
DO11	30	DO11
DO12	29	DO12
DO13	28	DO13
DO14	27	DO14
DO15	26	DO15
VCC_S	25	VCC_S
STB	24	STB
U10	23	U10
FB_S	22	FB_S
DRV_S	21	DRV_S
GLED2	20	GLED2
VLED2	19	VLED2
VLED1	18	VLED1
GLED1	17	GLED1
DRV_G	16	DRV_G
GND	15	GND
FB_G	14	FB_G
VGH	13	VGH
GND	12	GND
VGL	11	VGL
CSP	10	CSP
CSM	9	CSM
VCOM_L	8	VCOM_L
VCOM_H	7	VCOM_H
VCOM	6	VCOM
VCOM_O	5	VCOM_O
VCOM	4	VCOM
VCOM	3	VCOM
VCOM	2	VCOM
VCOM	1	VCOM
VCOM	0	VCOM

Connected50



Note: Application circuit for that customer provides private both LED driving V<sub>GH</sub> & V<sub>GL</sub> driving circuit.

Fig. 13 Application circuit for both LED driving and V<sub>GH</sub> & V<sub>GL</sub> driving circuit unused