Doc. version :	0.4
Total pages :	40
Date :	2009/2/24

Product Specification

5.0" COLOR TFT-LCD MODULE

Model Name： **A050VL01 V0**

Planned Lifetime:	From 2009/Jan To 2010/Dec
Phase-out Control:	From 2010/Jul To 2010/Dec
EOL Schedule:	2010/Dec

< >Preliminary Specification

< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2008/10/14		First draft.
0.1	2008/12/03	5	Modify the drawing of touch FPC pin direction
		19	Fig. 4 is corrected
		21, 24	Add the note for some disabled modes
0.2	2009/01/14	8	Modify power consumption
		10	Add I2C Timing Diagram
		12, 13	Add power on/off sequence
0.3	2009/02/24	22	Remove “Currently, AUO just supports periodically interrupt”
		26	Add cover lens suggestion
		3	Power consumption & weight
0.4	2009/04/03	4	Module drawing
		8	VDDI minimum voltage
		12	MDDI Interface characteristics (VESA V1.0)
		12	Dynamic Backlight Control Function
		16	Recommended Power On/Off Sequence
		17	Command Register Map
		19	Recommanded Register Map

Contents

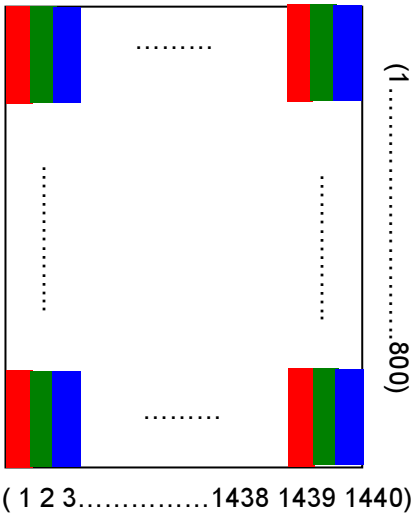
A. General Information

This product is for MID applications.

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	5.0(Diagonal)	
2	Display Resolution	dot	480RGB(H)×800(V)	
3	Overall Dimension	mm	71.1(H) × 119.4(V) × 2.75(T)	Note 1
4	Active Area	mm	64.8(H)×108.0(V)	
5	Pixel Pitch	mm	0.045(H)×0.135(V)	
6	Color Configuration	--	R. G. B. Stripe	Note 2
7	Color Depth	--	16.7M Colors	
8	NTSC Ratio	%	45	
9	Display Mode	--	Normally Black	
10	Panel Surface Treatment	--	Anti-Glare, 3H	
11	Weight	g	65.5	
12	Panel Power Consumption	mW	876	Note 3
13	Interface		MDDI	
14	Touch Panel		Charge-Sensing (Capacitive) Type	
15	Gray Scale Inversion		No GSI	

Note 1: Not include FPCs & cover lens. Refer next page to get further information.

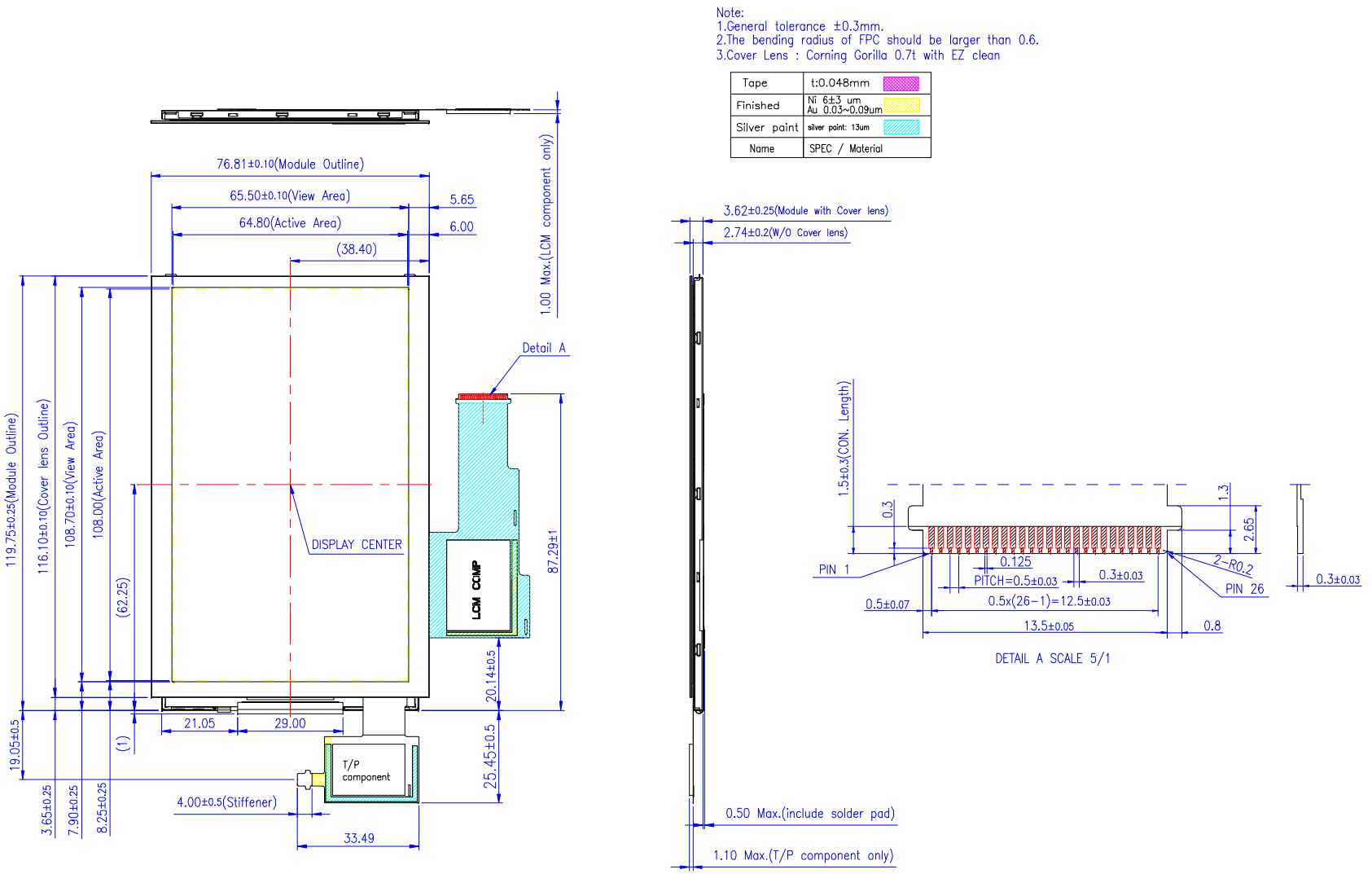
Note 2: Below figure shows dot stripe arrangement.



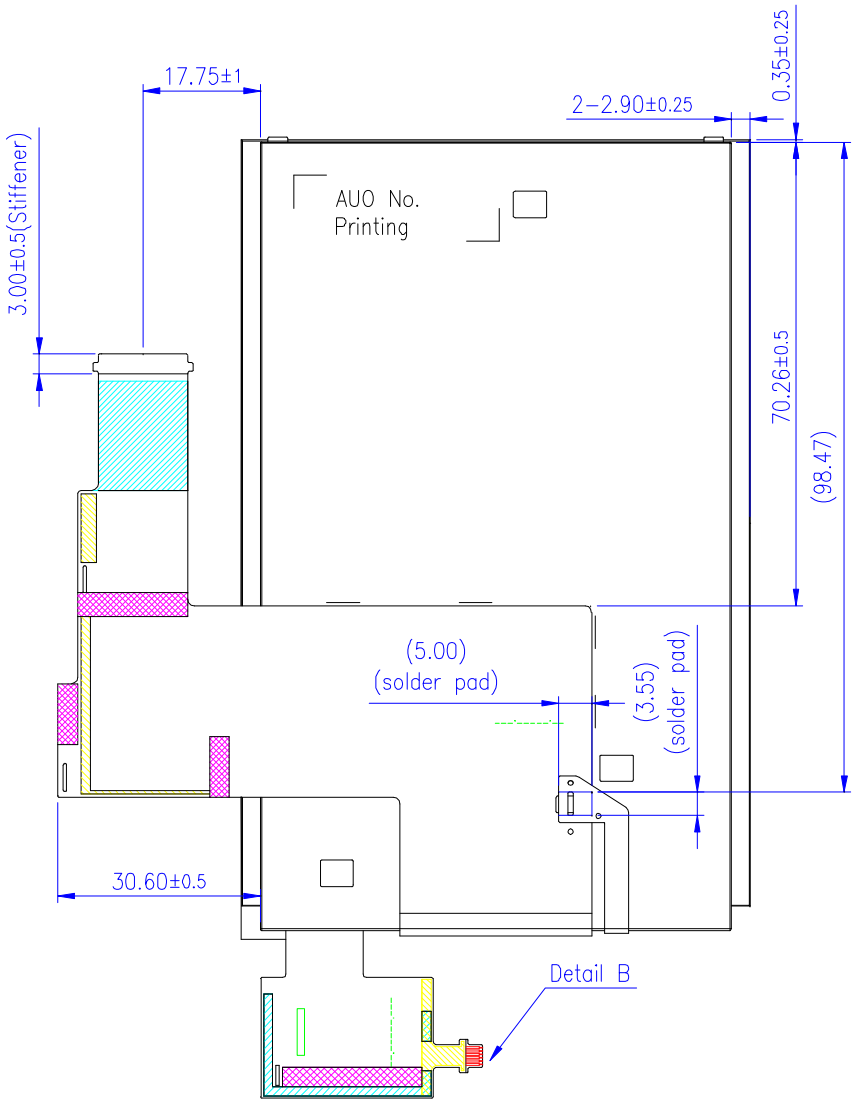
Note 3: Please refer to Electrical Characteristics chapter.

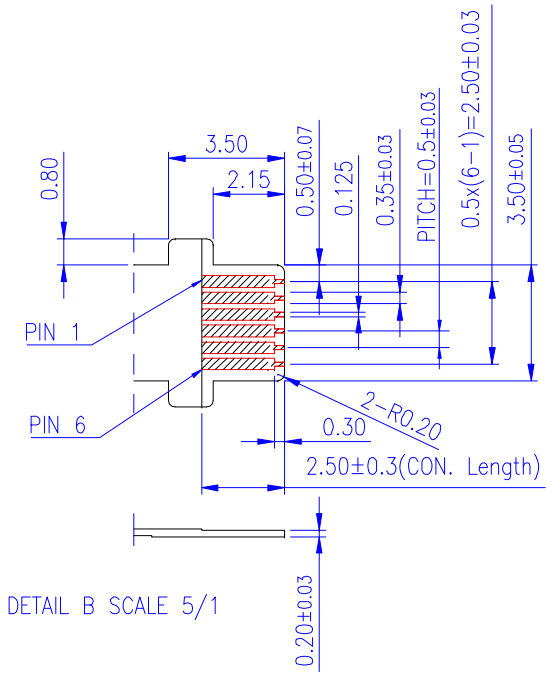
B. Outline Dimension

1. TFT-LCD Module – Front View



2. TFT-LCD Module – Rear View





C. Electrical Specifications

1. Pin Assignment

TFT LCD Panel Pin Assignment:

Recommended connector : FH34S-26S-0.5SH

Pin No.	Symbol	Type	Description	Remark
1	GND	P	Ground for digital circuit	
2	ALS_In	I	Ambient Light sensor In	Connect to GND if do not use.
3	GND	P	Ground for digital circuit	
4	TE	O	Tearing effect output pin to synchronize MCU to frame writing	If not sed, please open this pin.
5	GND	P	Ground for digital circuit	
6	I2C_SDA	I/O	Serial input/output data in I2C-Bus interface operation	Connect to GND if do not use.
7	I2C_SCL	I	Serial input clock in I2C-Bus interface operation	Connect to GND if do not use.
8	GND	P	Ground for digital circuit	
9	RESX	I	H/W reset pin. (Low active)	
10	GND	P	Ground for digital circuit	
11	LEDPWM	O	LED system PWM signal	If not sed, please open this pin.
12	GND	P	Ground for digital circuit	
13	MDDI_STBM	I	MDDI strobe negative signal	
14	MDDI_STBP	I	MDDI strobe positive signal	
15	GND	P	Ground for digital circuit	
16	MDDI_DM	I/O	MDDI data negative signal	
17	MDDI_DP	I/O	MDDI data positive signal	
18	GND	P	Ground for digital circuit	
19	VDDI	P	Digital interface supply voltage of digital	
20	GND	P	Ground for digital circuit	

21	GND	P	Ground for digital circuit	
22	VCI	P	Analog power supply voltage	
23	GND	P	Ground for digital circuit	
24	VLED-	P	Backlight LED cathode	
25	VLED+	P	Backlight LED anode	
26	GND	P	Ground for digital circuit	

Touch Sensor FPC Pin Assignment:

Recommended connector : FH19C-6S-0.5SH(0.5)

Pin No.	Symbol	Type	Description	Remark
1	GND	G	Touch Panel Ground	
2	VDD	P	Touch Panel Power Supply	
3	INT	O	Touched Interrupt Indicator	
4	SCL	I	Serial Communication Clock Input	
5	SDA	I/O	Serial Communication data input/output	
6	NC	-	NC	

Note 1: I: Input; O: Output; P: Power.

Note 2: For correct power on sequence please refer to section 5 “Power On/Off Sequence”

2. Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Input power supply	VDDI	V_{SS}=0V	-0.3	+4.6	V	
Analog power supply	VCI	V_{SS}=0V	-0.3	+4.6	V	

Note 1: If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also, if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

3. Electrical DC Characteristics

a. Typical Operation Condition (GND = 0V)

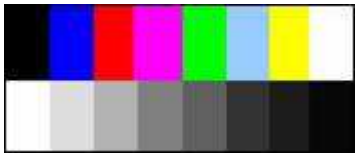
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Input power supply		VDDI	1.65	2.5	3.3	V	
Analog power supply		VCI	2.5	3.0	3.3	V	
Input Signal Voltage	H Level	V_{IH}	0.7VDDI	-	VDDI	V	
	L Level	V_{IL}	GND	-	0.3 VDDI	V	
Output Signal Voltage	H Level	V_{OH}	0.8 VDDI	-	VDDI	V	
	L Level	V_{OL}	GND	-	0.2 VDDI	V	

b. Power Consumption (GND=0V)

Mode	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Normal	P_N	VCI = 3.0V VDDI = 2.5V	-	100	150	mW	Note 1,2
Sleep	P_S		-	8	10	mW	Note 2,3
Deep Stand-by	P_{DS}		-	0.04	0.06	mW	Note 4

Note 1: Test condition is under typical Electrical DC and AC characteristics.

Note 2: Test pattern is the following picture (color bar).



Note 3: In MDDI active

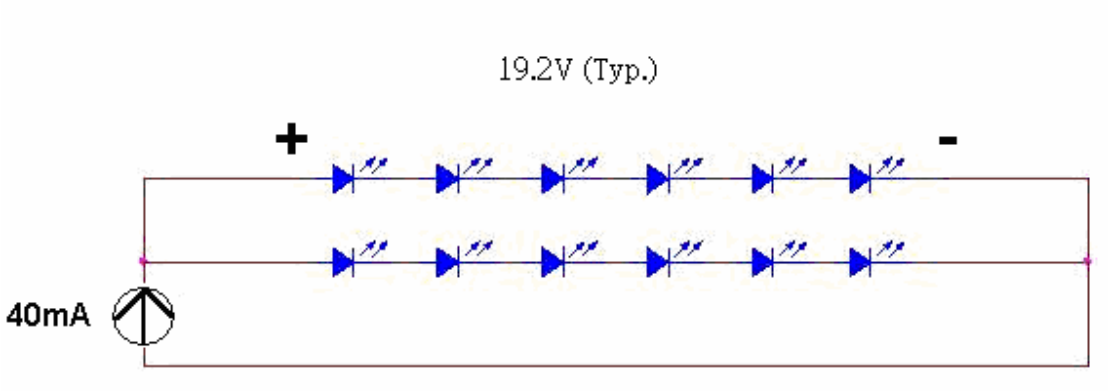
Note 4: In MDDI hibernation mode.

c. Backlight Driving Conditions

The backlight (LED module, Note 1) is suggested to drive by constant current with typical value.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Current	I_L	--	20	22	mA	Note 1
Power	P_L	--	768	950	mW	
LED Life Time	L_L	10,000	--	--	Hr	Note 2, 3

Note 1: LED backlight is two parallel strings and one LED for each string is as the following figure. Suggestion is driven by current 20mA for each LED string.

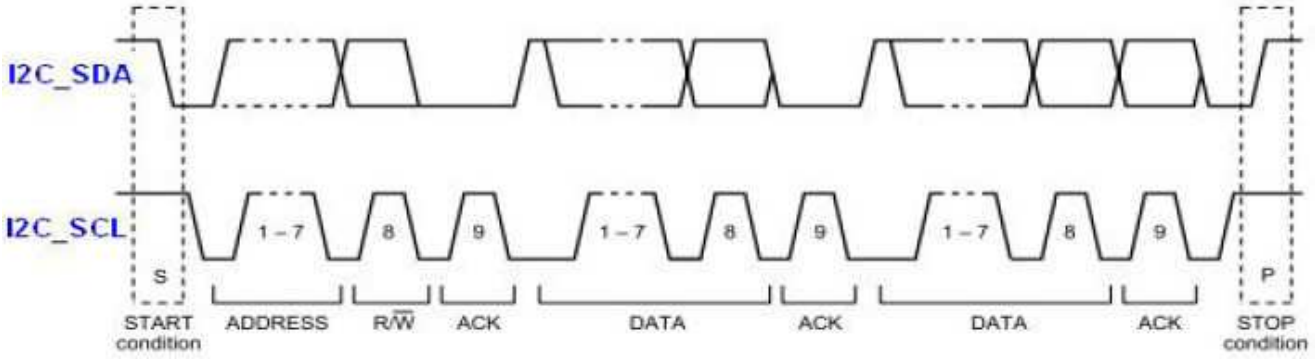


Note 2: Define “LED Lifetime”: brightness is decreased to 50% of the initial value. LED Lifetime is restricted under normal condition, ambient temperature = 25℃ and LED lightbar current = 20 mA.

Note 3: If it uses larger LED lightbar voltage/ current more than 20mA, it maybe decreases the LED lifetime.

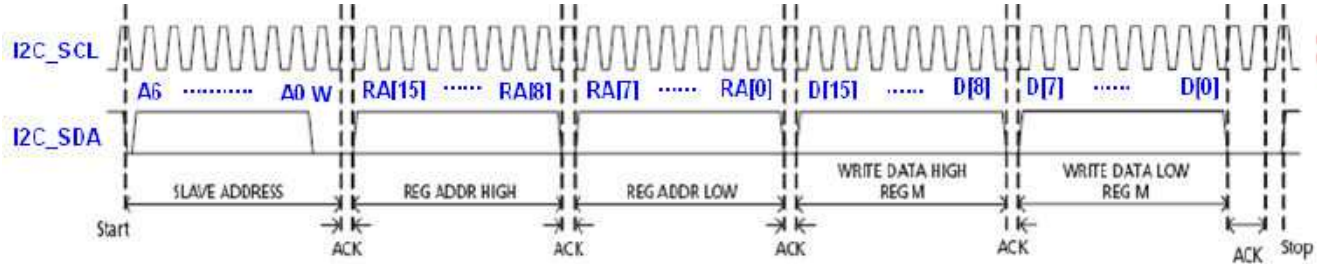
4. Electrical AC Characteristics

a. I2C Timing Diagram



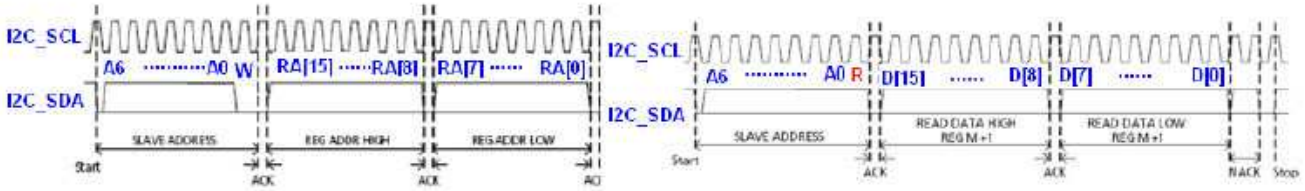
Note : Slave address is 1001100.

b. Register Write Sequence

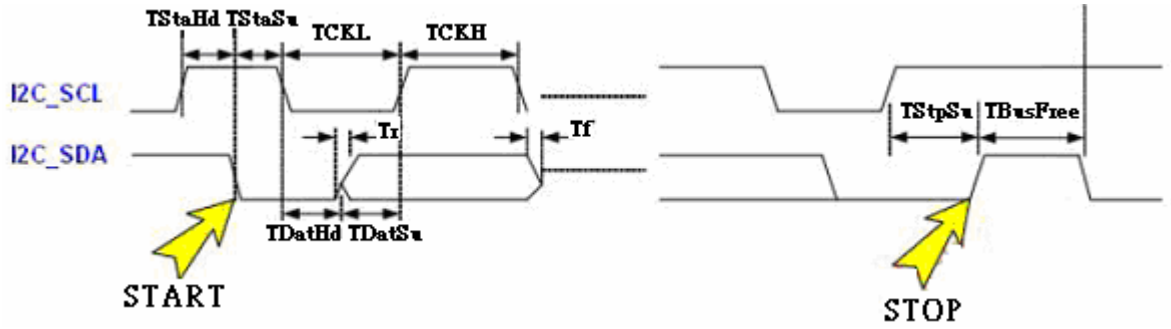


c. Register Read Sequence

S = start condition
P = stop condition
Sr = restart condition
A = acknowledge
Ā = no-acknowledge
slave to master
master to slave



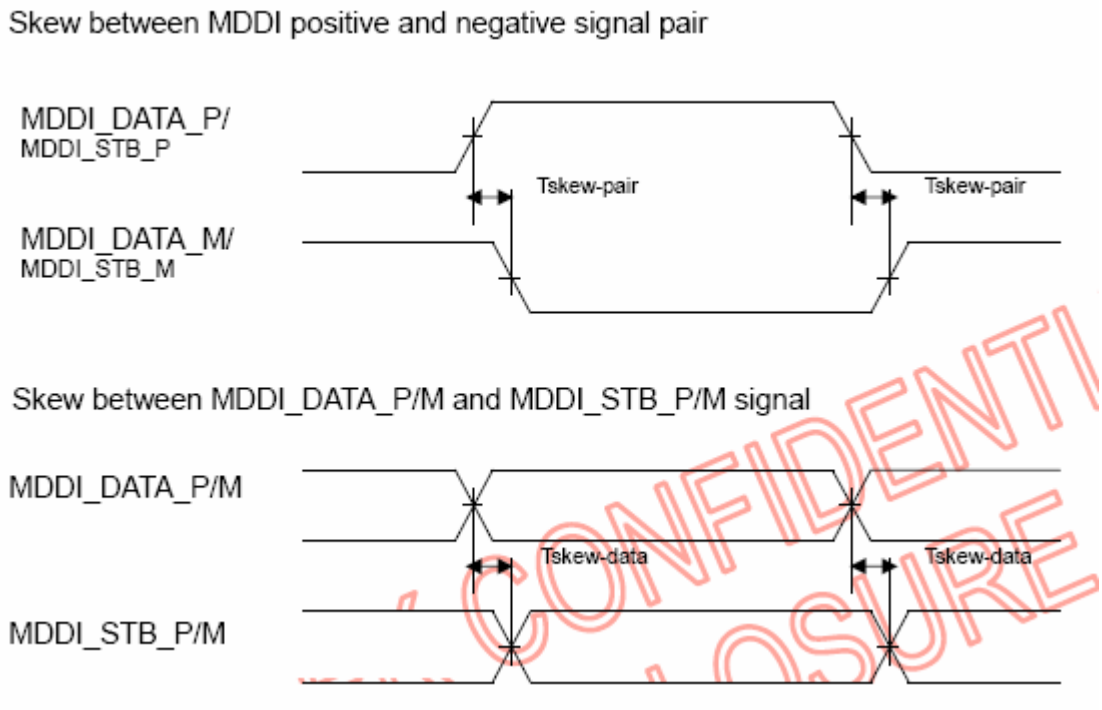
d. I2C Timing Characteristics



VDDI=1.65~3.3V, VCI=2.5~3.3V, TA=25℃

Item	Symbol	Min.	Typ.	Max.	Unit
Working Frequency	Fclk	-	-	400	KHz
I2C Clock Low	TckL	1250	-	-	ns
I2C Clock High	TckH	1250	-	-	ns
I2C Data ring time	Tr	-	-	300	ns
I2C Data falling time	Tf	-	-	300	ns
I2C Data hold time	TDatHd	0	-	-	ns
I2C Data setup time	TDatSu	100	-	-	ns
I2C Start Condition hold time	TStaHd	600	-	-	ns
I2C Start Condition setup time	TStaSu	600	-	-	ns
I2C Stop Condition setup time	TStpSu	600	-	-	ns
I2C Bus free time	TBusFree	1300	-	-	ns

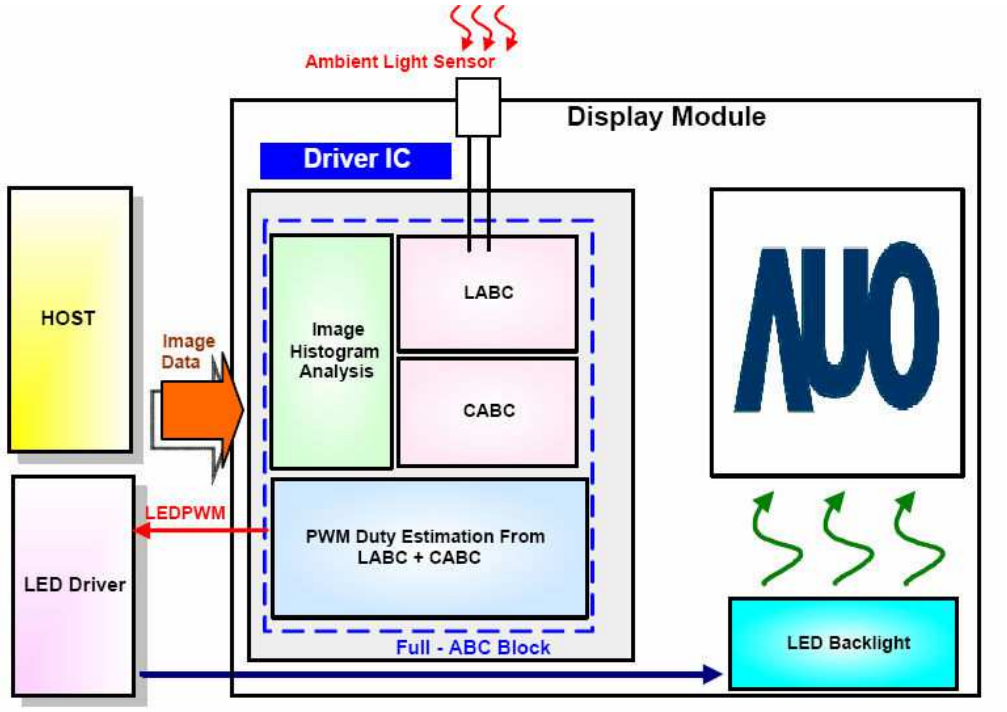
e. MDDI Interface characteristics (VESA V1.0)



VDDI=1.65~3.3V, VCI=2.5~3.3V, TA=25℃

Item	Symbol	Min.	Typ.	Max.	Unit
Data transfer rate	1/tBIT	-	350	400	Mbps
Differential transfer input skew	| Tskew-pair |	-	-	0.25	ns
Data_stb input skew	| Tskew-data |	-	-	0.3	ns

f. Dynamic Backlight Control Function



(a) PWM Control

The registers PWMDIV[7 : 0] can change the frequency of the PWM signal.

The PWM operation frequency “FOSC” can be selected by the register bit “PWMF”, so two PWM operation frequencies can be selected as shown in below table:

Register Bit “PWMF”	PWM Operation Frequency – “F_{OSC}”
0	5.5 MHz
1	11 MHz (Default)

The PWM operation frequency “FOSC” is “not” the real PWM frequency, the “FOSC” is used to provide clock source for the internal PWM circuit. Actually, the real PWM frequency can be quickly estimated by the bellow formula:

$$\text{PWM Frequency} = \frac{F_{OSC}}{256 \times PWMDIV[7:0]}$$

So the relations between “PWMF”, “FOSC”, actually PWM frequency are shown in below table:

Register Bit “PWMF”	PWM Operation Frequency – “F_{OSC}”	Real PWM Frequency
0	5.5 MHz	$\frac{5.5\,\text{MHz}}{256 \times PWMDIV[7:0]}$
1	11 MHz (Default)	$\frac{11\,\text{MHz}}{256 \times PWMDIV[7:0]}$

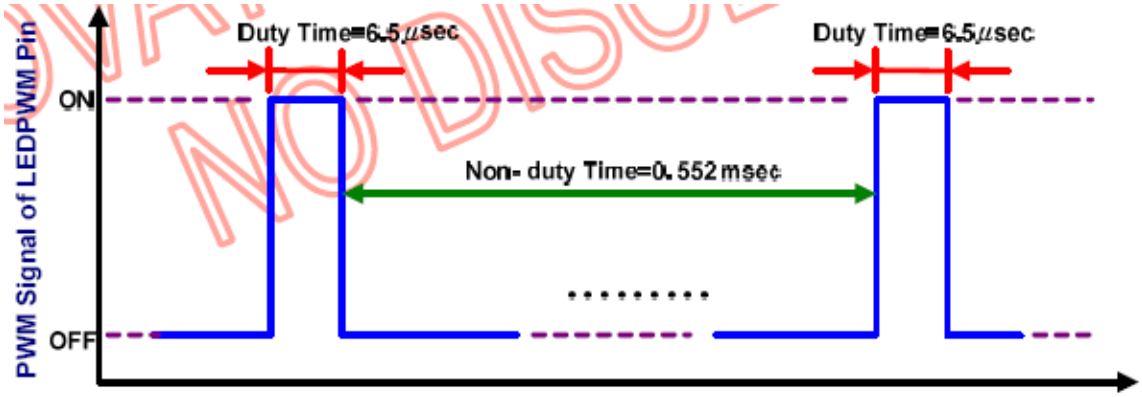
For Example: If the “PWMDIV[7 : 0]” = 0Ch, and “PWMF” = “0”, then:

In this condition, when PWM duty is estimated as “3” , then the duty time of the PWM Signal can be estimated as shown in below:

$$\text{PWM Duty Time} = \frac{3}{256} \times \frac{1}{1.79\,\text{KHz}} \approx 6.54\,\mu\text{sec}$$

$$\text{PWM Non-duty Time} = \frac{(256-3)}{256} \times \frac{1}{1.79\,\text{KHz}} \approx 0.552\,\text{msec}$$

The above duty calculations can be illustrated in below for detailed:

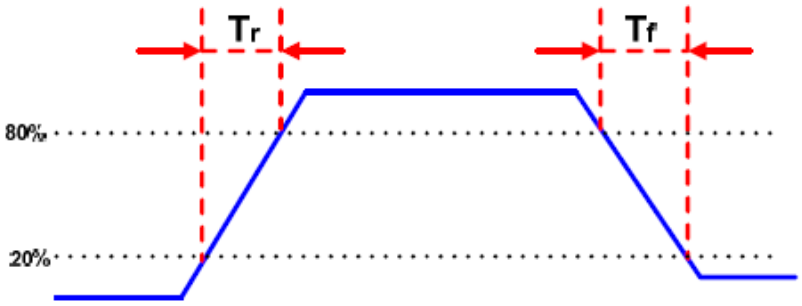


In the other way, there are some registers are simply introduced in below (See the chapter 6 for

details):

DBV[7 : 0]: Writing this register in address 5100h is used to adjust the backlight brightness value when LABC function is disabled (means the register bit “A” is set as “0”).

Note: The rising time (Tr) and falling time (Tf) of the “LED_PWM” signal are stipulated to be equal to or less than 15ns.



(b) CABC(Content Adaptive Brightness Control (CABC)

A Content Adaptive Brightness Control (CABC) function can be used to reduce the power consumption of the luminance source. Content adaptation means that content grey level scale can be increased while simultaneously decreasing brightness of the backlight to achieve same perceived brightness. The adjusted grey level scale and thus the power consumption reduction depend on the content of the image. The NVT CABC algorithm can adjust the brightness of each gray level without changing the original image contents.

The NVT CABC function provides four operation modes, and these modes can be selected by the register 5500h.

See command “Write Content Adaptive Brightness Control (5500h)” (CABC_COND[1 : 0]) for more information.

These four modes are described as:

- Off Mode:

Content Adaptive Brightness Control functionality is completely turn-off. In this mode, panel will use the original Gamma 2.2 registers setting for display. And if the function of “forced PWM duty” is turn-off (i.e.“FORCE_CABC_PWM” is set as ‘0’), the PWM duty of the “LEDPWM” pin is 100%.

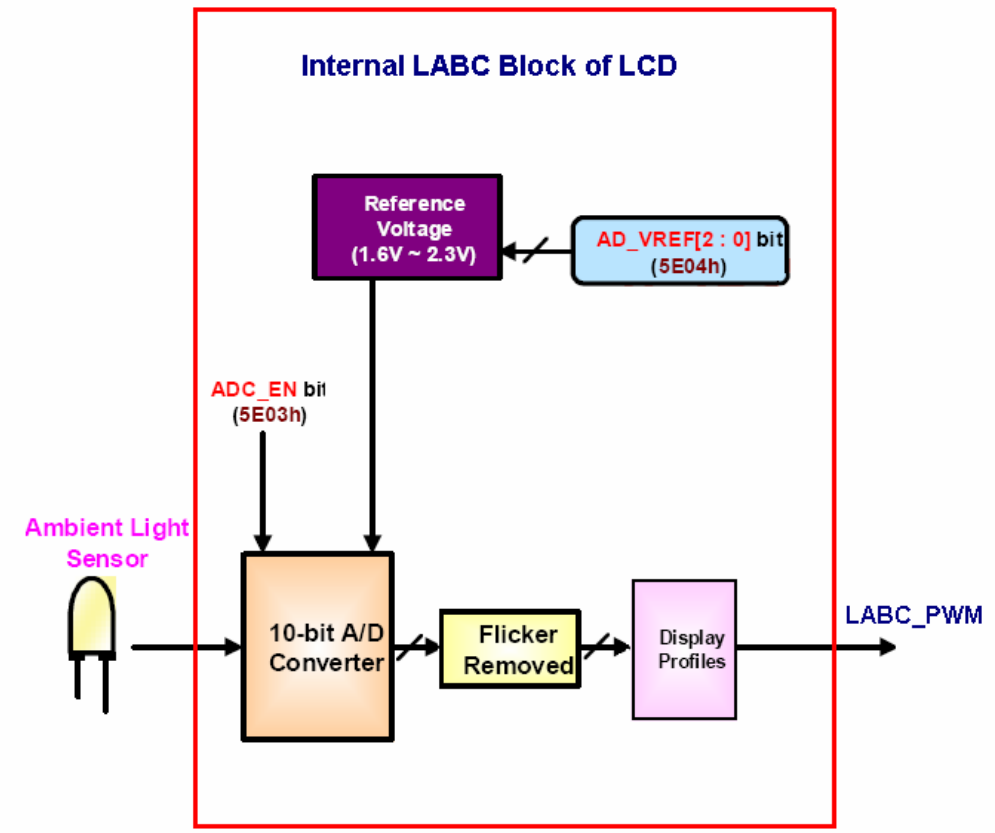
-Still Picture Mode (Still Mode):

This mode is used to gain a better display quality for still picture. Some image quality degradation would be acceptable. Ideal power consumption reduction ratio is more than 30%. The panel will automatically estimate a better gamma setting and PWM duty based on different image contents, so the reduction ratio of the power consumption of backlight is not a constant ratio, this ratio will vary between 10% ~ 40% with different image contents.

- Moving Image Mode (Moving Mode):

User can select this mode to keep the moving image quality and reduce the power consumption of backlight. It is focused on the biggest power reduction with image quality degradation. Idea power consumption reduction ratio is more than 30%.

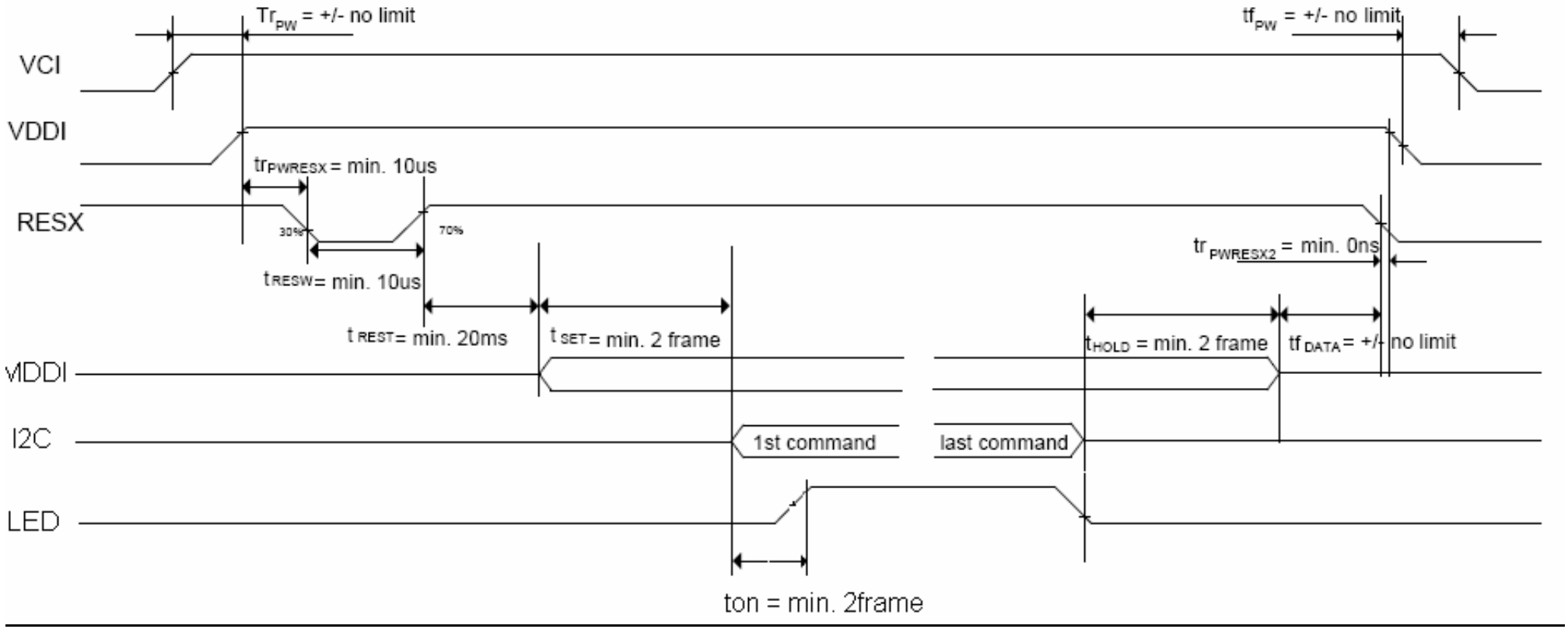
(c) Light Sensor based Automatic Backlight Control (LABC)



5. Power On/Off Characteristics

a. Recommended Power On/Off Sequence

The LCD adopts high voltage driver IC, so it could be permanently damaged under a wrong power on/off sequence. The suggested LCD power sequence is below:



6. Command Register Map

a. COMMAND DESCRIPTIONS

Addr.	Instruction	D15~D08	D07	D06	D05	D04	D03	D02	D01	D00
(1000h)	ENTER_SLEEP _MODE	-	-	-	-	-	-	-	-	-
(1100h)	EXIT_SLEEP_MODE	- -	-	-	-	-	-	-	-	-
(2800h)	SET_DISPLAY_OFF	-	-	-	-	-	-	-	-	-
(2900h)	SET_DISPLAY_ON	-	-	-	-	-	-	-	-	-
(2C00h)	WRITE_MEMORY _START	-	D7	D6	D5	D4	D3	D2	D1	D0
		-	:	:	:	:	:	:	:	:
		-	D7	D6	D5	D4	D3	D2	D1	D0

Addr.	Instruction	D15~D08	D07	D06	D05	D04	D03	D02	D01	D00
(C000h)	PWCTR1	-	VGMP[7]	VGMP[6]	VGMP[5]	VGMP[4]	VGMP[3]	VGMP[2]	VGMP[1]	VGMP[0]
(C002h)	PWCTR2	-	VGMN[7]	VGMN[6]	VGMN[5]	VGMN[4]	VGMN[3]	VGMN[2]	VGMN[1]	VGMN[0]
(C100h)	PWCTR3		-	VGCLKA[2]	VGCLKA[1]	VGCLKA[0]	BTHA[1]	BTHA[0]	BTLA[1]	BTLA[0]
(C200h)	PWCTR4	-	-	VBPA[2]	VBPA[1]	VBPA[0]	-	-	BTPA[1]	BTPA[0]
(C202h)	PWCTR5	-	-	VBNA[2]	VBNA[1]	VBNA[0]	-	-	BTNA[1]	BTNA[0]
(C700h)	VCOM	-	VM[7]	VM[6]	VM[5]	VM[4]	VM[3]	VM[2]	VM[1]	VM[0]

WRPFD : Write Profile Values for Display (5000h~500Fh)

Addr.	Instruction	D15~D08	D07	D06	D05	D04	D03	D02	D01	D00
(5000h)	WRPFD	0	0	STEP_OUTDP0[7]	STEP_OUTDP0[6]	STEP_OUTDP0[5]	STEP_OUTDP0[4]	STEP_OUTDP0[3]	STEP_OUTDP0[2]	STEP_OUTDP0[1]
(5001h)		0	0	STEP_OUTDP1[7]	STEP_OUTDP1[6]	STEP_OUTDP1[5]	STEP_OUTDP1[4]	STEP_OUTDP1[3]	STEP_OUTDP1[2]	STEP_OUTDP1[1]
(5002h)		0	0	STEP_OUTDP2[7]	STEP_OUTDP2[6]	STEP_OUTDP2[5]	STEP_OUTDP2[4]	STEP_OUTDP2[3]	STEP_OUTDP2[2]	STEP_OUTDP2[1]
(5003h)		0	0	STEP_OUTDP3[7]	STEP_OUTDP3[6]	STEP_OUTDP3[5]	STEP_OUTDP3[4]	STEP_OUTDP3[3]	STEP_OUTDP3[2]	STEP_OUTDP3[1]
(5004h)		0	0	STEP_OUTDP4[7]	STEP_OUTDP4[6]	STEP_OUTDP4[5]	STEP_OUTDP4[4]	STEP_OUTDP4[3]	STEP_OUTDP4[2]	STEP_OUTDP4[1]
(5005h)		0	0	STEP_OUTDP5[7]	STEP_OUTDP5[6]	STEP_OUTDP5[5]	STEP_OUTDP5[4]	STEP_OUTDP5[3]	STEP_OUTDP5[2]	STEP_OUTDP5[1]

Addr.	Instruction	D15~D08	D07	D06	D05	D04	D03	D02	D01	D00
(5300h)	WRCTRLD	0	0	0	BCTRL	A	DD	BL	0	0

This command is used to control the "LEDPWM" pin, dimming function for CABC, ambient light sensing, and LABC mode switching.

BCTRL : Turn On/Off the brightness control block with the dimming effect.
About the register "LEDPWPOL", please refer to the register "CTRLEDPWM (5301h)"

BCTRL	LEDPWPOL	LEDPWM Pin Final State	Backlight Final State
0	0	Keep "LOW" (0% PWM Duty) (Default)	OFF
1	0	PWM Output (High level is duty)	ON
0	1	Keep "HIGH" (0% PWM Duty)	OFF
1	1	Inversed PWM Output (Low level is duty)	ON

A : This command is used to control ambient light, brightness and gamma settings.

A	Ambient Light Sensing
0	OFF (Ambient Light Sensing OFF) (Default)
1	ON (Ambient Light Sensing ON)

DD : Enable/Disable dimming function only for CABC.

DD	CABC Dimming Function
0	Disabled
1	Enabled (Default)

BL : Turn On/Off the backlight control without dimming effect.

BL	Backlight Control
0	OFF
1	ON (Default)

When BL bit change from "1" to "0", backlight is turned off without gradual dimming, even if dimming-on (DD = "1") are selected.

WRHYSTE : Write Increment / Decrement Hysteresis (5700h~5717H)

Addr.	Instruction	D15~D08	D07	D06	D05	D04	D03	D02	D01	D00
(5700h)	WRHYSTE	0	IO1[15 : 8]							
(5701h)		0	IO1[7 : 0]							
(5702h)		0	D01[15 : 8]							
(5703h)			DO1[7 : 0]							
: :		: :	: :							
(5714h)		0	IO5[15 : 8]							
(5715h)		0	IO5[7 : 0]							
(5716h)		0	D06[15 : 8]							
(5717h)		0	IO6[7 : 0]							

7. Recommanded Register Map

a. Recommended Power On Register Setting

Number	Address	Data
1	1100h	-
2	C000h	8Ah
3	C002h	8Ah
4	C200h	02h
5	C202h	32h
6	C100h	40h
7	C700h	8Bh
Wait for more than 120ms		
8	2900h	-
9	2C00	-

b. Recommended Power Off Register Setting

Number	Address	Data
1	2800h	-
2	1100h	-

c. Recommended CABC On Register Setting

Number	Address	Data
1	5300h	2Ch
2	5500h	03h

d. Recommended CABC Off Register Setting

Number	Address	Data
1	5300h	24h

e. Recommended LABC On Register Setting

Number	Address	Data
1	5300h	34h
2	5500h	03h
3	5700h	00h
4	5701h	3Ch
5	5704h	01h
6	5705h	08h

7	5708h	01h
8	5709h	90h
9	570Ch	02h
10	570Dh	30h
11	5710h	02h
12	5711h	FCh
13	5714h	03h
14	5715h	FFh
15	5702h	00h
16	5703h	28h
17	5706h	00h
18	5707h	E0h
19	570Ah	01h
20	570Bh	40h
21	570Eh	02h
22	570Fh	08h
23	5712h	02h
24	5713h	ACh
25	5716h	03h
26	5717h	FFh

f. Recommended CABC Off Register Setting

Number	Address	Data
1	5300h	24h

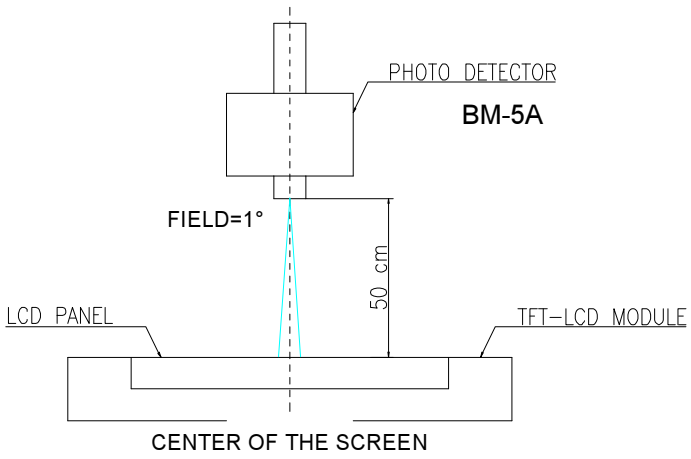
D. Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time								
Rise		Tr	θ=0°	--	20	35	ms	Note 3
Fall		Tf		--	15	35	ms	
Contrast ratio		CR	At optimized viewing angle	640	800	--		Note 4
Viewing Angle	Top		CR≥10	70	80	--	deg.	Note 5
	Bottom			70	80	--		
	Left			70	80	--		
	Right			70	80	--		
Brightness		Y_L	θ=0°	320	400	--	cd/m^2	Note 6
Chromaticity	White	X	θ=0°	0.27	0.31	0.35		
		Y	θ=0°	0.295	0.335	0.375		
	Red	X	θ=0°	0.54	0.58	0.62		
		Y	θ=0°	0.29	0.33	0.37		
	Green	X	θ=0°	0.29	0.33	0.37		
		Y	θ=0°	0.515	0.555	0.595		
	Blue	X	θ=0°	0.105	0.145	0.185		
		Y	θ=0°	0.065	0.105	0.145		
Uniformity		ΔY_L	%	70	75	--	%	Note 7

Note 1: Measured under Ambient temperature =25°C, and LED lightbar current I_L = 20mA in the dark room.

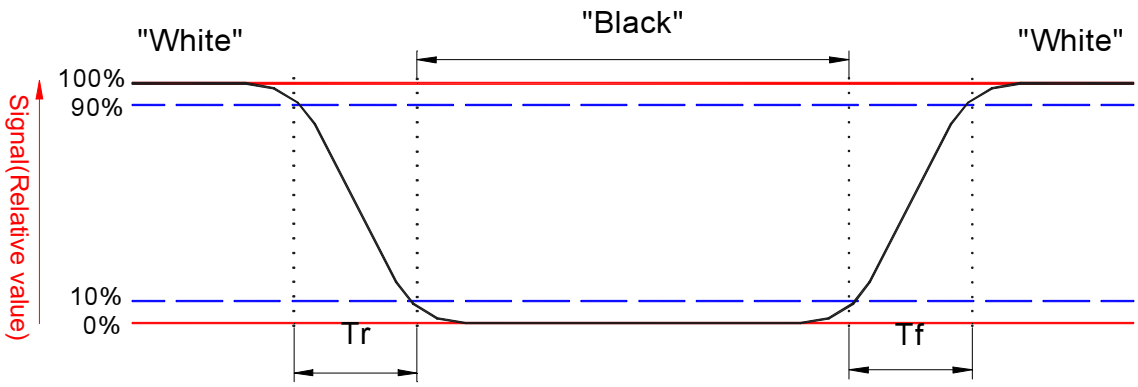
Note 2: To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5A, after 15 minutes operation.



Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white” (falling time) and from “white” to “black” (rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

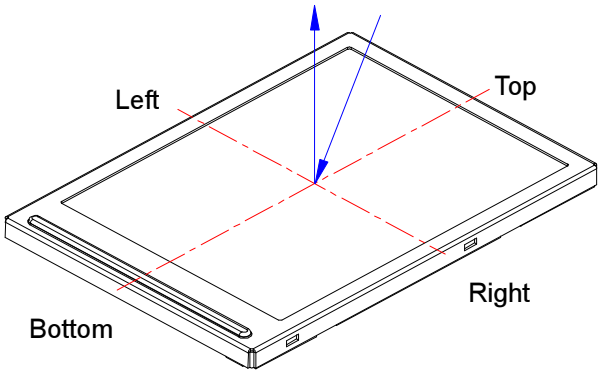


Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

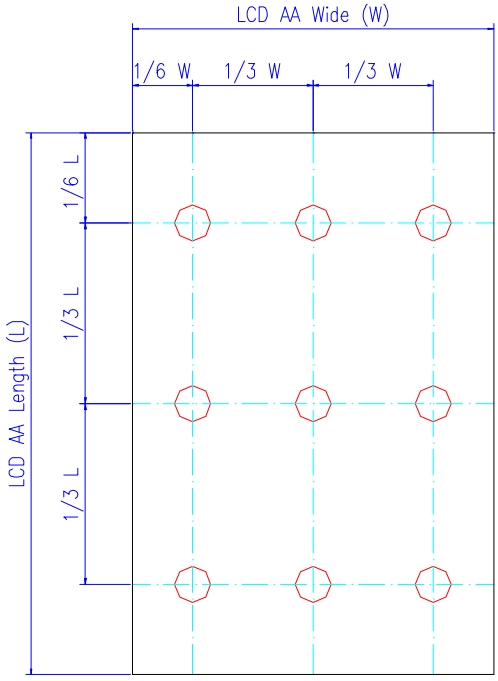
$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

Note 5. Definition of viewing angle, θ, Refer to figure as below.



Note 6: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 7: Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

E. Touch Panel Command and Register Map

1. I2C Protocol Definition

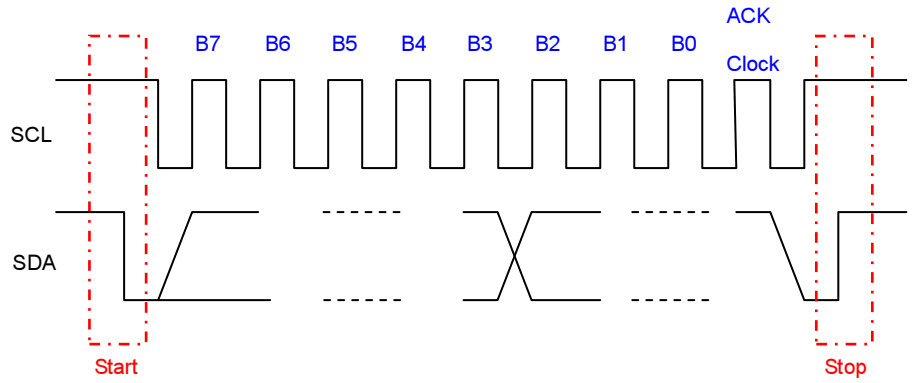


Figure 1. Standard I^2C Transaction Unit

The sensor controller supports standard I^2C protocol with SCL up to 400KHz. The device address is 0x5C. The chip also provides both single and sequential access. Figure 2 shows the write operation using single or sequential mode. Figure 3 also depicts the standard I2C transaction for single for sequential read mechanism.

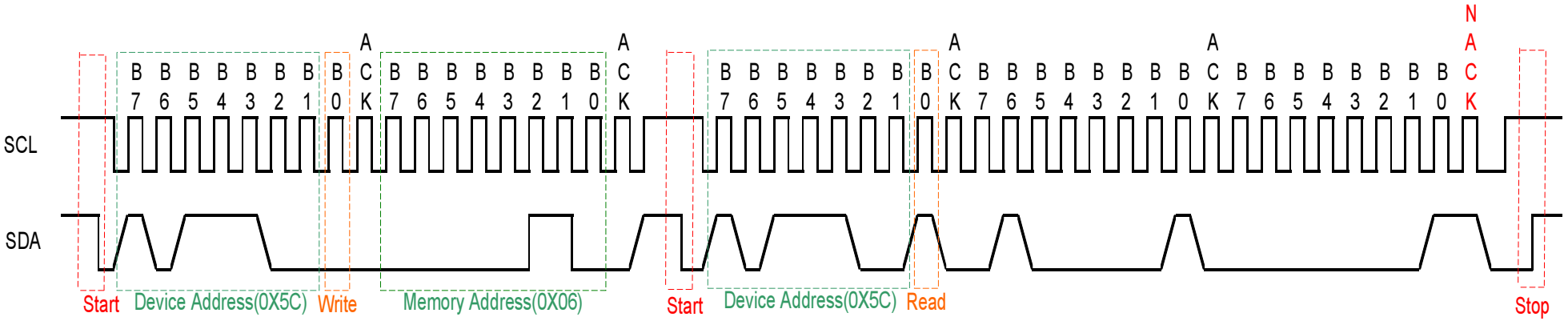
Write Operation																
Single	Start	Device Address (W)	A	Mem Addr	A	Data[0]	A	Stop								
Sequential	Start	Device Address (W)	A	Mem Addr	A	Data[0]	A	Data[1]	A	……	A	Data[n]	A	Stop		

Figure 2. Write Operation with Single/Multiply Access

Read Operation																
Single	Start	Device Address (W)	A	Mem Addr	A	Start	Device Address (R)	A	Data[0]	NA	Stop					
Sequential	Start	Device Address (W)	A	Mem Addr	A	Start	Device Address (R)	A	Data[0]	A	……	A	Data[n]	NA	Stop	

Figure 3. Read Operation with Single/Multiply Acce

Suppose the Y[3] raw data is 321. If only Y[3] is read, user should issue the waveform as following:



2. Raw Data Register Map

Addr.	Addr.(HEX)	Description	R/W	B7	B7	B7	B7	B7	B7	B7	B7
7	77	CH[7]_LSB	R	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]
7	77	CH[7]_SSB	R	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[S]	ADC_7[S]
7	77	CH[7]_LSB	R	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]
7	77	CH[7]_SSB	R	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[S]	ADC_7[S]
7	77	CH[7]_LSB	R	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]
7	77	CH[7]_SSB	R	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[S]	ADC_7[S]
7	77	CH[7]_LSB	R	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]
7	77	CH[7]_SSB	R	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[S]	ADC_7[S]
S	7S	CH[7]_LSB	R	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]
S	7S	CH[7]_SSB	R	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[S]	ADC_7[S]
77	7A	CH[7]_LSB	R	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]
77	7B	CH[7]_SSB	R	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[S]	ADC_7[S]
77	7C	CH[7]_LSB	R	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]
77	7D	CH[7]_SSB	R	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[S]	ADC_7[S]
77	7E	CH[7]_LSB	R	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]	ADC_7[7]
77	7S	CH[7]_SSB	R	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[77]	ADC_7[S]	ADC_7[S]
77	77	CH[S]_LSB	R	ADC_S[7]	ADC_S[7]	ADC_S[7]	ADC_S[7]	ADC_S[7]	ADC_S[7]	ADC_S[7]	ADC_S[7]
77	77	CH[S]_SSB	R	ADC_S[77]	ADC_S[77]	ADC_S[77]	ADC_S[77]	ADC_S[77]	ADC_S[77]	ADC_S[S]	ADC_S[S]
7S	77	CH[S]_LSB	R	ADC_S[7]	ADC_S[7]	ADC_S[7]	ADC_S[7]	ADC_S[7]	ADC_S[7]	ADC_S[7]	ADC_S[7]
7S	77	CH[S]_SSB	R	ADC_S[77]	ADC_S[77]	ADC_S[77]	ADC_S[77]	ADC_S[77]	ADC_S[77]	ADC_S[S]	ADC_S[S]
77	77	CH[77]_LSB	R	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]
77	77	CH[77]_SSB	R	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[S]	ADC_77[S]
77	77	CH[77]_LSB	R	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]
77	77	CH[77]_SSB	R	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[S]	ADC_77[S]
77	7S	CH[77]_LSB	R	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]
77	7S	CH[77]_SSB	R	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[S]	ADC_77[S]
77	7A	CH[77]_LSB	R	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]
77	7B	CH[77]_SSB	R	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[S]	ADC_77[S]
7S	7C	CH[77]_LSB	R	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]
7S	7D	CH[77]_SSB	R	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[S]	ADC_77[S]
77	7E	CH[77]_LSB	R	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]
77	7S	CH[77]_SSB	R	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[S]	ADC_77[S]
77	77	CH[77]_LSB	R	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]
77	77	CH[77]_SSB	R	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[S]	ADC_77[S]
77	77	CH[77]_LSB	R	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]
77	77	CH[77]_SSB	R	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[S]	ADC_77[S]
77	77	CH[7S]_LSB	R	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]
77	77	CH[7S]_SSB	R	ADC_7S[77]	ADC_7S[77]	ADC_7S[77]	ADC_7S[77]	ADC_7S[77]	ADC_7S[77]	ADC_7S[S]	ADC_7S[S]
7S	77	CH[7S]_LSB	R	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]
7S	77	CH[7S]_SSB	R	ADC_7S[77]	ADC_7S[77]	ADC_7S[77]	ADC_7S[77]	ADC_7S[77]	ADC_7S[77]	ADC_7S[S]	ADC_7S[S]
77	7S	CH[77]_LSB	R	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]
77	7S	CH[77]_SSB	R	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[S]	ADC_77[S]
77	7A	CH[77]_LSB	R	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]
77	7B	CH[77]_SSB	R	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[S]	ADC_77[S]
77	7C	CH[77]_LSB	R	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]
77	7D	CH[77]_SSB	R	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[S]	ADC_77[S]
77	7E	CH[77]_LSB	R	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]
77	7S	CH[77]_SSB	R	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[S]	ADC_77[S]
7S	77	CH[77]_LSB	R	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]
7S	77	CH[77]_SSB	R	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[S]	ADC_77[S]
77	77	CH[77]_LSB	R	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]
77	77	CH[77]_SSB	R	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[S]	ADC_77[S]
77	77	CH[77]_LSB	R	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]
77	77	CH[77]_SSB	R	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[S]	ADC_77[S]
77	77	CH[77]_LSB	R	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]
77	77	CH[77]_SSB	R	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[S]	ADC_77[S]
77	7S	CH[7S]_LSB	R	ADC_7S[7]	ADC_77[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]
77	7S	CH[7S]_SSB	R	ADC_7S[77]	ADC_77[77]	ADC_7S[77]	ADC_7S[77]	ADC_7S[77]	ADC_7S[77]	ADC_7S[S]	ADC_7S[S]
7S	7A	CH[7S]_LSB	R	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]	ADC_7S[7]
7S	7B	CH[7S]_SSB	R	ADC_7S[77]	ADC_77[77]	ADC_7S[77]	ADC_7S[77]	ADC_7S[77]	ADC_7S[77]	ADC_7S[S]	ADC_7S[S]
77	7C	CH[77]_LSB	R	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]
77	7D	CH[77]_SSB	R	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[S]	ADC_77[S]
77	7E	CH[77]_LSB	R	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]	ADC_77[7]
77	7S	CH[77]_SSB	R	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[77]	ADC_77[S]	ADC_77[S]

Note: Chip provides 10-bit ADC capability at least. While the unused ADC bit should be reserved as '0'

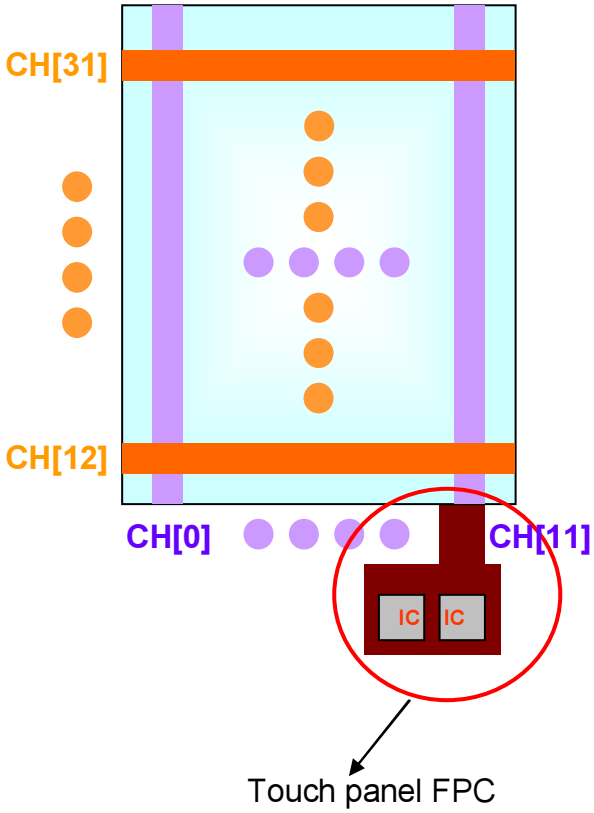


Figure4. Reference of channel location diagram

3. Coordinate Register Map

Addr.	Addr.(HEX)	Description	R/W	B7	B7	B7	B7	B7	B7	B7	B7
77	77	X7 (LSB)	R	X7[7]	X7[7]	X7[7]	X7[7]	X7[7]	X7[7]	X7[7]	X7[7]
77	77	] 7 (LSB)	R	] 7[7]	] 7[7]	] 7[7]	] 7[7]	] 7[7]	] 7[7]	] 7[7]	] 7[7]
77	77	X7 (LSB)	R	X7[7]	X7[7]	X7[7]	X7[7]	X7[7]	X7[7]	X7[7]	X7[7]
77	77	] 7 (LSB)	R	] 7[7]	] 7[7]	] 7[7]	] 7[7]	] 7[7]	] 7[7]	] 7[7]	] 7[7]
7]	77	X7 (] SB)	R	7	7	7	7	7	7	X7[ ]	X7[ ]
7]	77	] 7 (] SB)	R	7	7	7	7	7	7	] 7[ ]	] 7[ ]
77	77	X7 (] SB)	R	7	7	7	7	7	7	X7[ ]	X7[ ]
77	77	] 7 (] SB)	R	7	7	7	7	7	7	] 7[ ]	] 7[ ]

Note: (1) (X1, Y1) means left-up touched point
(X2, Y2) means right-down touched point

(2) The coordinate of X1 = X1(LSB) + X1(MSB)*256, X2 = X2(LSB) + X2(MSB)*256, Y1 = Y1(LSB) + Y1(MSB)*256, Y2 = Y2(LSB) + Y2(MSB)*256

(3)

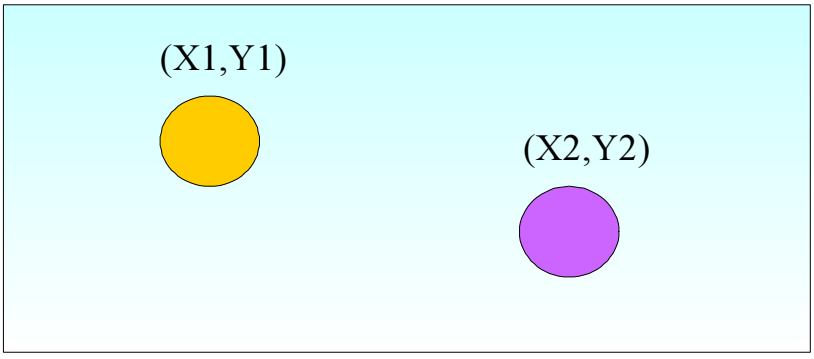


Figure5. Reference of touched point diagram

If touched point of (X1,Y1) 、(X2, Y2) is (14,50) and (280,160), the coordinate register map will be recorded as following:

Addr.	Addr.(HEX)	Description	R/W	B7	B7	B7	B7	B7	B7	B7	B7
77	77	X7 (LSB)	R	7	7	7	7	7	7	7	7
77	77	] 7 (LSB)	R	7	7	7	7	7	7	7	7
77	77	X7 (LSB)	R	7	7	7	7	7	7	7	7
77	77	] 7 (LSB)	R	7	7	7	7	7	7	7	7
7]	77	X7 (] SB)	R	7	7	7	7	7	7	7	7
7]	77	] 7 (] SB)	R	7	7	7	7	7	7	7	7
77	77	X7 (] SB)	R	7	7	7	7	7	7	7	7
77	77	] 7 (] SB)	R	7	7	7	7	7	7	7	7

4. Sensitivity and Noise Threshold

Addr.	Addr.(HEX)	Description	R/W	B7	B7	B7	B7	B7	B7	B7	B7
777	77	X_SENSITIVITY	R/W	X_SENSITIVITY[7:7]							
777	77	Y_SENSITIVITY	R/W	Y_SENSITIVITY[7:7]							

Note: (1) X_SENSITIVITY/Y_SENSITIVITY
X and Y Channels' sensitivity should be adjustable for coordinate calculation. These parameter doesn't effect the raw data output.
(2) The sensitivity is divided into 256 steps; '0' means most sensitive and '255' means least sensitive.
The coordinate calculation should according to given sensitivity setting. while the touch's raw data is greater than given parameter X_SENSITIVITY/Y_SENSITIVITY, the data is regarded as valid or will be seen as useless.

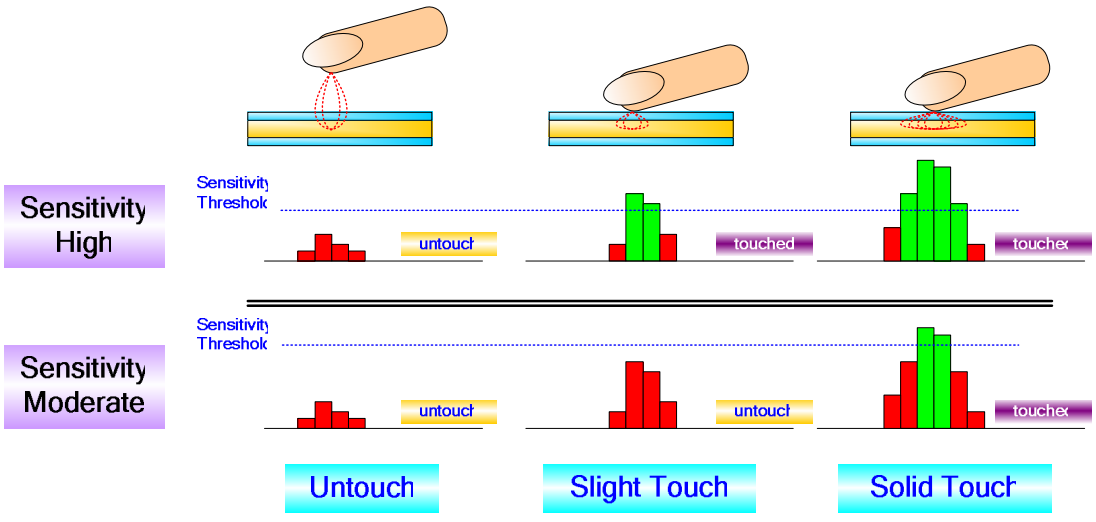


Figure 6. Sensitivity Adjustment

5. Interrupt Operation Mode

This chip should support both polling and interrupt way to get the coordinate and raw data by I2C interface. The figure below depicts the interruption operation.

5.1 Interrupt Mode Setting

Addr.	Addr.(HEX)	Description	R/W	B7	B7	B7	B7	B7	B7	B7	B7
777	77	INT_SETTING	R/W	7	7	7	7	EN_INT	INT_POL	INT_L ODE[7]	INT_L ODE[7]
777	77	INT_WIDTH	R/W	INT_WIDTH[7:7]							

Note: (1) EN_INT
0: Disable interrupt mechanism 1: Enable interrupt mechanism
(2) INT_POL
0: The interrupt is low-active 1: the interrupt is high-active
(3) INT_ MODE[1:0]
00: INT assert periodically 01: INT assert only when coordinate difference
10: Touch Indicate 11: Reserved (INT disabled)

5.2 Sensing Periodical Mode **(INT_MODE[1:0] = [0,0]).**

For sensing periodical mode, the INT_MODE[1:0] should be [0,0].
The data must be ready (including coordinate and raw data) before signal 'INT' rising.

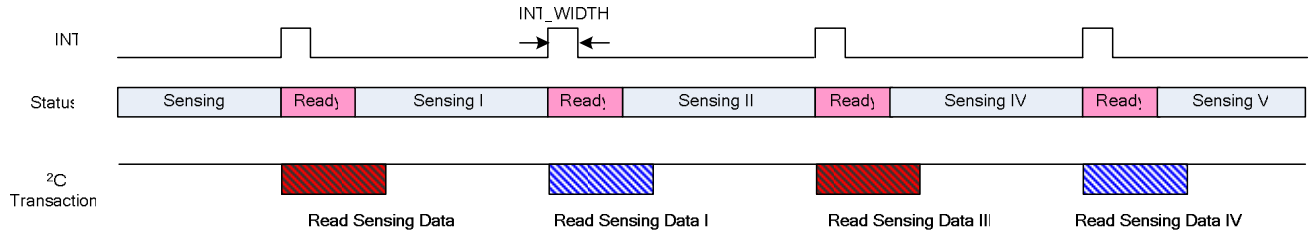


Figure 7: Interruption with INT_R auto-reset

5.3 Coordinate Compare Mode **(INT_MODE[1:0] = [0,1]).**

The INT signal will be asserted while coordinate changes under comparison mode (INT_MODE[1:0] = [0,1]).

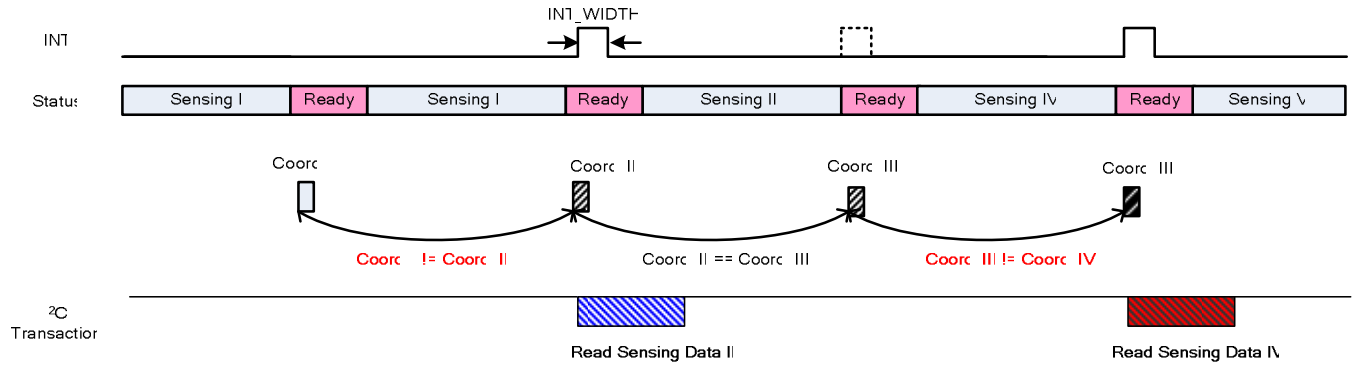


Figure 8: Interruption Flag under Coordinate Compare Mode

5.4 Touch Indicate Mode **(INT_MODE[1:0] = [1,0]).**

The interrupt will assert when the touch is valid. The interrupt should keep high until the touch is released.

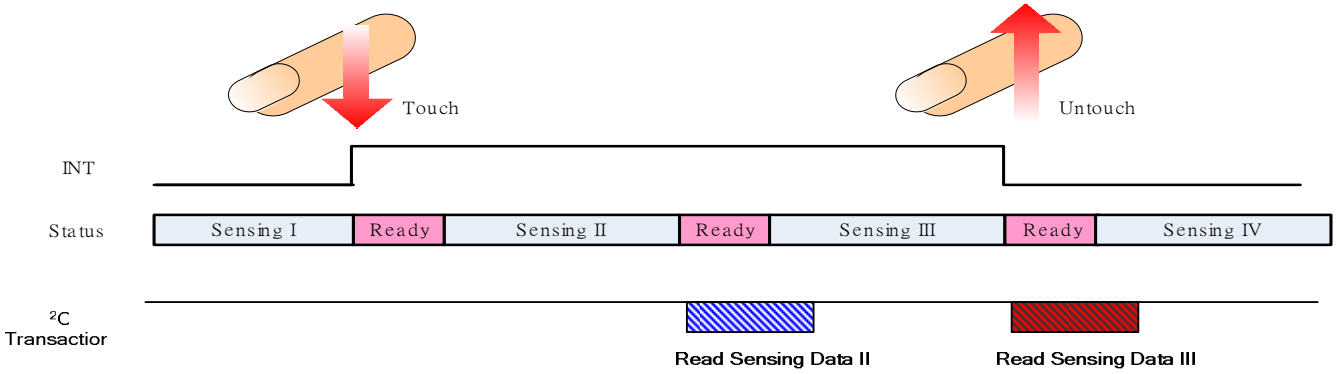
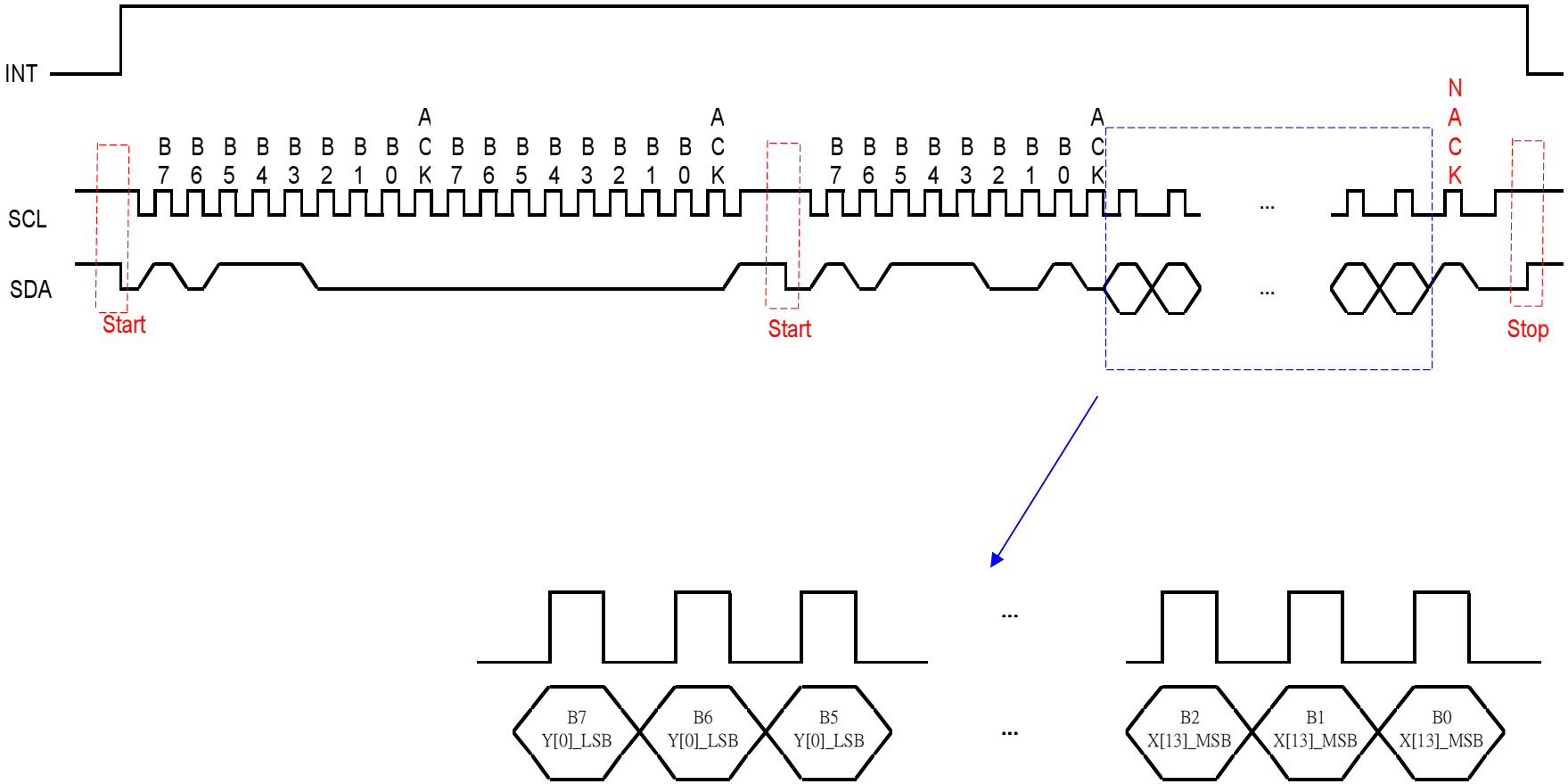


Figure 9: Touch Indicate Mode

Combination interrupt with I2C sequential read raw data operation for as following (for INT_MODE[1:0] = [1,0])



6. Power Mode (Currently, AUO just supports active mode)

Addr.	Addr.(HEX)	Description	R/W	B7	B7	B7	B7	B7	B7	B7	B7
777	77	7ower Mode	R/W	IDLE_7ERIOD[7]	IDLE_7ERIOD[7]	IDLE_7ERIOD[7]	IDLE_7ERIOD[7]	7	ALLOW_LEE7	7OWER_MODE[7]	7OWER_MODE[7]

The capacitive sensor controller support 3 steps of power saving: Active, Sleep, Deep Sleep, the following section describe relative scan rate and power consumption:

Active Mode:

The scan speed will reach 60Hz, this mode makes full-speed sensing and data process to provide best performance. the Power Mode is '0'.

Sleep Mode:

This mode will lower the scan speed down to 10Hz. Active Mode can enter sleep mode automatically or by command. When the system issues a command to change power mode to '1', the scan rate will switch to 10Hz at next scan cycle. When allow_sleep parameter is given, and user don't touch the screen longer than IDLE_PERIOD ms. the controller should also enter sleep mode directly and change the scan rate to 10 Hz immediately.

When user touches the screen in **active region**, the controller should return to Active mode. besides, when system assert a command to change the power mode to '0', the scan rate should also rise to 60Hz

Deep Sleep Mode:

When the chip enter deep sleep mode, all scan circuit should be shutdown to achieve minimum power consumption. When the chip enter deep sleep mode, all the registers are still accessible. The only way to leave/enter deep sleep mode is change the power mode by specific command. The power mode is defined as '2'

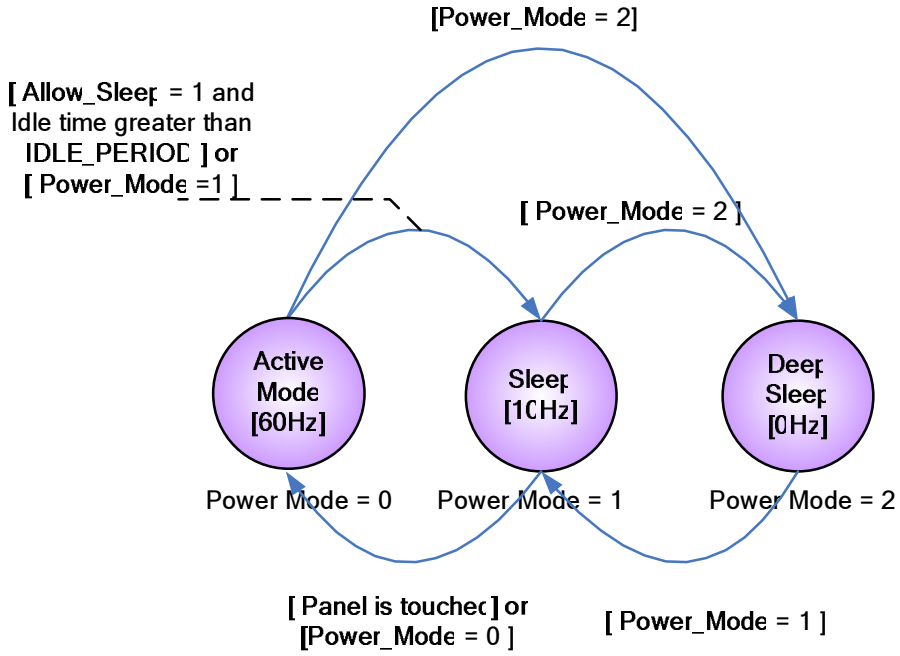
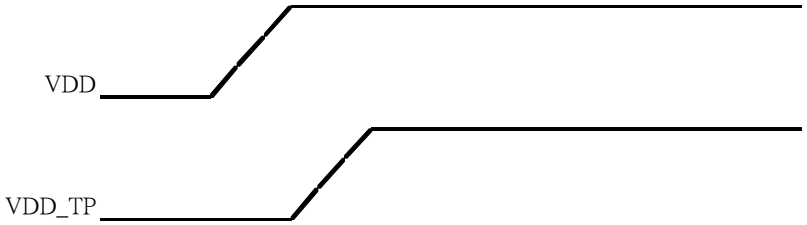


Figure 12. Power Mode Diagram

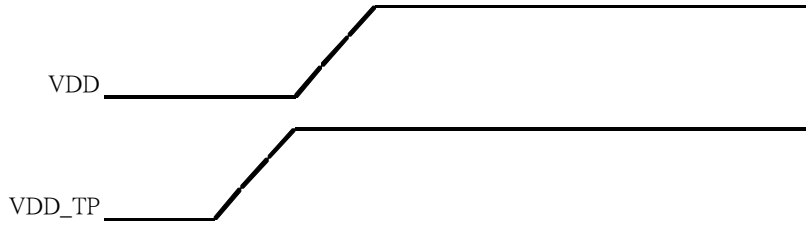
7. Power on/off Sequence (both have two cases)

- Power on Sequence

Case1:

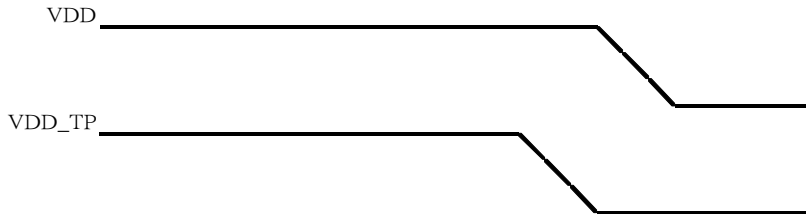


Case2:

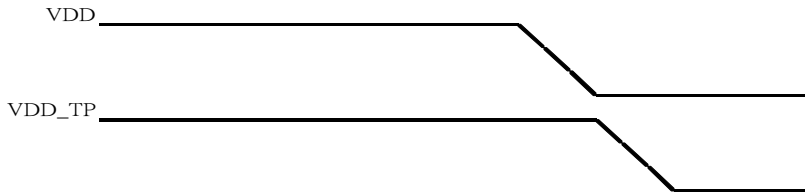


- Power off Sequences

Case1:



Case2:



8. Cover Lens Suggestion

1. Cover lens should be tempered glass, its maximum thickness should be thinner than 1.0mm.
   The suggested thickness is 0.7 mm.
2. The cover lens must use SVR or OCA film to attach to the panel and the thickness of SVR or OCA film will be slightly less than 200 um.

F. Reliability Test Items

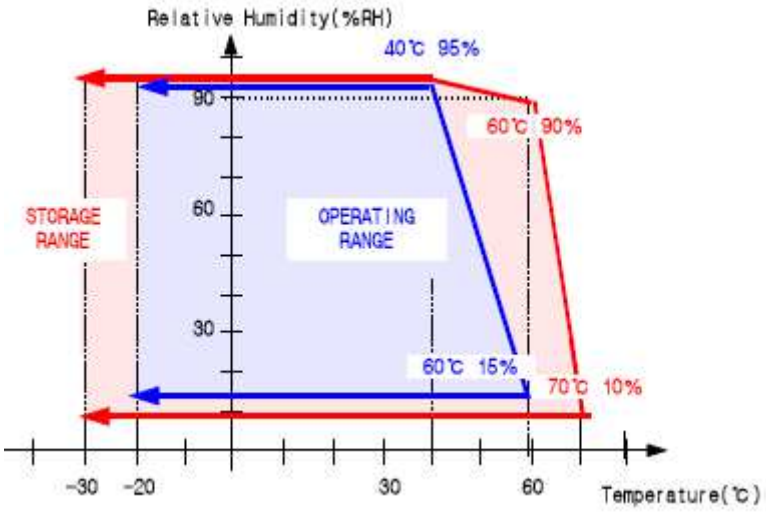
No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 80□ 240Hrs	
2	Low Temperature Storage	Ta= -30□ 240Hrs	
3	High Temperature Operation	Tp= 70□ 240Hrs	
4	Low Temperature Operation	Ta= -20□ 240Hrs	
5	High Temperature & High Humidity	Tp= 60□. 90% RH 240Hrs	Operation
6	Heat Shock	-25□~70□, 50 cycle, 2Hrs/cycle	Non-operation
7	Electrostatic Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B	Note 5
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 2 hours for each direction of X,Y,Z	Non-operation JIS C7021, A-10 condition A : 15 minutes
9	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
10	Vibration (With Carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	
12	Pressure	5kgf, 5sec	Note 6

Note 1: Ta: Ambient Temperature. Tp: Panel Surface Temperature

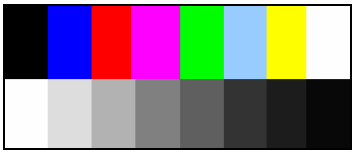
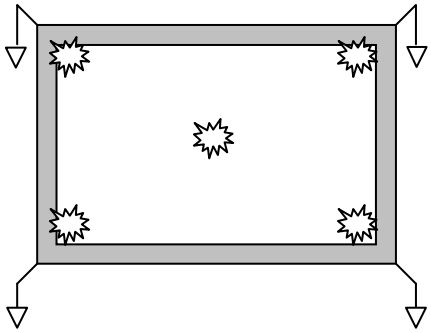
Note 2: In the standard conditions, there should not have display function NG issue occurred.

Note 3: All the cosmetic specification is judged before the reliability stress.

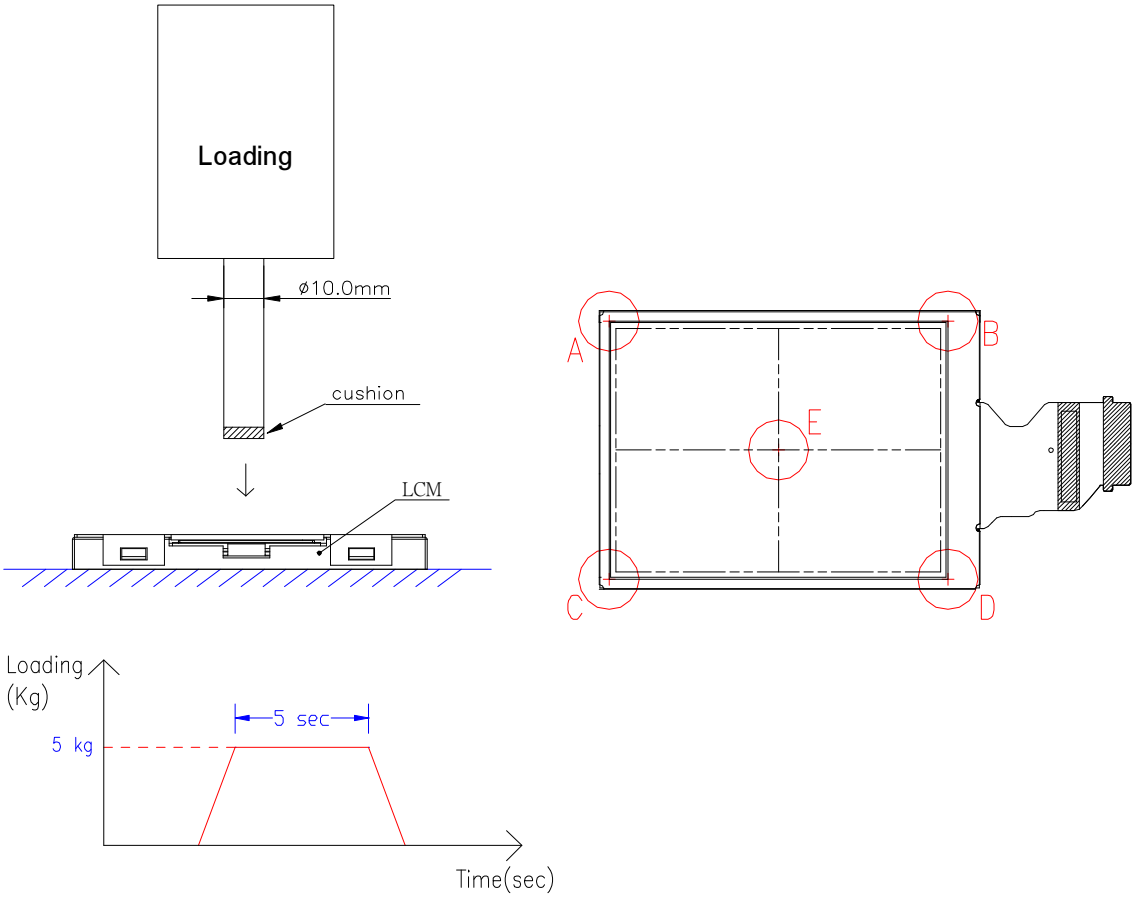
Note 4: Temperature and relative humidity range are shown in the following figure.



Note 5 : All test techniques follow IEC6100-4-2 standard.

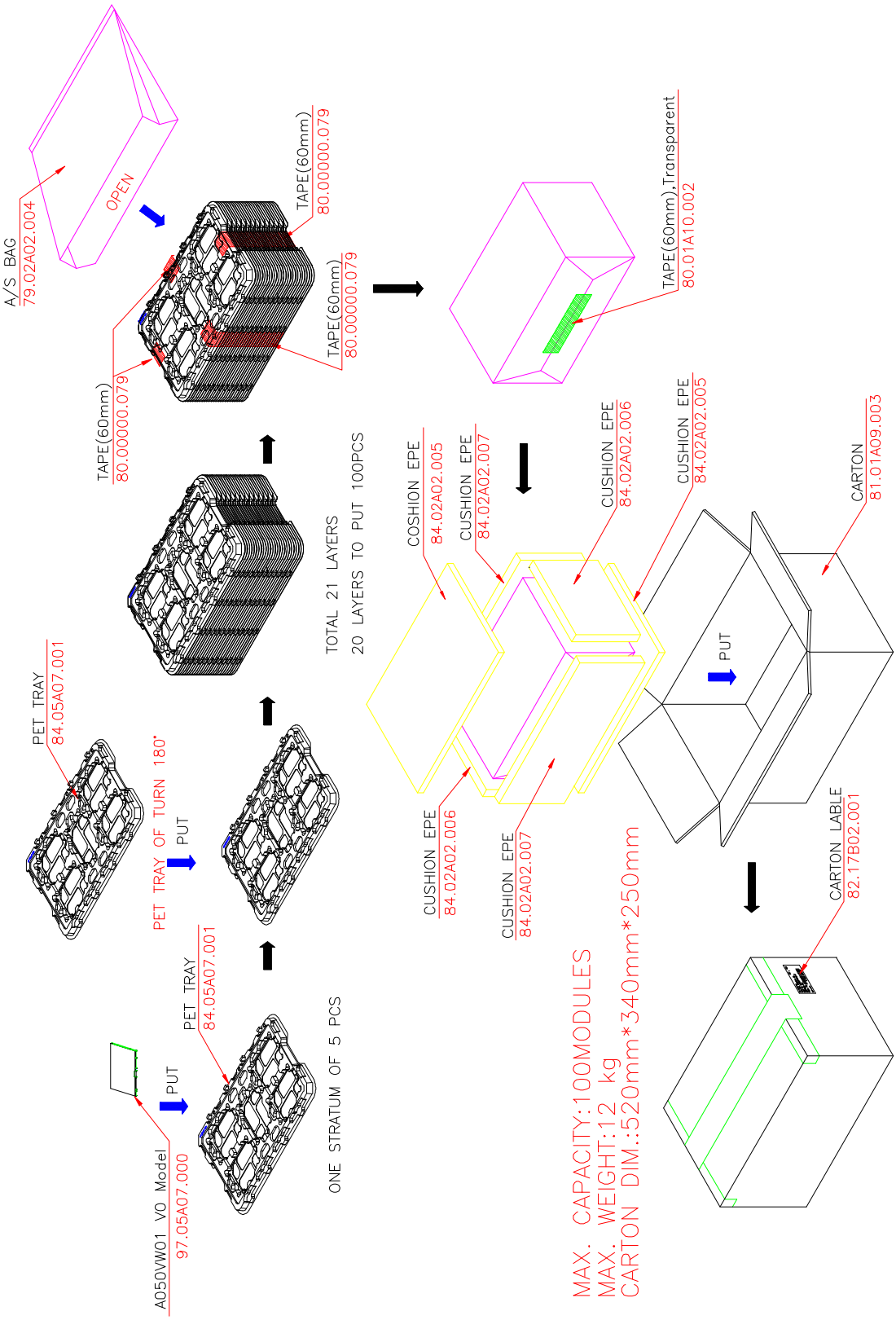
Test Condition		Note
Pattern	 Color Bar + 8 Gray Scale	
Procedure And Set-up	Contact Discharge：330Ω, 150pF, 1sec, 5 points, 10 times/point Air Discharge：330Ω, 150pF, 1sec, 5 points, 10 times/point  Note : 1. The metal casing is connected to ground (0V) at four corners. 2. All register commands are repeating transferred. 3. Judge the result after discharging.	
Criteria	B – Some performance degradation allowed. No data lost. Self-recoverable hardware failure.	

Note 6: The panel is tested as the following figure. The jig isψ10 mm made by Copper with rubber and the loading speed is 3mm/min on position A~E. After the condition, no glass crack will be found and panel function check is OK.(LC mura、LC bubble will not be guaranteed under this test)



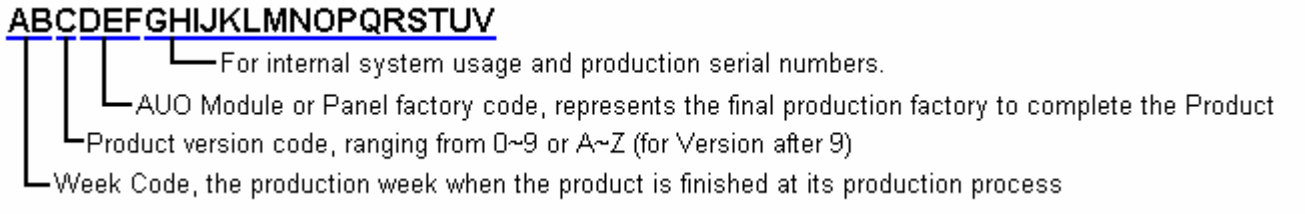
G. Packing and Marking

1. Packing Form



2. Module/Panel Label Information

The module/panel (collectively called as the “Product”) will be attached with a label of Shipping Number which represents the identification of the Product at a specific location. Refer to the Product outline drawing for detailed location and size of the label. The label is composed of a 22-digit serial number with the following definition:



Example:

501M06ZL06123456781Z05:

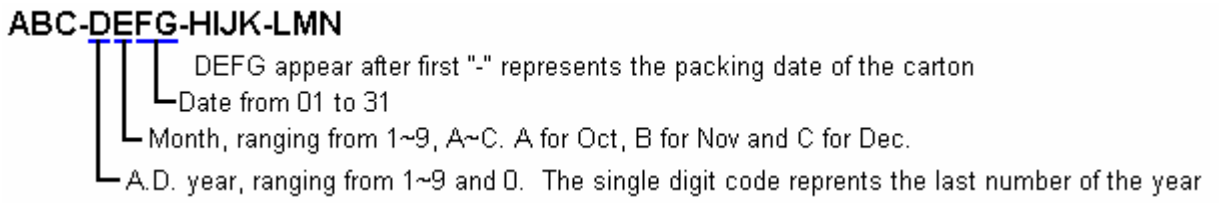
Product Manufacturing Week Code: WK50

Product Version: Version 1

Product Manufactuing Factory: M06

3. Carton Label Information

The packing carton will be attached with a carton label where packing Q’ty, AUO Model Name, AUO Part Number, Customer Part Number (Optional) and a series of Carton Number in 13 or 14 digits are printed. The Carton Number is apparing in the following format:



Refer to the drawing of packing format for the location and size of the carton label.

H. Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with TFT display module.
15. Static electricity will damage the module, please do not touch the module without any grounded device.
16. Do not disassemble and reassemble the module by self.
17. Be careful do not touch the rear side directly.
18. No strong vibration or shock. It will cause module broken.
19. Storage the modules in suitable environment with regular packing.
20. Be careful of injury from a broken display module.
21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.