*Document Version: 4*
*Date: 2005/05/06*

# Product Functional Specification

## 12.1 inch Wide XGA Color TFT LCD Module
## Model Name: A121EW01 V0

( ◆ ) Preliminary Specification
(  ) Final Specification

**Note: This Specification is subject to change without notice.**

# Contents

# II Record of Revision

| Version and Date | Page | Old description | New Description | Remark |
|---|---|---|---|---|
| V1. 2004/07/23 | All | First Release | NA | |
| V2. 2004/09/20 | 17-18 | Physical Size:<br>275.11(W) x 184.39(H) x 8.8(D) | Physical Size<br>276.7(W) x 184.7(H) x 8.8(D) | |
| V2. 2004/09/20 | 5 | Physical Size:<br>275.11(W) x 184.39(H) x 8.8(D) | Physical Size<br>276.7(W) x 184.7(H) x 8.8(D) | |
| V3. 2005/01/24 | 16 | | Revise Reliability Test Conditions | |
| V4. 2005/05/06 | 16 | | Revise Shock and Vibration test condition to meet JIS standard. | |
| | 17 | Lamp wire length: 100mm | Lamp wire length: 110mm | |

# 1.0 Handling Precautions

1) Do not press or scratch the surface harder than a HB pencil lead because the polarizers are very fragile and could be easily damaged.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water droplets or oil immediately. Long contact with the droplets may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Protect the module from static electricity and insure proper grounding when handling. Static electricity may cause damage to the CMOS Gate Array IC.
7) Do not disassemble the module.
8) Do not press the reflector sheet at the back of the module.
9) Avoid damaging the TFT module. Do not press the center of the CCFL Reflector when it was taken out from the packing container. Instead, press at the edge of the CCFL Reflector softly.
10) Do not rotate or tilt the signal interface connector of the TFT module when you insert or remove other connector into the signal interface connector.
11) Do not twist or bend the TFT module when installation of the TFT module into an enclosure (Notebook PC Bezel, for example). It should be taken into consideration that no bending/twisting forces are applied to the TFT module from outside when designing the enclosure. Otherwise the TFT module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local regulations for disposal.
13) The LCD module contains a small amount of material that has no flammability grade, so it should be supplied by power complied with requirements of limited power source (2.11, IEC60950 or UL1950).
14) The CCFL in the LCD module is supplied with Limited Current Circuit (2.4, IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.

# 2.0 General Description

This specification applies to the 12.1 inch wide Color TFT/LCD Module A121EW01 V0

This module is designed for a display unit of Portable Video Devices.

The screen format is intended to support the XGA (1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver).

All input signals are LVDS interface compatible.

This module does not contain an inverter card for backlight.

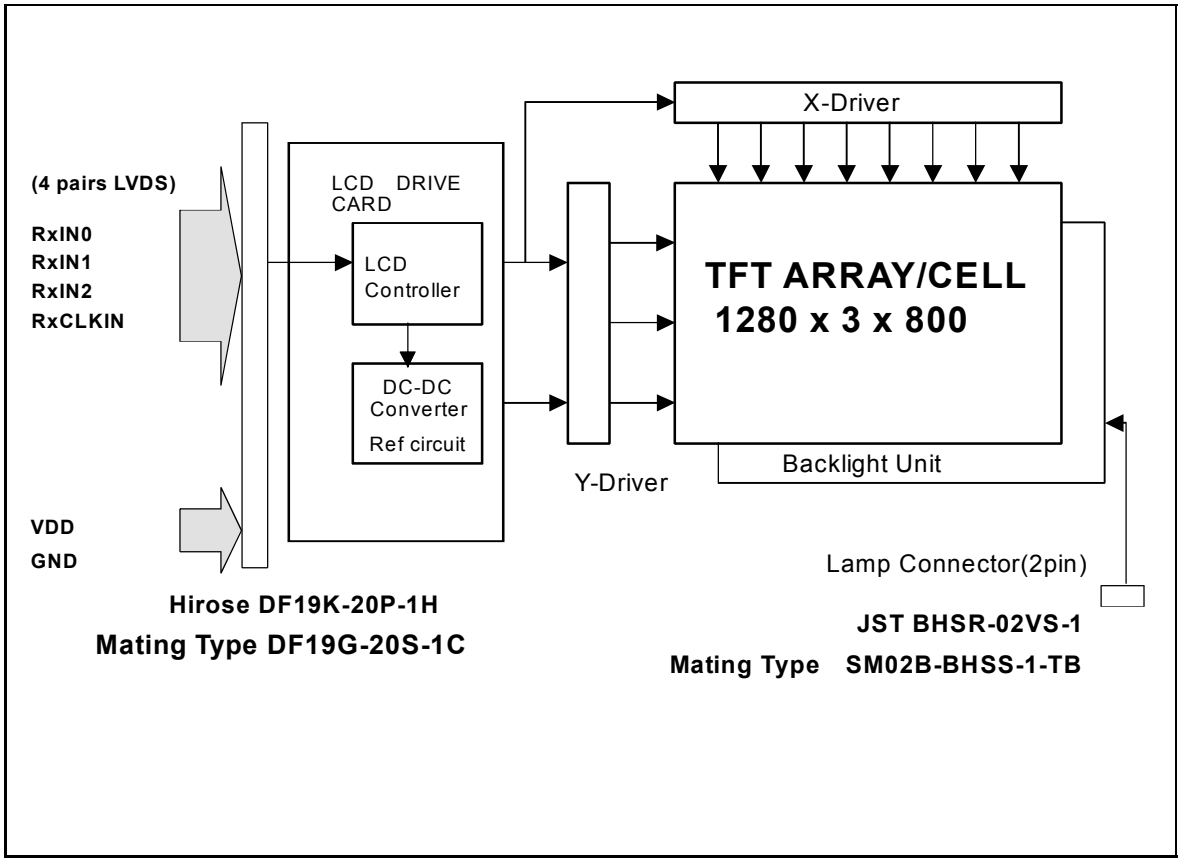
## 2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

| ITEMS | Unit | SPECIFICATIONS |
|---|---|---|
| Screen Diagonal | [mm] | 307.9(12.1" wide) |
| Active Area | [mm] | 261.12(H) x163.2 (V) |
| Pixels H x V | | 1280(x3) x 800 |
| Pixel Pitch | [mm] | 0.204 x 0.204 |
| Pixel Arrangement | | R.G.B. Vertical Stripe |
| Display Mode | | Normally White |
| Typical White Luminance(CCFL=6.0mA) | [cd/m$^2$] | 450 Typ. |
| Contrast Ratio | | 350:1 |
| Response Time | [msec] | 25 Typ. |
| Nominal Input Voltage VDD | [Volt] | +3.3 Typ. |
| Weight | [Grams] | 557g typ. |
| Physical Size | [mm] | 276.7(W) x 184.7(H) x 8.8(D) Max. |
| Electrical Interface | | LVDS |
| Color Depth | | 262K colors |
| Temperature Range<br>Operating<br>Storage (Shipping) | <br>[$^o$C]<br>[$^o$C] | <br>0 to +60<br>-20 to +60 |

## 2.2 Functional Block Diagram

The following diagram shows the functional block of the 12.1 inches Color TFT/LCD Module:



# 3.0 Absolute Maximum Ratings

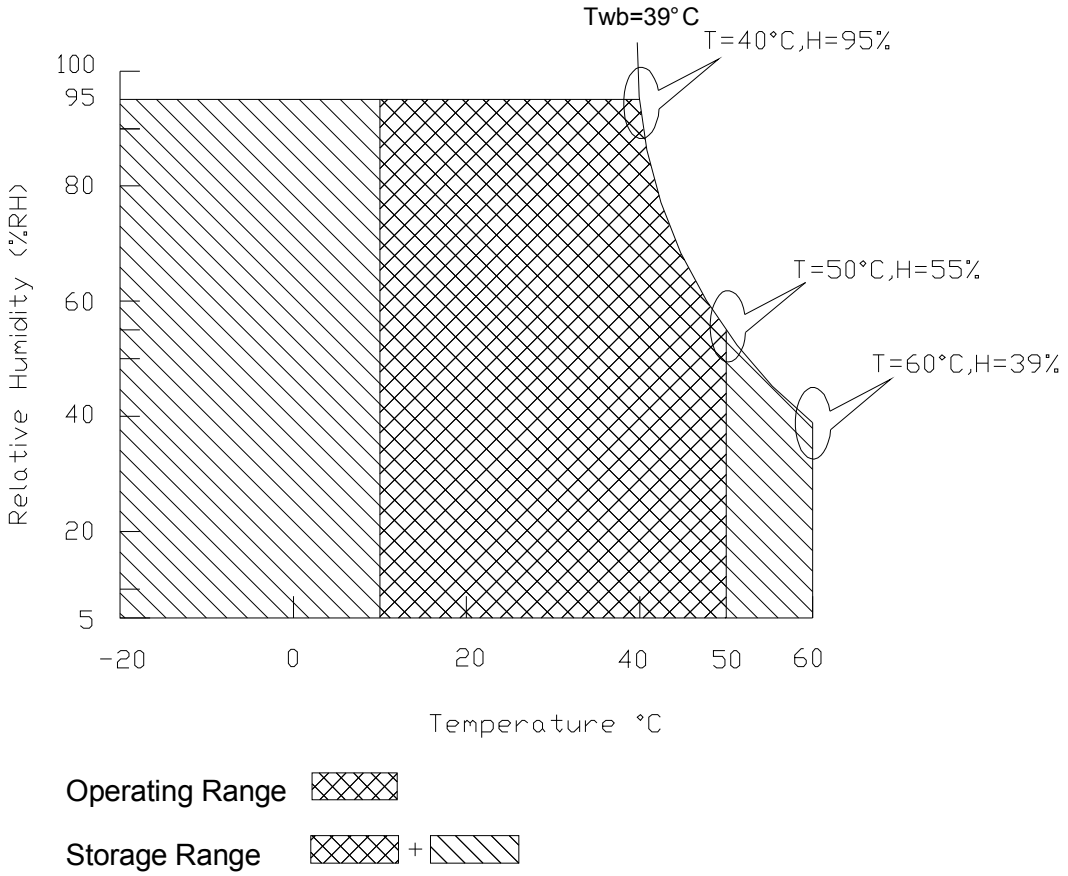
Absolute maximum ratings of the module is as following:

| Item | Symbol | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| Logic/LCD Drive Voltage | VDD | -0.3 | +4.0 | [Volt] | |
| Input Voltage of Signal | Vin | -0.3 | VDD+0.3 | [Volt] | |
| CCFL Current | ICFL | - | 7 | [mA] rms | |
| CCFL Ignition Voltage | Vs | - | TBD(25°C) | Vrms | Note 1 |
| Operating Temperature | TOP | 0 | +60 | [°C] | Note 2 |
| Operating Humidity | HOP | 5 | 90 | [%RH] | Note 2 |
| Storage Temperature | TST | -20 | +60 | [°C] | |
| Storage Humidity | HST | 5 | 90 | [%RH] | Note 2 |
| Vibration | | | 1.5, 10-500 | [G Hz] | |
| Shock | | | 200, 3 | [G ms] | Half sine wave |

Note 1 : Duration = 3sec

Note 2 : Maximum Wet-Bulb should be 39℃ and No condensation.

### Wet bulb temperature chart



# 4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25℃ condition:

| Item | Unit | Conditions | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| Viewing Angle | [degree] | Horizontal (Right) | 50 | 65 | - |
| | [degree] | CR = 10 (Left) | 50 | 65 | - |
| CR: Contrast Ratio | [degree] | Vertical (Upper) | 40 | 50 | - |
| | [degree] | CR = 10 (Lower) | 50 | 65 | - |
| Contrast ratio | | | 300 | 350 | - |
| Response Time | [msec] | Rising | - | 10 | 15 |
| | [msec] | Falling | - | 15 | 20 |
| Color / Chromaticity Coordinates (CIE) | | White x | 0.26 | 0.31 | 0.36 |
| | | White y | 0.28 | 0.33 | 0.38 |
| White Luminance CCFL @ 6.0mA | [cd/m$^2$] | Central | 380 | 450 | - |

# 5.0 Signal Interface

## 5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

| | |
|---|---|
| **Connector Name / Designation** | For Signal Connector |
| **Manufacturer** | Hirose |
| **Type / Part Number** | DF19K-20P-1H |
| **Mating Housing/Part Number** | DF19G-20S-1C |
| **Mating Contact/Part Number** | DF19-2830 SCFA |

| | |
|---|---|
| **Connector Name / Designation** | For Lamp Connector |
| **Manufacturer** | JST |
| **Type / Part Number** | BHSR-02VS-1 |
| **Mating Type / Part Number** | SM02B-BHSS-1-TB |

## 5.2 Signal Pin

| Pin# | Signal Name | Pin# | Signal Name |
|---|---|---|---|
| 1 | VDD | 2 | VDD |
| 3 | GND | 4 | GND |
| 5 | RxIN0- | 6 | RxIN0+ |
| 7 | GND | 8 | RxIN1- |
| 9 | RxIN1+ | 10 | GND |
| 11 | RxIN2- | 12 | RxIN2+ |
| 13 | GND | 14 | RxCLKIN- |
| 15 | RxCLKIN+ | 16 | GND |
| 17 | $V_{EDID}$ | 18 | NC |
| 19 | $CLK_{EDID}$ | 20 | $DATA_{EDID}$ |

## 5.3 Signal Description

The module uses a LVDS receiver embedded in AUO's ASIC. LVDS is a differential signal technology for LCD interface and high-speed data transfer device.

| Signal Name | Description |
|---|---|
| RxIN0-, RxIN0+ | LVDS differential data input(Red0-Red5, Green0) |
| RxIN1-, RxIN1+ | LVDS differential data input(Green1-Green5, Blue0-Blue1) |
| RxIN2-, RxIN2+ | LVDS differential data input(Blue2-Blue5, Hsync, Vsync, DSPTMG) |
| RxCLKIN-, RxCLKIN0+ | LVDS differential clock input |
| VDD | +3.3V Power Supply |
| GND | Ground |

**Note**: Input signals shall be in low status when VDD is off.

Internal circuit of LVDS inputs are as following.

| Signal Name | Description | |
|---|---|---|
| +RED5<br>+RED4<br>+RED3<br>+RED2<br>+RED1<br>+RED0 | Red Data 5 (MSB)<br>Red Data 4<br>Red Data 3<br>Red Data 2<br>Red Data 1<br>Red Data 0 (LSB)<br>**Red-pixel Data** | Red-pixel Data<br>Each red pixel's brightness data consists of these 6 bits pixel data. |
| +GREEN 5<br>+GREEN 4<br>+GREEN 3<br>+GREEN 2<br>+GREEN 1<br>+GREEN 0 | Green Data 5 (MSB)<br>Green Data 4<br>Green Data 3<br>Green Data 2<br>Green Data 1<br>Green Data 0 (LSB)<br>**Green-pixel Data** | Green-pixel Data<br>Each green pixel's brightness data consists of these 6 bits pixel data. |
| +BLUE 5<br>+BLUE 4<br>+BLUE 3<br>+BLUE 2<br>+BLUE 1<br>+BLUE 0 | Blue Data 5 (MSB)<br>Blue Data 4<br>Blue Data 3<br>Blue Data 2<br>Blue Data 1<br>Blue Data 0 (LSB)<br>**Blue-pixel Data** | Blue-pixel Data<br>Each blue pixel's brightness data consists of these 6 bits pixel data. |
| -DTCLK | **Data Clock** | The typical frequency is 65.0 MHz. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high. |
| DSPTMG | **Display Timing** | This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed. |
| VSYNC | **Vertical Sync** | The signal is synchronized to -DTCLK . |
| HSYNC | **Horizontal Sync** | The signal is synchronized to -DTCLK . |

**Note:** Output signals from any system shall be low or Hi-Z state when VDD is off.

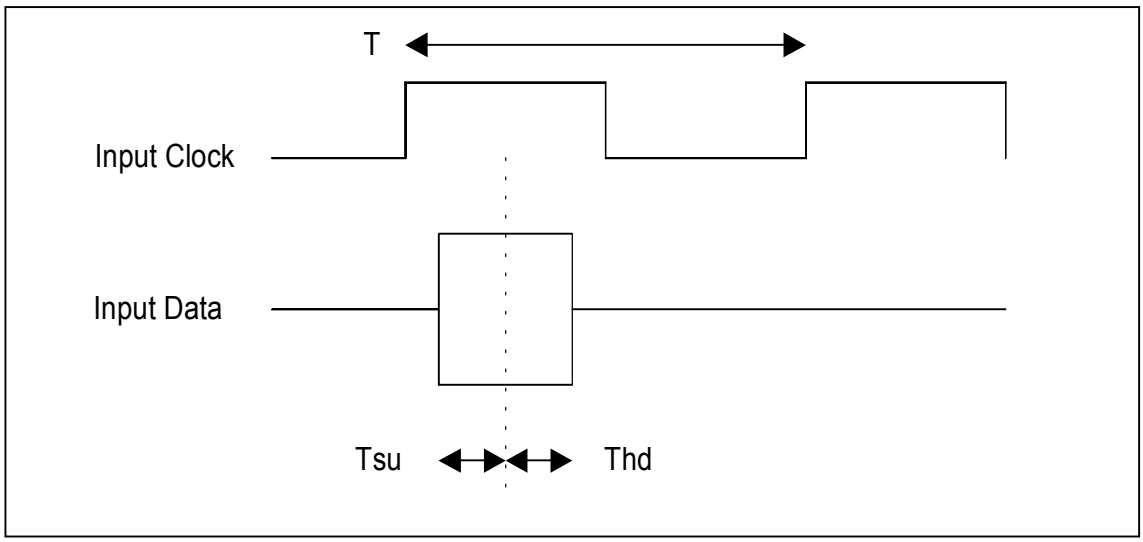
## 5.4 Signal Electrical Characteristics

Input signals shall be in low status when VDD is off.
It is recommended to refer the specifications of SN75LVDS86DGG (Texas Instruments) in detail.
Signal electrical characteristics are as follows;

| Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|
| Vth | Differential Input High Voltage(Vcm=+1.2V) | | 100 | [mV] |
| Vtl | Differential Input Low Voltage(Vcm=+1.2V) | -100 | | [mV] |

LVDS Macro AC characteristics are as follows:

| | Min. | Max. |
|---|---|---|
| Clock Frequency (F) | 20MHz | 85MHz |
| Data Setup Time (Tsu) | 600ps | |
| Data Hold Time (Thd) | 600ps | |

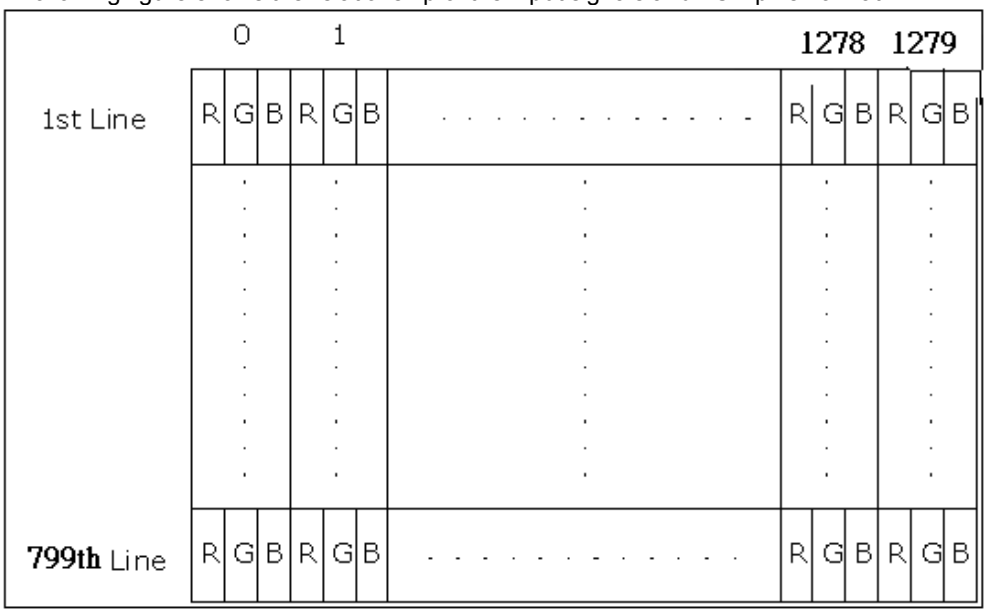



## 5.5 Signal for Lamp connector

| Pin # | Signal Name |
|---|---|
| 1 | Lamp High Voltage |
| 2 | Lamp Low Voltage |

# 6.0 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.




# 7.0 Parameter guide line for CCFL Inverter

| Parameter | Min | DP-1 | Max | Units | Condition |
|---|---|---|---|---|---|
| CCFL current(ICFL) | | 6.0 | 7.0 | [mA] rms | (Ta=25℃) **Note 2** |
| CCFL Frequency(FCFL) | 50 | | 70 | [KHz] | (Ta=25℃) **Note 3** |
| CCFL Ignition Voltage(Vs) | 1,400 | — | — | [Volt] rms | (Ta= 0℃) **Note 4** |
| CCFL Voltage (Reference) (VCFL) | — | 700 | — | [Volt] rms | (Ta=25℃) **Note 5** |
| Single CCFL Power consumption (PCFL) | — | 4.2 | — | [Watt] | (Ta=25℃) **Note 5** |

**Note 1**: DP-1 are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit ver carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CCFL is damaged.

*4 Generally, CCFL has some amount of delay time after applying start-up voltage. It is recommended to keep on applying start-up voltage for 1 [Sec] until discharge.

*5 The CCFL inverter operating frequency must be carefully chosen so that no interfering noise stripes on the screen were induced.

*6 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

**Note 2**: It should be employed the inverter, which has “Duty Dimming”, if ICCFL is less than 4mA.

**Note 3**: The CCFL inverter operating frequency should be carefully determined to avoid interference between inverter and TFT LCD.

**Note 4:** The inverter open voltage should be designed larger than the lamp starting voltage at T=0$^{o}$C, otherwise backlight may be blinking for a moment after turning on or not be able to turn on. The open voltage should be measured after ballast capacitor. If an inverter has shutdown function it should keep its open voltage. for longer than 1 second even if lamp connector is open.

**Note 5**: Calculator value for reference (ICFL×VCFL=PCFL)

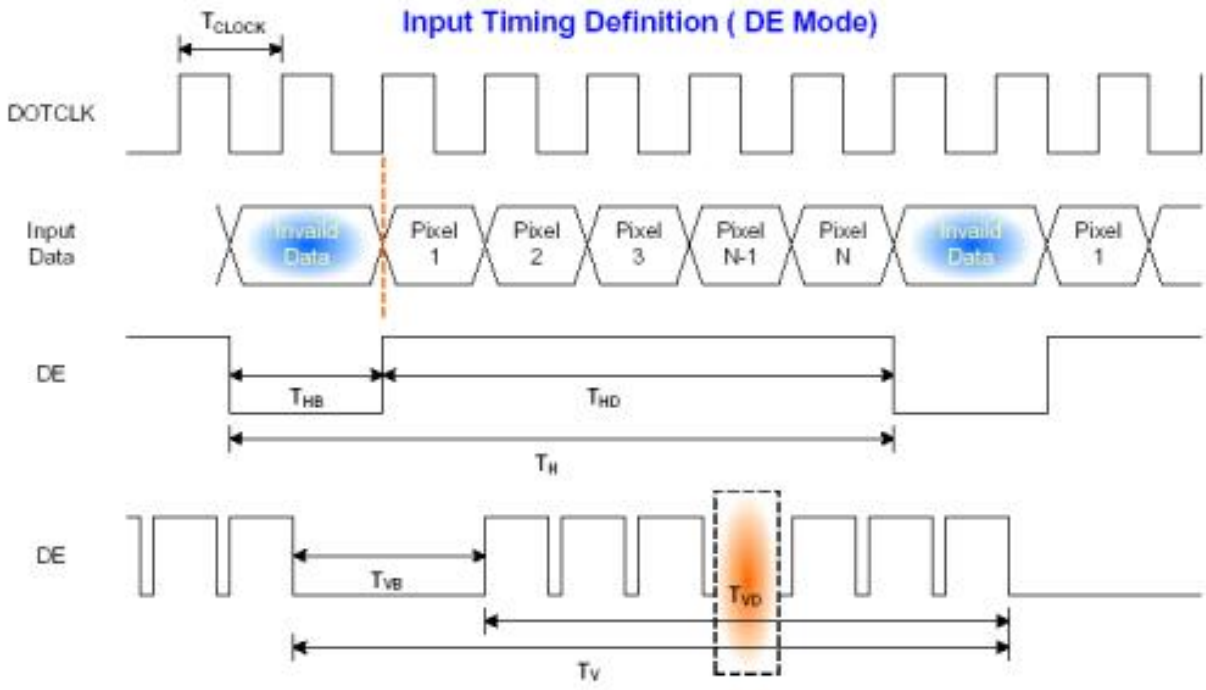
# 8.0 Timing Control

## 8.1 Timing Characteristics

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications.

| Parameter | | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|---|
| Clock frequency | | 1/ $T_{Clock}$ | 50 | 68.9 | 85 | MHz | |
| Vertical Section | Period | $T_V$ | 803 | 816 | 832 | $T_{Line}$ | |
| | Active | $T_{VD}$ | 800 | 800 | 800 | | |
| | Blanking | $T_{VB}$ | 3 | 16 | 32 | | |
| Horizontal Section | Period | $T_H$ | 1302 | 1408 | 1700 | $T_{Clock}$ | |
| | Active | $T_{HD}$ | 1280 | 1280 | 1280 | | |
| | Blanking | $T_{HB}$ | 22 | 128 | 420 | | |
| End-frame checking period | | tEF | | 2 | | $T_{Line}$ | |
| DE checking period | | tDE | | 6400 | | $T_{Line}$ | 8 Frames |

## 8.2 Timing Definition



# 9.0 Power Consumption

Input power specifications are as follows;

| Symbol | Parameter | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|---|
| **Module** | | | | | | |
| VDD | Logic/LCD Drive Voltage | 3.0 | 3.3 | 3.6 | [Volt] | Load Capacitance 20uF |
| PDD | VDD Power | | 1.6 | | [Watt] | All Black Pattern |
| PDD Max | VDD Power max | | | 1.7 | [Watt] | Max Pattern **(Note 1)** |
| IDD | IDD Current | | 400 | | mA | 64 Grayscale Pattern |
| IDD Max | IDD Current max | | | 420 | mA | Vertical stripe line Pattern **(Note 1)** |
| VDDrp | Allowable Logic/LCD Drive Ripple Voltage | | | 500 | [mV] p-p | |
| VDDns | Allowable Logic/LCD Drive Ripple Noise | | | 100 | [mV] p-p | |
| **Lamp (Single Lamp Features)** | | | | | | **(Note 2)** |
| ICFL | CCFL current | 4.0 | 6.0 | 7.0 | [mA] rms | (Ta=25℃) |
| VCFL | CCFL Voltage (Reference) | — | TBD | — | [Volt] rms | (Ta=25℃) |
| VSCFL | CCFL Starting Voltage (Reference) | TBD | — | — | [Volt] rms | (Ta=25℃) |
| PCFL | CCFL Power consumption | — | TBD | — | [Watt] | (Ta=25℃) |

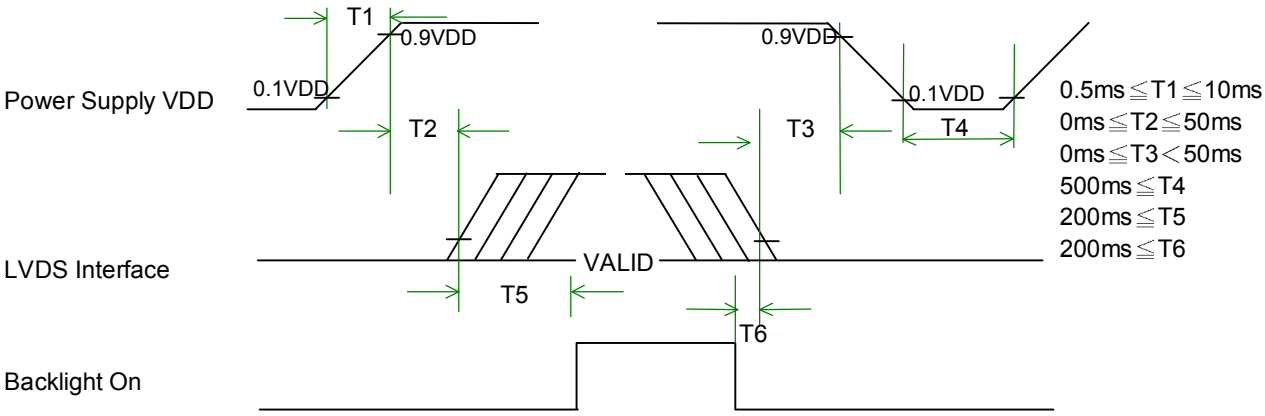
**Note 1: VDD=3.3V**

**Note 2: A121EW01 V0 Module includes dual lamps**

# 10. Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.

Sequence of Power-on/off and signal-on/off




Apply the lamp voltage within the LCD operating range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal.

# 11.0 Reliability /Safety Requirement

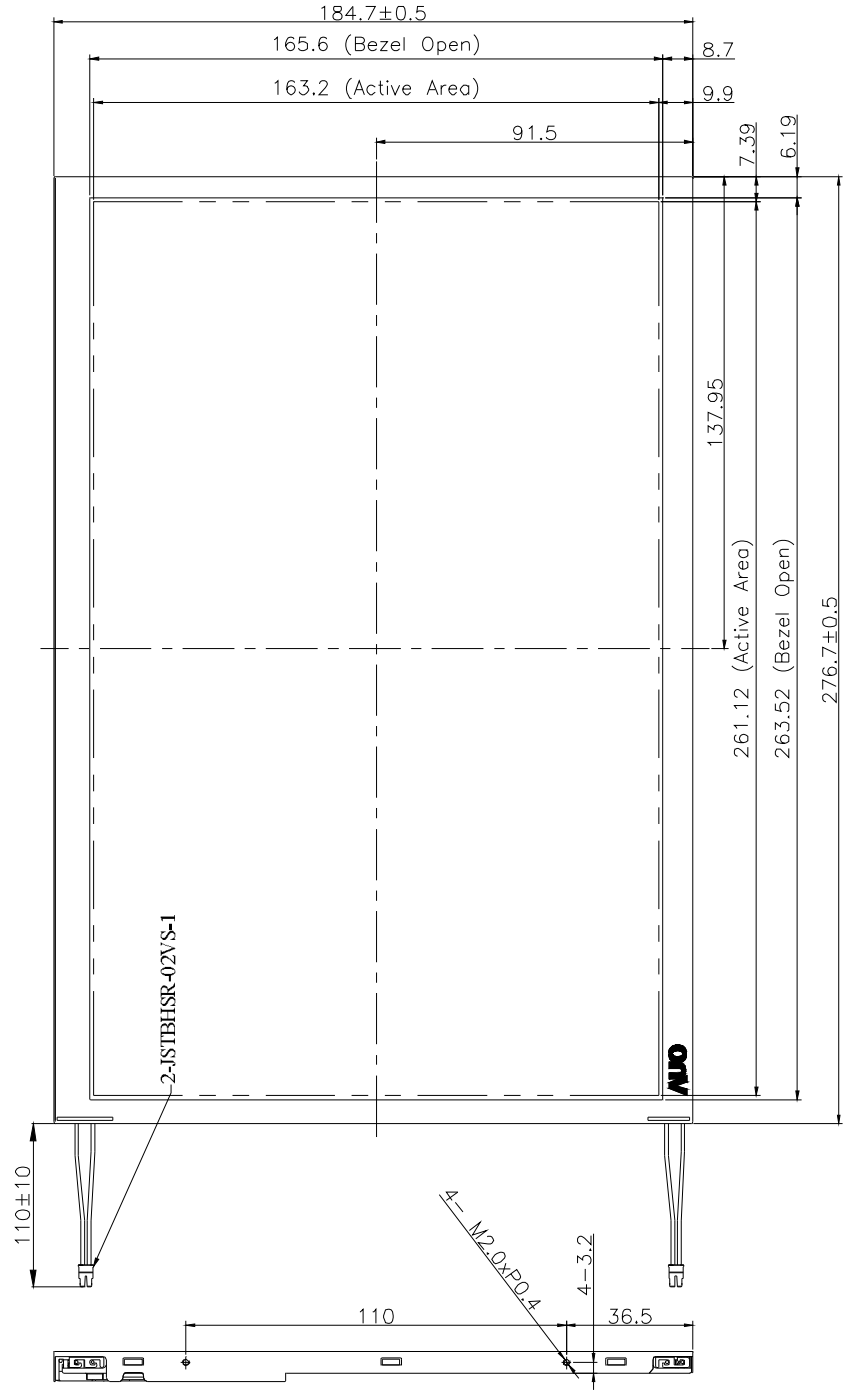
## Reliability Test Conditions

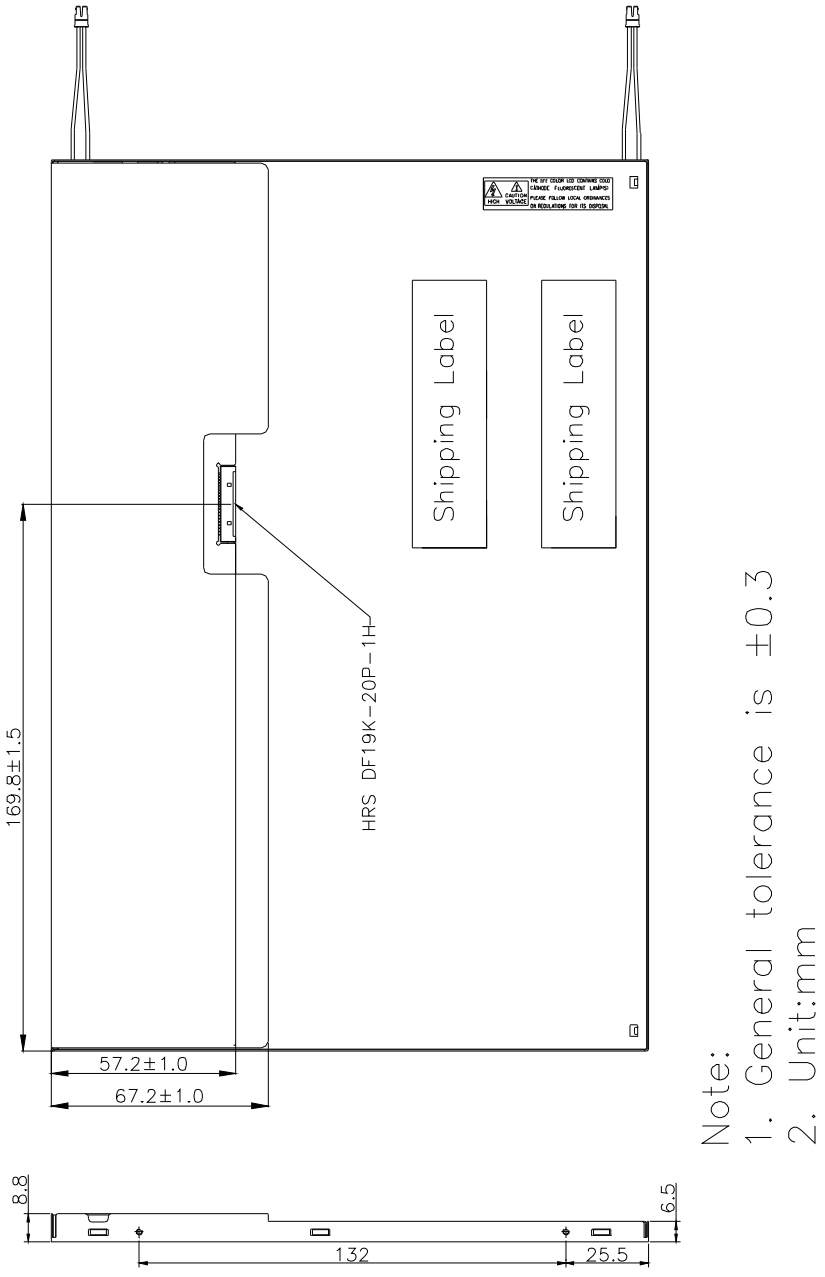
| No. | Test items | Conditions | Remark |
|---|---|---|---|
| 1 | High temperature storage | Ta= 60℃ 240Hrs | |
| 2 | Low temperature storage | Ta= 0℃ 240Hrs | |
| 3 | High temperature operation | Tp= 60℃ 240Hrs | |
| 4 | Low temperature operation | Ta= -20℃ 240Hrs | |
| 5 | High temperature and high humidity | Tp= 50℃, 80% RH 240Hrs | Operation |
| 6 | Thermal shock | -20°C to +60°C, Ramp ≤20°C/min, Duration at Temp. = 30min, Test Cycles = 50 | Non-operation |
| 7 | Vibration | Frequency range : 8~33.3Hz<br>Stoke : 1.3mm<br>Sweep : 2.9G, 33.3 ~<br>Cycle : 15 minutes<br>2 hours for each direction of X,Z<br>4 hours for Y direction | JIS D1601, A-10 Condition A |
| 8 | Mechanical shock | 100G, 6ms, ±X,±Y,±Z<br>3 times for each direction | JIS C0041, A-7 Condition C |
| 9 | Vibration (with carton) | Random vibration:<br>$0.015G^2$/Hz from 5~200Hz<br>–6dB/octave from 200~500Hz | IEC 68-34 |
| 10 | Drop (with carton) | Height: 60cm<br>1 corner, 3 edges, 6 surfaces | JIS Z0202 |

Note1: Ta: Ambient temperature.
Note2: Tp: Panel Surface Temperature
Note3: All the cosmetic specification is judged before the reliability stress.

**CCFL Life Time:** 10,000 hours minimum
The" CCFL Life Time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃, $I_L$=6mA.

# 12. Outline drawing






Note:
1. General tolerance is ±0.3
2. Unit:mm