Product Functional Specification

13.3 inch XGA Color TFT/LCD Module
Model Name:L133X1
B133XN01

( ) Preliminary Specification
(◆) Final Specification

Note: This Specification is subject to change without notice.

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1.0 Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CFL Reflector edge.
Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

2.0 General Description

This specification applies to the 13.3 inch Color TFT/LCD Module L133X1.

This module is designed for a display unit of notebook style personal computer.

The screen format is intended to support the XGA (1024(H) x 768(V)) screen and 262,144 colors (RGB 6-bit data driver).

All input signals are LVDS interface compatible.

This module does not contain a inverter card for backlight.

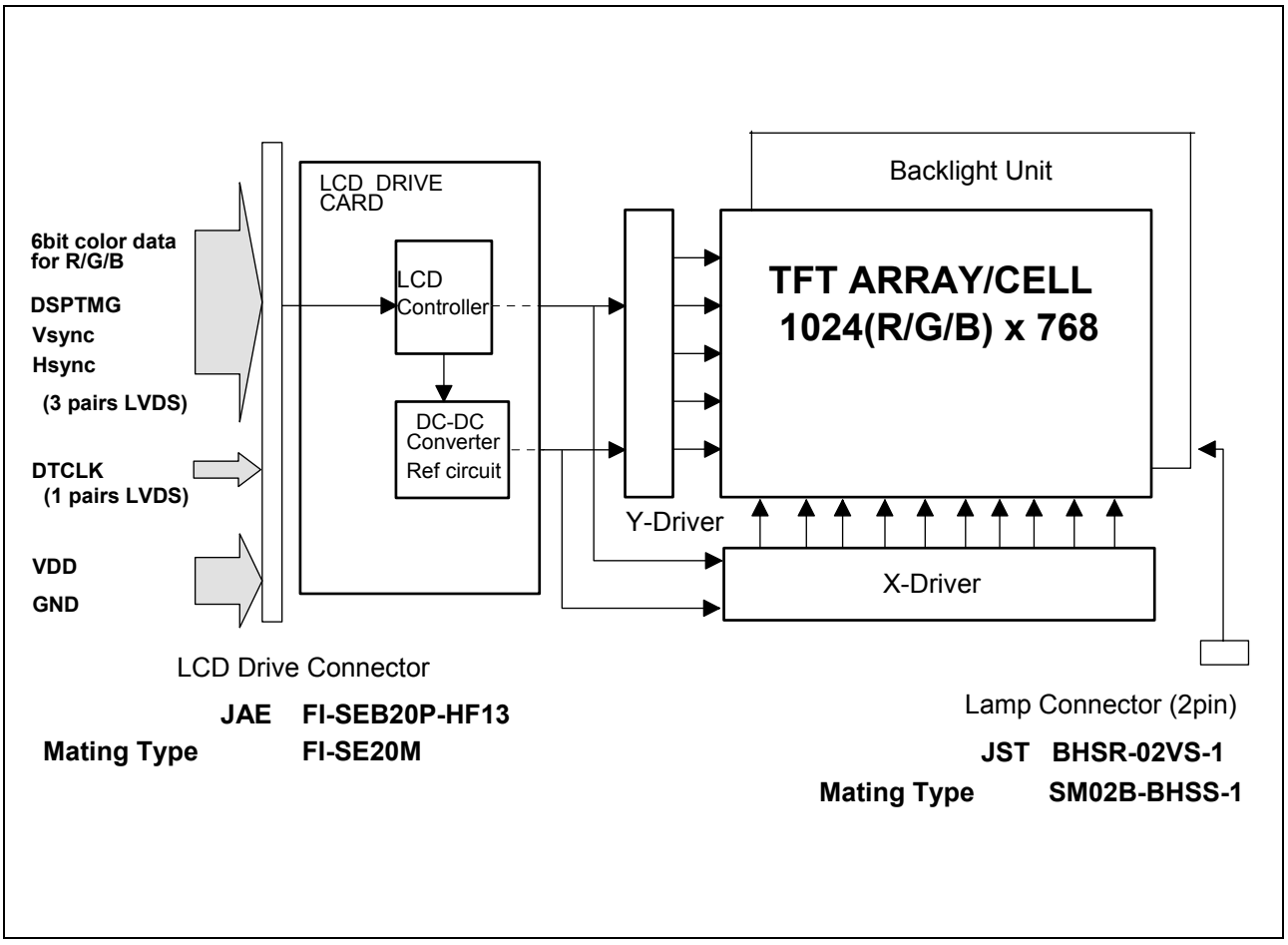
2.1 Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

ITEMS	SPECIFICATIONS
Screen Diagonal [mm]	33.8(13.3")
Active Area [mm]	270.336(H) x 202.752(V)
Pixels H x V	1024(x3) x 768
Pixel Pitch [mm]	0.264(per one triad) x 0.264
Pixel Arrangement	R.G.B. Vertical Stripe
Display Mode	Normally White
Nominal Input Voltage [Volt] VDD	 +3.3 V
Typical Power Consumption [watt] (VDD line + VCFL line)	 4.0(w/o Inverter, All Black Pattern)
Weight [grams]	515 Typ.
Physical Size [mm]	292(W) x 215(H) x 6.5(D) typ., 6.8(D) max.
Electrical Interface	R/G/B Data, 3 Sync, Signals,Clock (4 pairs LVDS)
Support Color	Native 262,144 colors (RGB 6-bit data driver)
Temperature Range (℃) Operating Storage (Shipping)	 0 to +50 -20 to +60

2.2 Functional Block Diagram

The following diagram shows the functional block of the 13.3 inches Color TFT/LCD Module:



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	+4.75	+5.25	V	
CFL Inrush current	ICFLL	-	20	mA	Note 2
CFL Current	ICFL	3.0	6.8	mArms	
Operating Temperature	TOP	0	+50	℃	Note 1
Operating Humidity	HOP	8	95	%RH	Note 1
Storage Temperature	TST	-20	+60	℃	Note 1
Storage Humidity	HST	8	95	%RH	Note 1
Vibration(MAX)			1.5 / 10-200	G/ Hz	
Shock(MAX)			50 / 18	G/ ms	

Note 1 : Maximum Wet-Bulb should be 39℃ and No condensation.

Note 2 : Duration=50 msec.

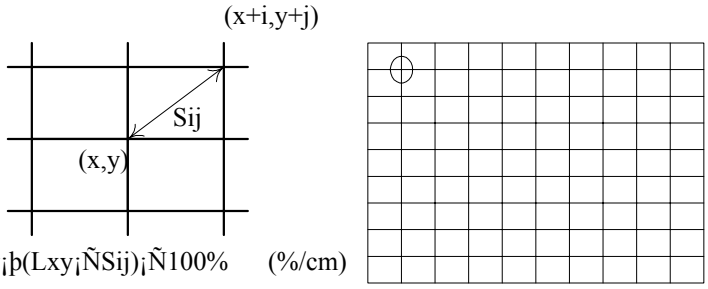
4.0 Optical Characteristics (for Reference)

The optical characteristics are measured under stable conditions as follows under 25℃ condition:

Item	Conditions		Min.	Typ.	Max.
Viewing Angle	Horizontal	(Right)	40		
(Degrees)	K ε 10	(Left)	40		
	Vertical	(Upper)	10	20	
K:Contrast Ratio	K ε 10	(Lower)	20	35	
Contrast ratio			100	150	
Response Time	Rising			30	50
(ms)	Falling			30	50
Color	Red	x	0.537	0.577	0.617
Chromaticity	Red	y	0.308	0.338	0.368
(CIE)	Green	x	0.280	0.310	0.340
	Green	y	0.533	0.563	0.593
	Blue	x	0.128	0.158	0.188
	Blue	y	0.117	0.157	0.197
	White	x	0.282	0.310	0.338
	White	y	0.326	0.346	0.366
White Luminance (cd/㎡) CFL 6mA			120		
Luminance (*Note)	L ALL		60%		
Uniformity	L ADJ				15%

*Note :

Divide both the horizontal and vertical lengths of the active area into 10 equivalent units and measure the luminance of 81 cross points to evaluate the luminance ratios of adjustment points and all points of screen after the test sample being warmed up for 20 mins.



¡ýLxy-Lij¡ý¡þ(Lxy¡ÑSij)¡Ñ100% (%/cm)

L ALL = L MIN / L MAX , where L MIN is the minimum luminance of all screen 81 points and L MAX is the maximum luminance of all screen 81 points

L ADJ = ｜Lxy-Lij｜／(Lxy×Sij)×100%, where Lxy is the luminance at point (x,y), Lij is the

luminance at point (x+i, y+j), Sij is the distance between point (x,y) and (x+i, y+j).

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	FI-SEB20P-HF13

Mating Housing/Part Number	FI-SE20M

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1

5.2 Signal Pin

Pin#	Signal Name	Pin#	Signal Name
1	VDD	2	VDD
3	Return/GND	4	Rerturn/GND
5	Reserved	6	Reserved
7	LVDS GND	8	Rxin0-
9	Rxin0+	10	LVDS GND
11	Rxin1-	12	Rxin1+
13	LVDS GND	14	Rxin2-
15	Rxin2+	16	LVDS GND
17	Rxclk-	18	Rxclk+
19	LVDS GND	20	Reserved
Shell	Frame GND		

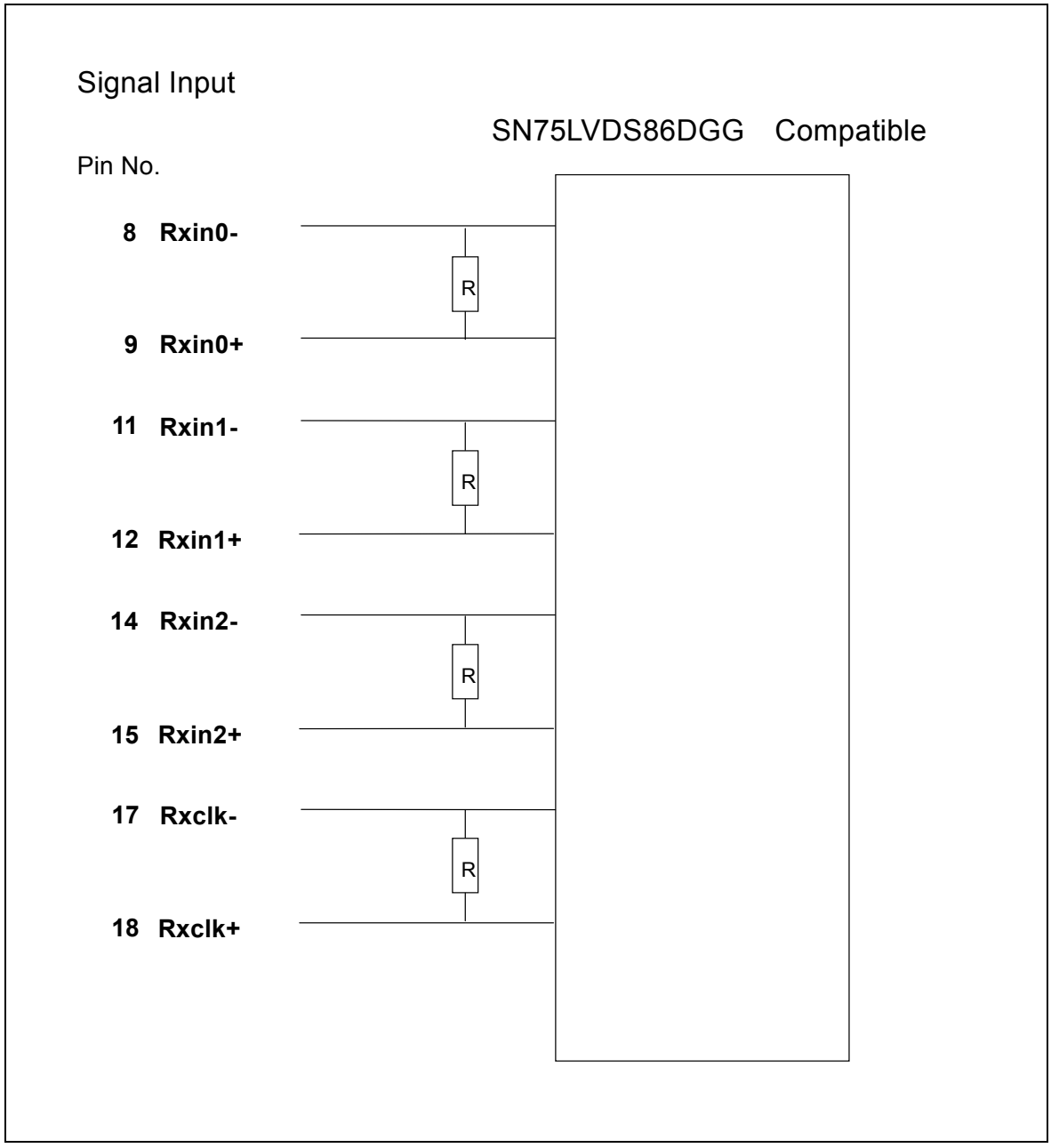
5.3 Signal Description

The module using a LVDS receiver SN75LVDS86DGG(Texas Instruments) or compatible. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84DGG(negative edge sampling) or compatible.

PIN#	SIGNAL NAME	Description
1	VDD	+3.3V Power Supply
2	VDD	+3.3V Power Supply
3	GND	Ground
4	GND	Ground
5	Reserved	Reserved for future use
6	Reserved	Reserved for future use
7	LVDS GND	Ground

8	Rxin0-	Negative LVDS differential data input (R0-R5, G0)
9	Rxin0+	Positive LVDS differential data input (R0-R5, G0)
10	LVDS GND	Ground
11	Rxin1-	Negative LVDS differential data input (G1-G5, B0-B1)
12	Rxin1+	Positive LVDS differential data input (G1-G5, B0-B1)
13	LVDS GND	Ground
14	Rxin2-	Negative LVDS differential data input (B2-B5, HSYNC,VSYNC,DSPTMG)
15	Rxin2+	Positive LVDS differential data input (B2-B5, HSYNC,VSYNC,DSPTMG)
16	LVDS GND	Ground
17	Rxclk-	Negative LVDS differential clock input
18	Rxclk+	Positive LVDS differential clock input
19	LVDS GND	Ground
20	Reserved	Reserved for LVDS MFG test
Shell	Frame GND	Connected to Return/GND pin through 0 ohm jumper

Internal circuit of LVDS inputs are as follows.



The module uses a 100 ohm resistor between positive and negative data lines of each receiver input.

SIGNAL NAME	Description	
+RED5 +RED4 +RED3 +RED2 +RED1 +RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) **Red-pixel Data**	Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN 5 +GREEN 4 +GREEN 3 +GREEN 2 +GREEN 1 +GREEN 0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) **Green-pixel Data**	Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 +BLUE 4 +BLUE 3 +BLUE 2 +BLUE 1 +BLUE 0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) **Blue-pixel Data**	Each blue pixel's brightness data consists of these 6 bits pixel data.
-DTCLK	**Data Clock**	The typical frequency is 65.0 MHz. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG	**Display Timing**	This signal is strobed at te falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	**Vertical Sync**	The signal is synchronized to -DTCLK .
HSYNC	**Horizontal Sync**	The signal is synchronized to -DTCLK .

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

5.4 Signal Electrical Characteristics

Each signal characteristics are as follows;

Parameter	Condition	Min	Max	UNITS
Vth	Differential Input High Voltage(Vcm=+1.2V)		100	mV
Vtl	Differential Input Low Voltage(Vcm=+1.2V)	-100		mV

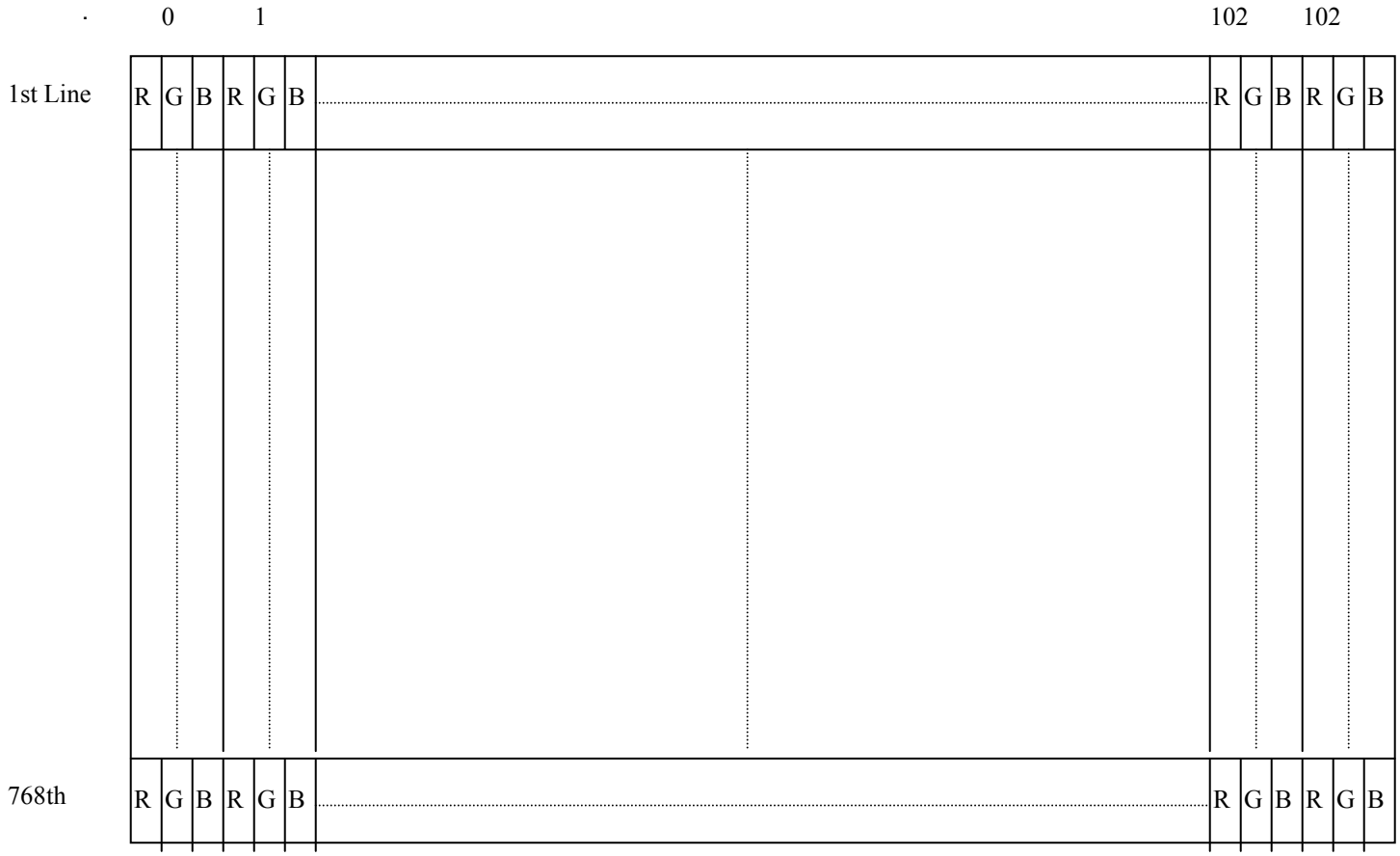
(*) It is recommended to refer the specifications of SN75LVDS86DGG (Texas Instruments) in detail.

5.5 Signal for Lamp connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

6.0 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format.



7.0 Parameter guide line for CFL Inverter

SYMBOL	PARAMETER	MIN	D.P-1 Note 1 1	D.P-2 Note2	MAX	UNITS	CONDITIO N
(L63)	White Luminance	-	90	150	-	cd/m^2	(Ta=25℃)
ICFL	CFL current	3.0	3.4	6.0	6.8	mArms	(Ta=25℃)
ICFLL	CFL Inrush current	-	-	-	20	mA	**Note 3**
fCFL	CFL Frequency	30	40	40	70	KHz	(Ta=25℃) **Note 4**
ViCFL	CFL Ignition Voltage				880	Vrms	(Ta= 0℃) **Note 6**
VCFL	CFL Discharge Voltage (Reference)		510	470		Vrms	(Ta=25℃) **Note 5**
PCFL	CFL Power consumption		1.7	2.8		W	(Ta=25℃) **Note 5**

Note 1: Design Point-1 ; At White Luminance 90 cd/m^2, PCFL=1.7W is required.
Note 2: Design Point-2 ; At White Luminance 150 cd/m^2, PCFL=2.8W is required.
Note 3: (duration=50 (msec))
Note 4: CFL Frequency should be carefully determined to avoid interference between inverter and TFT LCD
Note 5: Calculator value for reference (ICFL×VCFL=PCFL)
Note 6: CFL inverter should be able to give out a power that has a generating capacity of over 880 voltage. Lamp units need 880 voltage minimum for ignition.

8.0 Interface Timings

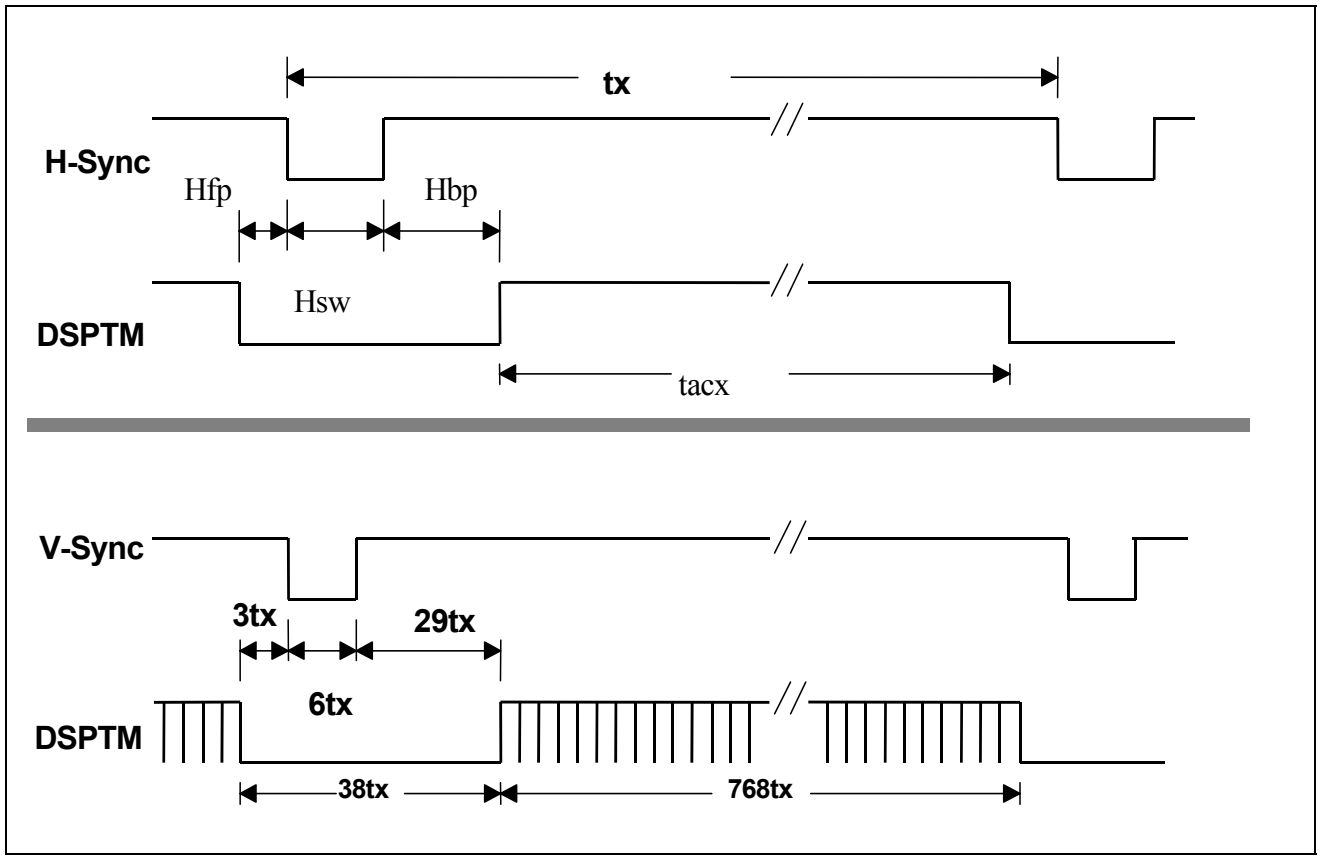
Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS86DGG (Texas Instruments) or equivalent.

8.1 Timing Characteristics

Symbol		MIN	TYP	MAX	Unit
fdck	DTCLK Frequency		65.00		MHz
tck	DTCLK cycle time		15.38		nsec
tx	X total time	1206	1344	2047	tck
tacx	X active time	129	1024		tck
tbkx	X blank time	90	320		tck
Hsync	H frequency		48.363		KHz
Hsw	H-Sync width	2	136		tck
Hbp	H back porch	1	160		tck
Hfp	H front porch	0	24		tck
ty	Y total time	771	806	1023	tx
tacy	Y active time		768		tx
Vsync	Frame rate	(55)	60	61	Hz
Vw	V-sync Width	1	6		tx
Vfp	V-sync front porch	1	3		tx
Vbp	V-sync back porch	7	29	63	tx

Note: Hsw(H-sync width) + Hbp(H-sync back porch) should be less than 515 tck.

8.2 Timing Definition


tx
H-Sync
Hfp
Hbp
Hsw
DSPTM
tacx
V-Sync
3tx
29tx
6tx
DSPTM
38tx
768tx

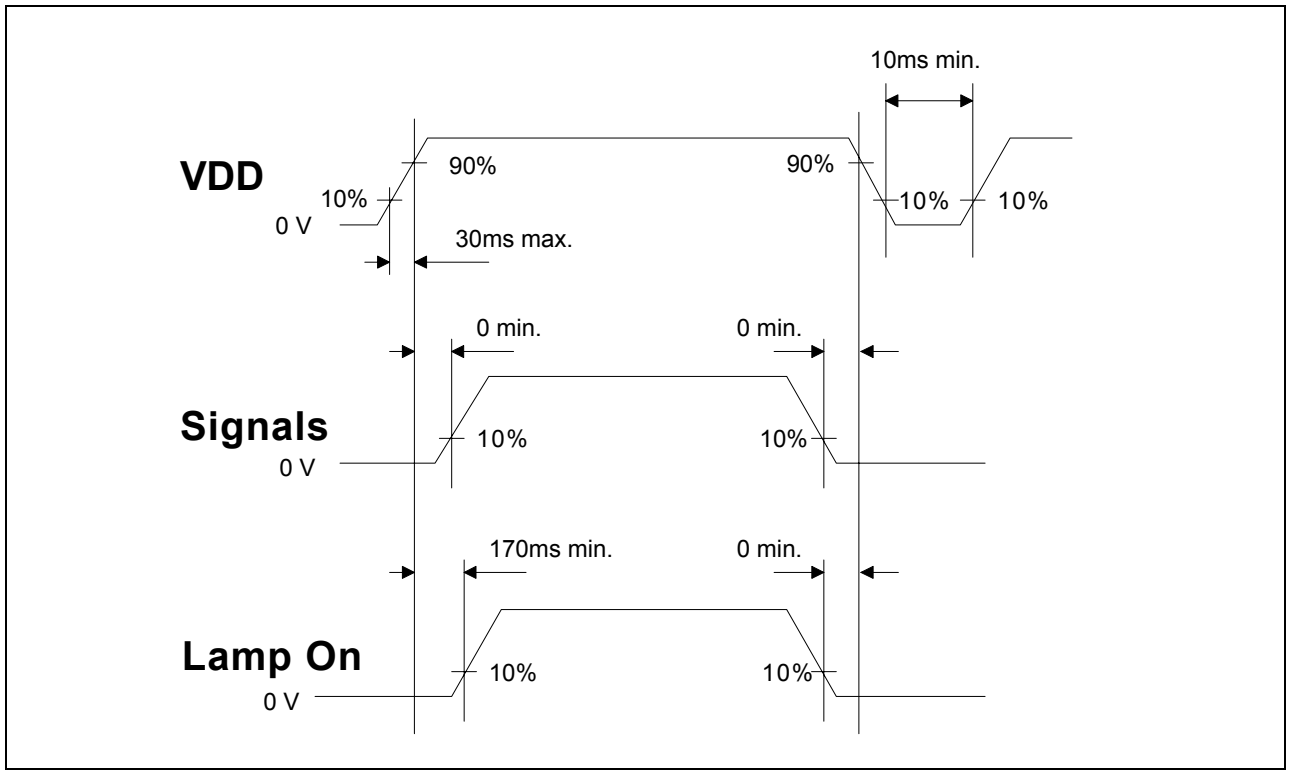
9.0 Power Consumption

Input power specifications are as follows;

SYMBOL	PARAMETER	Min	Typ	Max	UNITS	CONDITION
VDD	Logic/LCD Drive Voltage	4.75	5.00	5.25	V	Load Capacitance 100uF typ
PDD	VDD Power		1.2	1.3	W	All Black Pattern
PDDmax	VDD Power max			1.60	W	Sub-pixel checker
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	mVp-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	mVp-p	

10.0 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



11.0 Mechanical Characteristics

This module is side mounted type by 4 screws(M2.5).

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