Version: 0
Date: 2005/5/2

Product Functional Specification

14.0 inch WXGA Color TFT LCD Module
Model Name: B140EW01 V.3
--- RoHS Compliance

( ) Preliminary Specification
(u) Final Specification

Note: This Specification is subject to change without notice.

Contents

II Record of Revision

Version and Date	Page	Old description	New Description	Remark
V.0 2005/05/02	All	First Release	NA	

1.0 Handling Precautions

1) Do not press or scratch the surface harder than a HB pencil lead because the polarizers are very fragile and could be easily damaged.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water droplets or oil immediately. Long contact with the droplets may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Protect the module from static electricity and insure proper grounding when handling. Static electricity may cause damage to the CMOS Gate Array IC.
7) Do not disassemble the module.
8) Do not press the reflector sheet at the back of the module.
9) Avoid damaging the TFT module. Do not press the center of the CCFL Reflector when it was taken out from the packing container. Instead, press at the edge of the CCFL Reflector softly.
10) Do not rotate or tilt the signal interface connector of the TFT module when you insert or remove other connector into the signal interface connector.
11) Do not twist or bend the TFT module when installation of the TFT module into an enclosure (Notebook PC Bezel, for example). It should be taken into consideration that no bending/twisting forces are applied to the TFT module from outside when designing the enclosure. Otherwise the TFT module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local regulations for disposal.
13) The LCD module contains a small amount of material that has no flammability grade, so it should be supplied by power complied with requirements of limited power source (2.11, IEC60950 or UL1950).
14) The CCFL in the LCD module is supplied with Limited Current Circuit (2.4, IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.

2.0 General Description

This specification applies to the 14.0 inch Color TFT/LCD Module B140EW01

This module is designed for a display unit of notebook style personal computer.

The screen format is intended to support the WXGA (1280(H) x 768(V)) screen and 262k colors (RGB 6-bits data driver).

All input signals are LVDS interface compatible.

This module does not contain an inverter card for backlight.

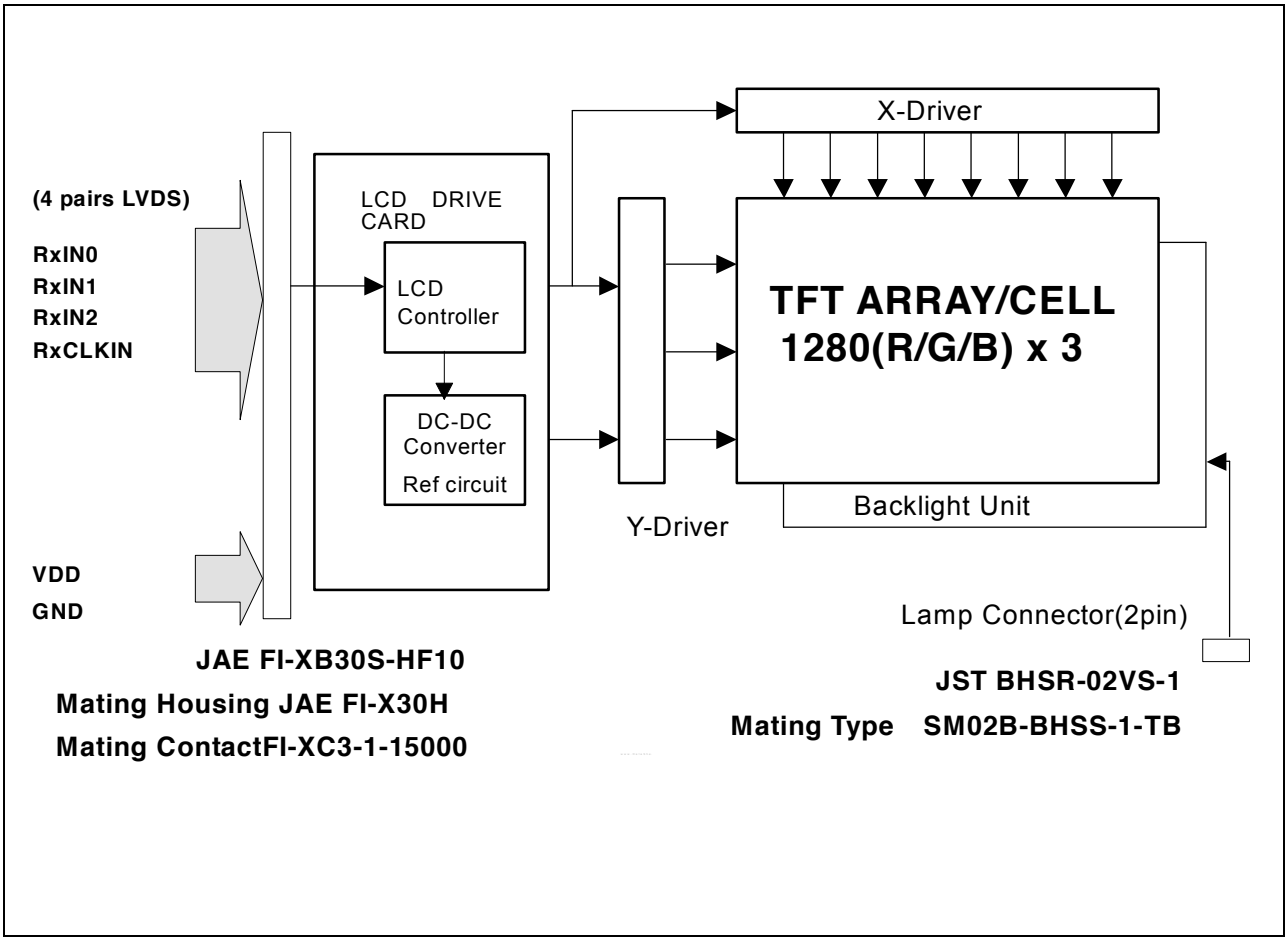
2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	355.6 (14.0")
Active Area	[mm]	305.28(H) x 183.17(V)
Pixels H x V		1280(x3) x 768
Pixel Pitch	[mm]	0.2385
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
Typical White Luminance (CCFL=6.0mA)	[cd/m^2]	200 Typ.(5 points average)
Contrast Ratio		250 : 1 Min ,300:1 Typ
Response Time	[msec]	25 Typ.
Nominal Input Voltage VDD	[Volt]	+3.3 Typ.
Typical Power Consumption (VDD line + VCFL line)	[Watt]	5.8 Watt (w/o Inverter)@ LCM circuit 1.6 Watt (typ.), B/L input 4.2 Watt (typ.)
Weight	[Grams]	440g Typ. (w/o Inverter)
Physical Size	[mm]	320(W) x 199(H) x 5.7(D) Max.
Electrical Interface		R/G/B Data, 3 Sync, Signals, Clock (4 pairs LVDS)
Support Color		Native 262K colors (RGB 6-bit data driver)
Surface treatment		Haze 25, hard coating 3H,AG
Temperature Range Operating Storage (Shipping)	 [^{o}C] [^{o}C]	 0 to +50 -20 to +60

2.2 Functional Block Diagram

The following diagram shows the functional block of the 14.0 inches Color TFT/LCD Module:



3.0 Absolute Maximum Ratings

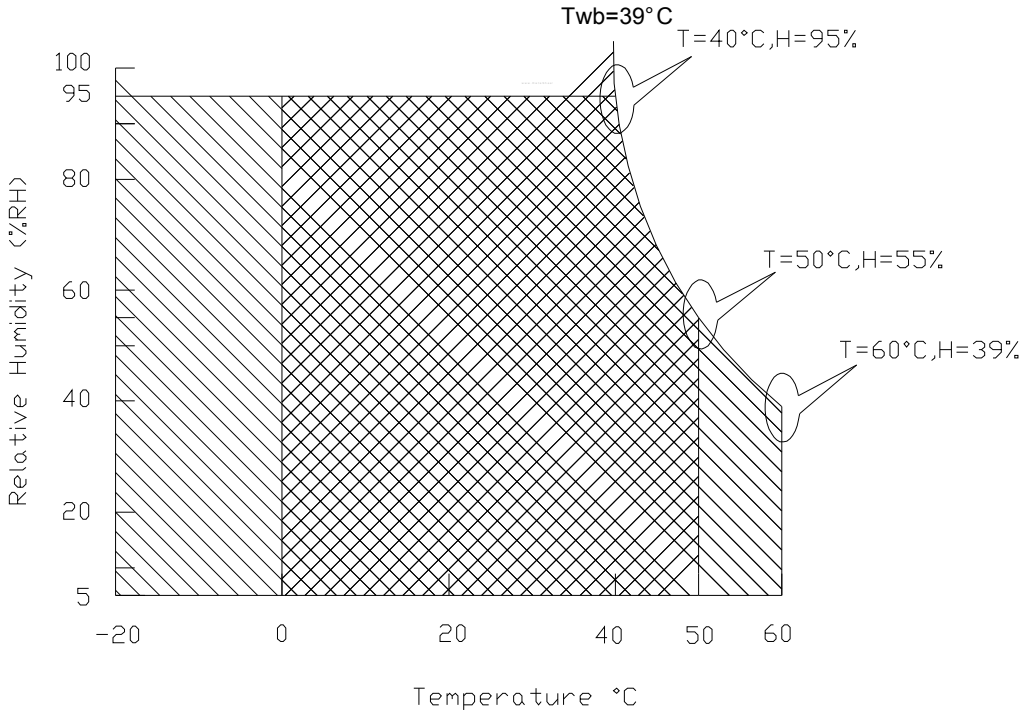
Absolute maximum ratings of the module is as following:

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	[Volt]	
Input Voltage of Signal	Vin	-0.3	VDD+0.3	[Volt]	
CCFL Current	ICFL	2.5	7	[mA] rms	
CCFL Ignition Voltage	Vs	—	1200	Vrms	**Note 1**
Operating Temperature	TOP	0	+50	[°C]	**Note 2**
Operating Humidity	HOP	5	95	[%RH]	**Note 2**
Storage Temperature	TST	-20	+60	[°C]	**Note 2**
Storage Humidity	HST	5	95	[%RH]	**Note 2**
Vibration			1.5Sin 10-500	[G Hz]	
Shock			240, 2	[G ms]	Half sine wave

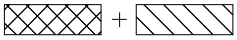
Note 1: Duration = 50msec

Note 2: Maximum Wet-Bulb should be 39℃ and No condensation.

Wet bulb temperature chart



Operating Range

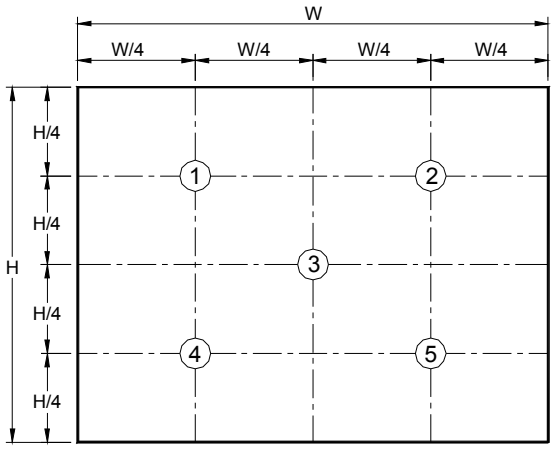
Storage Range 

4.0 Optical Characteristics

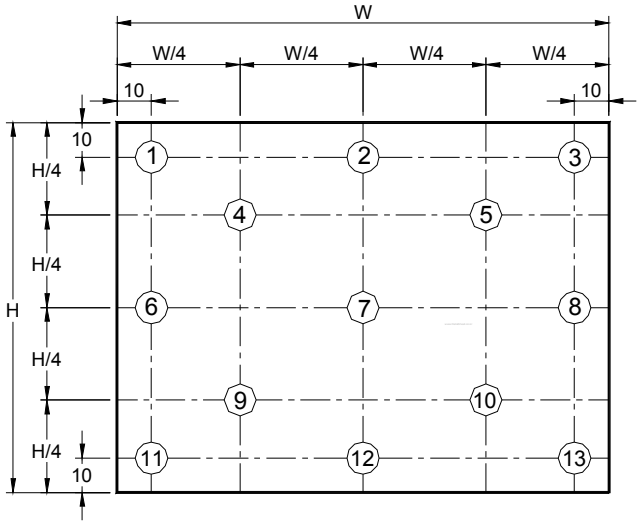
The optical characteristics are measured under stable conditions as follows under 25℃ condition:

Item	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing Angle (CR = 10) CR: Contrast Ratio	[degrees]	Horizontal (Right)	40	45	-	
		(Left)	40	45	-	
		Vertical (Upper)	15	20	-	
		(Lower)	30	35	-	
Uniformity		5 Points	-		1.2	(1)
		13 Points	-		1.5	(2)
Contrast ratio (Center)			250	300	-	
Response Time	[msec]	Rising	-	15	20	
		Falling	-	10	15	
Color Chromaticity Coordinates (CIE) (Normal view angle)		Red x	0.560	0.590	0.620	
		Red y	0.300	0.330	0.360	
		Green x	0.290	0.320	0.350	
		Green y	0.510	0.540	0.570	
		Blue x	0.120	0.150	0.180	
		Blue y	0.100	0.130	0.160	
		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	
White Luminance (CCFL 6.0mA)	[cd/m^2]	5 points average	--	200	-	(1)
Cross talk	%		--	---	1.4	(3)

Note (1): 5 points position (Display area: 305.28 mm x 183.17 mm)



Note (2): 13 points position



Note (3): Definition of Cross Talk (D_{CT})

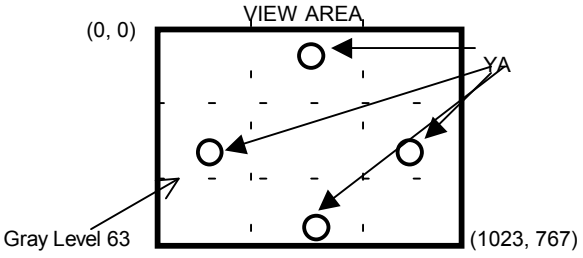
$D_{CT} = | Y_B – Y_A | / Y_A \times 100$ (%)

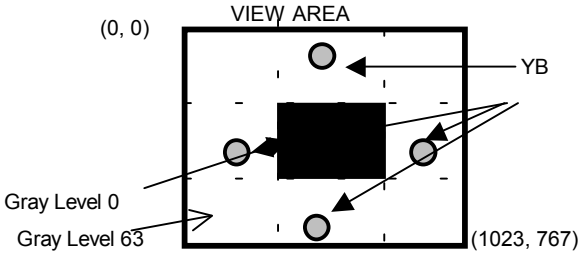
Y_A ,Y_B = (511,127) or (170,383) or (853,383) or (511,639)

Where :

Y_A = Luminance of measured location without darkest gray pattern (cd/m^2)

Y_B = Luminance of measured location with darkest gray pattern (cd/m^2)





5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	FI-XB30S-HF10
Mating Housing/Part Number	FI-X30H
Mating Contact/Part Number	FI-XC3-1-15000

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

5.2 Signal Pin

Pin#	Signal Name	Pin#	Signal Name
1	GND	2	VDD
3	VDD	4	V_{EDID}
5	NC	6	CLK_{EDID}
7	$DATA_{EDID}$	8	RxIN0-
9	RxIN0+	10	GND
11	RxIN1-	12	RxIN1+
13	GND	14	RxIN2-
15	RxIN2+	16	GND
17	RxCLKIN-	18	RxCLKIN+
19	GND	20	NC
21	NC	22	GND
23	NC	24	NC
25	GND	26	NC
27	NC	28	GND
29	NC	30	NC

5.3 Signal Description

The module uses a LVDS receiver embedded in AUO's ASIC. LVDS is a differential signal technology for LCD interface and high-speed data transfer device.

Signal Name	Description
V_{EDID}	+3.3V EDID Power
CLK_{EDID}	EDID Clock Input
$DATA_{EDID}$	EDID Data Input
RxIN0-, RxIN0+	LVDS differential data input(Red0-Red5, Green0)
RxIN1-, RxIN1+	LVDS differential data input(Green1-Green5, Blue0-Blue1)
RxIN2-, RxIN2+	LVDS differential data input(Blue2-Blue5, Hsync, Vsync, DSPTMG)
RxCLKIN-, RxCLKIN0+	LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

Note: Input signals shall be in low status when VDD is off.

Internal circuit of LVDS inputs are as following.

Signal Name	Description	
+RED5 +RED4 +RED3 +RED2 +RED1 +RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) **(Red-pixel Data)**	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN 5 +GREEN 4 +GREEN 3 +GREEN 2 +GREEN 1 +GREEN 0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) **(Green-pixel Data)**	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 +BLUE 4 +BLUE 3 +BLUE 2 +BLUE 1 +BLUE 0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) **(Blue-pixel Data)**	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
-DTCLK	**Data Clock**	The typical frequency is 71.1 MHz. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG	**Display Timing**	This signal is stored at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.

VSYNC	**Vertical Sync**	The signal is synchronized to -DTCLK .
HSYNC	**Horizontal Sync**	The signal is synchronized to -DTCLK .

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

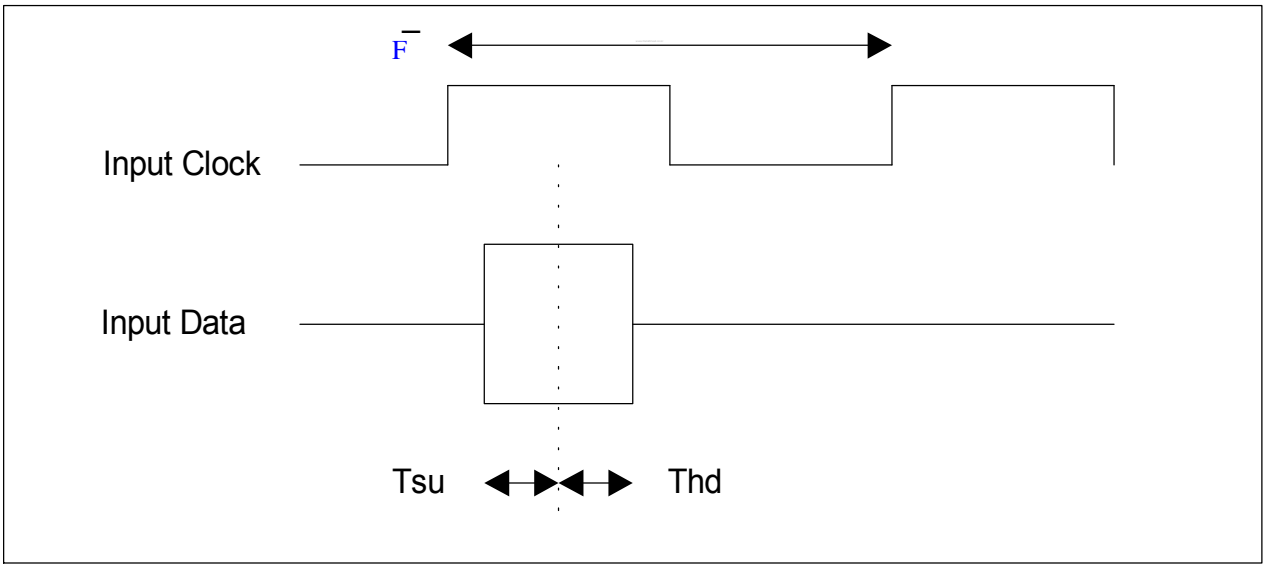
5.4 Signal Electrical Characteristics

Input signals shall be in low status when VDD is off.
It is recommended to refer the specifications of SN75LVDS86DGG (Texas Instruments) in detail.
Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Voltage(Vcm=+1.2V)	—	100	[mV]
Vtl	Differential Input Low Voltage(Vcm=+1.2V)	-100	—	[mV]

LVDS Macro AC characteristics are as follows:

	Min.	Max.
Clock Frequency (F)	60.7MHz	85MHz
Data Setup Time (Tsu)	600ps	
Data Hold Time (Thd)	600ps	



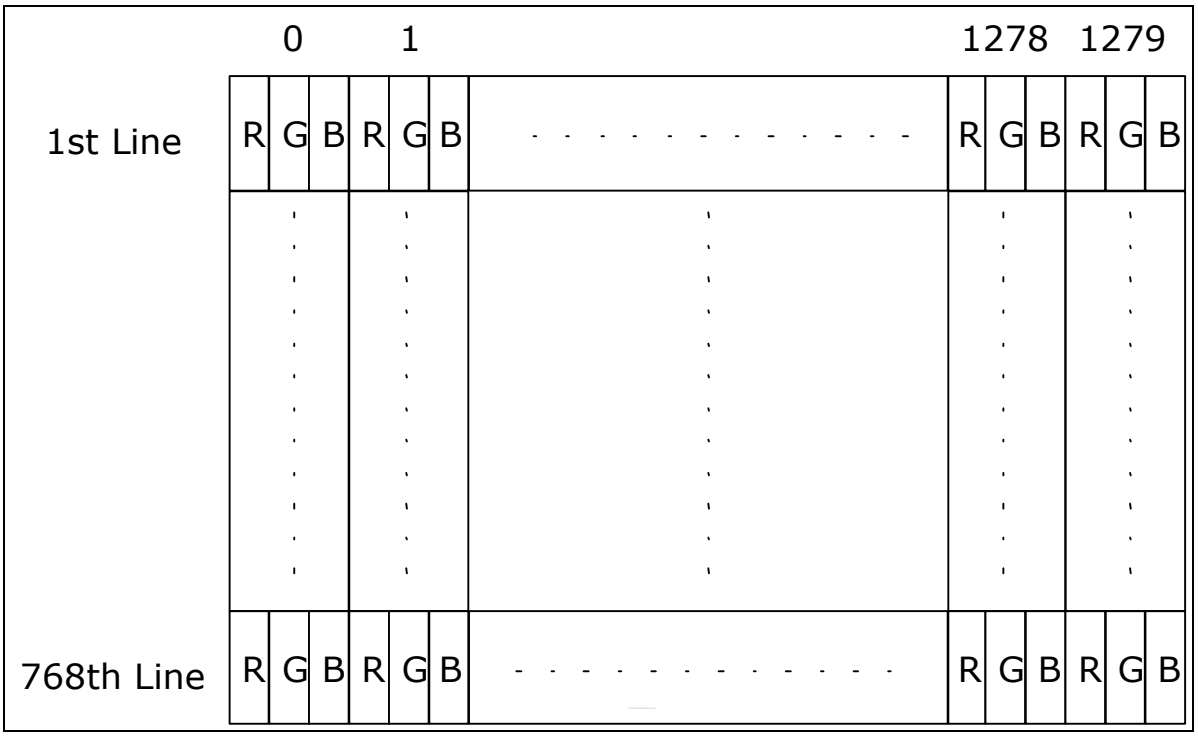
5.5 Signal for Lamp connector

Pin #	Signal Name
1	Lamp High Voltage

2	Lamp Low Voltage

6.0 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



7.0 Parameter guide line for CCFL Inverter

Parameter	Min	DP-1	Max	Units	Condition
White Luminance 5 points average	170	200	—	[cd/m^2]	(Ta=25℃)
CCFL current (ICFL)	2.5	6.0	7.0	[mA] rms	(Ta=25℃) **(Note 2)**
CCFL Frequency (FCFL)	50	60	65	[KHz]	(Ta=25℃) **(Note 3)**
CCFL Ignition Voltage (Vs)	—	1000	1200	[Volt] rms	(Ta= 25℃) **(Note 4)**
CCFL Voltage (Reference) (VCFL)	—	650	—	[Volt] rms	(Ta=25℃) **(Note 5)**
CCFL Power consumption (PCFL)	—	4.2	—	[Watt]	(Ta=25℃) **(Note 5)**

Note 1: DP-1 are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.
*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.
*3 In designing an inverter, it is suggested to check safety circuit ver carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CCFL is damaged.
*4 Generally, CCFL has some amount of delay time after applying start-up voltage. It is recommended to keep on applying start-up voltage for 1 [Sec] until discharge.
*5 The CCFL inverter operating frequency must be carefully chosen so that no interfering noise stripes on the screen were induced.
*6 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter, which has "Duty Dimming", if ICCFL is less than 4mA.

Note 3: The CCFL inverter operating frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The inverter open voltage should be designed larger than the lamp starting voltage at T=0°C, otherwise backlight may be blinking for a moment after turning on or not be able to turn on. The open voltage should be measured after ballast capacitor. If an inverter has shutdown function it should keep its open voltage. for longer than 1 second even if lamp connector is open.

Note 5: Calculator value for reference (ICFL×VCFL=PCFL)

8.0 Interface Timings

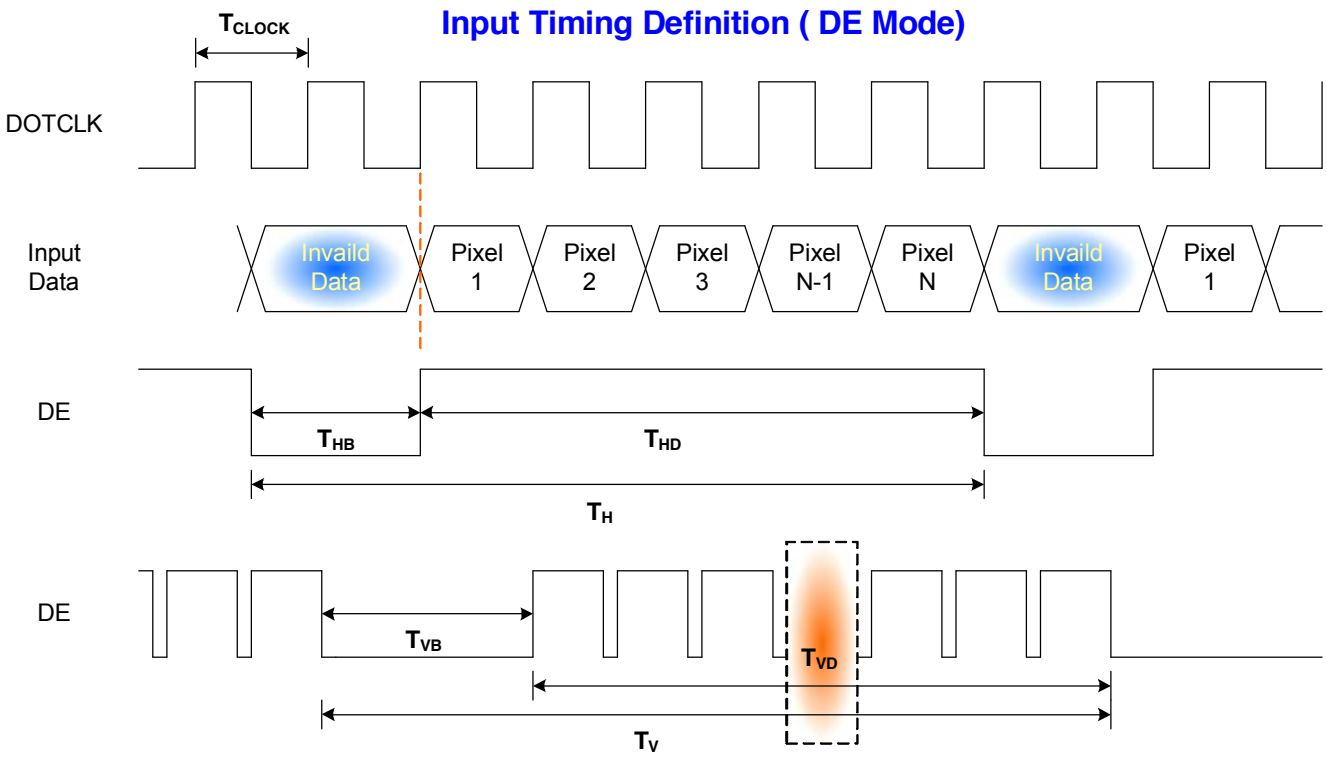
Basically, interface timings should match the VESA 1024x768 /60Hz (VG901101) manufacturing guide line timing.

8.1 Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit
DOTCLK	DOTCLK Frequency	**(TBD)**	71.1	**(TBD)**	[MHz]
T_{CLOCK}	DOTCLK cycle time	**(TBD)**	14.06	**(TBD)**	[nsec]
T_H	X total time	—	1440	—	[tck]
T_{HD}	X active time	—	1280	—	[tck]
T_{HB}	X blank time	—	160	—	[tck]
T_V	Y total time	—	823	—	[tx]
T_{VD}	Y active time	—	768	—	[tx]
Vsync	Frame rate	—	60	—	[Hz]

Note: DE mode

8.2 Timing Definition



9.0 Power Consumption

Input power specifications are as follows;

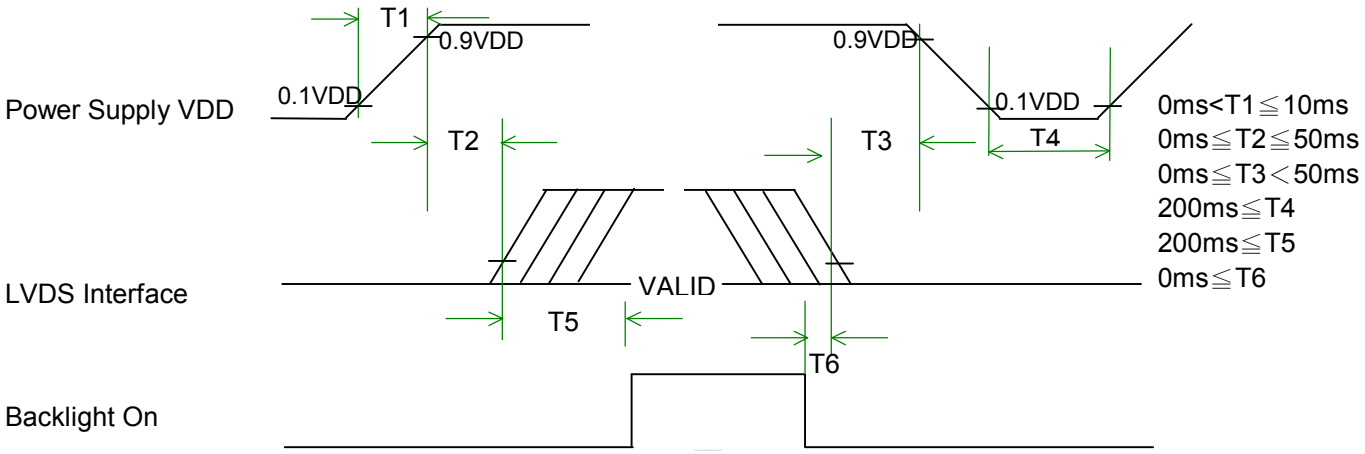
Symbol	Parameter	Min	Typ	Max	Units	Condition
Module						
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	Load Capacitance 20uF
PDD	VDD Power	—	1.6	—	[Watt]	
PDD Max	VDD Power max	—	(TBD)	—	[Watt]	Max Pattern **(Note)**
IDD	IDD Current	—	(TBD)	—	mA	64 Grayscale Pattern
IDD Max	IDD Current max	—	(TBD)	—	mA	Vertical stripe line Pattern **(Note)**
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	—	—	100	[mV] p-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise	—	—	100	[mV] p-p	
Lamp						
ICFL	CCFL current	2.5	6.0	7.0	[mA] rms	(Ta=25℃)
VCFL	CCFL Voltage (Reference)	—	650	—	[Volt] rms	(Ta=25℃)
PCFL	CCFL Power consumption	—	4.2	—	[Watt]	(Ta=25℃)
Total Power Consumption	5.8 Watt (w/o Inverter,)@LCM circuit 1.6 Watt (typ.),B/L input 4.2 Watt(typ.)					

Note: VDD=3.3V

10. Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.

Sequence of Power-on/off and signal-on/off



Apply the lamp voltage within the LCD operating range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal.

11.0 Reliability /Safety Requirement

11.1 Reliability Test Conditions

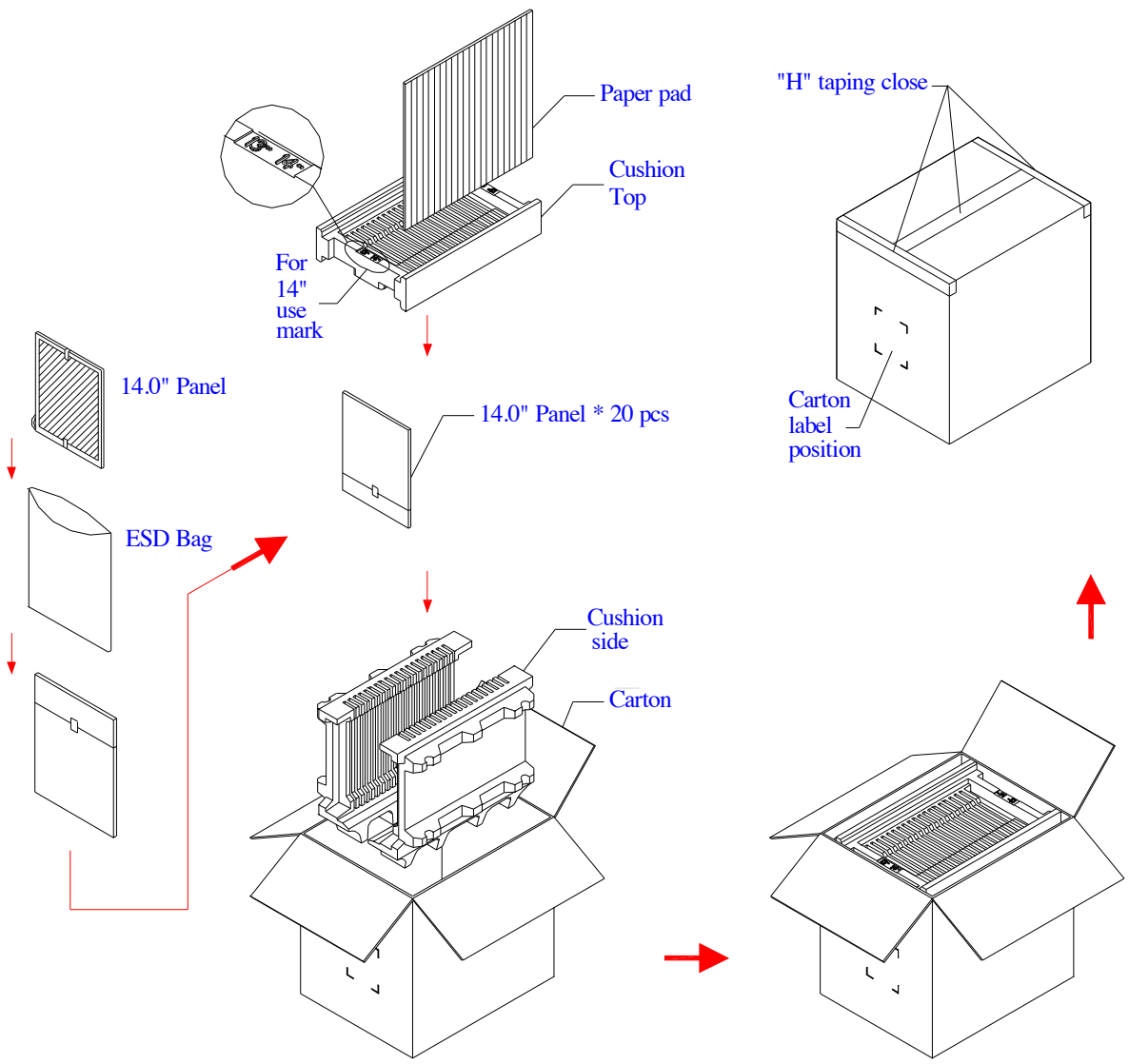
Items	Required Condition
Temperature Humidity Bias	40℃/90%,300Hr
High Temperature Operation	50℃/Dry,300Hr
Low Temperature Operation	0℃,500Hr
Continuous Life	25℃ ,2000 hours
On/Off Test	ON/30 sec. OFF/30sec., 30,000 cycles
Hot Storage	60℃/40% RH ,240 hours
Cold Storage	-20℃/50% RH ,240 hours
Thermal Shock Test	-20℃/30 min ,60℃/30 min 100cycles
Hot Start Test	50℃/1 Hr min. Power on/off per 5 minutes, 5 times
Cold Start Test	0℃/1 Hr min. Power on/off per 5 minutes, 5 times
Shock Test (Non-Operating)	240G, 2ms, Half-sine wave
Vibration Test (Non-Operating)	Sinusoidal vibration, 1.5G zero-to-peak, 10 to 500 Hz, 0.5 octave/minute in each of three mutually perpendicular axes.
ESD	Contact : operation ±8KV / non-operation ±10KV Air : operation ±15KV / non-operation ±20KV
Altitude Test	10000 ft / operation / 8Hr 30000 ft / non-operation / 24r
Maximum Side Mount Torque	2.5 kgf.cm .

CCFL Life: 10,000 hours minimum
MTBF(Excluding the CCFL) : 30,000 hours with a confidence level 90%

11.2 Safety

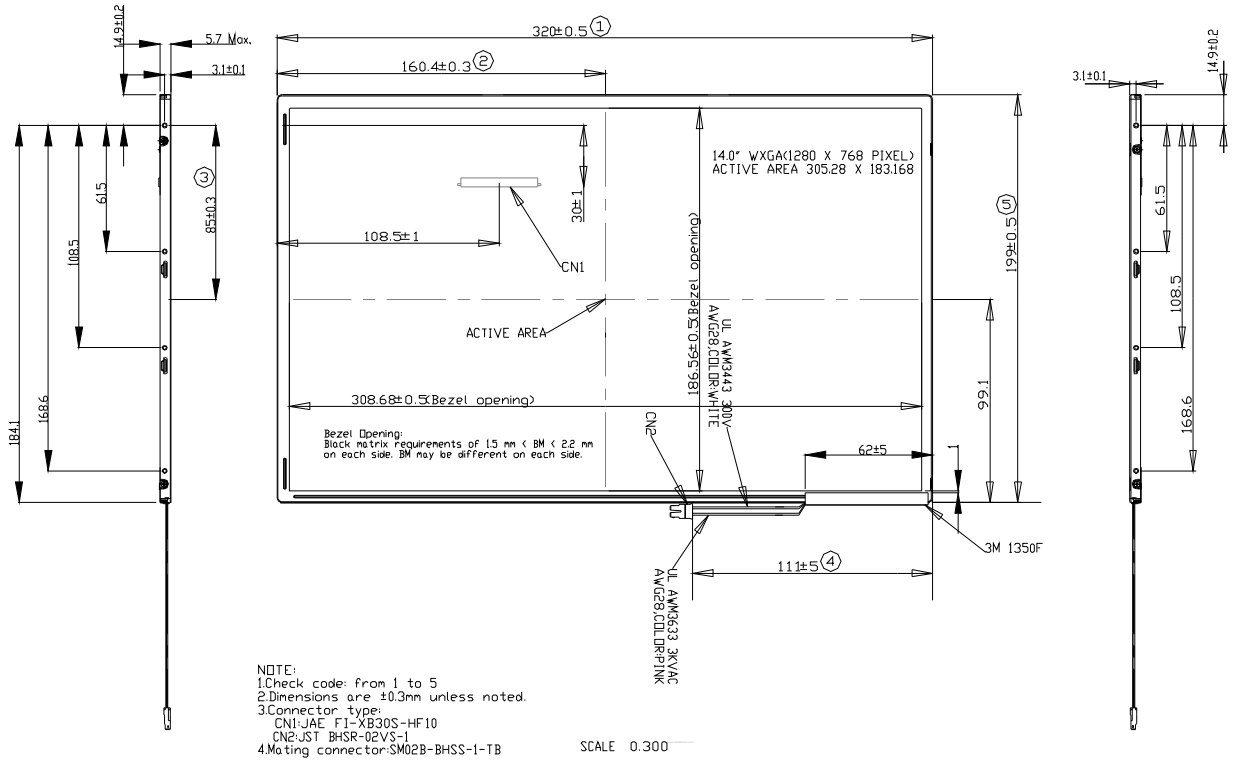
UL1950

12.0 Packing dimension

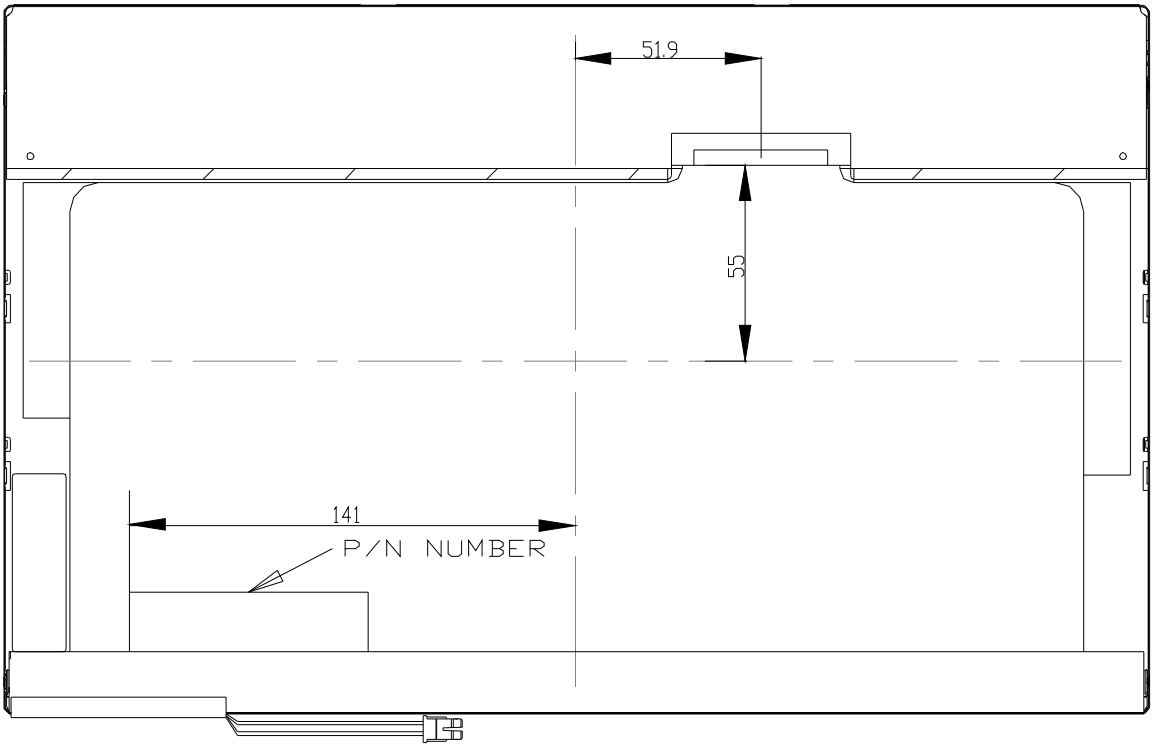


13.0 Mechanical Characteristics

13.1 LCM Outline dimension (Front View)

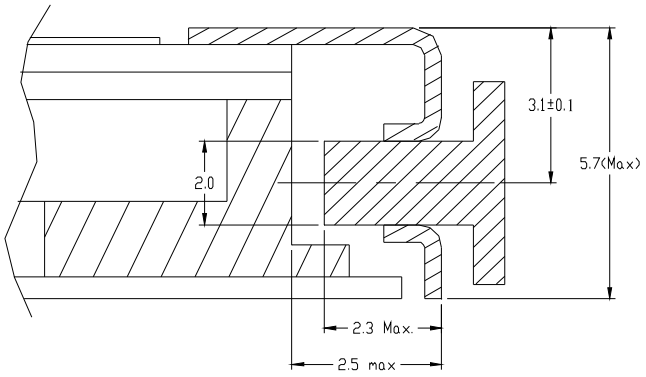


13.2 LCM Outline Dimension (Rear View)



13.3 Screw Hole Depth and Center Position

Screw hole maximum depth, from side surface =2.5 mm (See drawing)
Screw hole center location, from front surface = 3.1 ± 0.1mm (See drawing)
Suggestions: Customers' Screw maximum length = 2.3 mm (See drawing)
Screw Torque: Maximum2.5 kgf-cm



14.0 EDID Data

Address HEX	FUNCTION	Value HEX	Value BIN	Value DEC
00	Header	00	00000000	0
01		FF	11111111	255
02		FF	11111111	255
03		FF	11111111	255
04		FF	11111111	255
05		FF	11111111	255
06		FF	11111111	255
07		00	00000000	0
08	EISA Manuf. Code LSB	06	00000110	6
09	Compressed ASCII	AF	10101111	175
0A	Product Code	33	00110011	51
0B	hex, LSB first	13	00010011	19
0C	32-bit ser #	00	00000000	0
0D		00	00000000	0
0E		00	00000000	0
0F		00	00000000	0
10	Week of manufacture	01	00000001	1
11	Year of manufacture	0F	00001111	15
12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	03	00000011	3
14	Video input definition	80	10000000	128
15	Max H image size	21	00100001	33
16	Max V image size	14	00010100	20
17	Display Gamma	78	01111000	120
18	Feature support	0A	00001010	10
19	Red/green low bits	05	00000101	5
1A	Blue/white low bits	50	01010000	80
1B	Red x/ high bits	97	10010111	151

1C	Red y	57	01010111	87
1D	Green x	4F	01001111	79
1E	Green y	8F	10001111	143
1F	Blue x	26	00100110	38
20	Blue y	21	00100001	33
21	White x	50	01010000	80
22	White y	54	01010100	84
23	Established timing 1	00	00000000	0
24	Established timing 2	00	00000000	0
25	Manufacturer's Timing	00	00000000	0
26	Standard timing #1	01	00000001	1
27		01	00000001	1
28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1
2B		01	00000001	1
2C	Standard timing #4	01	00000001	1
2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Pixel Clock/10,000 (LSB)	C6	11000110	198
37	Pixel Clock/10,000 (MSB)	1B	00011011	27
38	Horiz. Active pixels(Lower 8 bits)	00	00000000	0
39	Horiz.Blanking (Lower 8 bits)	A0	10100000	160
3A	Horiz. Active pixels:Horiz. Blanking (Upper4:4 bits)	50	01010000	80
3B		00	00000000	0
3C		37	00110111	55
3D	Vert. Active pixels:Vert. Blanking (Upper4:4 bits)	30	00110000	48

3E		10	00010000	16
3F		70	01110000	112
40	Vert. Sync. Offset=xx lines, Sync Width=xx lines	13	00010011	19
41	Horz. Ver. Sync/Width (upper 2 bits)	00	00000000	0
42	Hori. Image size (Lower 8 bits)	31	00110001	49
43	Vert. Image size (Lower 8 bits)	B7	10110111	183
44	Hori. Image size : Vert. Image size (Upper 4 bits)	10	00010000	16
45		00	00000000	0
46		00	00000000	0
47		18	00011000	24
48	Detailed timing/monitor	00	00000000	0
49	descriptor #2	00	00000000	0
4A		00	00000000	0
4B		0F	00001111	15
4C		00	00000000	0
4D		00	00000000	0
4E		00	00000000	0
4F		00	00000000	0
50		00	00000000	0
51		00	00000000	0
52		00	00000000	0
53		00	00000000	0
54		00	00000000	0
55		00	00000000	0
56		00	00000000	0
57		00	00000000	0
58		00	00000000	0
59		20	00100000	32
5A	Detailed timing/monitor	00	00000000	0
5B	descriptor #3	00	00000000	0
5C		00	00000000	0
5D		FE	11111110	254
5E		00	00000000	0
5F		41	01000001	65

60		55	01010101	85
61		4F	01001111	79
62		0A	00001010	10
63		20	00100000	32
64		20	00100000	32
65		20	00100000	32
66		20	00100000	32
67		20	00100000	32
68		20	00100000	32
69		20	00100000	32
6A		20	00100000	32
6B		20	00100000	32
6C	Detailed timing/monitor	00	00000000	0
6D	descriptor #4	00	00000000	0
6E		00	00000000	0
6F		FE	11111110	254
70		00	00000000	0
71		42	01000010	66
72		31	00110001	49
73		34	00110100	52
74		30	00110000	48
75		45	01000101	69
76		57	01010111	87
77		30	00110000	48
78		31	00110001	49
79		20	00100000	32
7A		56	01010110	86
7B		33	00110011	51
7C		20	00100000	32
7D		0A	00001010	10
7E	Extension Flag	00	00000000	0
7F	Checksum	E8	11101000	232