( ) Preliminary Specifications
(V) Final Specifications

Module	14.1" WXGA+ Color TFT-LCD
Model Name	B141PW04 V0 (HW 0A) DELL P/N: GX968
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**	**Approved by**	**Date**
Checked & Approved by	**Date**	**Prepared by**	
Adam Liang	05/19/2008		

Note: This Specification is subject to change without notice.

NBBU Marketing Division / AU Optronics corporation

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2007/01/04	All	First Edition for Customer		
0.2 2008/02/26	All	Customer sample edition		
0.3 2008/05/02	All	Final edition		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostic breaddown.

2. General Description

B141PW04 V0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the WXGA+ (1440(H) x 900(V)) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B141PW04 V0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

<table>
<tr><th>Items</th><th>Unit</th><th>Specifications</th></tr>
<tr><td>Screen Diagonal</td><td>[mm]</td><td>357.7 (14.1W”)</td></tr>
<tr><td>Active Area</td><td>[mm]</td><td>303.48 (H) x 189.68 (V)</td></tr>
<tr><td>Pixels H x V</td><td></td><td>1440 x 3 (RGB) x 900</td></tr>
<tr><td>Pixel Pitch</td><td>[mm]</td><td>0.2108 x 0.2108</td></tr>
<tr><td>Pixel Format</td><td></td><td>R.G.B. Vertical Stripe</td></tr>
<tr><td>Display Mode</td><td></td><td>Normally White</td></tr>
<tr><td>White Luminance (ILED=20mA)
(Note: ILED is LED current)</td><td>[cd/m^2]</td><td>300 typ. (5 points average)
250 min. (5 points average)(Note1)</td></tr>
<tr><td>Luminance Uniformity</td><td></td><td>1.25 max. (5 points)</td></tr>
<tr><td>Contrast Ratio</td><td></td><td>400 min</td></tr>
<tr><td>Response Time</td><td>[ms]</td><td>8 typ / 15 Max</td></tr>
<tr><td>Nominal Input Voltage VDD</td><td>[Volt]</td><td>+3.3 typ.</td></tr>
<tr><td>Power Consumption</td><td>[Watt]</td><td>5.5 max. (Include Logic and Blu power, without LED efficiency))</td></tr>
<tr><td>Weight</td><td>[Grams]</td><td>375 max.</td></tr>
<tr><td>Physical Size</td><td>[mm]</td><td>
<table>
<tr><td></td><td>L</td><td>W</td><td>T</td></tr>
<tr><td>Max</td><td>320.0</td><td>207.0</td><td>5.5</td></tr>
<tr><td>Typical</td><td>319.5</td><td>206.5</td><td>-</td></tr>
<tr><td>Min</td><td>319.0</td><td>206.0</td><td>-</td></tr>
</table>
</td></tr>
<tr><td>Electrical Interface</td><td></td><td>2 channel LVDS</td></tr>
<tr><td>Surface Treatment</td><td></td><td>Anti-Glare, Hardness 3H,
Haze 11%</td></tr>
<tr><td>Support Color</td><td></td><td>262K colors (RGB 6-bit)</td></tr>
</table>

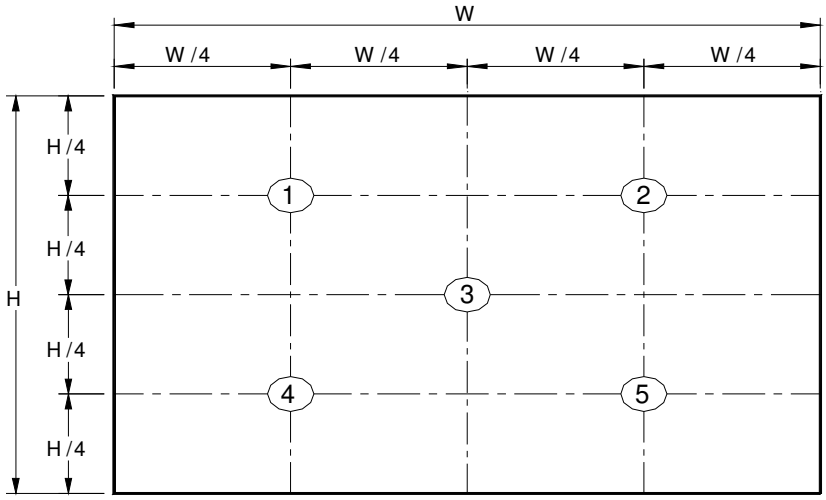
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +65
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

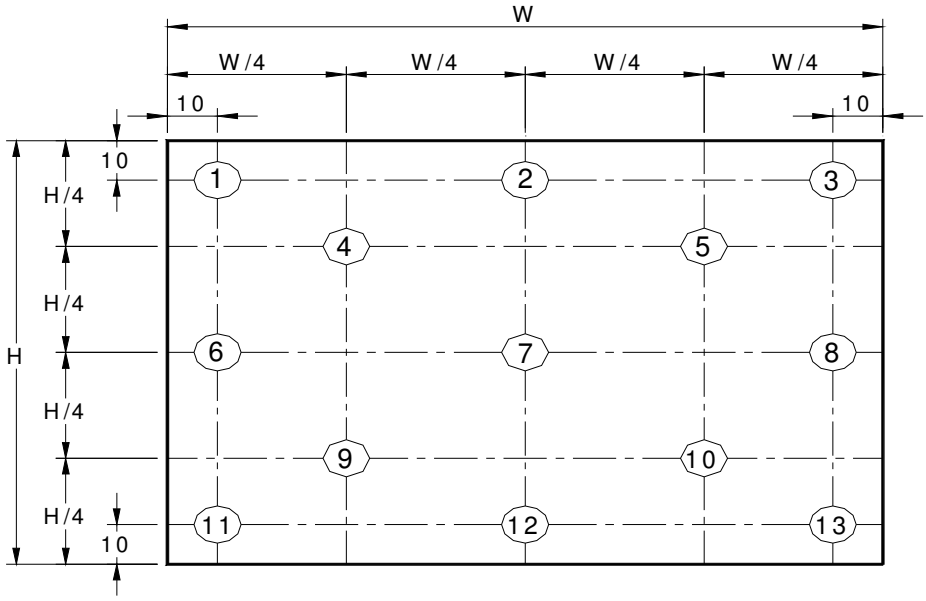
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance (I_{LED}=20mA)	[cd/m^2]	5 points average	250	300	-	1, 4, 5.
Viewing Angle	[degree] [degree]	Horizontal (Right) CR = 10 (Left)	- -	40 40	- -	4, 9
	[degree] [degree]	Vertical (Upper) CR = 10 (Lower)	- -	15 30	- -	
Luminance Uniformity		5 Points	-	-	1.25	1, 3, 4
Luminance Uniformity		13 Points	-	-	1.53	2, 3, 4
CR: Contrast Ratio			400	-	-	4, 6
Cross talk	%				4	4, 7
Response Time	[msec]	Rising	-	-	-	4, 8
	[msec]	Falling	-	-	-	
	[msec]	Rising + Falling	-	8	15	
Chromaticity of color Coordinates (CIE 1931)		Red x	0.550	0.580	0.610	4, 9
		Red y	0.310	0.340	0.370	
		Green x	0.280	0.310	0.340	
		Green y	0.520	0.550	0.580	
		Blue x	0.125	0.155	0.185	
		Blue y	0.125	0.155	0.185	
		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

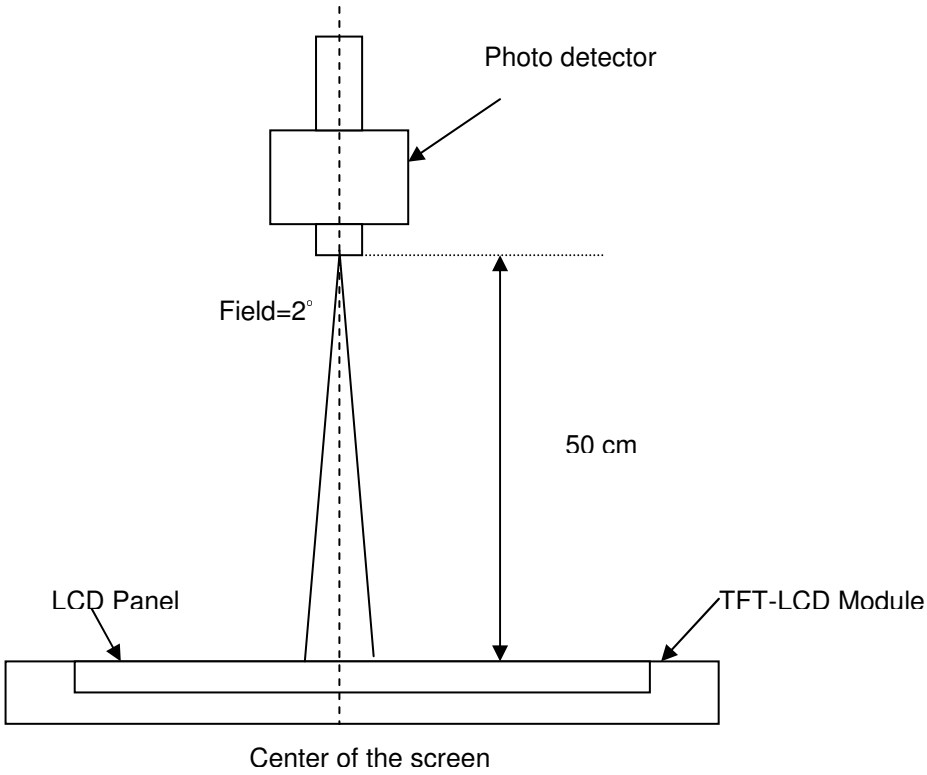
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

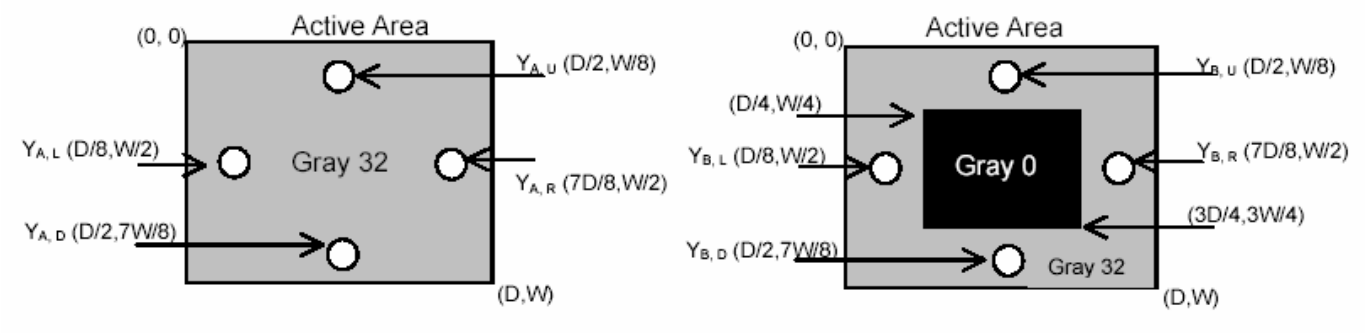
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where

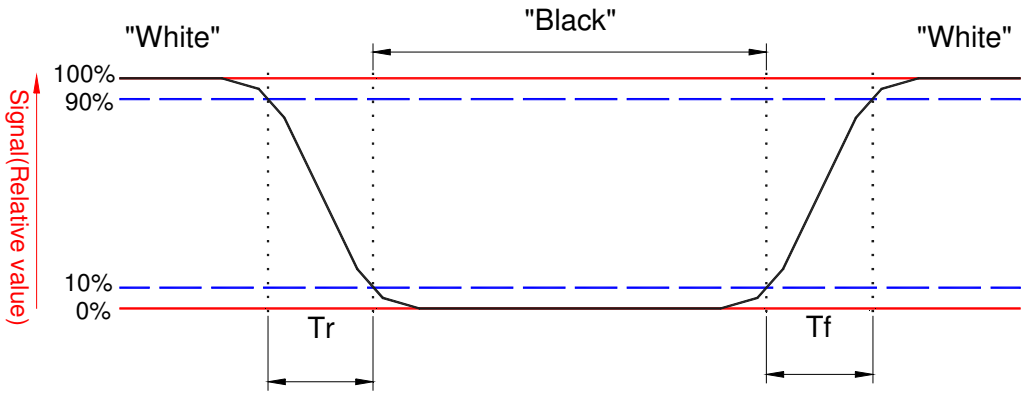
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



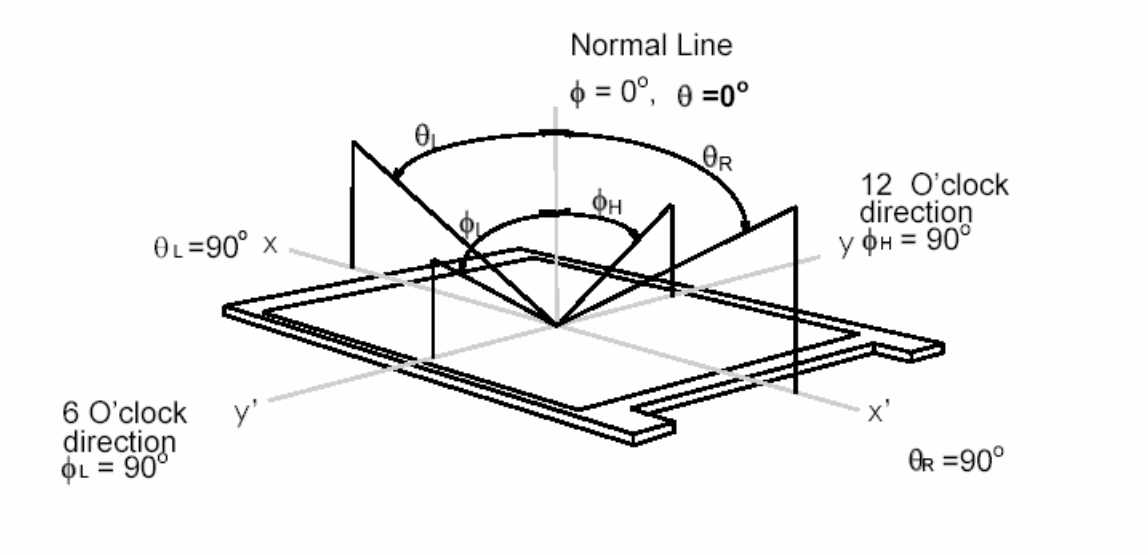
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



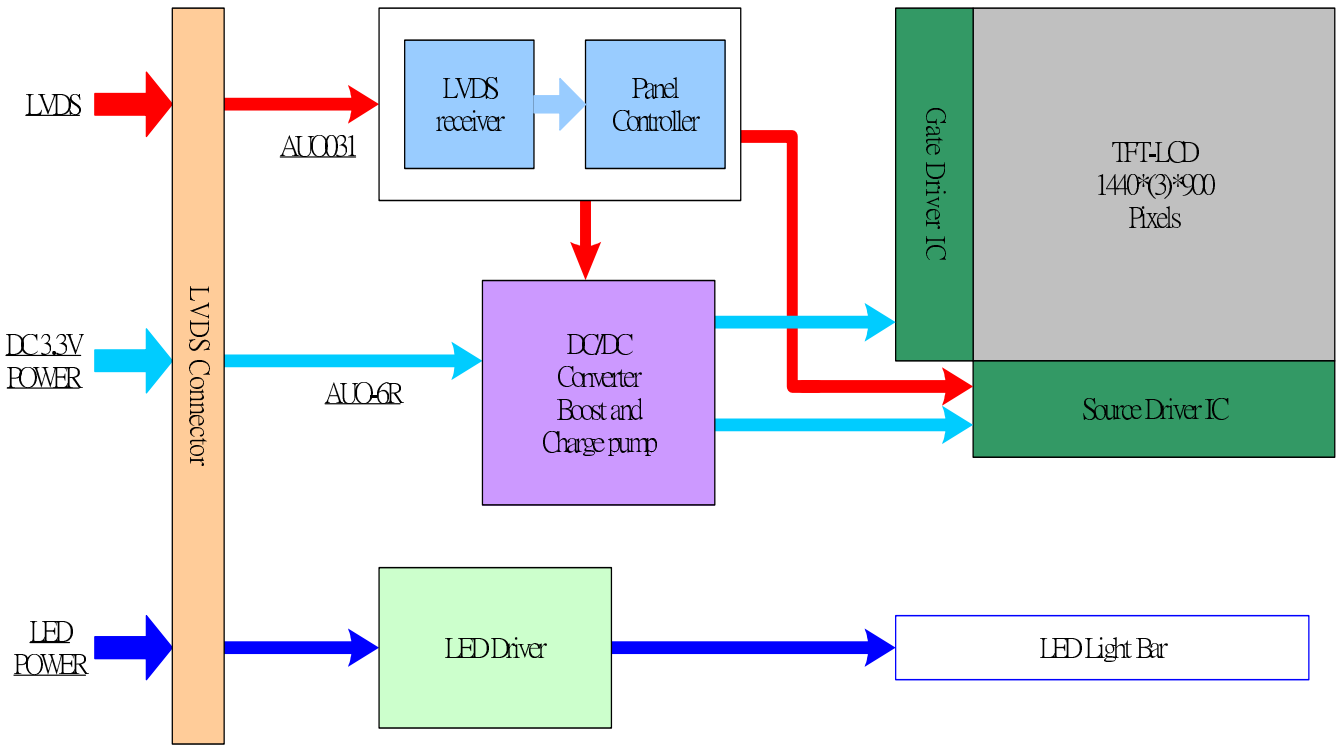
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 14.1 inches wide Color TFT/LCD Module:



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

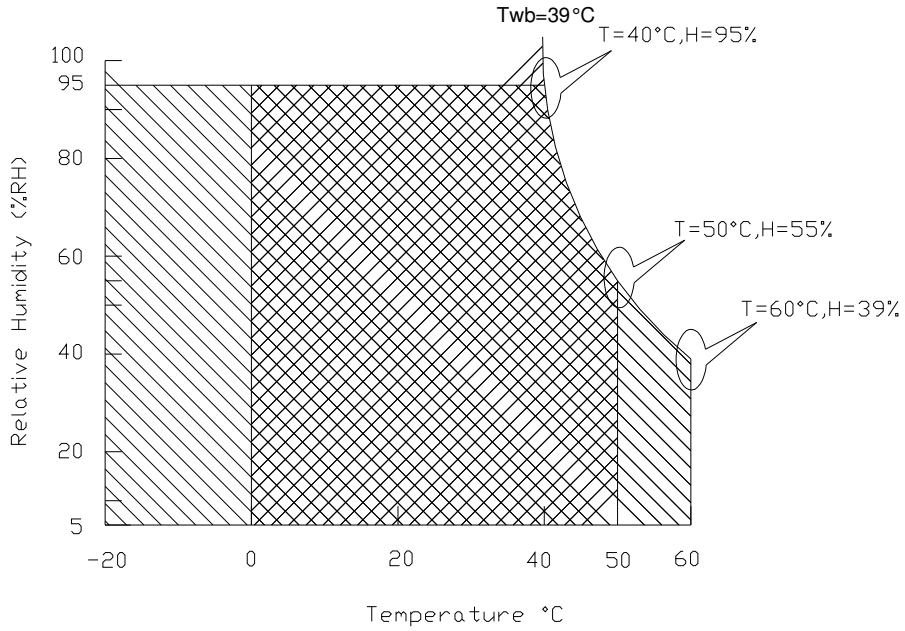
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

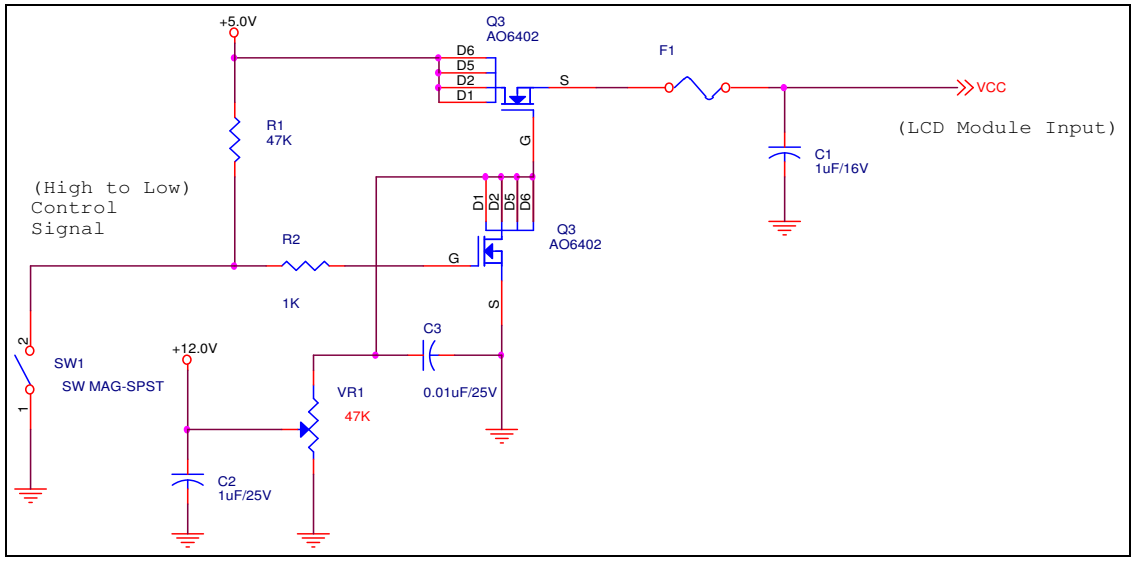
Input power specifications are as follows;

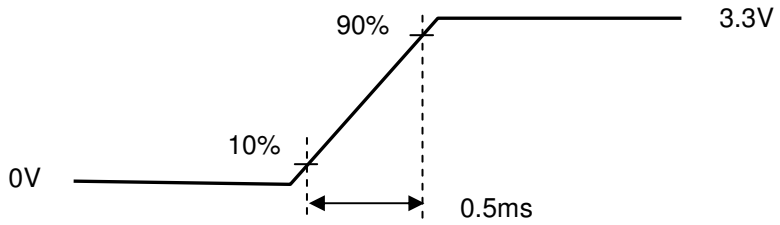
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.5	[Watt]	Note 1/2
IDD	IDD Current	-	310	415	[mA]	Note 1/2
IRush	Inrush Current	-	-	2000	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Pattern

Note 2：Typical Measurement Condition: Mosaic Pattern

Note 3：Measure Condition





Vin rising time

5.1.2 Signal Electrical Characteristics

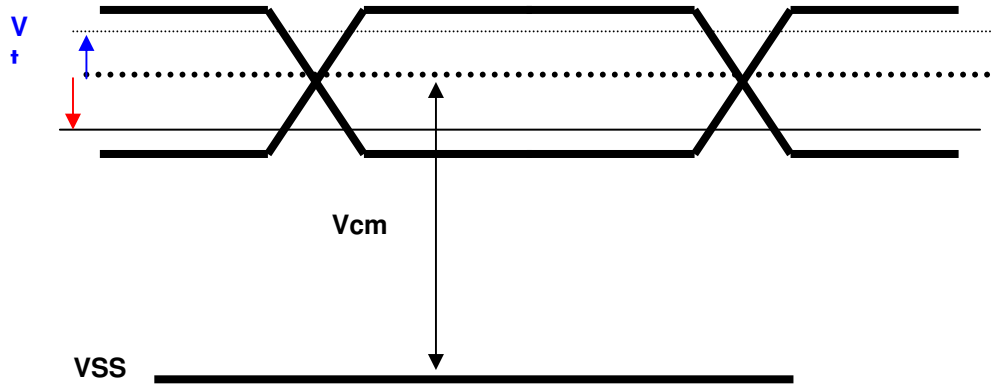
Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of THC63LVDF84A (Thine Electronics Inc.) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)	-	100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100	-	[mV]
Vcm	Differential Input Common Mode Voltage	1.1	1.45	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

LED Parameter guideline for LED driving selection

Parameter	Symbol	Min	Typ	Max	Units	Condition
LED Forward Voltage	V_F	2.8	3.2	3.5	[Volt]	(Ta=25℃)
LED Forward Current	I_F		20	20.6	[mA]	(Ta=25℃)
LED Power consumption	P_{LED}		3.456		[Watt]	(Ta=25℃) Note 1
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃) I_F=20 mA Note 2

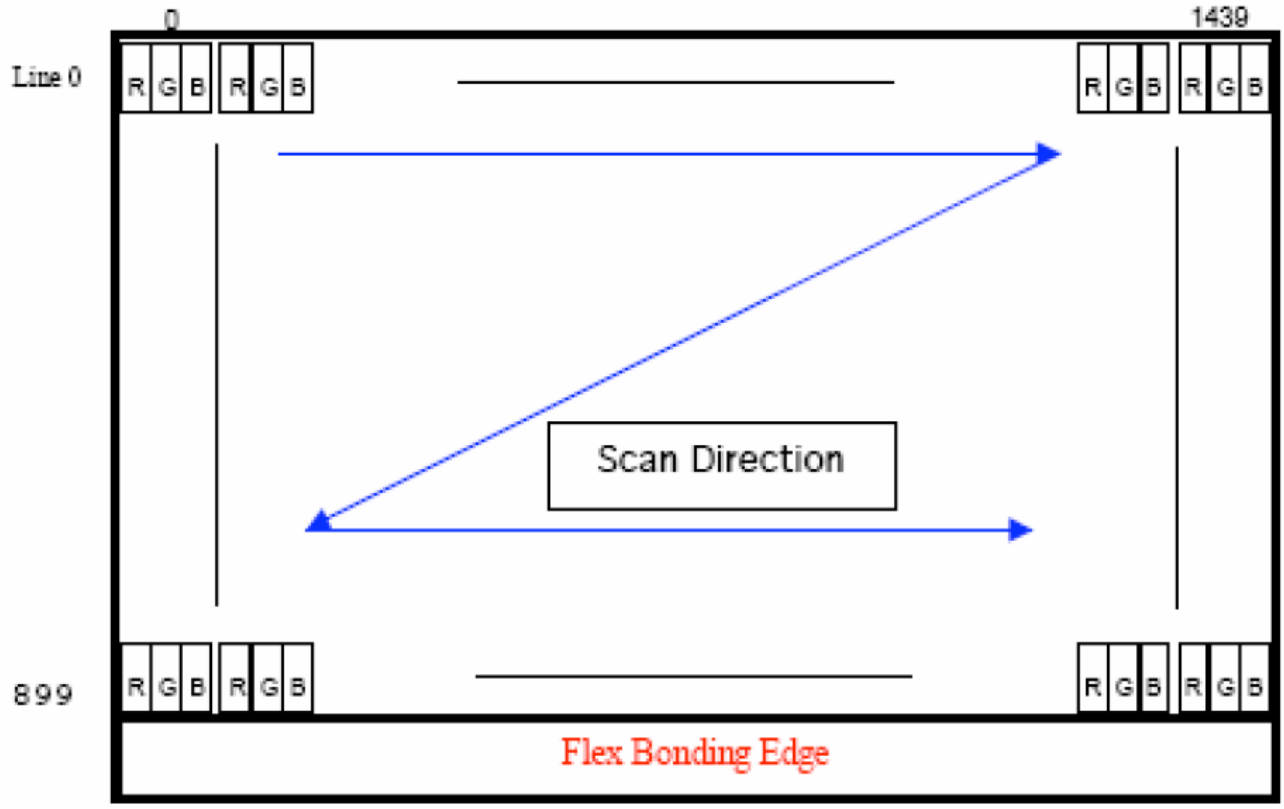
Note 1: Calculator value for reference $P_{LED} = I_F \times V_F \times$ LED(Qty)

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

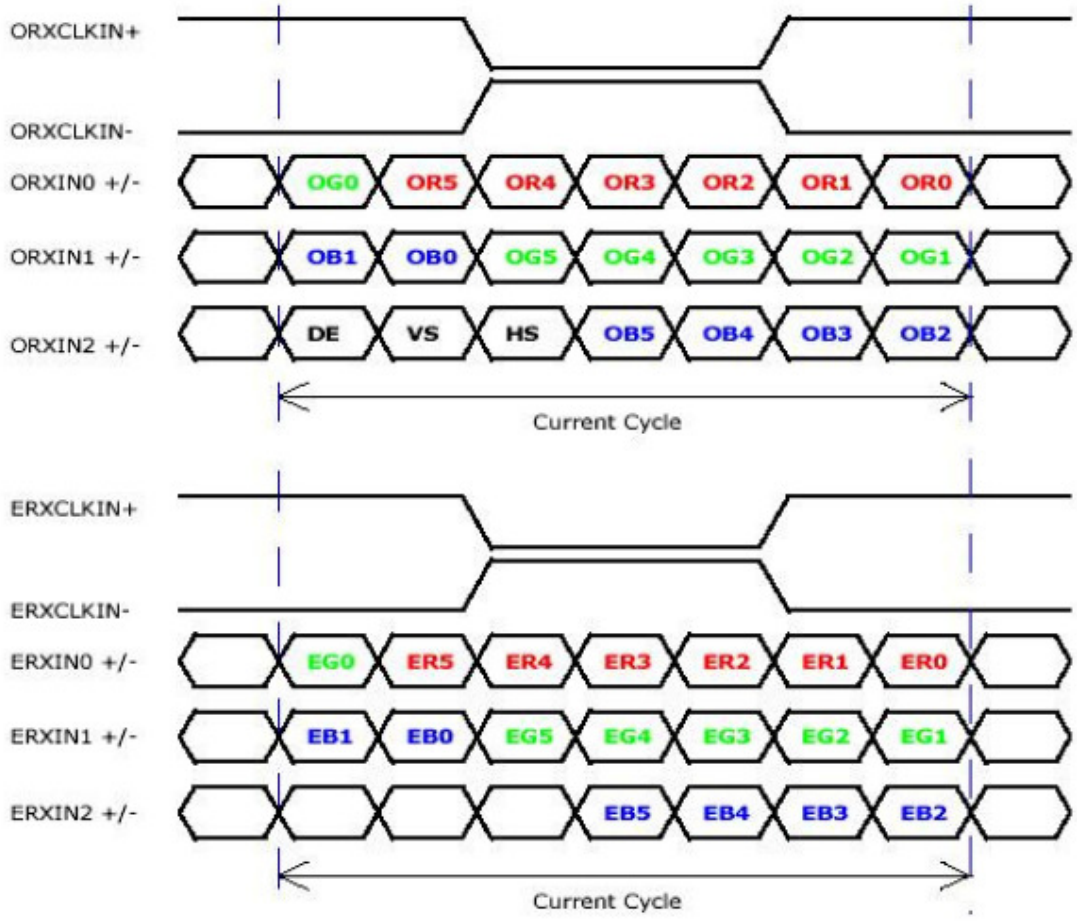
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



Signal Name	Description
V_{EDID}	+3.3V EDID Power
CLK_{EDID}	EDID Clock Input
$DATA_{EDID}$	EDID Data Input
ORXIN0-, ORXIN0+	Odd LVDS differential data input(ORed0-ORed5, OGreen0)
ORXIN1-, ORXIN1+	Odd LVDS differential data input(OGreen1-OGreen5, OBlue0-OBlue1)
ORXIN2-, ORXIN2+	Odd LVDS differential data input(OBlue2-OBlue5, Hsync, Vsync, DE)
ORXCLKIN-, ORXCLKIN+	Odd LVDS differential clock input
ERXIN0-, ERXIN0+	Even LVDS differential data input(ERed0-ERed5, EGreen0)
ERXIN1-, ERXIN1+	Even LVDS differential data input(EGreen1-EGreen5, EBlue0-EBlue1)
ERXIN2-, ERXIN2+	Even LVDS differential data input(EBlue2-EBlue5)
ERXCLKIN-, ERXCLKIN+	Even LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

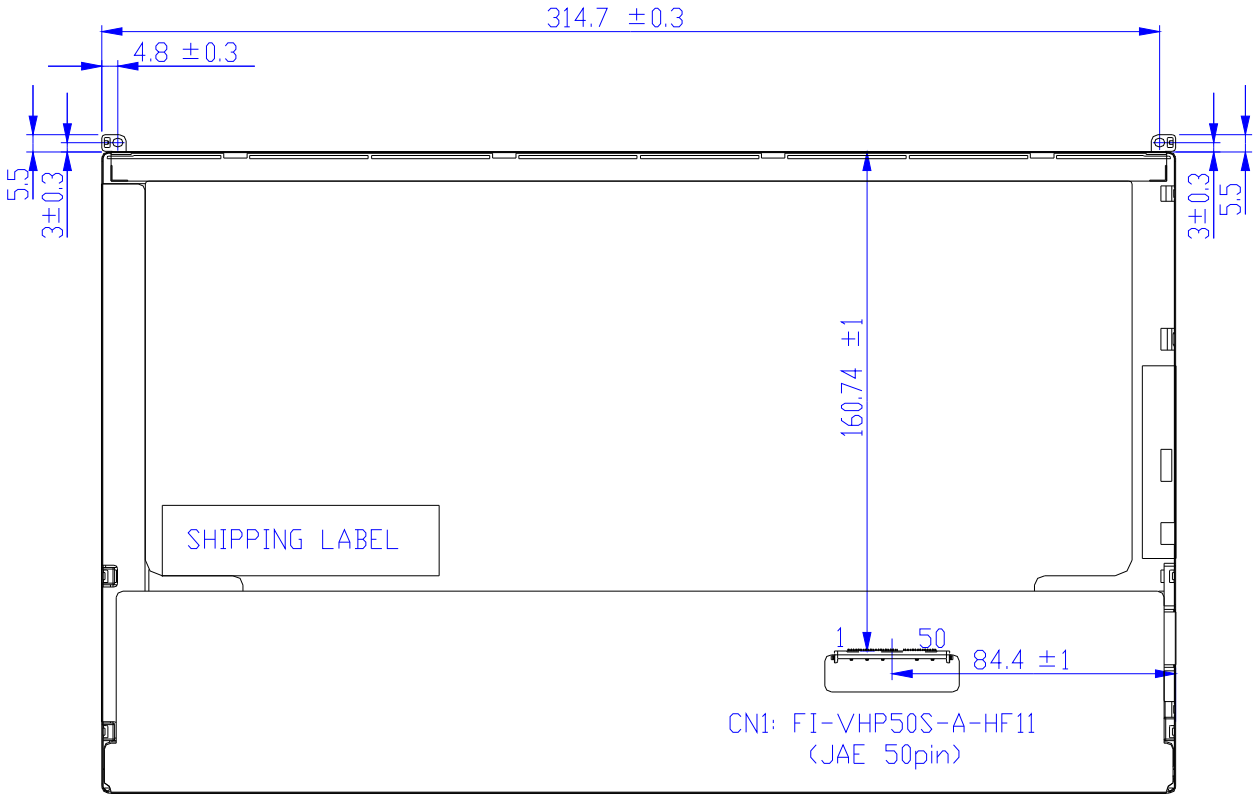
6.3 Integration Interface and Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

1	Test Loop	Test Loop (only to pin 30)
2	VEEDID	EDID 3.3V power
3	VSS	Ground (Panel logic, BL logic)
4	CLK EEDID	EDID clock
5	DATA EEDID	EDID data
6	VSS	Ground (Panel logic, BL logic)
7	Odd_Rin0-	- LVDS differential data input (R0-R5, G0)
8	Odd_Rin0+	+ LVDS differential data input (R0-R5, G0)
9	VSS1	Ground – Shield LVDS Ch1
10	Odd_Rin1-	- LVDS differential data input (G1-G5, B0-B1) (odd pixels)
11	Odd_Rin1+	+ LVDS differential data input (G1-G5, B0-B1) (odd pixels)
12	VSS2	Ground – Shield LVDS Ch2
13	Odd_Rin2-	- LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
14	Odd_Rin2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
15	VSS3	Ground – Shield LVDS Ch3
16	Odd_ClkIN-	- LVDS differential clock input (odd pixels)
17	Odd_ClkIN+	+ LVDS differential clock input (odd pixels)
18	VSS4	Ground – Shield LVDS Ch4
19	Even_Rin0-	- LVDS differential data input (R0-R5, G0) (even pixels)
20	Even_Rin0+	+ LVDS differential data input (R0-R5, G0) (even pixels)
21	VSS5	Ground – Shield LVDS Ch5
22	Even_Rin1-	- LVDS differential data input (G1-G5, B0-B1) (even pixels)
23	Even_Rin1+	+ LVDS differential data input (G1-G5, B0-B1) (even pixels)
24	VSS6	Ground – Shield LVDS Ch6
25	Even_Rin2-	- LVDS differential data input (B2-B5, HS, VS, DE) (even pixels)
26	Even_Rin2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (even pixels)
27	VSS7	Ground – Shield LVDS Ch7
28	Even_ClkIN-	- LVDS differential clock input (even pixels)
29	Even_ClkIN+	+ LVDS differential clock input (even pixels)
30	Test Loop	Test Loop (only to pin 1)
31	CONNTST	Connector test (this pin connected to pin 50 only) See note 1
32	VDD	Logic power 3.3V (Panel logic, BL logic)
33	VDD	Logic power 3.3V (Panel logic, BL logic)
34	TEST (BIST_EN)	Panel Self Test

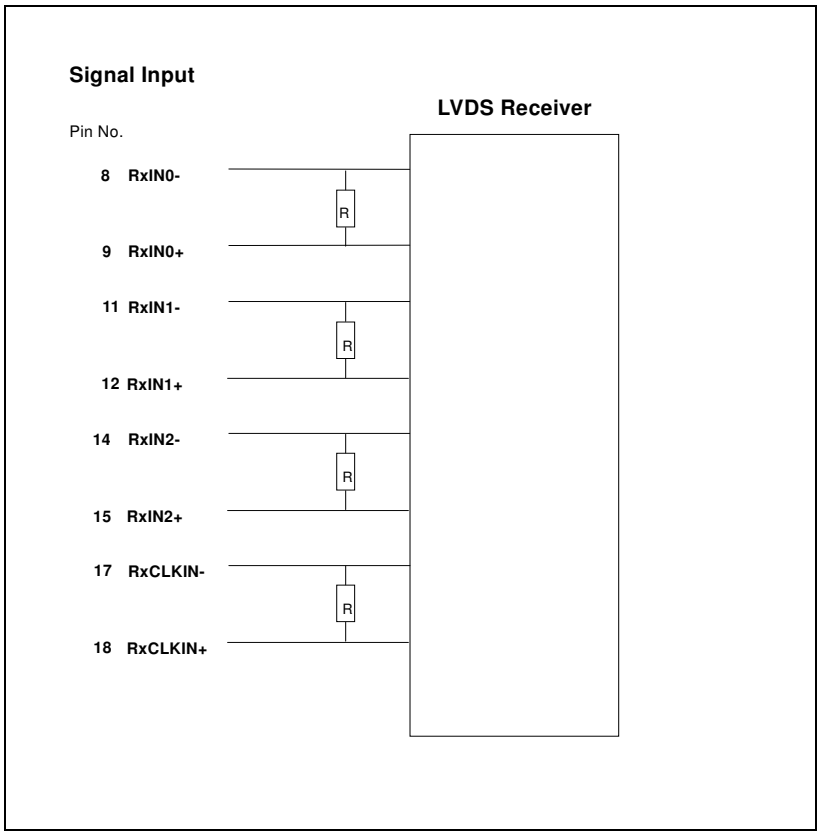
35	+5V_ALW	
36	VSS	
37	VSS	
38	PWM_BL	PWM brightness control
39	VBL-	LED power return
40	VBL-	LED power return
41	VBL-	LED power return
42	VBL-	LED power return
43	NC	no connect
44	VBL+	7V - 20V LED power
45	VBL+	7V - 20V LED power
46	VBL+	7V - 20V LED power
47	VBL+	7V - 20V LED power
48	SMB_DATA	SMBus Data
49	SMB_CLK	SMBus Clk
50	CONNTST	Connector test (this pin to be connected to pin 31 only) See note 1

Note1: Start from right side



Note2: Input signals shall be low or High-impedance state when VDD is off.

internal circuit of LVDS inputs are as following.
The module uses a 100ohm resistor between positive and negative data lines of each receiver input



6.4 Interface Timing

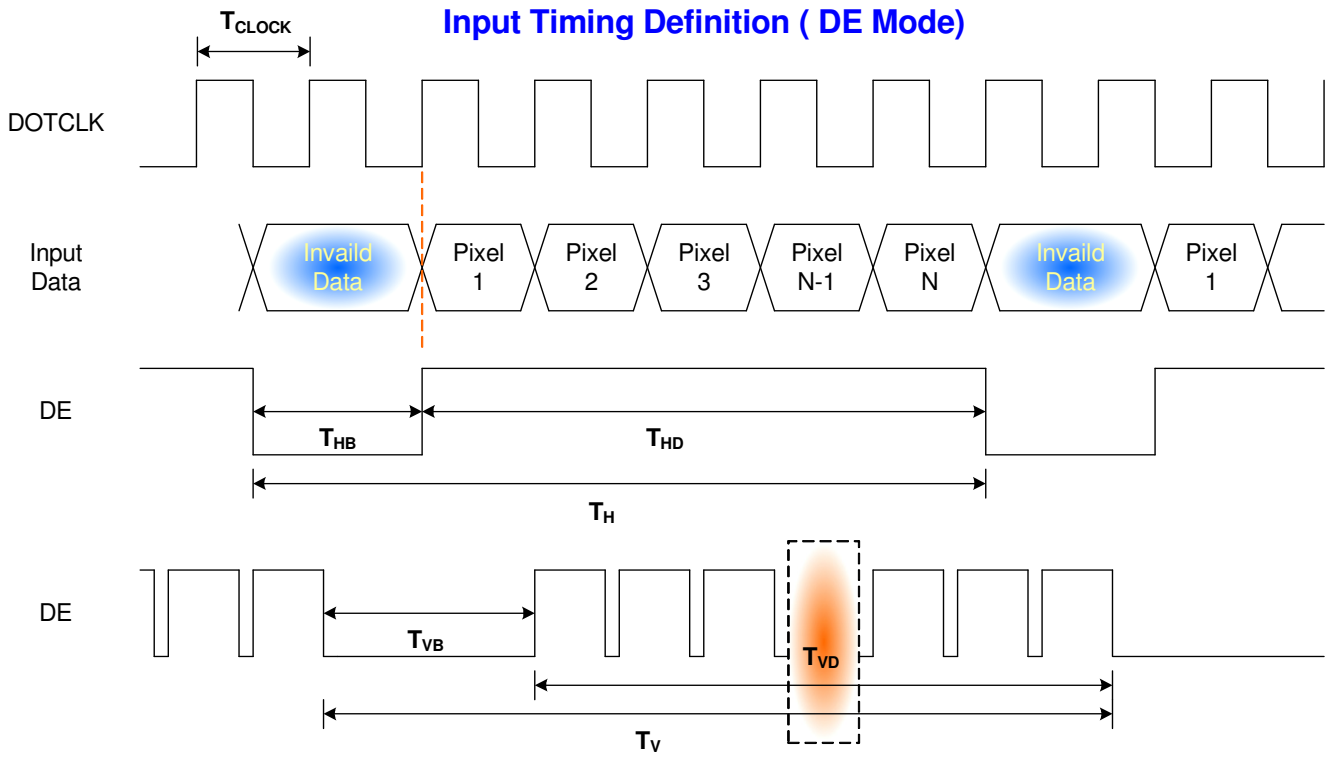
6.4.1 Timing Characteristics

Basically, interface timings should match the 1440x900 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	50	60	-	Hz
Clock frequency		1/ T_{Clock}		48.2	60.2	MHz
Vertical Section	Period	T_V	904	912	2048	T_{Line}
	Active	T_{VD}	900	900	900	
	Blanking	T_{VB}	4	12		
Horizontal Section	Period	T_H	760	880	1024	T_{Clock}
	Active	T_{HD}	720	720	720	
	Blanking	T_{HB}	40	160		

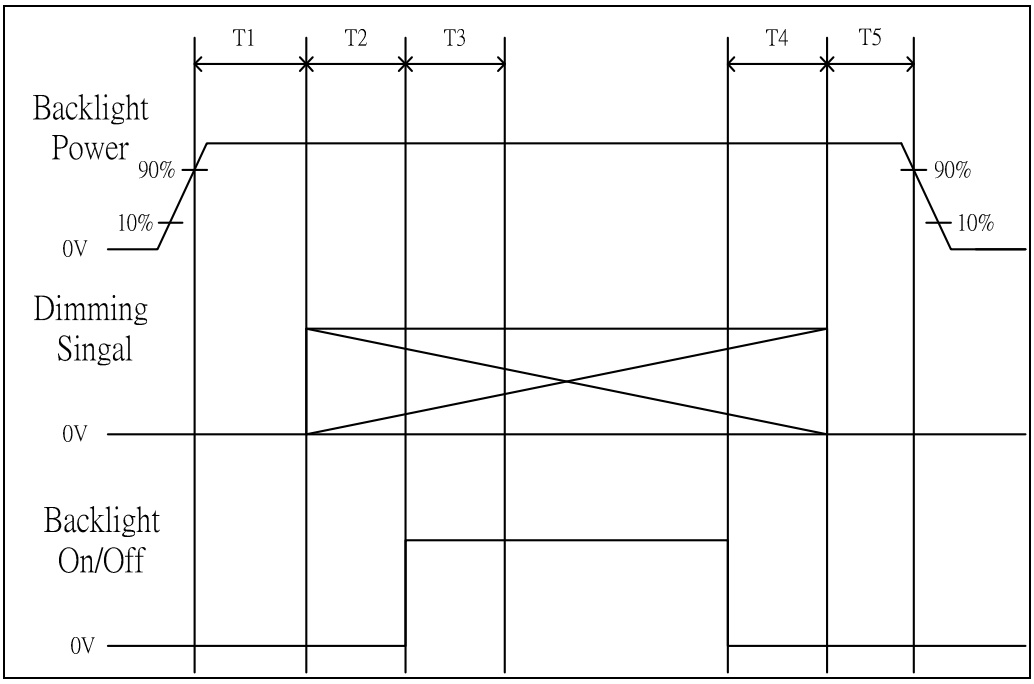
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

LED on/off sequence is as follows. Interface signals are also shown in the chart.



Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)

Note: The duty of LED dimming signal should be more than 20% in T2 and T3.

7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	FI-VHP50S-A-HF11
Mating Housing/Part Number	FI-VHP50C-A

8. LED Driving Specification

8.1 Connector Description

It is a intergrative interface and comibe into LVDS connector. The type and mating refer to section 7.

8.2 Pin Assignment

PIN#	Signal Name	Description
31	CONNTST	Connector test (this pin connected to pin 50 only) See note 1
32	VDD	Logic power 3.3V (Panel logic, BL logic)
33	VDD	Logic power 3.3V (Panel logic, BL logic)
34	TEST (BIST_EN)	Panel Self Test
35	+5V_ALW	
36	VSS	
37	VSS	
38	PWM_BL	PWM brightness control
39	VBL-	LED power return
40	VBL-	LED power return
41	VBL-	LED power return
42	VBL-	LED power return
43	NC	no connect
44	VBL+	7V - 20V LED power
45	VBL+	7V - 20V LED power
46	VBL+	7V - 20V LED power
47	VBL+	7V - 20V LED power
48	SMB_DATA	SMBus Data
49	SMB_CLK	SMBus Clk
50	CONNTST	Connector test (this pin to be connected to pin 31 only) See note 1

9. Vibration and Shock Test

9.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

9.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

10. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 95%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 65℃, 20%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 300h	
Thermal Shock Test	Ta=-40℃to 65℃, Duration at 30 min, 50 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

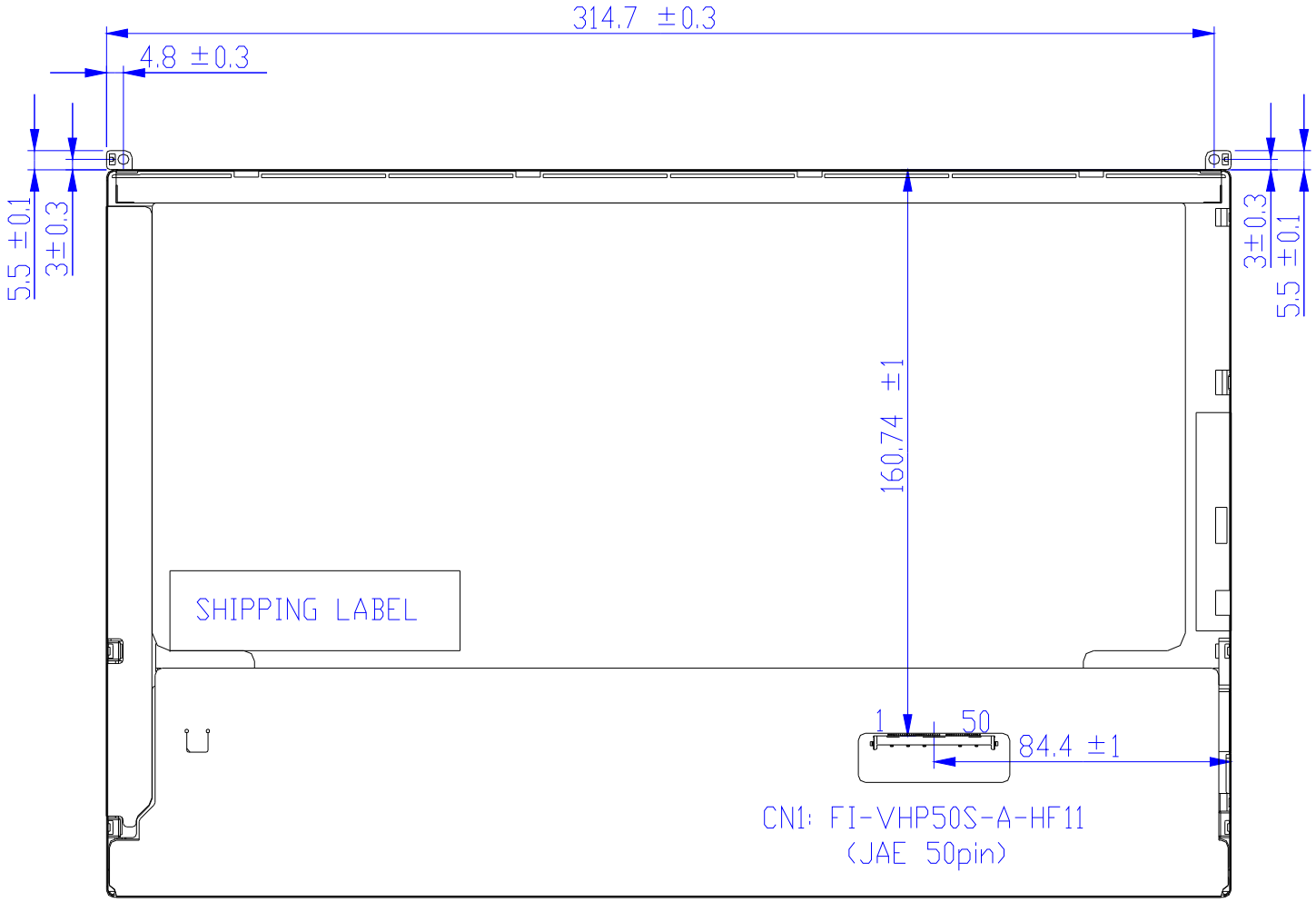
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

. Self-recoverable. No hardware failures.

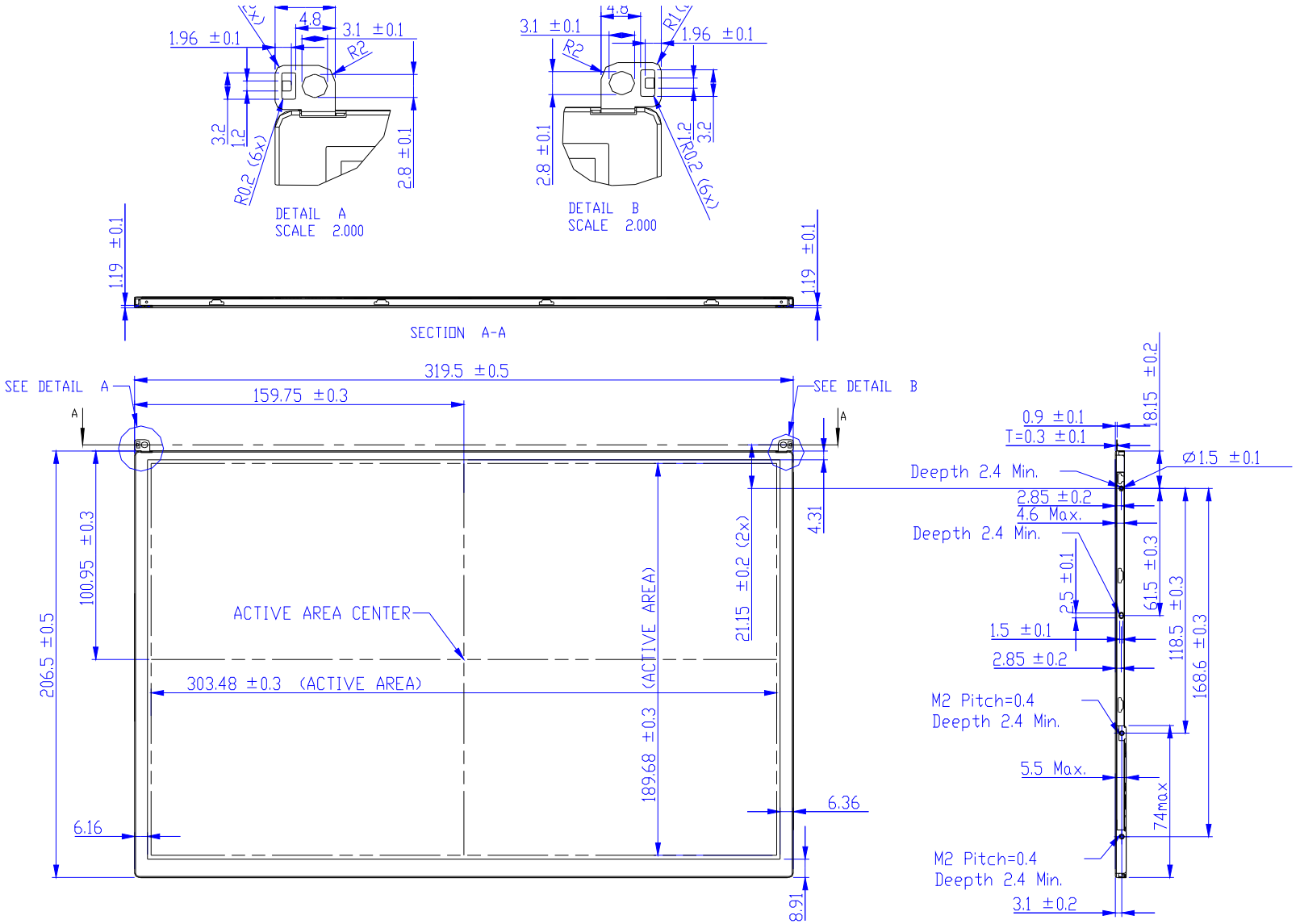
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

11. Mechanical Characteristics

11.1 LCM Outline



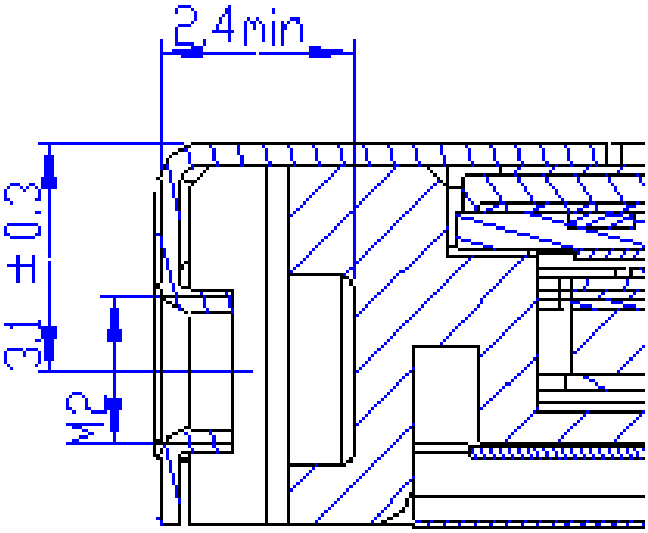
Dimension


DETAIL A
SCALE 2.000
DETAIL B
SCALE 2.000
SECTION A-A
SEE DETAIL A
SEE DETAIL B
319.5 ±0.5
159.75 ±0.3
206.5 ±0.5
100.95 ±0.3
ACTIVE AREA CENTER
303.48 ±0.3 (ACTIVE AREA)
189.68 ±0.3 (ACTIVE AREA)
21.15 ±0.2 (2x)
4.31
6.36
6.16
8.91
Deepth 2.4 Min.
2.85 ±0.2
4.6 Max.
2.5 ±0.1
1.5 ±0.1
M2 Pitch=0.4
5.5 Max.
74max
3.1 ±0.2
18.15 ±0.2
0.9 ±0.1
T=0.3 ±0.1
Ø1.5 ±0.1
61.5 ±0.3
118.5 ±0.3
168.6 ±0.3

11.2 Screw Hole Depth and Center Position

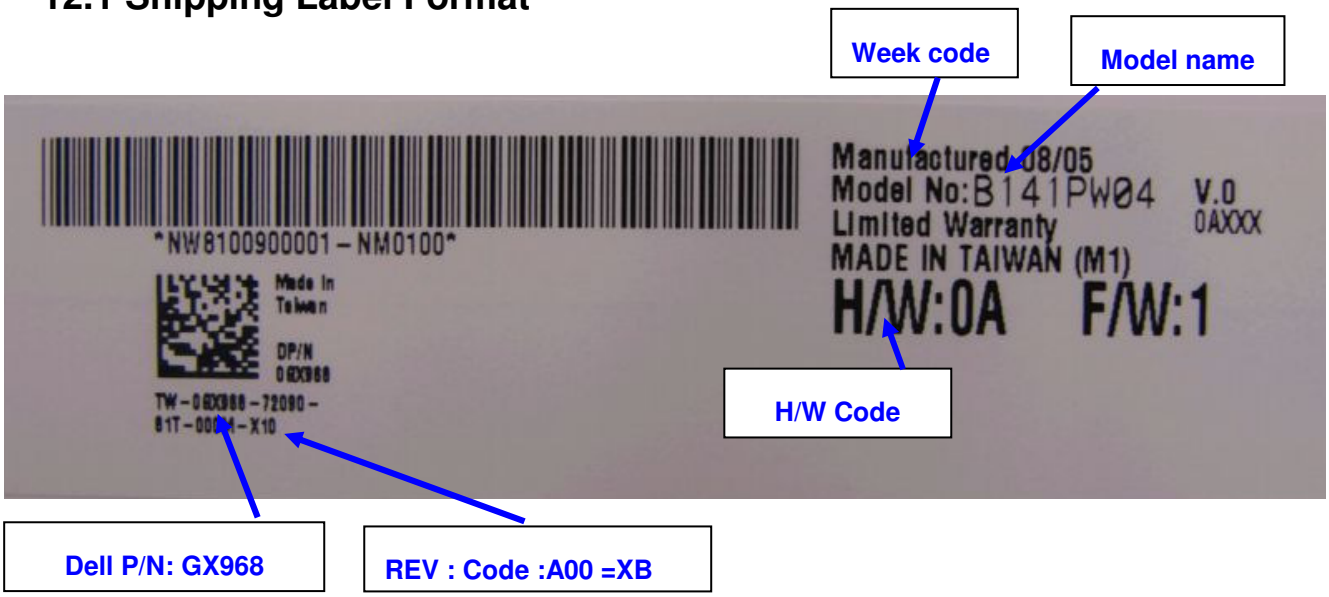
Screw hole minimum depth, from side surface = 2.4 mm (See drawing)

Screw hole center location, from front surface = 3.1 ± 0.3mm (See drawing)
Screw Torque: Maximum 2.5 kgf-cm



12. Shipping and Package

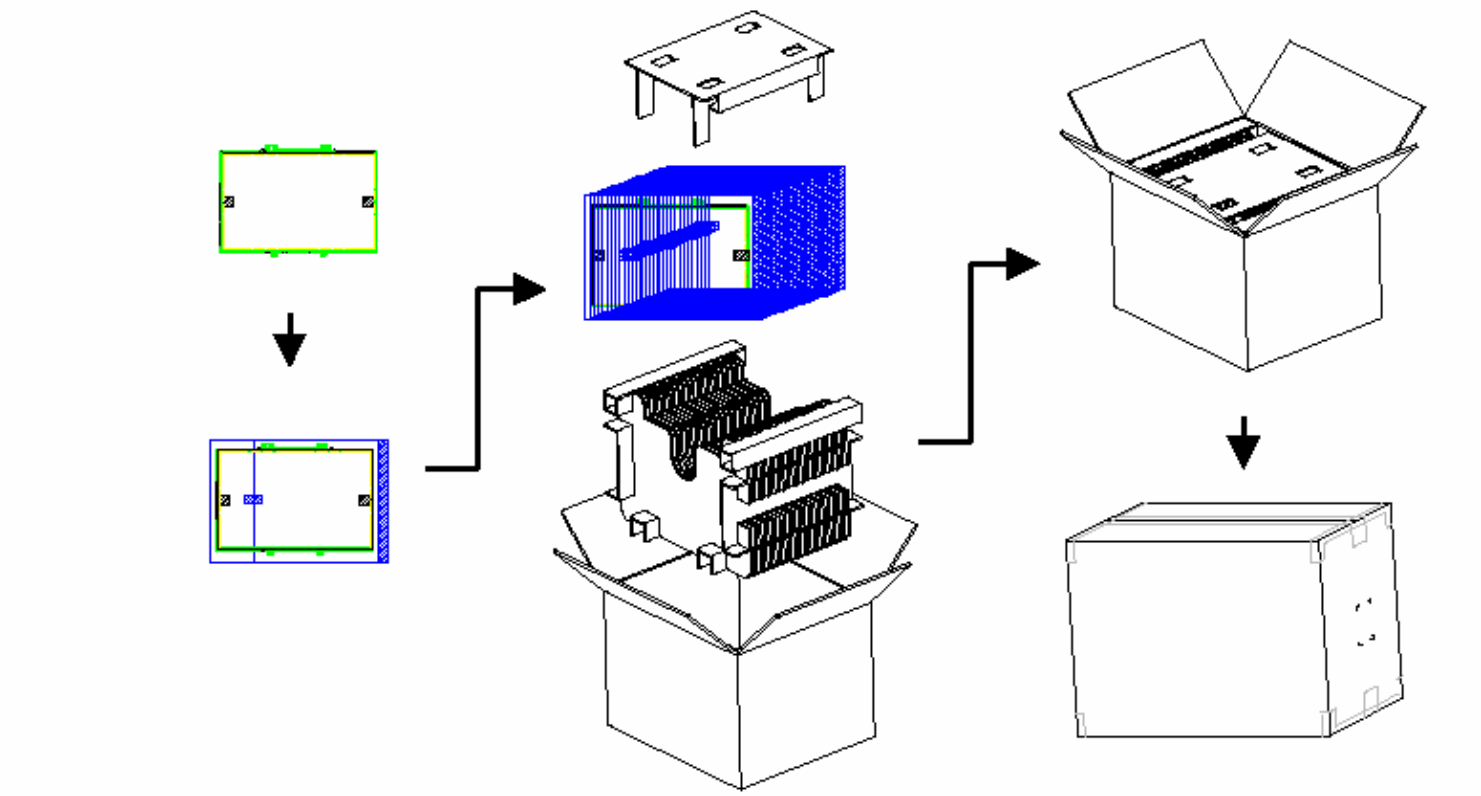
12.1 Shipping Label Format

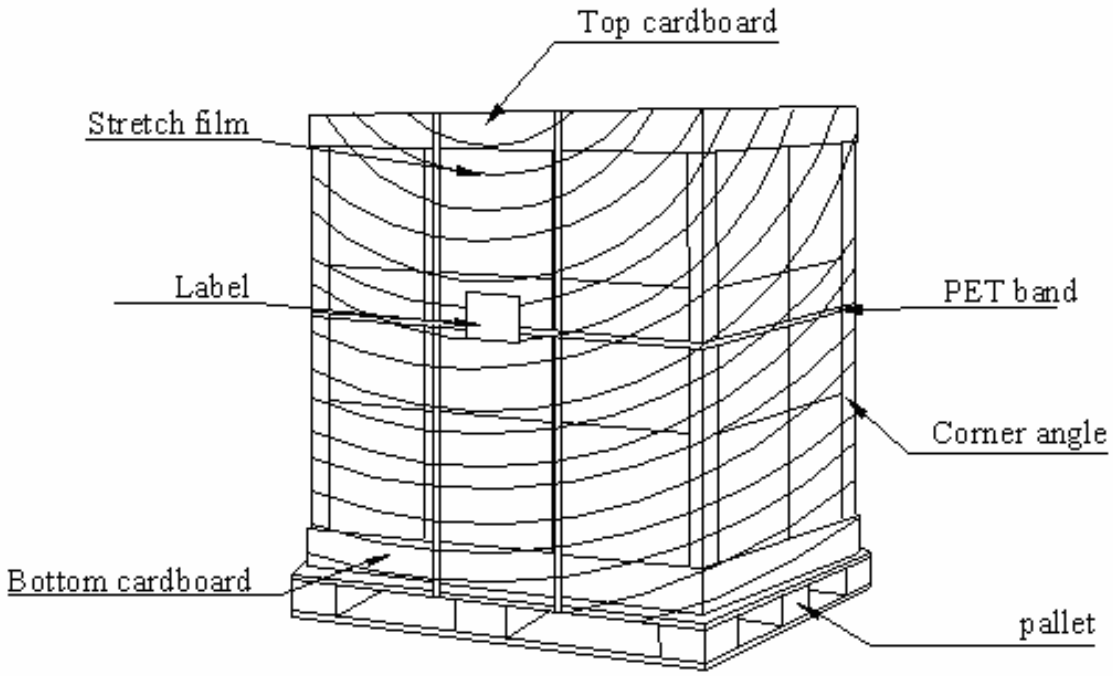


Build Name(s)	Revision Code(s)
SST (WS)	X00, X01, X02, … X09
PT (ES)	X10, X11, X12, … X19
ST (CS)	X20, X21, X23, … X29
XB (MP)	A00, A01, A02, … A99

12.2 Carton package

The outside dimension of carton is 412 (L)mm x 377 (W)mm x 307 (H)mm





13. Appendix: EDID description

Byte (hex)	Field Name and Comments	Value (hex)
0	Header	00
1	Header	FF
2	Header	FF
3	Header	FF
4	Header	FF
5	Header	FF
6	Header	FF
7	Header	00
8	EISA manufacture code = 3 Character ID	06
9	EISA manufacture code (Compressed ASCII)	AF
0A	Panel Supplier Reserved – Product Code	47
0B	Panel Supplier Reserved – Product Code	40
0C	LCD module Serial No - Preferred but Optional (“0” if not used)	00
0D	LCD module Serial No - Preferred but Optional (“0” if not used)	00
0E	LCD module Serial No - Preferred but Optional (“0” if not used)	00
0F	LCD module Serial No - Preferred but Optional (“0” if not used)	00
10	Week of manufacture	01
11	Year of manufacture	11
12	EDID structure version # = 1	01
13	EDID revision # = 3	03
14	Video I/P definition = Digital I/P (80h)	90
15	Max H image size = cm(Rounded to cm)	1E
16	Max V image size = cm(Rounded to cm)	13
17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120	78
18	Feature support (no DPMS, Active off, RGB, timing BLK 1)	0A
19	Red/Green Low bit (RxRy/GxGy)	89
1A	Blue/White Low bit (BxBy/WxWy)	E5
1B	Red X Rx =	94
1C	Red Y Ry =	57
1D	Green X Gx =	54
1E	Green Y Gy =	93
1F	Blue X Bx =	27
20	Blue Y By =	22
21	White X Wx =	50
22	White Y Wy =	54
23	Established timings 1 (00h if not used)	00
24	Established timings 2 (00h if not used)	00
25	Manufacturer’s timings (00h if not used)	00

26	Standard timing ID1 (01h if not used)	01
27	Standard timing ID1 (01h if not used)	01
28	Standard timing ID2 (01h if not used)	01
29	Standard timing ID2 (01h if not used)	01
2A	Standard timing ID3 (01h if not used)	01
2B	Standard timing ID3 (01h if not used)	01
2C	Standard timing ID4 (01h if not used)	01
2D	Standard timing ID4 (01h if not used)	01
2E	Standard timing ID5 (01h if not used)	01
2F	Standard timing ID5 (01h if not used)	01
30	Standard timing ID6 (01h if not used)	01
31	Standard timing ID6 (01h if not used)	01
32	Standard timing ID7 (01h if not used)	01
33	Standard timing ID7 (01h if not used)	01
34	Standard timing ID8 (01h if not used)	01
35	Standard timing ID8 (01h if not used)	01
36	Pixel Clock/10,000 (LSB)	30
37	Pixel Clock/10,000 (MSB)	2A
38	Horizontal Active = pixels (lower 8 bits)	A0
39	Horizontal Blanking (Thbp) = 320 pixels (lower 8 bits)	12
3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	52
3B	Vertical Active = lines	84
3C	Vertical Blanking (Tvbp) = lines (DE Blanking typ. for DE only panels)	0C
3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30
3E	Horizontal Sync, Offset (Thfp) = pixels	40
3F	Horizontal Sync, Pulse Width = pixels	20
40	Vertical Sync, Offset (Tvfp) = lines Sync Width = lines	33
41	Horizontal Vertical Sync Offset/Width upper 2 bits	00
42	Horizontal Image Size = mm	2F
43	Vertical image Size = mm	BD
44	Horizontal Image Size / Vertical image size	10
45	Horizontal Border = 0 (Zero for Notebook LCD)	00
46	Vertical Border = 0 (Zero for Notebook LCD)	00
47	if display uses standard blanking (HSyncPolarity = POS, VSyncPolarity = NEG) , for DVD compliance.	1A
48	Pixel Clock/10,000 (LSB)	52
49	Pixel Clock/10,000 (MSB)	1C
4A	Horizontal Active = xxxx pixels (lower 8 bits)	A0
4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	12
4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	52
4D	Vertical Active = xxxx lines	84
4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	0C

4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30
50	Horizontal Sync, Offset (Thfp) = xxxx pixels	40
51	Horizontal Sync, Pulse Width = xxxx pixels	20
52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	33
53	Horizontal Vertical Sync Offset/Width upper 2 bits	00
54	Horizontal Image Size =xxx mm	2F
55	Vertical image Size = xxx mm	BD
56	Horizontal Image Size / Vertical image size	10
57	Horizontal Border = 0 (Zero for Notebook LCD)	00
58	Vertical Border = 0 (Zero for Notebook LCD)	00
59	if display uses standard blanking (HSyncPolarity = POS, VSyncPolarity = NEG) , for DVD compliance.	1A
5A	Flag	00
5B	Flag	00
5C	Flag	00
5D	Dummy Descriptor	FE
5E	Flag	00
5F	Dell P/N 1st Character : G	47
60	Dell P/N 2nd Character : X	58
61	Dell P/N 3rd Character : 9	39
62	Dell P/N 4th Character : 6	36
63	Dell P/N 5th Character : 8	38
64	EEDID Revision = A00	80
65	Manufacturer P/N	42
66	Manufacturer P/N	31
67	Manufacturer P/N	34
68	Manufacturer P/N	31
69	Manufacturer P/N	50
6A	Manufacturer P/N	57
6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	34
6C	Flag	00
6D	Flag	00
6E	Flag	00
6F	Data Type Tag:	00
70	Flag	00
71	SMBUS Value = nits	00
72	SMBUS Value = nits	00
73	SMBUS Value = nits	00
74	SMBUS Value = nits	00
75	SMBUS Value = nits	00
76	SMBUS Value = nits	00

77	SMBUS Value = nits	00
78	SMBUS Value = nits	00
79	Bit[1:0] 00: reserved, 01: single LVDS, 10: dual LVDS, 11: reserved Bit[2] 0: No RTC support, 1: RTC support Bit[7:3] Reserved	02
7A	Bit[0] 0: No BIST support, 1: BIST support Bit[7:1] Reserved	01
7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A
7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20
7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20
7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00
7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	CE