(V) Preliminary Specifications
( ) Final Specifications

Module	15.4” WXGA+ Color TFT-LCD
Model Name	B154EW02 V3
Dell P/N	GR452
Inverter	Foxconn+MPS(3A)

Customer	**Date**	**Approved by**	**Date**
Checked & Approved by		**Prepared by**	
Note: This Specification is subject to change without notice.		MDBU Marketing Division / AU Optronics corporation	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.0 2006/05/22	All	First Edition for Customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(, IEC60950 or UL1950), or be applied exemption.
14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit(IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.

2. General Description

B154EW02 V3 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WXGA (1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver). All input signals are LVDS interface compatible. Inverter of backlight is not included.

B154EW02 V3 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications
Screen Diagonal	[mm]	391 (15.4W")
Active Area	[mm]	331.2 X 207.0
Pixels H x V		1280x3(RGB) x 800
Pixel Pitch	[mm]	0.2588X0.2588
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance (I_{CCFL}=6.0mA) Note: I_{CCFL} is lamp current	[cd/m^2]	220 typ. (5 points average) 200 min. (5 points average) (Note1)
Luminance Uniformity		1.25 max. (5 points)
Contrast Ratio		400 typ 300 min.
Optical Rise Time/Fall Time	[msec]	4/12 typ.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Power Consumption	[Watt]	6.0 max.(without inverter)
Weight	[Grams]	525 typ. 550 max.
Physical Size	[mm]	344.0 typ. x 222.0 typ. x 6.1 max.
Electrical Interface		1 channel LVDS
Surface Treatment		Glare, Hardness 3H
Support Color		262K colors (RGB 6-bit)

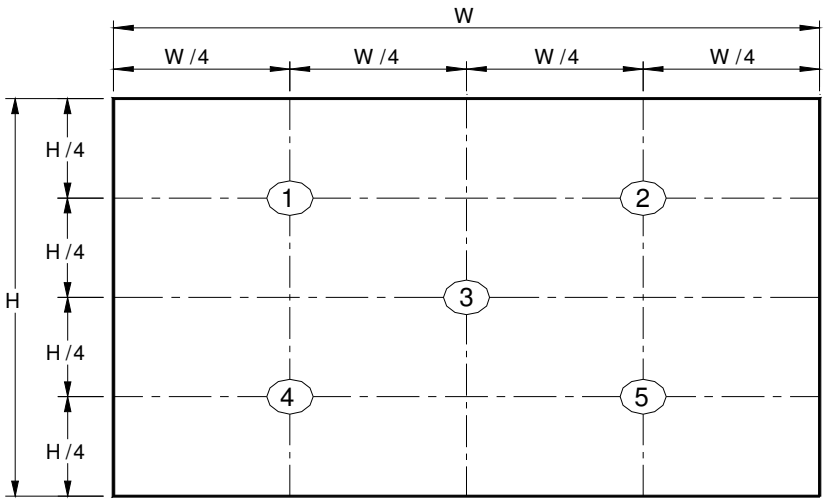
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

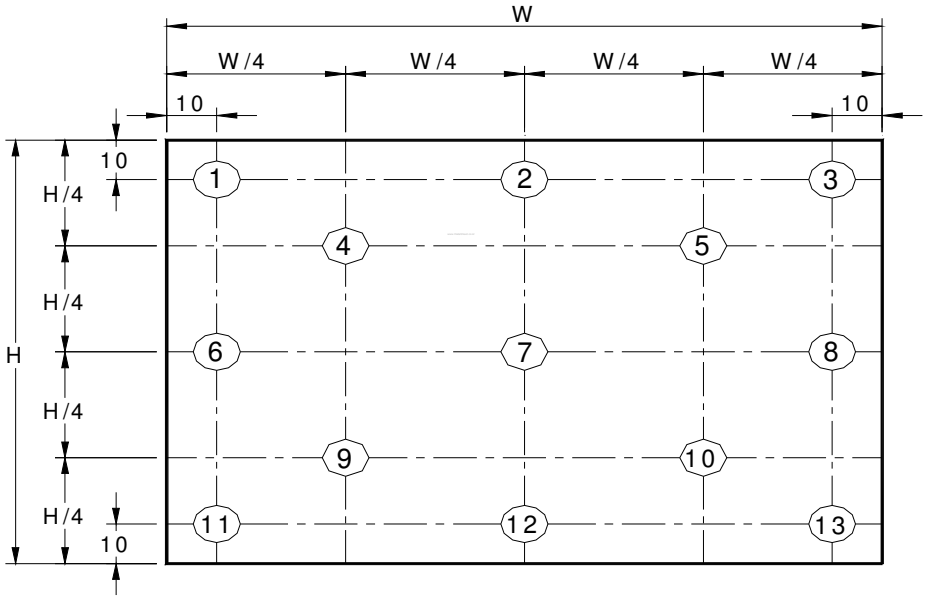
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance I_{CCFL}=6.0mA	[cd/m^2]	5 points average	200	220	-	1, 4, 5.
Viewing Angle	[degree] [degree]	Horizontal (Right) CR = 10 (Left)	- -	45 45	- -	8
	[degree] [degree]	Vertical (Upper) CR = 10 (Lower)	- -	15 35	- -	
Luminance Uniformity		5 Points			1.25	1
Luminance Uniformity		13 Points			1.50	2
CR: Contrast Ratio			300	400	-	6
Cross talk	%				4	7
Response Time	[msec]	Rising	-	4	8	8
	[msec]	Falling	-	12	17	
	[msec]	Rising + Falling		16	25	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.560	0.590	0.620	2,8
		Red y	0.315	0.345	0.375	
		Green x	0.285	0.315	0.345	
		Green y	0.520	0.555	0.585	
		Blue x	0.135	0.155	0.175	
		Blue y	0.135	0.155	0.175	
		White x	0.293	0.313	0.333	
		White y	0.309	0.329	0.349	

Note 1: 5 points position (Display area : 331.2mm x 207.0mm)



Note 2: 13 points position



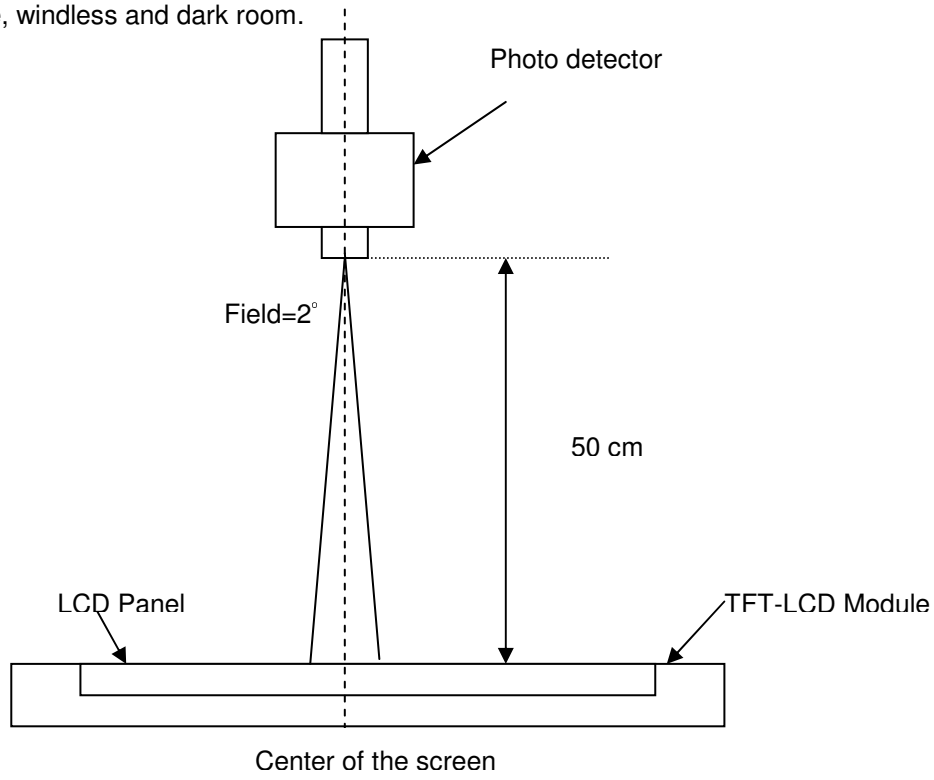
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

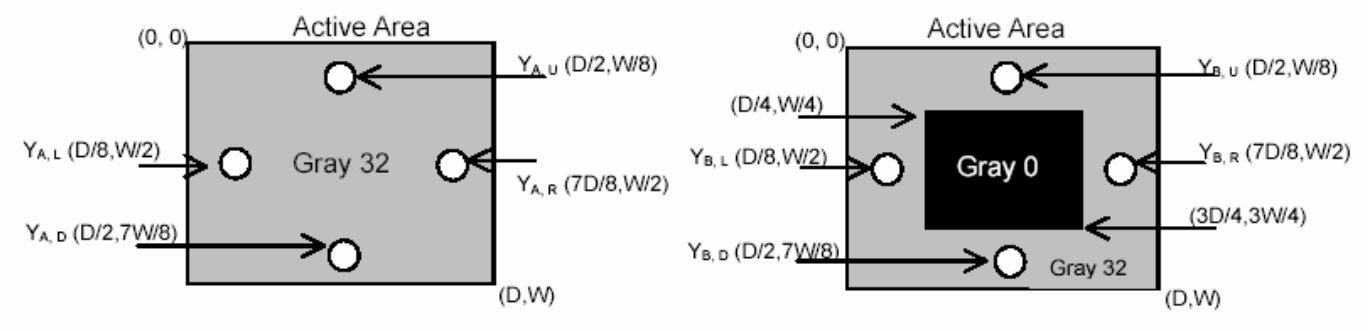
Note 7： Definition of Cross Talk (CT)

$CT = |Y_B - Y_A| / Y_A \times 100\ (\%)$

Where

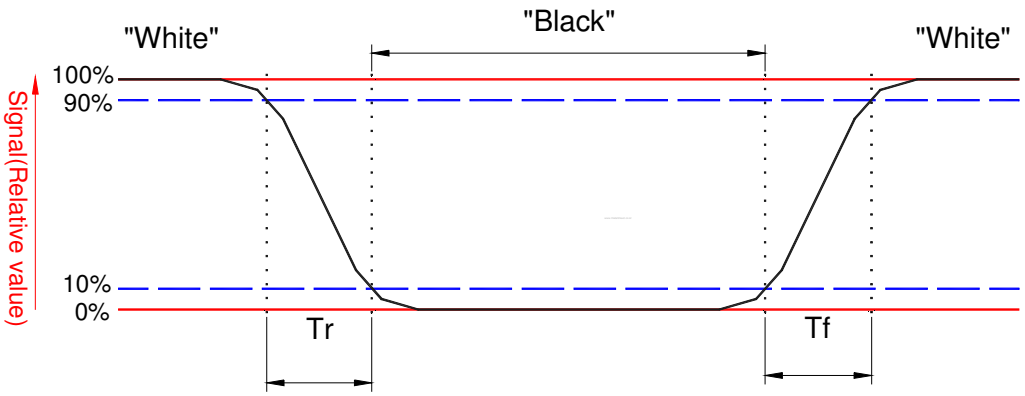
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



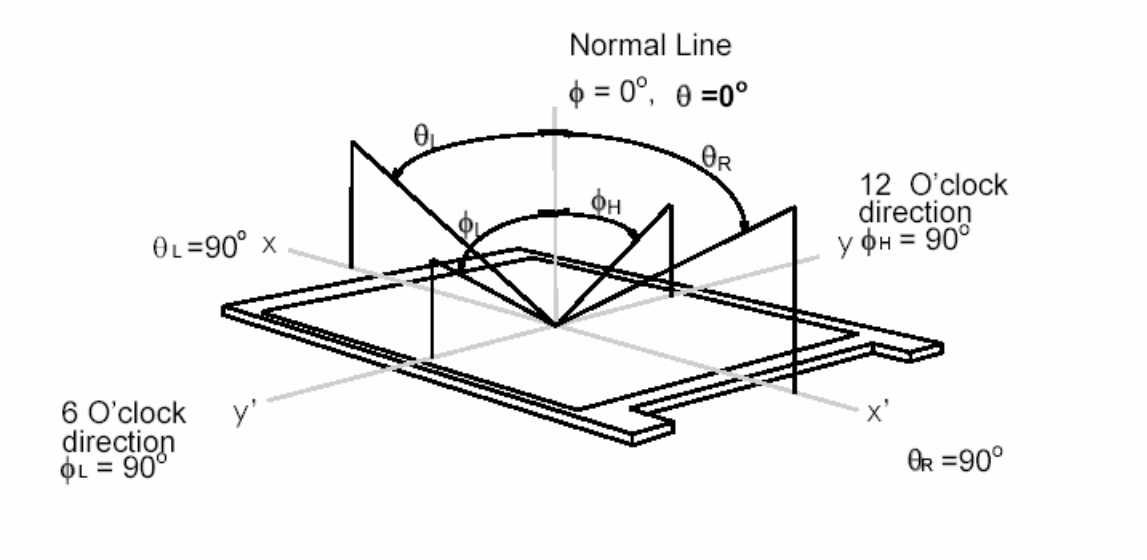
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



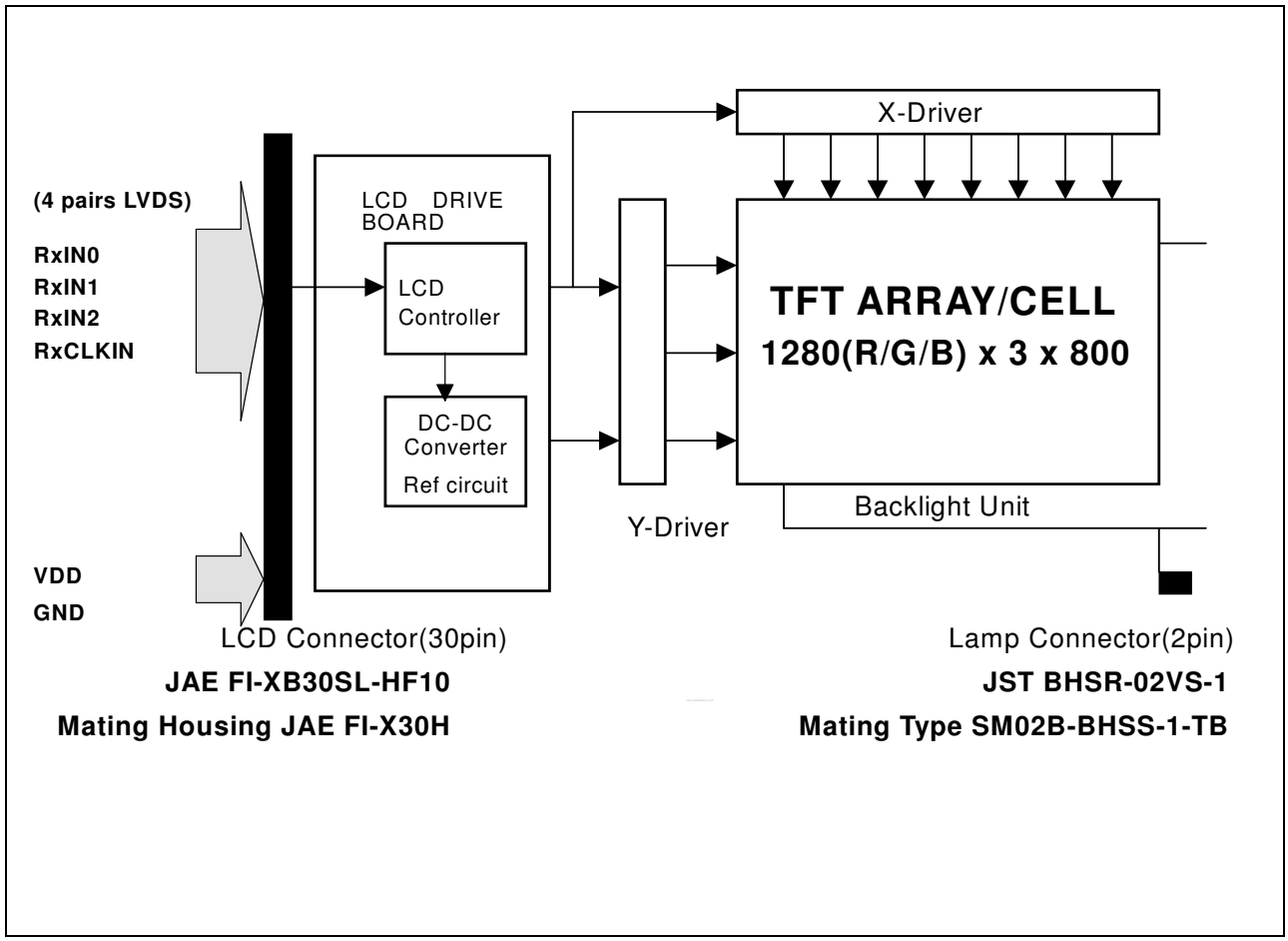
Note 8. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 15.4 inches wide Color TFT/LCD Module:



4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICCFL	-	6.5	[mA] rms	Note 1,2

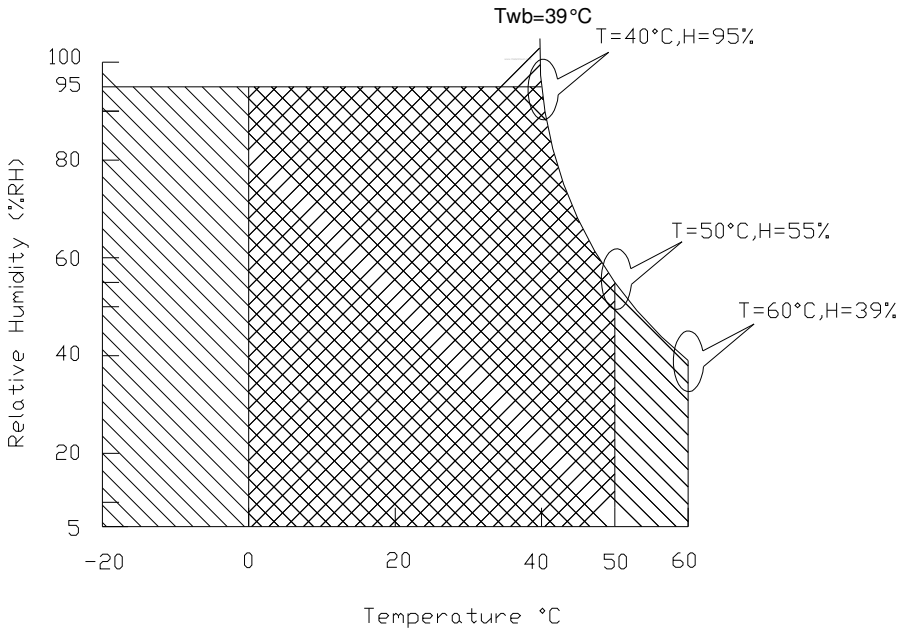
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range Storage Range

5. Electrical characteristics

5.1 TFT LCD Module

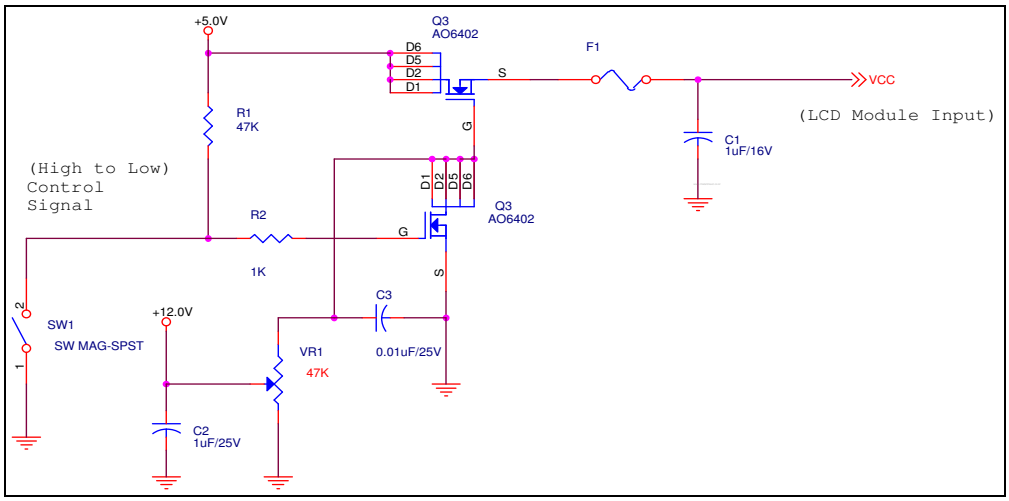
5.1.1 Power Specification

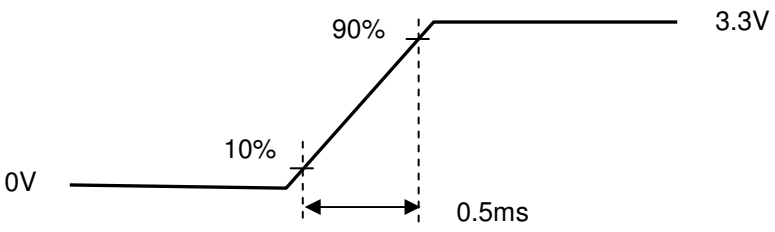
Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power			1.6	[Watt]	Note 1
IDD	IDD Current		350	450	[mA]	Note 1
IRush	Inrush Current			2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Patterm

Note 2：Measure Condition





Vin rising time

5.1.2 Signal Electrical Characteristics

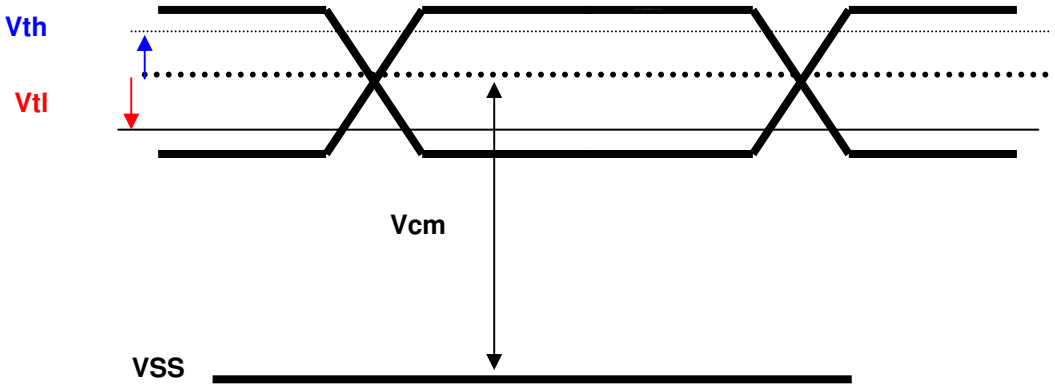
Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of THC63LVDF84A(Thine Electronics Inc.) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]
Vcm	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance 5 points average	200	220	-	[cd/m^2]	(Ta=25℃)
CCFL current(I_{CCFL})	2.0	6.5	7.0	[mA] rms	(Ta=25℃) Note 2
CCFL Frequency(F_{CCFL})	40	62	80	[KHz]	(Ta=25℃) Note 3,4
CCFL Ignition Voltage(Vs)			1750	[Volt] rms	(Ta= 0℃) Note 5
CCFL Ignition Voltage(Vs)			1500	[Volt] rms	(Ta= 25℃) Note 5
CCFL Voltage (Reference) (V_{CCFL})	628	700	792	[Volt] rms	(Ta=25℃) Note 6
CCFL Power consumption (P_{CCFL})	-	4.55	5.25	[Watt]	(Ta=25℃) Note 6
CCFL discharge time(sec)	1				(Ta= 25℃) Note 1*4

Note 1: Typ are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CCFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CCFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has “Duty Dimming”, if ICCFL is less than 4mA.

Note 3: CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

Note 5: CCFL inverter should be able to give out a power that has a generating capacity of over 1,750 voltage. Lamp units need 1,700 voltage for ignition.

Note 6: Calculator value for reference ($I_{CCFL} \times V_{CCFL} = P_{CCFL}$)

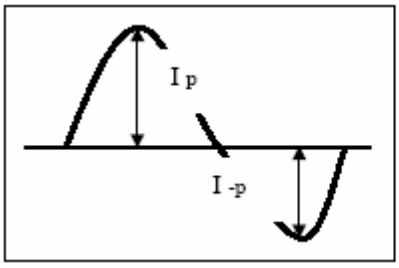
Note 7: Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following.

It shall help increase the lamp lifetime and reduce leakage current.

a. The asymmetry rate of the inverter waveform should be less than 10%.

b. The distortion rate of the waveform should bewithin $\sqrt{2}$ ±10%.

* Inverter output waveform had better be more similar to ideal sine wave.



* Asymmetry rate:

$| I_p - I_{-p} | / I_{rms} * 100\%$

* Distortion rate

I_p (or I_{-p}) / I_{rms}

5.3 Inverter Characteristic

Foxconn with MPS

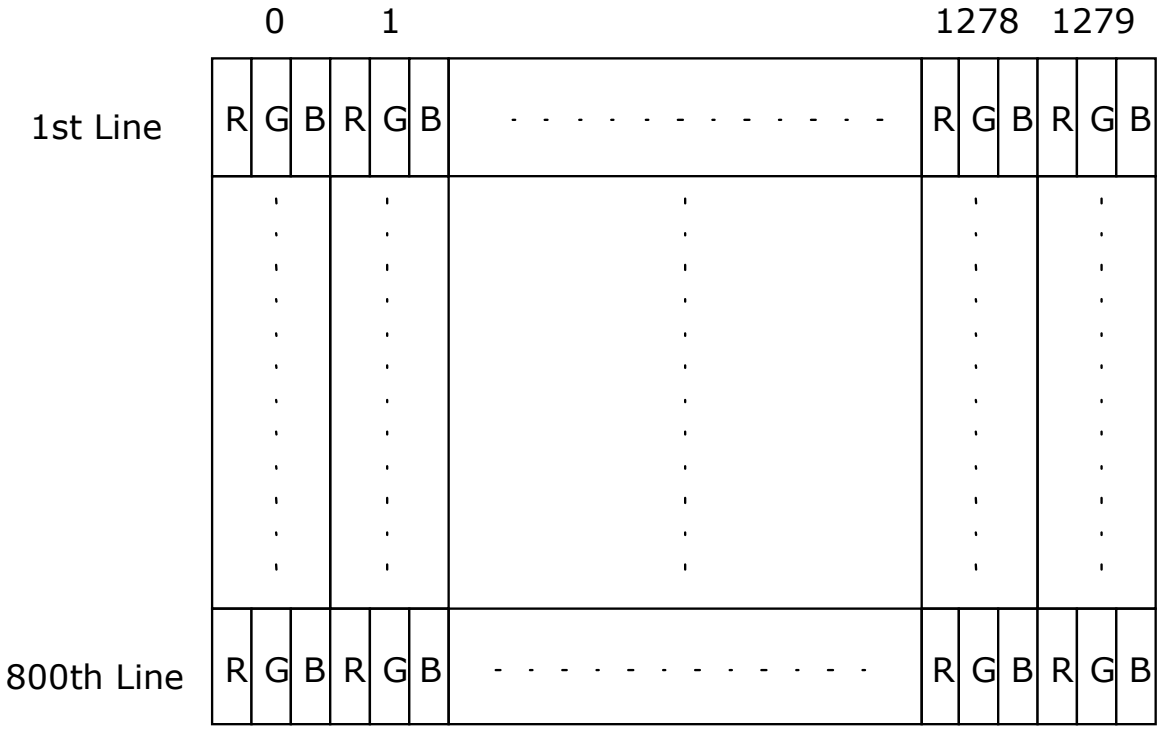
Electrical Characteristics : Vin= 7.5V~21V, Ta=25℃

No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Input Voltage	INV_SRC	-	7.5	14.0	21.0	V
2	Input Voltage	5VALW	-	4.85	-	5.20	V
3	Input Current	Iin	Vin=14.0V, max. output	-	0.420	-	A
4	Input Power	Pin	Vin=14.0V, Iout=6.5mA	-	-	6.20	W
5	Backlight ON/OFF Control(1)	ON	Enable the inverter	2.0	-	5.25	V
		OFF	Disable the inverter	-0.3	-	0.8	V
6	SMBus Mode Brightness Adjust	SMB_DAT	Min. output: 00H Max. output: FFH	00	-	FF	Hex.
7	DPST mode (System side PWM input)	PWM(Hz)	-	-	10	-	KHz
		PWM Voltage	-	3.135	3.30	3.465	V
		Signal intensity	-	00	-	FF	Hex
8	Output Voltage	Vout	Max. output	-	700	-	Vrms
9	Output Current	Iout (Min)	Ta=25℃, after running 30 min.	1.2	1.5	1.8	mArms
		Iout (Max)		6.3	6.5	6.8	mArms
10	Frequency	Freq	Max. output	45	55	65	KHz
11	Output Power	Pout	Vin=14.0V, Iout(Max)	-	4.96	-	W
12	Burst Mode Frequency	f_B		-	200	-	Hz
13	Ambient Light input signal			5	-	1000	Lux
14	Open Lamp Voltage(2)	Vopen	No Load	1400	-	-	Vrms
15	Striking Time	Ts	No Load	0.6	1.0	1.4	Sec
16	Efficiency	η	Vin=7.5V, Max. output, Load=100K	-	80	-	%
17	Start –up time			-	-	0.1	Sec

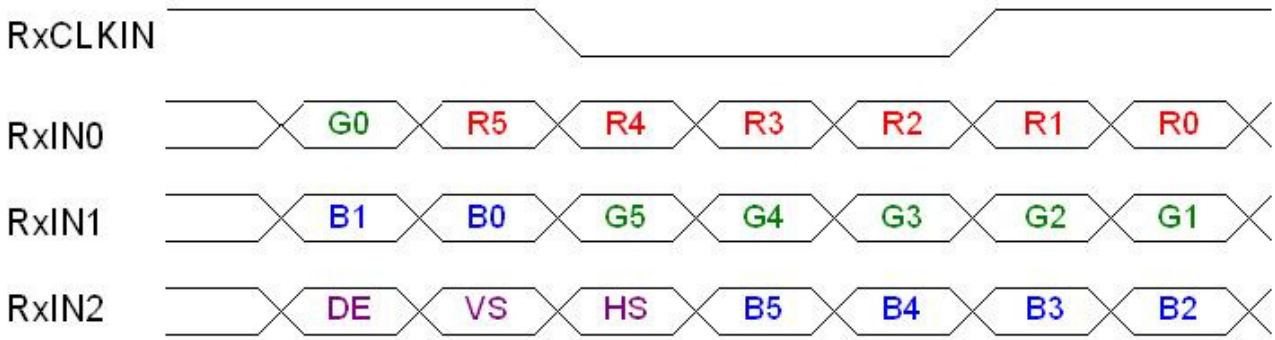
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The typical frequency is 68.9 MHZ.. The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

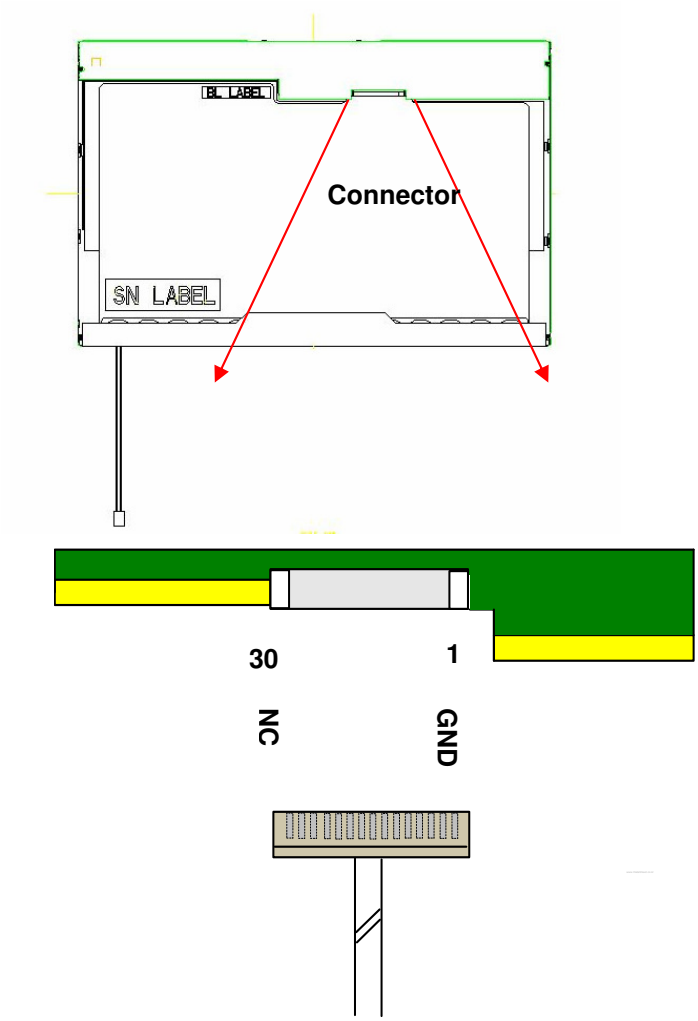
Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Signal Description/Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

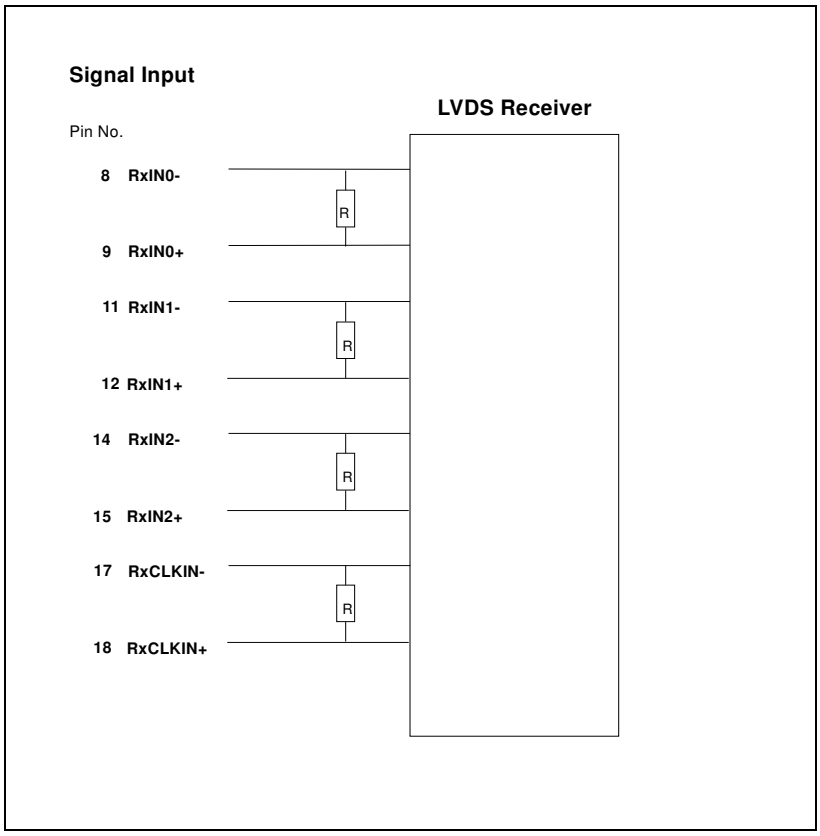
PIN#	Signal Name	Description
1	GND	Ground
2	VDD	+3.3V Power Supply
3	VDD	+3.3V Power Supply
4	V_{EDID}	+3.3V EDID Power
5	NC	No Connection (Reserve for AUO test)
6	CLK_{EDID}	EDID Clock Input
7	$DATA_{EDID}$	EDID Data Input
8	RxIN0-	LVDS differential data input(R0-R5, G0)
9	RxIN0+	LVDS differential data input(R0-R5, G0)
10	GND	Ground
11	RxIN1-	LVDS differential data input(G1-G5, B0-B1)
12	RxIN1+	LVDS differential data input(G1-G5, B0-B1)
13	GND	Ground
14	RxIN2-	LVDS differential data input(B2-B5, HS, VS, DE)
15	RxIN2+	LVDS differential data input(B2-B5, HS, VS, DE)
16	GND	Ground
17	RxCLKIN-	LVDS differential clock input
18	RxCLKIN+	LVDS differential clock input
19	GND	Ground
20	GND	Ground
21	NC	No Connection (Reserve for AUO test)
22	NC	No Connection (Reserve for AUO test)
23	NC	No Connection (Reserve for AUO test)
24	NC	No Connection (Reserve for AUO test)
25	NC	No Connection (Reserve for AUO test)
26	NC	No Connection (Reserve for AUO test)
27	NC	No Connection (Reserve for AUO test)
28	NC	No Connection (Reserve for AUO test)
29	NC	No Connection (Reserve for AUO test)
30	NC	No Connection (Reserve for AUO test)

Note1: Start from right side



Note2: Input signals shall be low or High-impedance state when VDD is off.

internal circuit of LVDS inputs are as following.
The module uses a 100ohm resistor between positive and negative data lines of each receiver input



6.4 Interface Timing

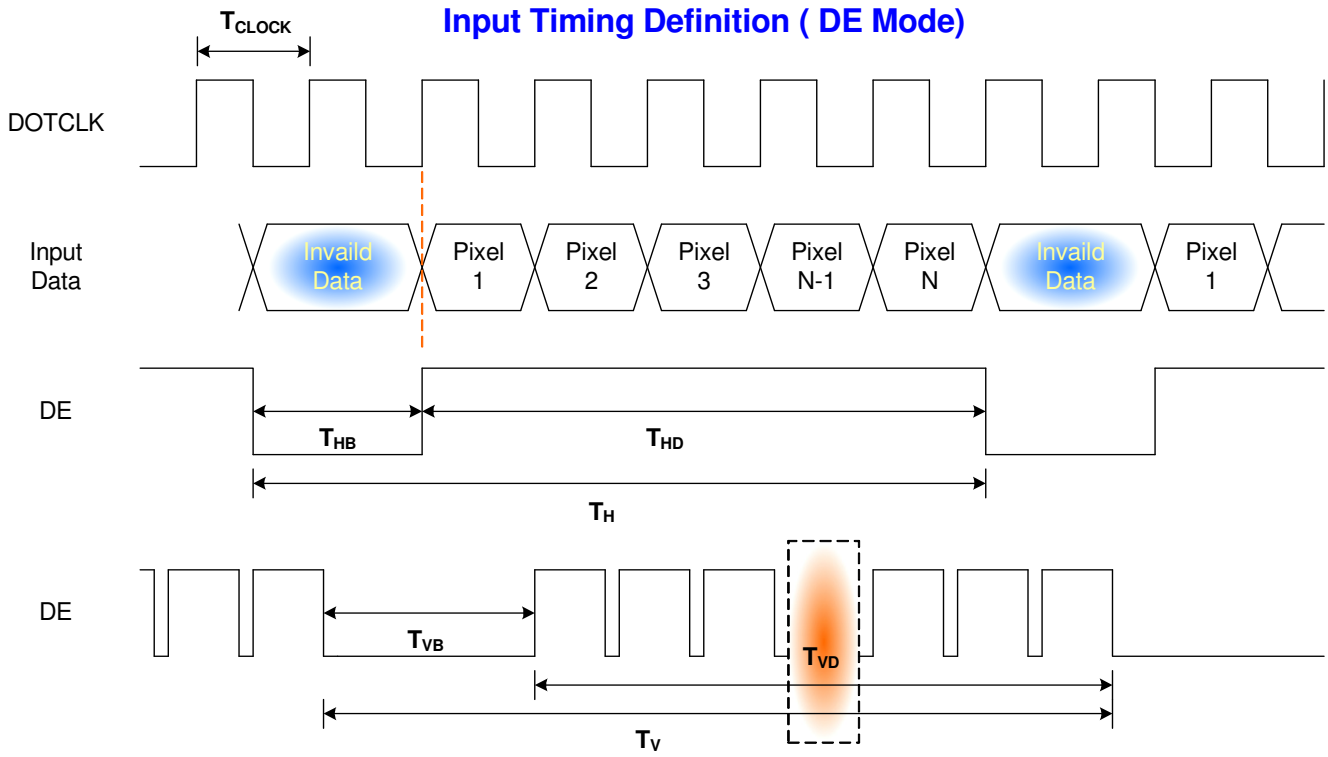
6.4.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	50	60	-	Hz
Clock frequency		$1/T_{Clock}$	50	68.9	80	MHz
Vertical Section	Period	T_V	803	816	1023	T_{Line}
	Active	T_{VD}	800	800	800	
	Blanking	T_{VB}	3	16	223	
Horizontal Section	Period	T_H	1303	1408	2047	T_{Clock}
	Active	T_{HD}	-	1280	-	
	Blanking	T_{HB}	23	128	767	

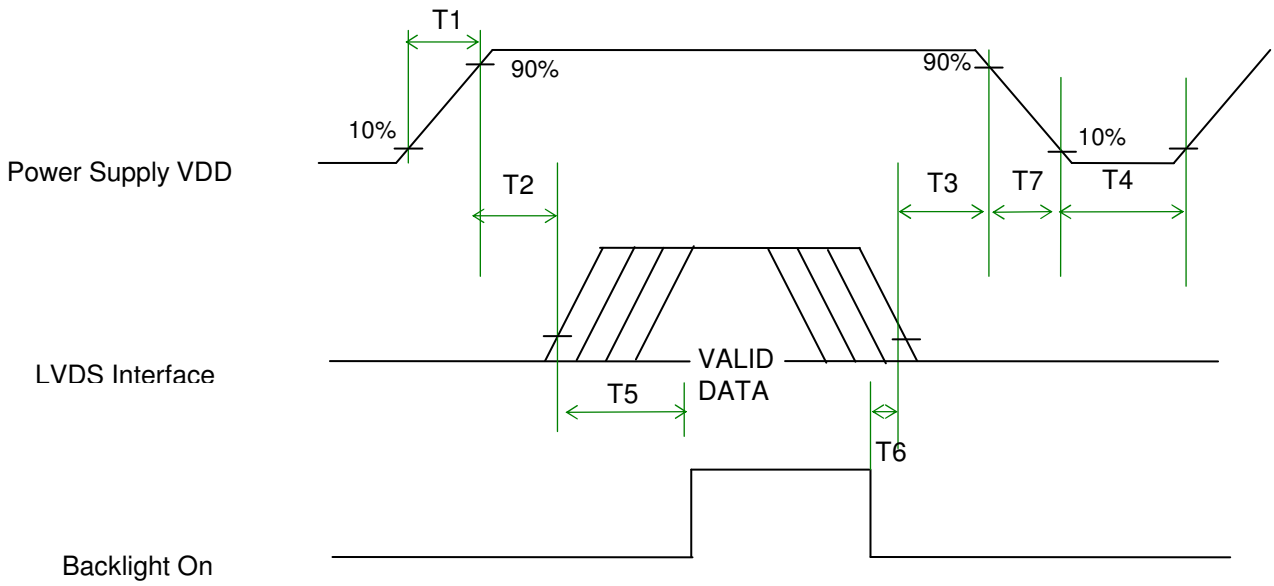
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)

7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or compatible
Type / Part Number	FI-XB30SL-HF10 or compatible
Mating Housing/Part Number	FI-X30H or compatible

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Red	Lamp High Voltage
2	White	Lamp Low Voltage

8. Vibration and Shock Test

8.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.3G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

8.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

9. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	40℃/90%,300Hr	
High Temperature Operation	50℃/Dry,300Hr	
Low Temperature Operation	0℃,300Hr	
On/Off Test	25℃,150hrs(ON/10 sec. OFF/10sec., 10,000 cycles)	
Hot Storage	60℃/35% RH ,250 hours	
Cold Storage	-20℃/50% RH ,250 hours	
Thermal Shock Test	-20℃/30 min ,60℃/30 min 100cycles	
Hot Start Test	50℃/1 Hr min. power on/off per 5 minutes, 5 times	
Cold Start Test	0℃/1 Hr min. power on/off per 5 minutes, 5 times	
Shock Test (Non-Operating)	220G, 2ms, Half-sine wave	
Vibration Test (Non-Operating)	Random vibration, 1.3 G zero-to-peak, 10 to 500 Hz, 30 mins in each of three mutually perpendicular axes.	
ESD	Contact : ±8KV/ operation Air : ±15KV / operation	Note 1
Room temperature Test	25℃, 2000hours, Operating with loop pattern	

Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

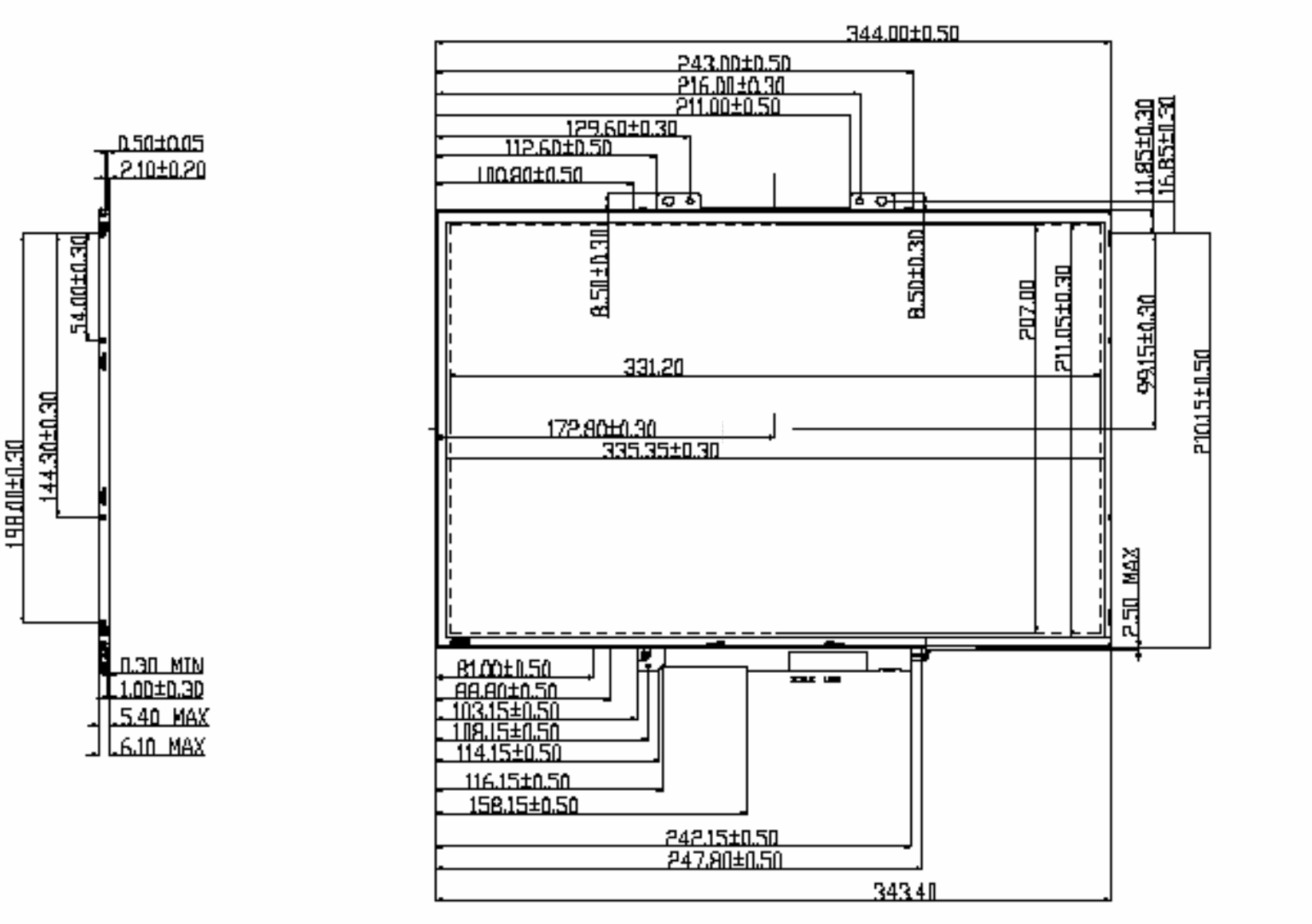
. Self-recoverable. No hardware failures.

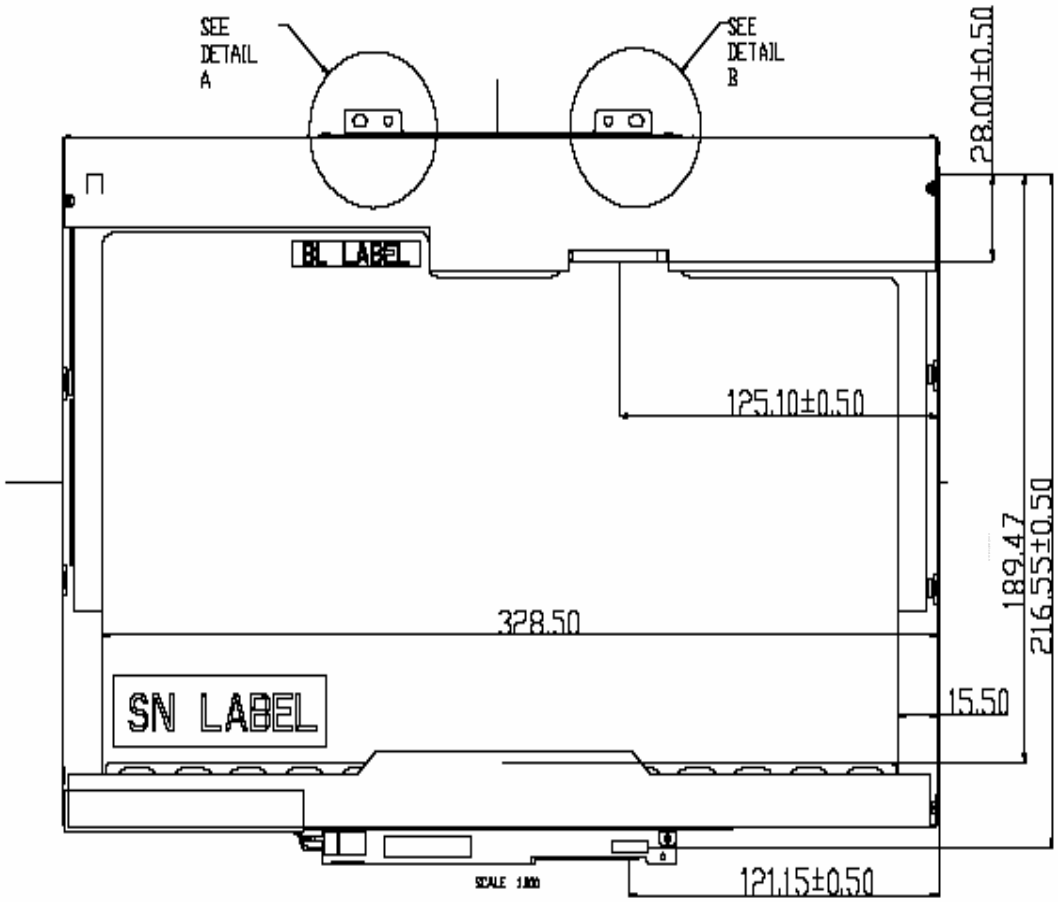
Note2: CCFL Life time: 10,000 hours minimum under normal module usage.

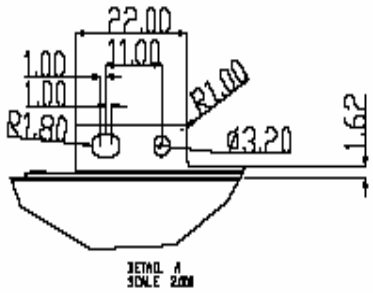
Note3: MTBF (Excluding the CCFL): 30,000 hours with a confidence level 90%

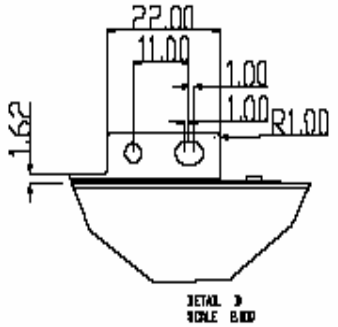
10. Mechanical Characteristics

10.1 LCM Outline Dimension




SEE
DETAIL
A
SEE
DETAIL
B
28.00±0.50
BL LABEL
125.10±0.50
189.47
216.55±0.50
328.50
SN LABEL
15.50
121.15±0.50
SCALE 1.000

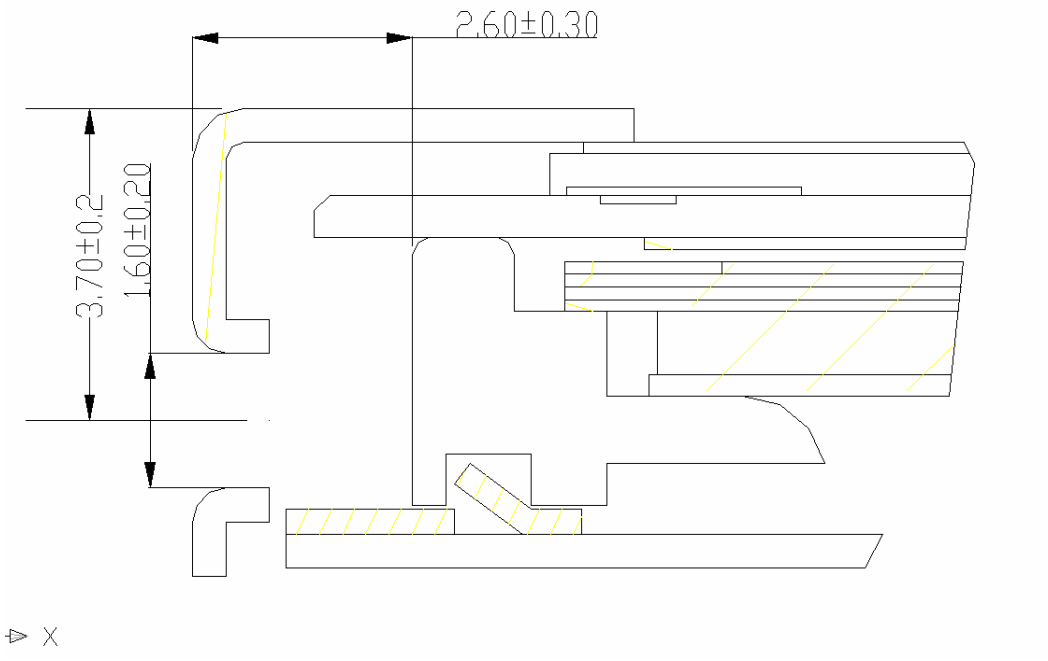

22.00
11.00
1.00
1.00
R1.00
R1.80
Ø3.20
1.62
DETAIL A
SCALE 2.000


22.00
11.00
1.00
1.00
R1.00
1.62
DETAIL B
SCALE 8.000

10.2 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface =2.3 mm (See drawing)

Screw hole center location, from front surface = 3.7 ± 0.2mm (See drawing)
Screw Torque: Maximum 2.5 kgf-cm



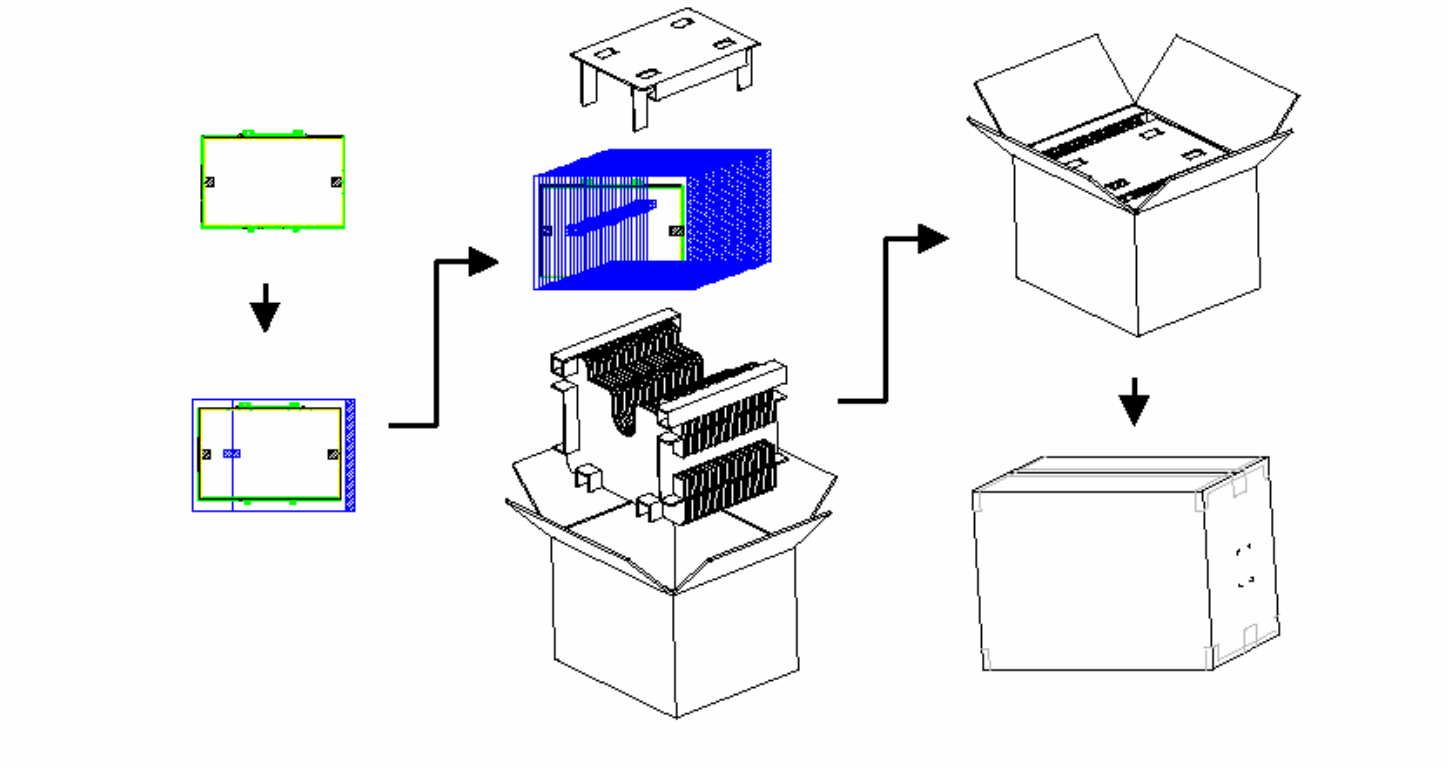
11. Shipping and Package

11.1 Shipping Label Format

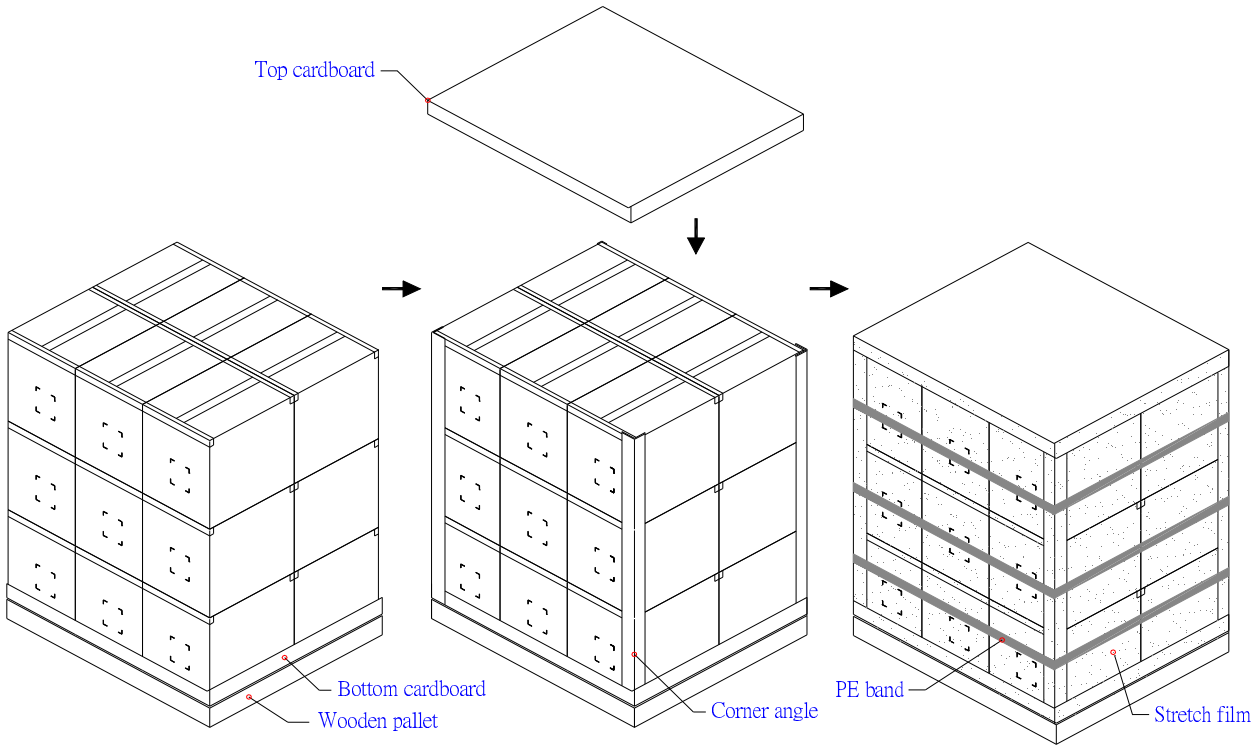
IC Combination	Control Code	H/W
1. Source Novatek Gate IC: Novatek 2. Foxconn with MPS	3AXXG	3A

11.2. Carton package

The outside dimension of carton is 455 (L)mm x 380 (W)mm x 355 (H)mm



11.3 Shipping package of palletizing sequence



Note : Limit of box palletizing = Max 3 layers(ship and stock conditions)

12. Appendix: EDID description

B154EW02 V3(97.15B16.303) EDID Table

	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)	Value (DEC)
Header	0	Header	00	00000000	0
	1	Header	FF	11111111	255
	2	Header	FF	11111111	255
	3	Header	FF	11111111	255
	4	Header	FF	11111111	255
	5	Header	FF	11111111	255
	6	Header	FF	11111111	255
	7	Header	00	00000000	0
Vendor / Product EDID Version	8	EISA manufacture code = 3 Character ID	06	00000110	6
	9	EISA manufacture code (Compressed ASCII)	AF	10101111	175
	0A	Panel Supplier Reserved – Product Code	74	01110100	116
	0B	Panel Supplier Reserved – Product Code	23	00100011	35
	0C	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	0D	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	0E	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	0F	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	10	Week of manufacture	01	00000001	1
	11	Year of manufacture	10	00010000	16
	12	EDID structure version # = 1	01	00000001	1
	13	EDID revision # = 3	03	00000011	3
Display Parameters	14	Video I/P definition = Digital I/P (80h)	80	10000000	128
	15	Max H image size = (Rounded to cm)	21	00100001	33
	16	Max V image size = (Rounded to cm)	15	00010101	21
	17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120	78	01111000	120
	18	Feature support (no DPMS, Active off, RGB, timing BLK 1)	0A	00001010	10
Panel Color Coordinates	19	Red/Green Low bit (RxRy/GxGy)	1C	00011100	28
	1A	Blue/White Low bit (BxBy/WxWy)	F5	11110101	245
	1B	Red X	97	10010111	151
	1C	Red Y	58	01011000	88
	1D	Green X	50	01010000	80
	1E	Green Y	8E	10001110	142
	1F	Blue X	27	00100111	39
	20	Blue Y	27	00100111	39
	21	White X	50	01010000	80
	22	White Y	54	01010100	84
Established Timings	23	Established timings 1 (00h if not used)	00	00000000	0
	24	Established timings 2 (00h if not used)	00	00000000	0
	25	Manufacturer’s timings (00h if not used)	00	00000000	0
Standard Timing ID	26	Standard timing ID1 (01h if not used)	01	00000001	1
	27	Standard timing ID1 (01h if not used)	01	00000001	1
	28	Standard timing ID2 (01h if not used)	01	00000001	1

	29	Standard timing ID2 (01h if not used)	01	00000001	1
	2A	Standard timing ID3 (01h if not used)	01	00000001	1
	2B	Standard timing ID3 (01h if not used)	01	00000001	1
	2C	Standard timing ID4 (01h if not used)	01	00000001	1
	2D	Standard timing ID4 (01h if not used)	01	00000001	1
	2E	Standard timing ID5 (01h if not used)	01	00000001	1
	2F	Standard timing ID5 (01h if not used)	01	00000001	1
	30	Standard timing ID6 (01h if not used)	01	00000001	1
	31	Standard timing ID6 (01h if not used)	01	00000001	1
	32	Standard timing ID7 (01h if not used)	01	00000001	1
	33	Standard timing ID7 (01h if not used)	01	00000001	1
	34	Standard timing ID8 (01h if not used)	01	00000001	1
	35	Standard timing ID8 (01h if not used)	01	00000001	1
Timing Descripter #1	36	Pixel Clock/10,000 (LSB)	C7	11000111	199
	37	Pixel Clock/10,000 (MSB)	1B	00011011	27
	38	Horizontal Active (lower 8 bits)	00	00000000	0
	39	Horizontal Blanking (Thbp) (lower 8 bits)	A0	10100000	160
	3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	50	01010000	80
	3B	Vertical Active	20	00100000	32
	3C	Vertical Blanking (Tvbp) (DE Blanking typ. for DE only panels)	17	00010111	23
	3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000	48
	3E	Horizontal Sync, Offset (Thfp)	30	00110000	48
	3F	Horizontal Sync, Pulse Width	20	00100000	32
	40	Vertical Sync, Offset (Tvfp) Sync Width	36	00110110	54
	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
	42	Horizontal Image Size	4B	01001011	75
	43	Vertical image Size	CF	11001111	207
	44	Horizontal Image Size / Vertical image size	10	00010000	16
	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
	46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
	47	Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives, **DE only note: LSB is set to "1" if panel is DE-timing only. H/V can be ignored.**	19	00011001	25
Timing Descripter #2	48	Pixel Clock/10,000 (LSB)	26	00100110	38
	49	Pixel Clock/10,000 (MSB)	17	00010111	23
	4A	Horizontal Active = xxxx pixels (lower 8 bits)	00	00000000	0
	4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	A0	10100000	160
	4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	50	01010000	80
	4D	Vertical Active = xxxx lines	20	00100000	32
	4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	17	00010111	23

	4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000	48
	50	Horizontal Sync, Offset (Thfp) = xxxx pixels	30	00110000	48
	51	Horizontal Sync, Pulse Width = xxxx pixels	20	00100000	32
	52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	36	00110110	54
	53	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
	54	Horizontal Image Size =xxx mm	4B	01001011	75
	55	Vertical image Size = xxx mm	CF	11001111	207
	56	Horizontal Image Size / Vertical image size	10	00010000	16
	57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
	58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
	59	Module “A” Revision = Example: 00, 01, 02, 03, etc.	00	00000000	0
Timing Descripter #3 Dell specific information	5A	Flag	00	00000000	0
	5B	Flag	00	00000000	0
	5C	Flag	00	00000000	0
	5D	Dummy Descriptor	FE	11111110	254
	5E	Flag	00	00000000	0
	5F	Dell P/N 1st Character	47	01000111	71
	60	Dell P/N 2nd Character	52	01010010	82
	61	Dell P/N 3rd Character	34	00110100	52
	62	Dell P/N 4th Character	35	00110101	53
	63	Dell P/N 5th Character	32	00110010	50
	64	LCD Supplier EEDID Revision #	00	00000000	0
	65	Manufacturer P/N	42	01000010	66
	66	Manufacturer P/N	31	00110001	49
	67	Manufacturer P/N	35	00110101	53
	68	Manufacturer P/N	34	00110100	52
	69	Manufacturer P/N	45	01000101	69
	6A	Manufacturer P/N	57	01010111	87
	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	32	00110010	50
Timing Descripter #4	6C	Flag	00	00000000	0
	6D	Flag	00	00000000	0
	6E	Flag	00	00000000	0
	6F	Data Type Tag:	FE	11111110	254
	70	Flag	00	00000000	0
	71	SMBUS Value	2C	00101100	44
	72	SMBUS Value	3C	00111100	60
	73	SMBUS Value	49	01001001	73
	74	SMBUS Value	52	01010010	82
	75	SMBUS Value	73	01110011	115
	76	SMBUS Value	A1	10100001	161
	77	SMBUS Value	C0	11000000	192
	78	SMBUS Value = max nits (Typically = 00h)	FF	11111111	255
	79	Number of LVDS receiver chips = ‘01’ or ‘02’	01	00000001	1
	7A	BIST Enable: Yes = ‘01’ No = ‘00’	01	00000001	1
	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010	10

	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
Checksum	7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000	0
	7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	4B	01001011	75