



# Product Specification

AU OPTRONICS CORPORATION

- ( V ) Preliminary Specifications
- ( ) Final Specifications

<b>Module</b>	15.4" WSXGA+ Color TFT-LCD
<b>Model Name</b>	B154SW01 V1

Customer	Date
<b>Checked &amp; Approved by</b>	

Note: This Specification is subject to change without notice.

Approved by	Date
<b>Prepared by</b>	

MDBU Marketing Division /  
AU Optronics corporation



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## Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2007/03/02	All	First Edition for Customer		



## 1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
- 13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(, IEC60950 or UL1950), or be applied exemption.
- 14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit(IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.



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## 2. General Description

B154SW01 V1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WSXGA+ (1680(H) x 1050(V)) screen and 262k colors (RGB 6-bits data driver). All input signals are LVDS interface compatible. Inverter of backlight is not included.

B154SW01 V1 is designed for a display unit of notebook style personal computer and industrial machine.

### 2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications
Screen Diagonal	[mm]	390.8 (15.4"W)
Active Area	[mm]	331.38 X 207.11
Pixels H x V		1680 x 3(RGB) x 1050
Pixel Pitch	[mm]	0.19725X0.19725
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance (I <sub>CCFL</sub> =6.0mA) Note: I <sub>CCFL</sub> is lamp current	[cd/m <sup>2</sup> ]	200 typ. (5 points average) 180 min. (5 points average) (Note1)
Luminance Uniformity		1.3 max. (5 points)
Contrast Ratio		400 typ 300 min.
Optical Rise Time/Fall Time	[msec]	6/10 typ.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Power Consumption	[Watt]	2.5 max.
Weight (with Inverter)	[Grams]	585 max.
Physical Size	[mm]	344.0 typ. x 222.0 typ. x 6.5 max.
Electrical Interface		2 channel LVDS
Surface Treatment		Anti-Glare, Hardness 3H



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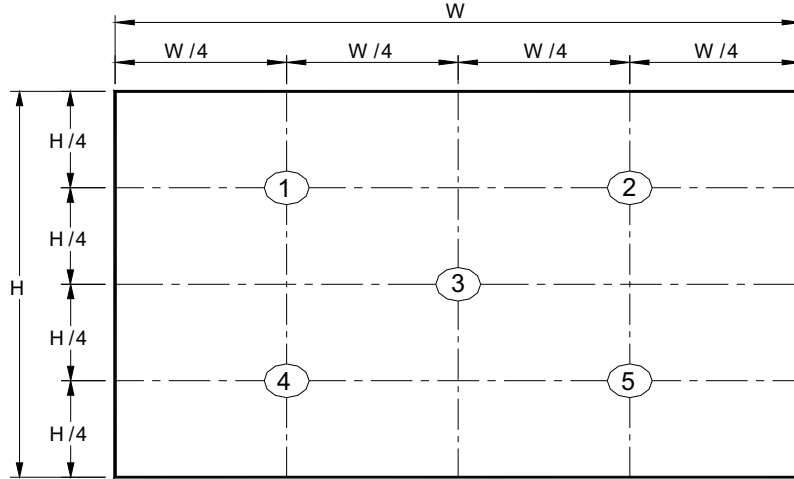
Support Color		262K colors ( RGB 6-bit )
Temperature Range		
Operating	[°C]	0 to +50
Storage (Non-Operating)	[°C]	-20 to +60
RoHS Compliance		RoHS Compliance

## 2.2 Optical Characteristics

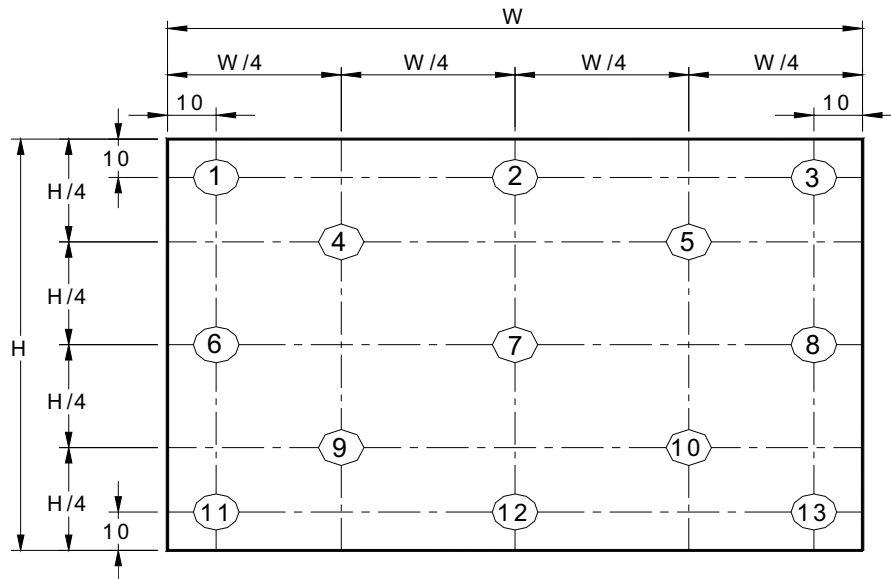
The optical characteristics are measured under stable conditions at 25°C (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance ICCFL=6.0mA	[cd/m <sup>2</sup> ]	5 points average	180	200	-	1, 4, 5.
Viewing Angle	[degree]	Horizontal (Right) CR = 10 (Left)	60	65	-	8
	[degree]		60	65	-	
	[degree]	Vertical (Upper) CR = 10 (Lower)	40	45	-	
	[degree]		50	55	-	
Luminance Uniformity		5 Points			1.3	1
Luminance Uniformity		13 Points			1.52	2
CR: Contrast Ratio			300:1	400:1	-	6
Cross talk	%				4	7
Response Time	[msec]	Rising	-	6	8	8
	[msec]	Falling	-	10	17	
	[msec]	Rising + Falling		16	25	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.556	0.576	0.596	2,8
		Red y	0.310	0.330	0.350	
		Green x	0.292	0.312	0.332	
		Green y	0.530	0.550	0.570	
		Blue x	0.141	0.161	0.181	
		Blue y	0.128	0.148	0.168	
		White x	0.293	0.313	0.333	
		White y	0.309	0.329	0.349	

Note 1: 5 points position (Display area : 331.38mm x 207.11mm)



Note 2: 13 points position



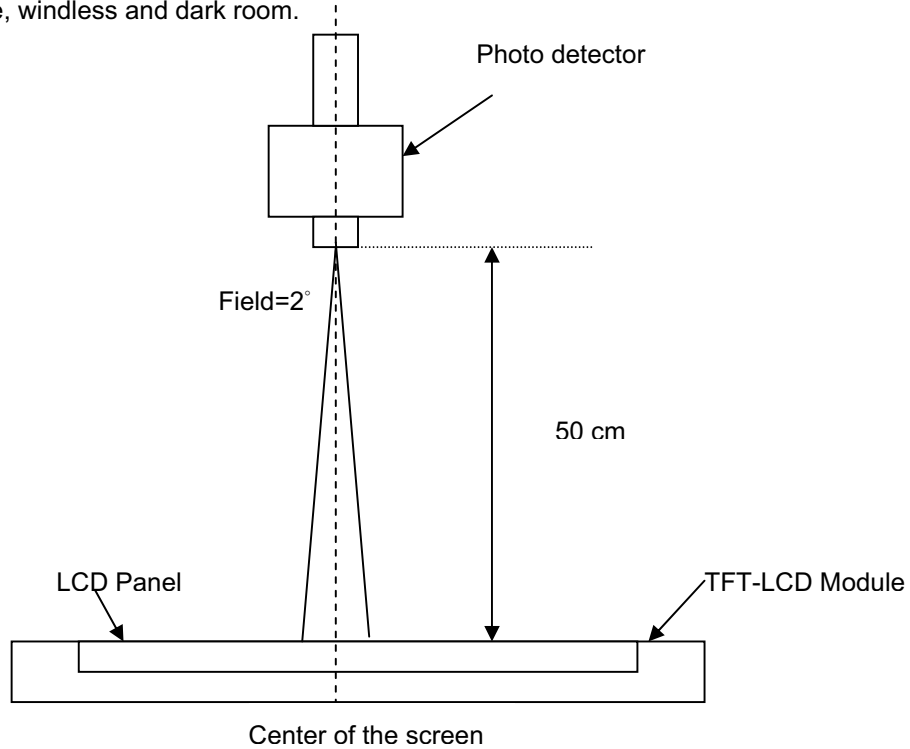
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{w5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{w13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 5 : Definition of Average Luminance of White ( $Y_L$ ):

Measure the luminance of gray level 63 at 5 points ,  $Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5$

$L (x)$  is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

$Y_A$  = Luminance of measured location without gray level 0 pattern ( $\text{cd}/\text{m}^2$ )

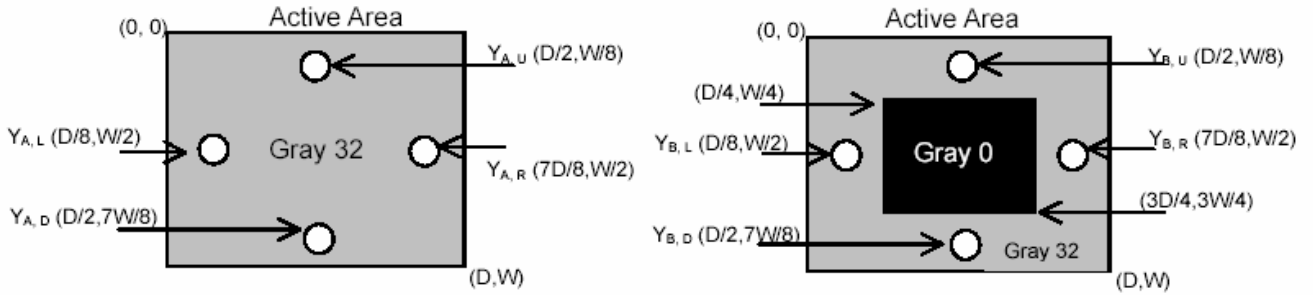




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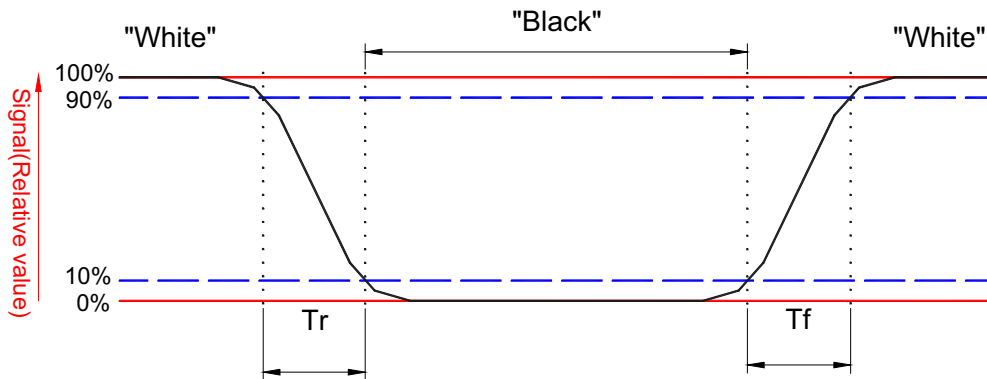
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$Y_B$  = Luminance of measured location with gray level 0 pattern (cd/m<sup>2</sup>)



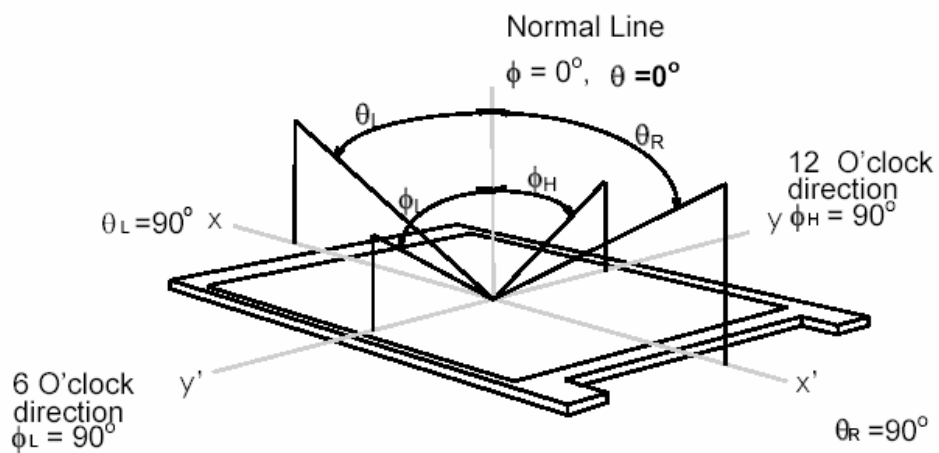
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 8. Definition of viewing angle

Viewing angle is the measurement of contrast ratio  $\geq 10$ , at the screen center, over a  $180^\circ$  horizontal and  $180^\circ$  vertical range (off-normal viewing angles). The  $180^\circ$  viewing angle range is broken down as follows;  $90^\circ$  ( $\theta$ ) horizontal left and right and  $90^\circ$  ( $\Phi$ ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



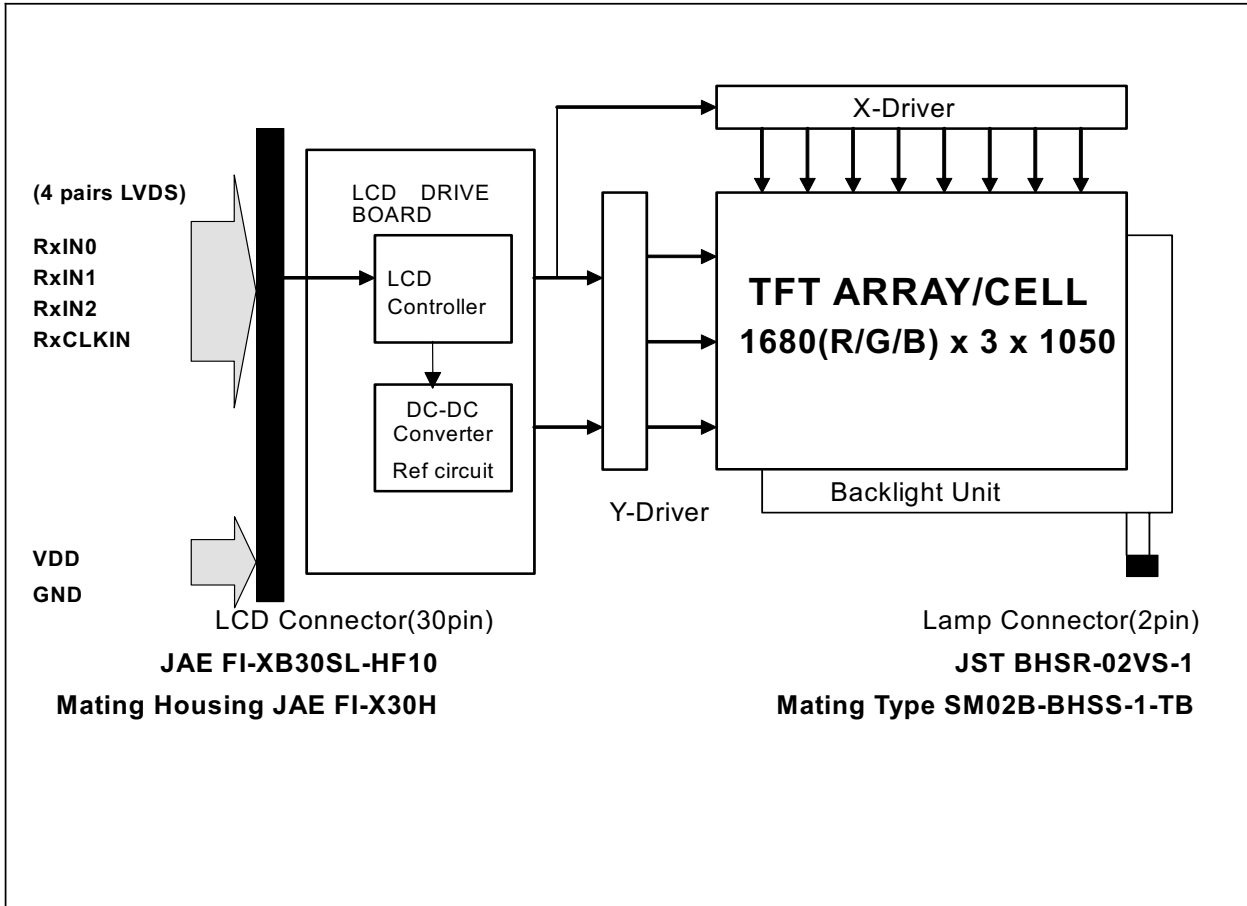


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## 3. Functional Block Diagram

The following diagram shows the functional block of the 15.4 inches wide Color TFT/LCD Module:





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## 4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

### 4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

### 4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICCFL	-	7.0	[mA] rms	Note 1,2

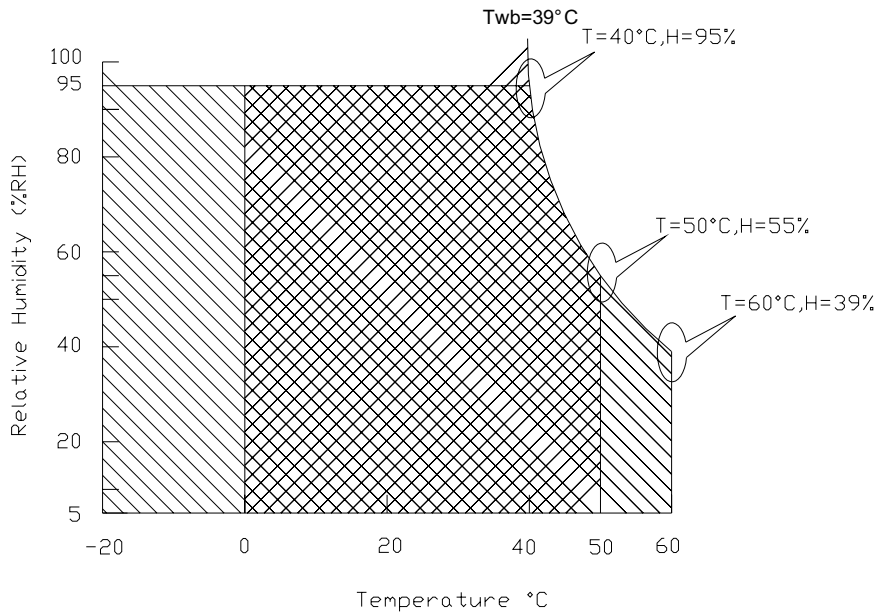
### 4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: At Ta (25°C )

Note 2: Permanent damage to the device may occur if exceed maximum values

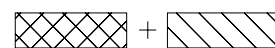
Note 3: For quality performance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range



Storage Range





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## 5. Electrical characteristics

### 5.1 TFT LCD Module

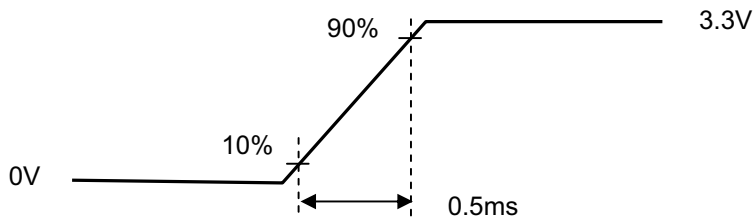
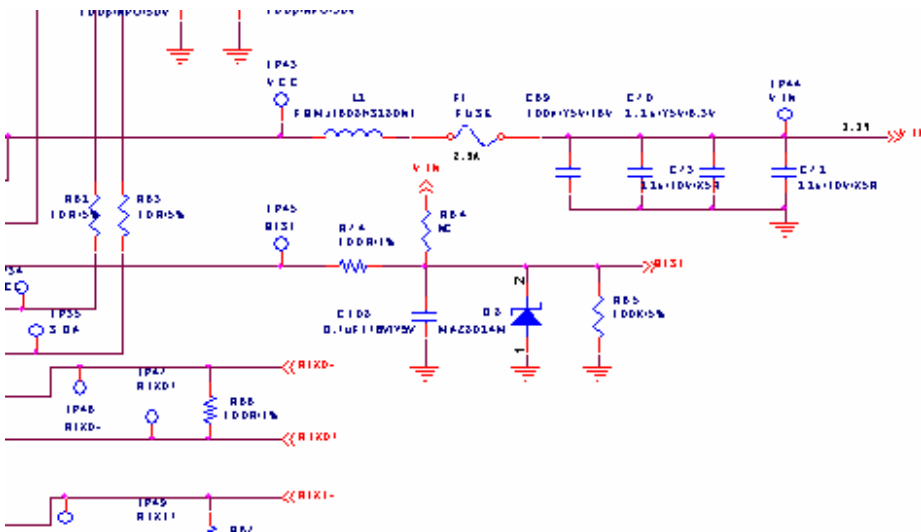
#### 5.1.1 Power Specification

Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power			2.5	[Watt]	Note 1
IDD	IDD Current		700	800	[mA]	Note 1
I <sub>rush</sub>	Inrush Current			2000	[mA]	Note 2
VDD <sub>rp</sub>	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Patternm

Note 2 : Measure Condition



V<sub>in</sub> rising time

## 5.1.2 Signal Electrical Characteristics

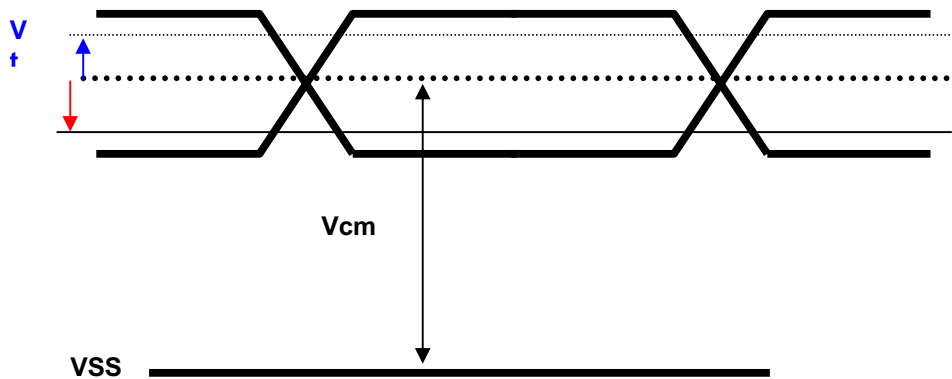
Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of THC63LVDF84A(Thine Electronics Inc.) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]
Vcm	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform





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## 5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance 5 points average	180	200	-	[cd/m <sup>2</sup> ]	(Ta=25°C)
CCFL current(I <sub>CCFL</sub> )	2.0	6.0	7	[mA] rms	(Ta=25°C)
CCFL Frequency(F <sub>CCFL</sub> )	50	55	60	[KHz]	Note 2 (Ta=25°C) Note 3,4
CCFL Ignition Voltage(V <sub>s</sub> )	1650			[Volt] rms	(Ta= 0°C) Note 5
CCFL Ignition Voltage(V <sub>s</sub> )	1460			[Volt] rms	(Ta= 25°C) Note 5
CCFL Voltage (Reference) (V <sub>CCFL</sub> )	700	730	945	[Volt] rms	(Ta=25°C) Note 6
CCFL Power consumption (P <sub>CCFL</sub> )	-	4.38		[Watt]	(Ta=25°C) Note 6

Note 1: Typ are AUO recommended Design Points.

\*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

\*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

\*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

\*4 Generally, CCFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

\*5 CCFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

\*6 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has "Duty Dimming", if ICCFL is less than 4mA.

Note 3: CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.



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Note 5: CCFL inverter should be able to give out a power that has a generating capacity of over 1,430 voltage. Lamp units need 1,400 voltage minimum for ignition.

Note 6: Calculator value for reference ( $I_{CCFL} \times V_{CCFL} = P_{CCFL}$ )

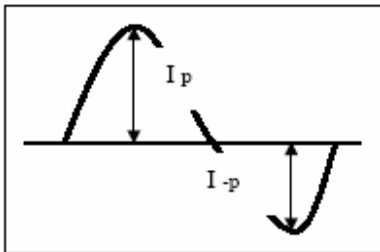
Note 7: Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following.

It shall help increase the lamp lifetime and reduce leakage current.

a. The asymmetry rate of the inverter waveform should be less than 10%.

b. The distortion rate of the waveform should be within  $\sqrt{2} \pm 10\%$ .

\* Inverter output waveform had better be more similar to ideal sine wave.



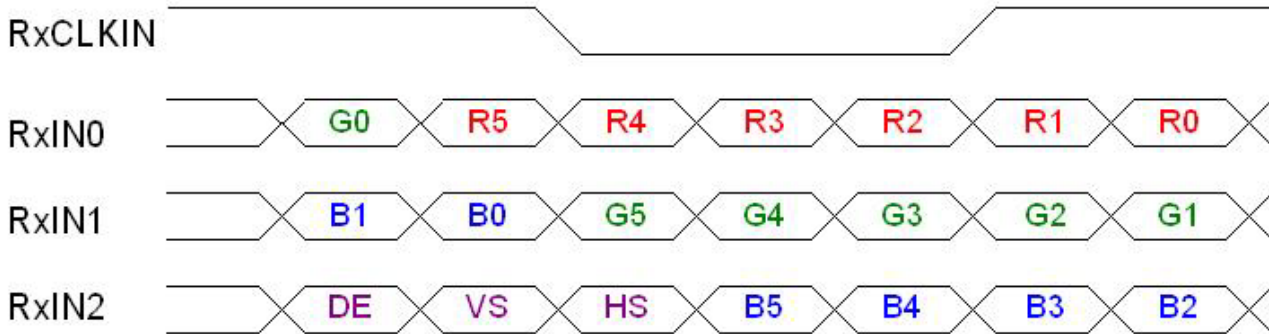
\* Asymmetry rate:  
$$\frac{|I_p - I_{-p}|}{I_{rms}} * 100\%$$

\* Distortion rate  
$$I_p \text{ (or } I_{-p}) / I_{rms}$$





## 6.2 The input data format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
	Red-pixel Data	
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
	Green-pixel Data	
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
	Blue-pixel Data	
RxCLKIN	Data Clock	The typical frequency is 64.9 MHz. The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN.
HS	Horizontal Sync	The signal is synchronized to RxCLKIN.

Note: Output signals from any system shall be low or High-impedance state when VDD is off.



## 6.3 Signal Description/Pin Assignment

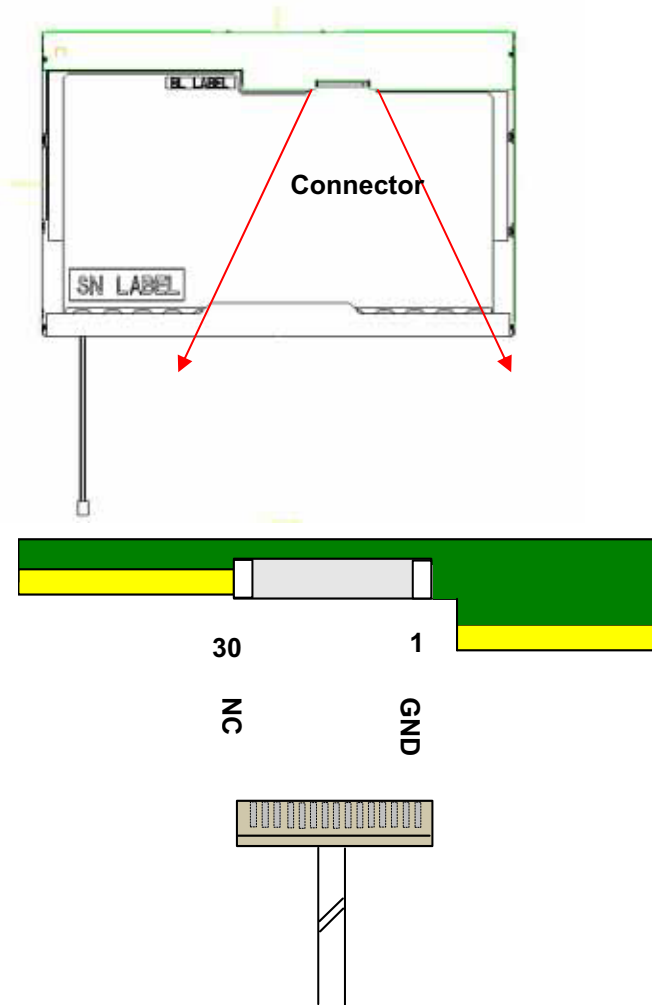
LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN#	Signal Name	Description
1	GND	Ground
2	VDD	+3.3V Power Supply (typical)
3	VDD	+3.3V Power Supply (typical)
4	V <sub>EDID</sub>	+3.3V EDID Power
5	NC	Reserved for supplier test point
6	CLK <sub>EDID</sub>	EDID Clock Input
7	DATA <sub>EDID</sub>	EDID Data Input
8	RxIN0-	LVDS differential data input(R0-R5, G0) (odd pixels)
9	RxIN0+	LVDS differential data input(R0-R5, G0) (odd pixels)
10	GND	Ground
11	RxIN1-	LVDS differential data input(G1-G5, B0-B1) (odd pixels)
12	RxIN1+	LVDS differential data input(G1-G5, B0-B1) (odd pixels)
13	GND	Ground
14	RxIN2-	LVDS differential data input(B2-B5, HS, VS, DE) (odd pixels)
15	RxIN2+	LVDS differential data input(B2-B5, HS, VS, DE) (odd pixels)
16	GND	Ground
17	RxCLKIN-	LVDS differential clock input (odd pixels)
18	RxCLKIN+	LVDS differential clock input (odd pixels)
19	GND	Ground
20	Even_RxIN0-	LVDS differential data input (R0-R5,G0) (even pixels)
21	Even_RxIN0+	LVDS differential data input (R0-R5,G0) (even pixels)
22	GND	Ground
23	Even_RxIN1-	LVDS differential data input (G1-G5,B0-B1) (even pixels)
24	Even_RxIN1+	LVDS differential data input (G1-G5,B0-B1) (even pixels)
25	GND	Ground
26	Even_RxIN2-	LVDS differential data input (B2-B5,HS,VS,DE) (even pixels)
27	Even_RxIN2+	LVDS differential data input (B2-B5,HS,VS,DE) (even pixels)
28	GND	Ground
29	Even_RxCLKIN-	LVDS differential clock input (even pixels) , 2.1V
30	Even_RxCLKIN+	LVDS differential clock input (even pixels) , 2.1V

【Note 1】 Relation between LVDS signals and actual data shows below section(4-2).

【Note 2】 The shielding case is connected with signal GND.

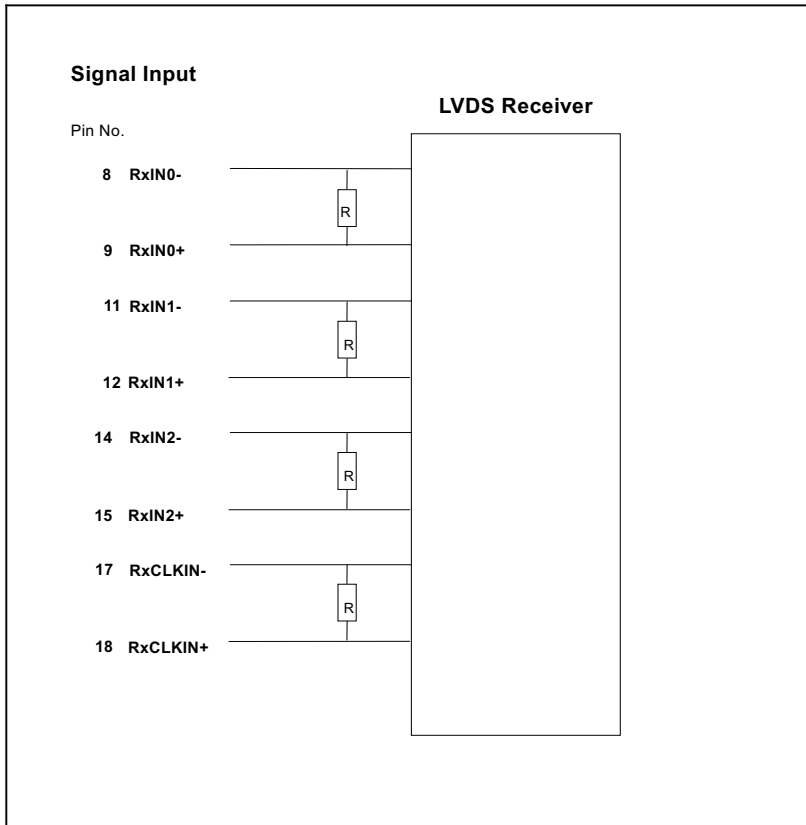
Note1: Start from right side



Note2: Input signals shall be low or High-impedance state when VDD is off.

internal circuit of LVDS inputs are as following.

The module uses a 100ohm resistor between positive and negative data lines of each receiver input





## 6.4 Interface Timing

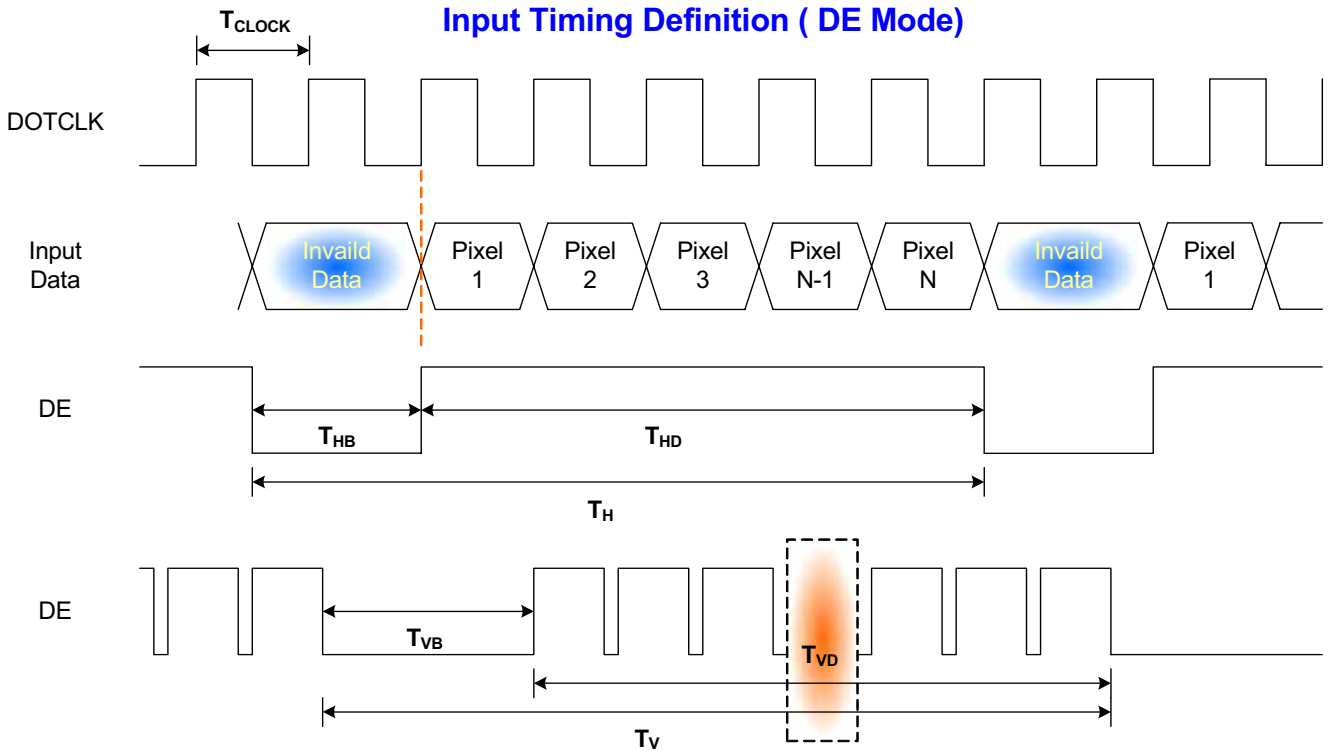
### 6.4.1 Timing Characteristics

Basically, interface timings should match the 1680x1050 /60Hz manufacturing guide line timing.

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Frame Rate	-	50	60	-	Hz	
Clock frequency	$1/T_{\text{Clock}}$	40	59.5	80	MHz	
Vertical Section	Period	$T_V$	1080	1080	1080	$T_{\text{Line}}$
	Active	$T_{VD}$	1050	1050	1050	
	Blanking	$T_{VB}$	30	30	30	
Horizontal Section	Period	$T_H$	1840	1840	1840	$T_{\text{Clock}}$
	Active	$T_{HD}$	1680	1680	1680	
	Blanking	$T_{HB}$	160	160	160	

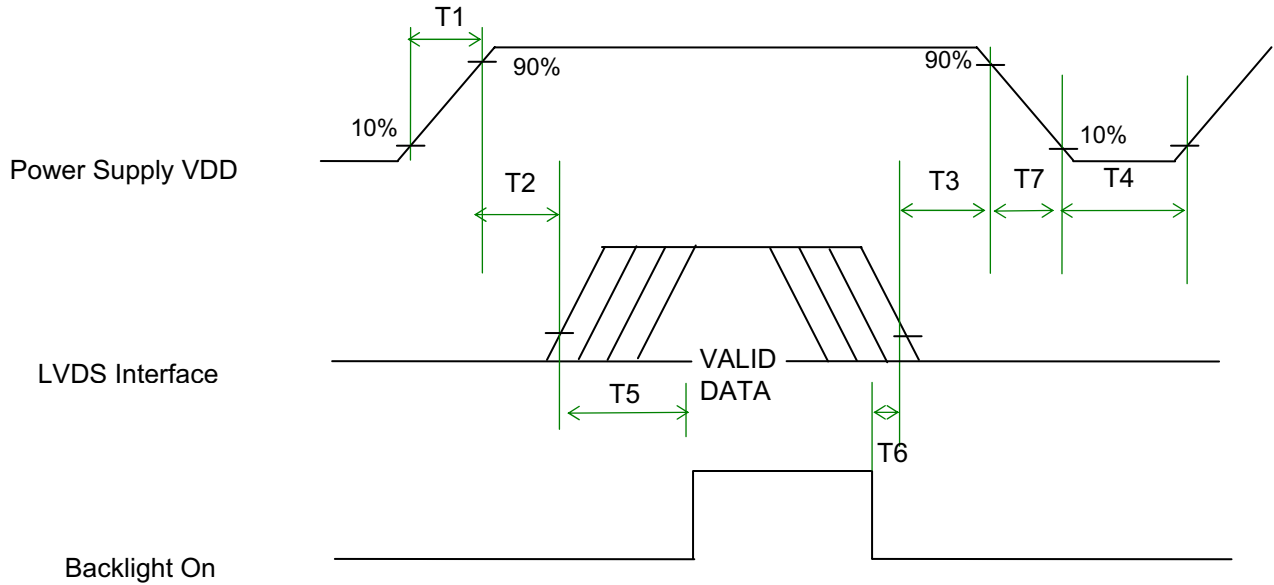
Note : DE mode only

## 6.4.2 Timing diagram



## 6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



### Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)





## 7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

### 7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or compatible
Type / Part Number	FI-XB30SL-HF10 or compatible
Mating Housing/Part Number	FI-X30H or compatible

### 7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

### 7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Red	Lamp High Voltage
2	White	Lamp Low Voltage



## 8. Vibration and Shock Test

### 8.1 Vibration Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 2.16G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

### 8.2 Shock Test Spec:

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 200 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .three time for each side



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## 9. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	40°C/95%,250Hr	
High Temperature Operation	50°C/Dry,250Hr	
Low Temperature Operation	0°C,250Hr	
On/Off Test	25°C,150hrs(ON/10 sec. OFF/10sec., 30,000 cycles)	
Hot Storage	60°C/35% RH ,240 hours	
Cold Storage	-20°C/50% RH ,240 hours	
Thermal Shock Test	-20°C/30 min ,60°C/30 min 100cycles	
Hot Start Test	50°C/1 Hr min. power on/off per 5 minutes, 5 times	
Cold Start Test	0°C/1 Hr min. power on/off per 5 minutes, 5 times	
Shock Test (Non-Operating)	200G, 2ms, Half-sine wave, 3 times for each $\pm x,y,z$ direction	
Vibration Test (Non-Operating)	Random vibration, 2.16 G zero-to-peak, 10 to 500 Hz, 30 mins in each of three mutually perpendicular axes.	
ESD	Contact : $\pm 8KV$ / operation Air : $\pm 15KV$ / operation	Note 1
Room temperature Test	25°C, 2000hours, Operating with loop pattern	

Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

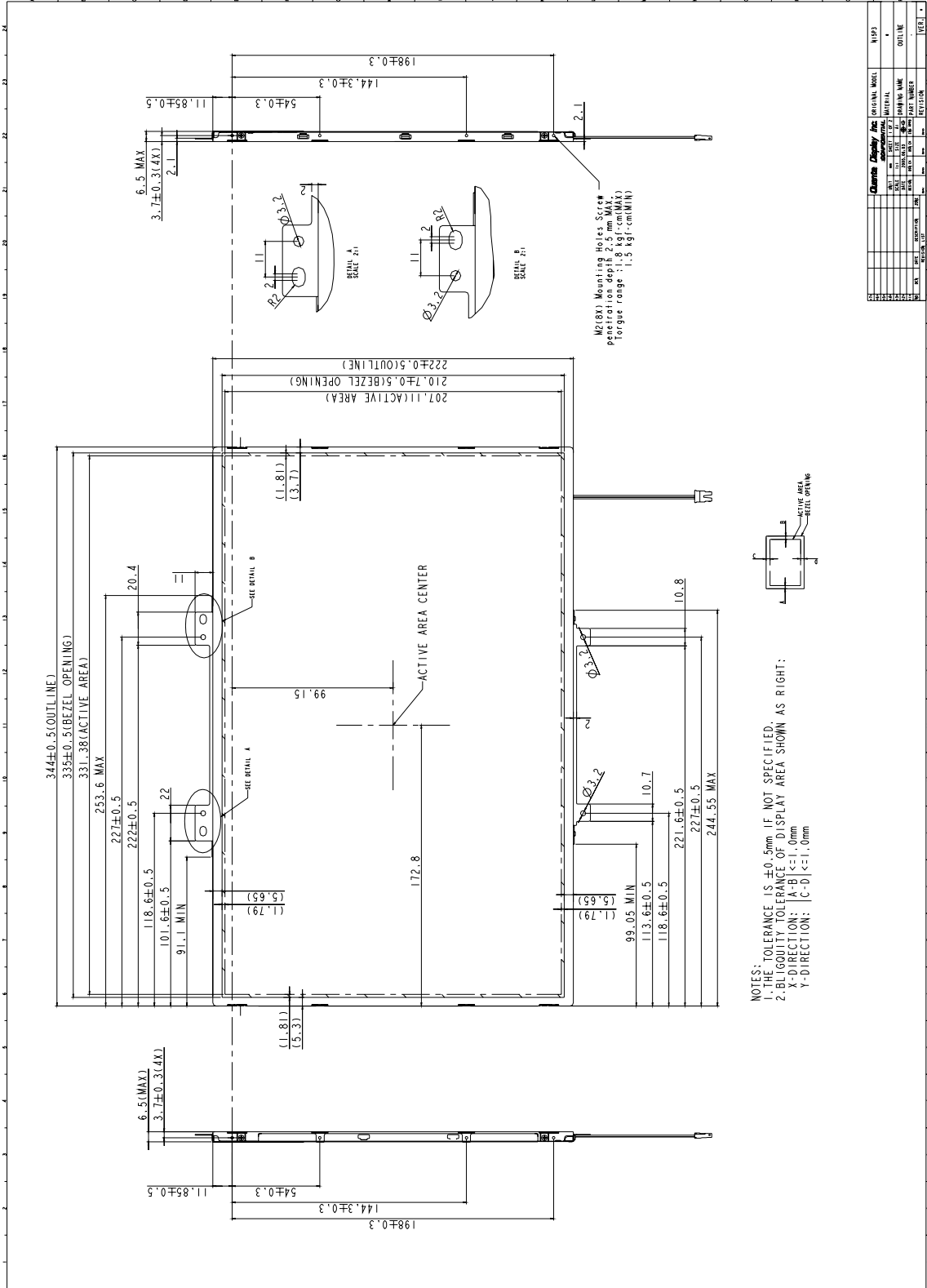
. Self-recoverable. No hardware failures.

Note2: CCFL Life time: 10,000 hours minimum under normal module usage.

Note3: MTBF (Excluding the CCFL): 30,000 hours with a confidence level 90%

# 10. Mechanical Characteristics

## 10.1 LCM Outline Dimension







# 11. Shipping and Package

B154SW01

## 11.1 Shipping Label Format

The diagram shows a shipping label with the following text and callouts:

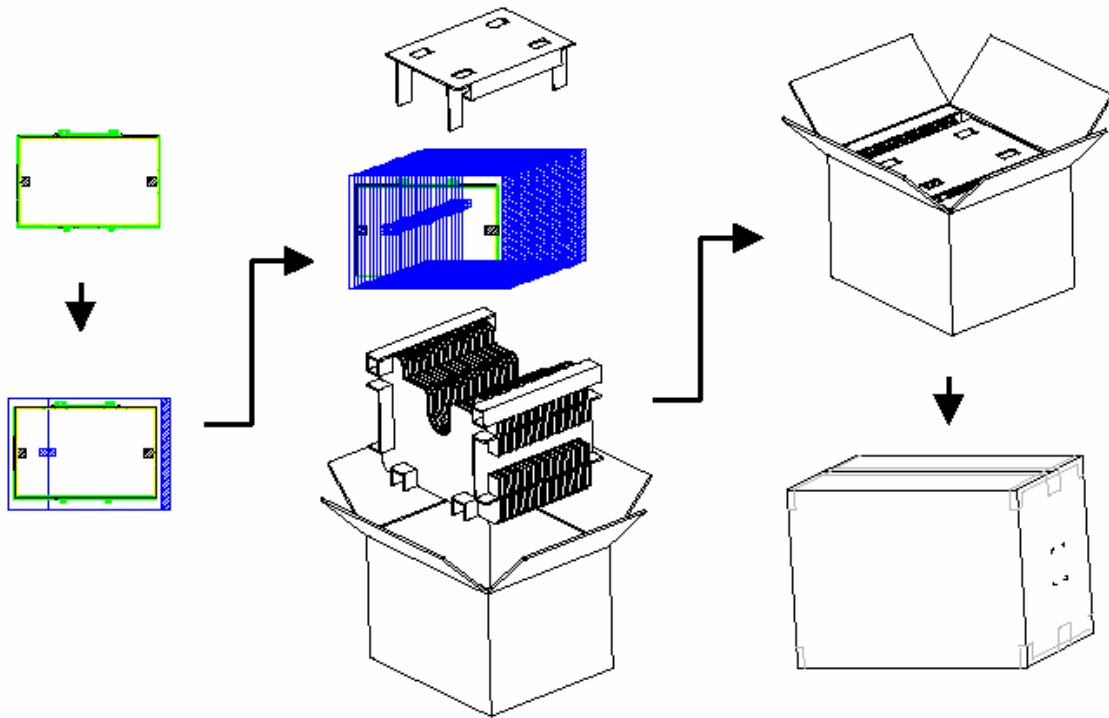
- Week code:** 05/27
- Model:** B154SW01
- Control code:** V1
- Other text on label:** Manufactured 05/27, Model No. B154SW01, AU Optronics, MADE IN CHINA (S1), H/W: 1, F/W: 1, OA30G, RoHS, E204356

A yellow box highlights a barcode area containing the following alphanumeric codes:

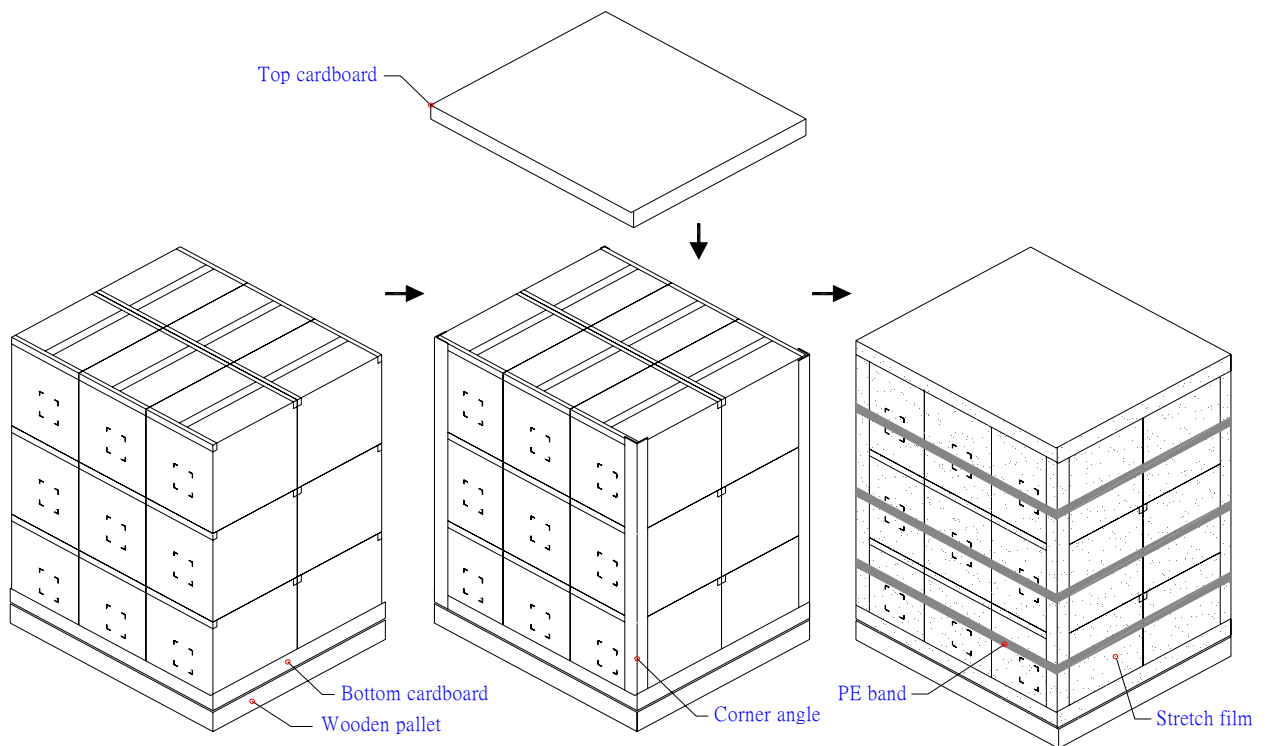
11S	42T0332Z	1ZC7A	C00000	608	P/N	42T0332	FRU	42T0333
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## 11.2. Carton package

The outside dimension of carton is 455 (L)mm x 380 (W)mm x 355 (H)mm



## 11.3 Shipping package of palletizing sequence



Note : Limit of box palletizing = Max 3 layers(ship and stock conditions)



## 12. Appendix: EDID description

This is the EDID (Extended Display Identification Data) data format to support displays as defined in the VESA Plug & Display. (Ver. 06022005)

**B154SW01 V1 EDID Code**                      **Release time**                      **2006/10/20 00:00**

Byte (decimal)	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
<b>Header</b>				
0	00	Header	00	00000000
1	01	Header	FF	11111111
2	02	Header	FF	11111111
3	03	Header	FF	11111111
4	04	Header	FF	11111111
5	05	Header	FF	11111111
6	06	Header	FF	11111111
7	07	Header	00	00000000
<b>Vendor/Product ID/EDID Version</b>				
8	08	EISA manufacture code = QDS	44	01000100
9	09	EISA manufacture code (Compressed ASCII)	93	10010011
10	0A	Product code (61); LSB 0063	3F	00111111
11	0B	Product code MSB	00	00000000
12	0C	LCD module Serial No (fixed "0")	00	00000000
13	0D	LCD module Serial No (fixed "0")	00	00000000
14	0E	LCD module Serial No (fixed "0")	00	00000000
15	0F	LCD module Serial No (fixed "0")	00	00000000
16	10	Week of manufacture	00	00000000
17	11	Year of manufacture – 1990, 2005-1990=15=F (hex)	0F	00001111
18	12	EDID structure version # = 1	01	00000001
19	13	EDID revision # = 3	03	00000011
<b>Display Parameter</b>				
20	14	Video I/P definition = Digital I/P	80	10000000
21	15	Max H image size (cm) = 33cm	21	00100001
22	16	Max V image size (cm) = 20cm	14	00010100
23	17	Display gamma ( 2.2 ±00 ) –100= 120	78	01111000
24	18	Feature (no DMPS, Active off, RGB, timing BLK1)	0A	00001010
<b>Panel Color Coordinates</b>				
25	19	Red/Green Low bit	2E	00101110
26	1A	Blue/White Low bit	A0	10100000

27	1B	Red X (Rx)(written value “0.567”)	91	10010001
28	1C	Red Y (Ry)(written value “0.331”)	54	01010100
29	1D	Green X (Gx)(written value “0.308”)	4E	01001110
30	1E	Green Y (Gy)(written value “0.553”)	8D	10001101
31	1F	Blue X (Bx)(written value “0.159”)	28	00101000
32	20	Blue Y (By)(written value “0.143”)	24	00100100
33	21	White X (Wx)(written value “0.313”)	50	01010000
34	22	White Y (Wy)(written value “0.329”)	54	01010100
<b>Established Timings</b>				
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
<b>Standard Timing ID</b>				
37	25	Manufacture’s reserved timing	00	00000000
38	26	Standard timing ID1	01	00000001
39	27	Standard timing ID1	01	00000001
40	28	Standard timing ID2	01	00000001
41	29	Standard timing ID2	01	00000001
42	2A	Standard timing ID3	01	00000001
43	2B	Standard timing ID3	01	00000001
44	2C	Standard timing ID4	01	00000001
45	2D	Standard timing ID4	01	00000001
46	2E	Standard timing ID5	01	00000001
47	2F	Standard timing ID5	01	00000001
48	30	Standard timing ID6	01	00000001
49	31	Standard timing ID6	01	00000001
50	32	Standard timing ID7	01	00000001
51	33	Standard timing ID7	01	00000001
52	34	Standard timing ID8	01	00000001
53	35	Standard timing ID8	01	00000001
<b>Timing Descriptor #1</b>				
54	36	Pixel Clock/10,000 (LSB) 11900=2E7Ch	7C	01111100
55	37	Pixel Clock/10,000 (MSB)	2E	00101110
56	38	Horizontal Active 1680=690h “90”	90	10010000
57	39	Horizontal Blanking (Thbp) 160=A0h “A0”	A0	10100000
58	3A	Horizontal Active/Horizontal Blanking (Thbp) “60h”	60	01100000
59	3B	Vertical Active 1050=41Ah “1A”	1A	00011010
60	3C	Vertical Blanking 30 (Tvbp)=1Eh “1E”	1E	00011110
61	3D	Vertical active/Vertical blanking (Tvbp) “40”	40	01000000

62	3E	Horizontal Sync, Offset (Thfp) 48=30h "30"	30	00110000
63	3F	Horizontal Sync, Pulse Width 32=20h "20"	20	00100000
64	40	Vertical Sync, Offset (Tvfp)/Sync Width	36	00110110
65	41	Horizontal/Vertical Sync Offset/Width upper 2 bits	00	00000000
66	42	Horizontal Image Size 331.2mm=14Bh "4B"	4B	01001011
67	43	Vertical Image Size 207.0mm=CFh "CF"	CF	11001111
68	44	Horizontal Image Size / Vertical Image Size	10	00010000
69	45	Horizontal Border	00	00000000
70	46	Vertical Border	00	00000000
71	47	Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives, DE only note: LSB is set to "1" if panel is DE-timing only. H/V can be ignored.	18	00011000
<b>Timing Descriptor #: Manufacturer Specified Range Timing Descriptor</b>				
72	48	Detailed timing descriptor#2	00	00000000
73	49	Flag	00	00000000
74	4A	Reserved	00	00000000
75	4B	Dummy Descriptor	0F	00001111
76	4C	Flag	00	00000000
77	4D	Value=HSPW(Min)/2 (pixel clks)      06=06h	06	00000110
78	4E	Value=HSPW(Max) /2 (pixel clks)      110=6Eh	6E	01101110
79	4F	Value=Thbp(Min)/2 (pixel clks)      06=06h	06	00000110
80	50	Value=Thbp(Max)/2 (pixel clks)      60=3Ch	3C	00111100
81	51	Value=VSPW(Min)/2 (line pulses)      01=01h	01	00000001
82	52	Value=VSPW(Max)/2 (line pulses)      20=14h	14	00010100
83	53	Value=Tvbp(Min)/2 (line pulses)      01=01h	01	00000001
84	54	Value=Tvbp(Max)/2 (line pulses)      15=0Fh	0F	00001111
85	55	Thp(Min)=Value*2+HA (pixel clks)      1032=408h =08h	08	00001000
86	56	Thp(Max)=Value*2+HA (pixel clks)      2047=7FFh=FFh	FF	11111111
87	57	Tvp(Min)=Value*2+VA (line pulses)      803=323h=23h	23	00100011
88	58	Tvp(Max)=Value*2+VA (line pulses)      2047=7FFh=FFh	FF	11111111
89	59	Module "A" Revision= 0	00	00000000
<b>Timing Descriptor #3 ASCII String: Supplier Name</b>				
90	5A	Flag	00	00000000
91	5B	Flag	00	00000000
92	5C	Flag	00	00000000
93	5D	Data Type Tag : Module serial number	FE	11111110
94	5E	Flag	00	00000000
95	5F	1 <sup>st</sup> character of String="Q"	51	01010001
96	60	2 <sup>nd</sup> character of String="U"	55	01010101

97	61	3 <sup>rd</sup> character of String="A"	41	01000001
98	62	4 <sup>th</sup> character of String="N"	4E	01001110
99	63	5 <sup>th</sup> character of String="T"	54	01010100
100	64	6 <sup>th</sup> character of String="A"	41	01000001
101	65	7 <sup>th</sup> character of String="D"	44	01000100
102	66	8 <sup>th</sup> character of String="I"	49	01001001
103	67	9 <sup>th</sup> character of String="S"	53	01010011
104	68	10 <sup>th</sup> character of String="P"	50	01010000
105	69	11 <sup>th</sup> character of String="L"	4C	01001100
106	6A	12 <sup>th</sup> character of String="A"	41	01000001
107	6B	13 <sup>th</sup> character of String="Y"	59	01011001
<b>Timing Descriptor #4 ASCII String: Supplier P/N</b>				
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000
110	6E	Flag	00	00000000
111	6F	Data Type Tag : Module Name	FE	11111110
112	70	Flag	00	00000000
113	71	Q	51	01010001
114	72	D	44	01000100
115	73	1	31	00110001
116	74	5	35	11000101
117	75	A	41	01000001
118	76	L	4C	01001100
119	77	0	30	00110000
120	78	1	31	00110001
121	79	Product revision: 3	33	00110011
122	7A	Terminate with ASCII code 0AH	0A	00001010
123	7B	Pad Field with ASCII code 20H	20	00100000
124	7C	Pad Field with ASCII code 20H	20	00100000
125	7D	Pad Field with ASCII code 20H	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	29	00101001