( ) Preliminary Specifications
(V) Final Specifications

Module	**15.6”(15.55”) HD 16:9 Color TFT-LCD with LED Backlight design**
Model Name	B156XW02 V5 (H/W:1A)
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**	**Approved by**	**Date**
		Emerson Huang	4/12/2010
Checked & Approved by	**Date**	**Prepared by**	**Date**
		Lacasis Liu	4/12/2010
Note: This Specification is subject to change without notice.		**NBBU Marketing Division AU Optronics corporation**	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
1.0 2010/04/12	All	First Edition for Customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostic breakdown.

2. General Description

B156XW02 V5 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are Display Port interface compatible.

B156XW02 V5 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	394.91			
Active Area	[mm]	344.23 X193.54			
Pixels H x V		1366x3(RGB) x 768			
Pixel Pitch	[mm]	0.252X0.252			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (I_{LED}=20mA) **(Note: ILED is LED current)**	[cd/m²]	220 typ. (5 points average) 190 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		500 typ			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	5.6 max. (Include Logic and Blu power)			
Weight	[Grams]	450 max.			
Physical Size **Include bracket**	[mm]		Min.	Typ.	Max.
		Length	-	359.3	360
		Width	-	209.5	210
		Thickness	-	-	5.5
Electrical Interface		1 channel Display port			
Glass Thickness	[mm]	0.5			
Surface Treatment		Glare, Hardness 3H, Reflection 4.3%			
Support Color		262K colors (RGB 6-bit)			

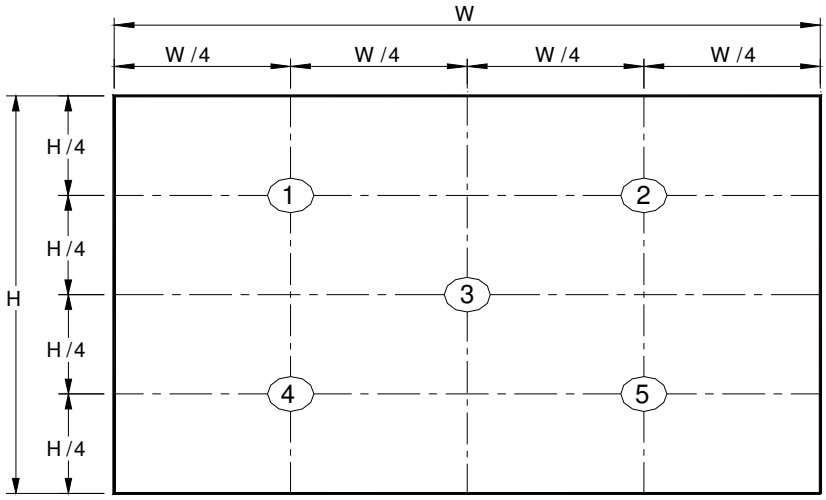
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

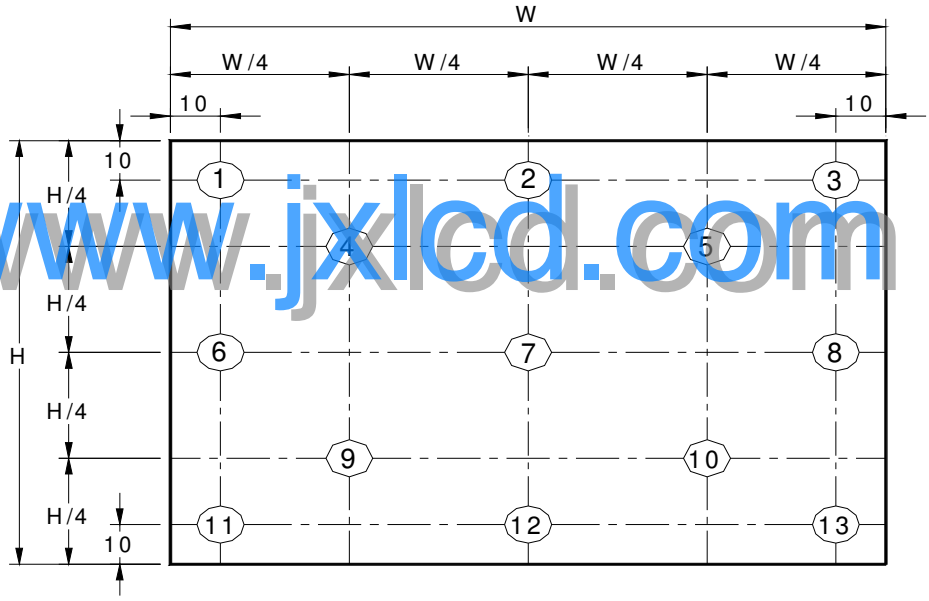
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=22mA			5 points average	190	220	-	cd/m²	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right) CR = 10	40	45	-	degree	4, 9
		θ_L	(Left)	40	45	-		
		ϕ_H	Vertical (Upper) CR = 10	10	15	-		
		ϕ_L	(Lower)	30	35	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.65		2, 3, 4
Contrast Ratio		CR		-	500	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_r	Rising	-	6	-	msec	4, 8
		T_f	Falling	-	2	-		
		T_{RT}	Rising + Falling	-	8	16		
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.593	0.623	0.653		4
		Ry		0.321	0.351	0.381		
	Green	Gx		0.306	0.336	0.366		
		Gy		0.544	0.574	0.604		
	Blue	Bx		0.118	0.148	0.178		
		By		0.023	0.053	0.083		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	60	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

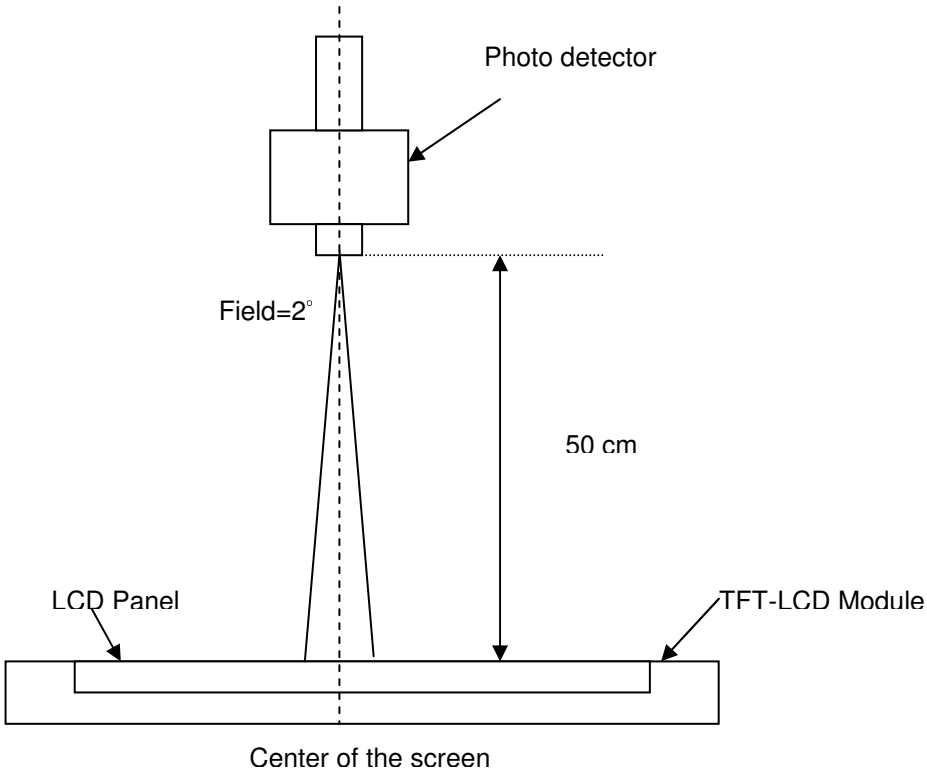
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

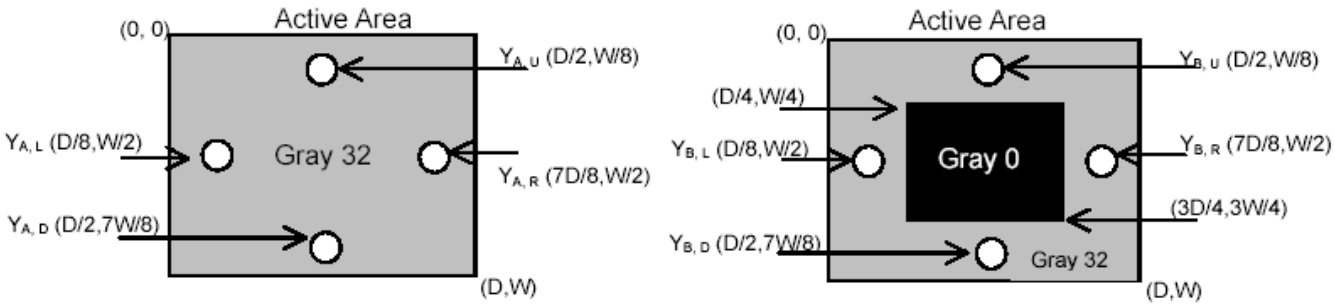
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where

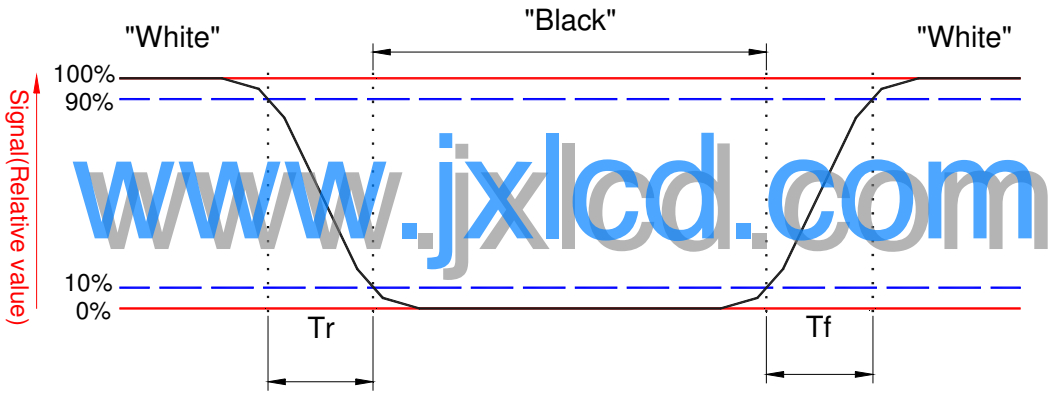
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



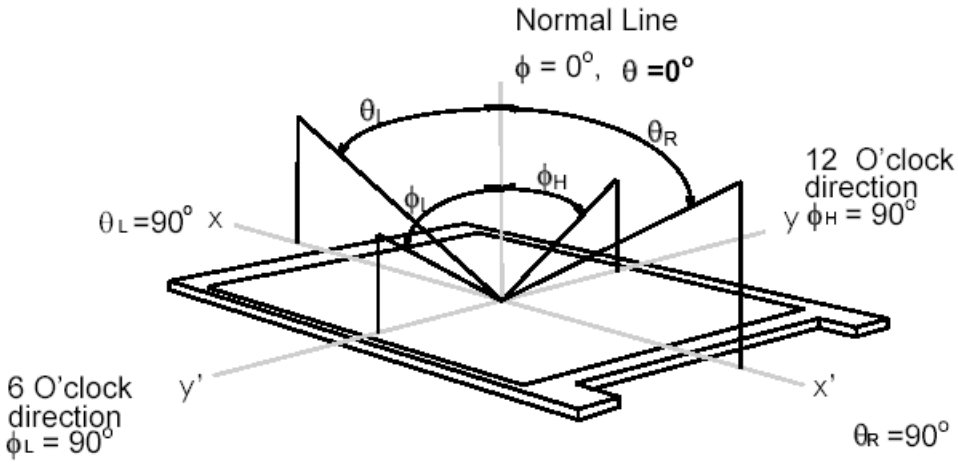
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



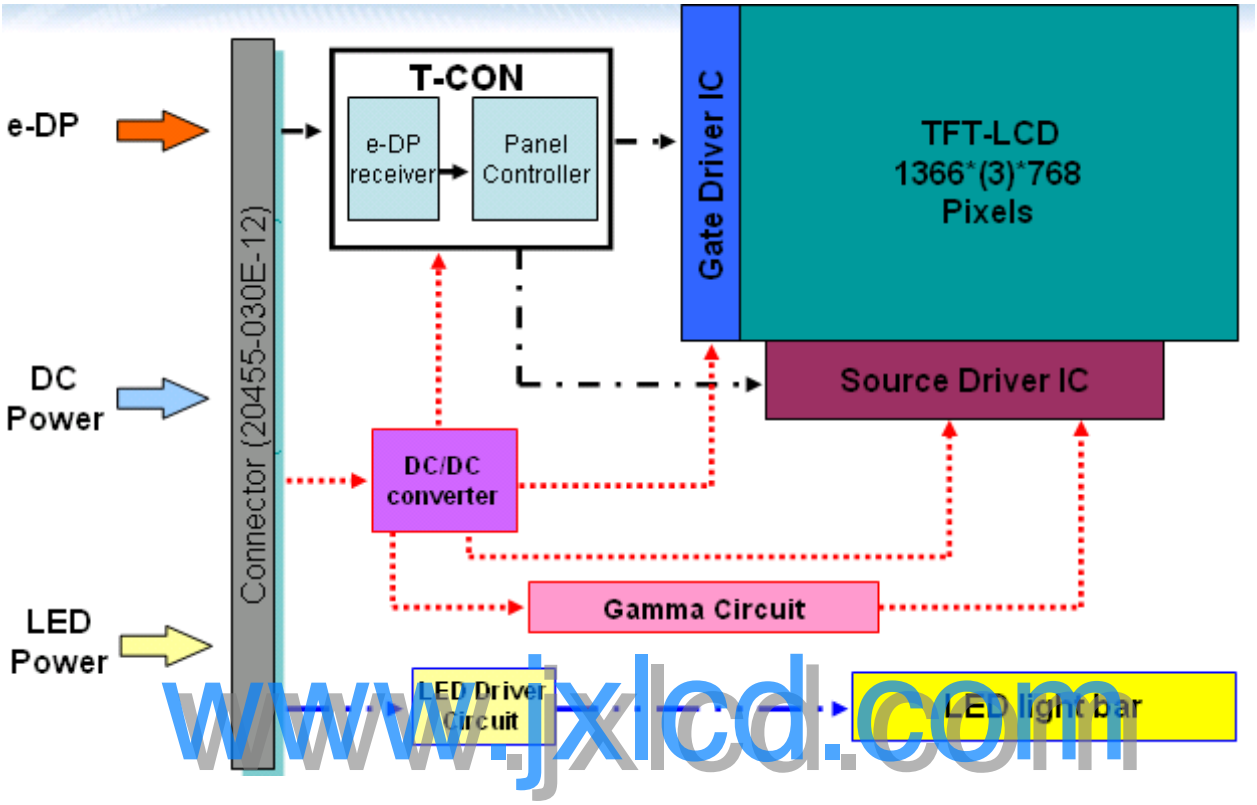
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 15.6 inches wide Color TFT/LCD 40 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

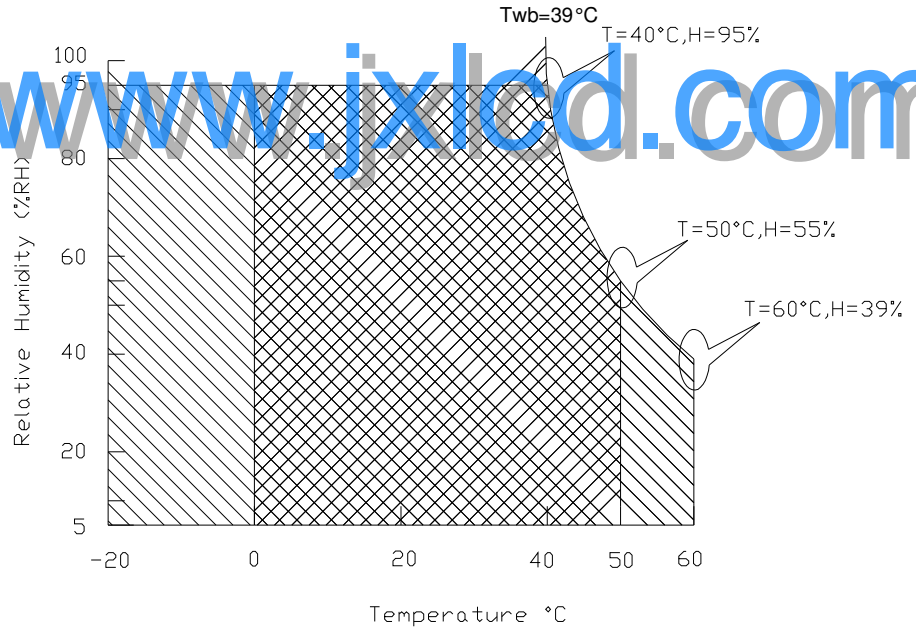
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

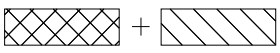
Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range 

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

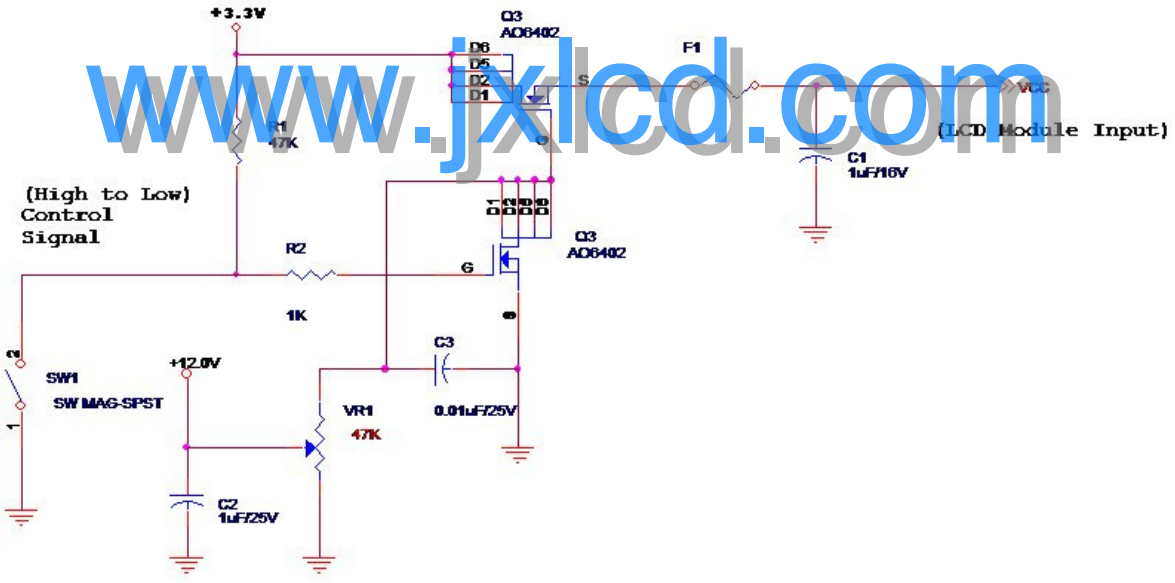
Input power specifications are as follows;

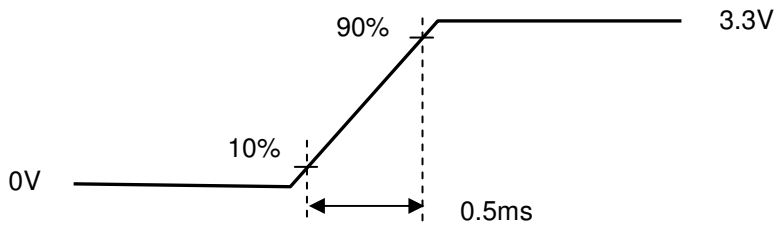
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.2	[Watt]	Note 1
IDD	IDD Current	-	250	400	[mA]	Note 1
IRush	Inrush Current	-	-	1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Note 2：Measure Condition





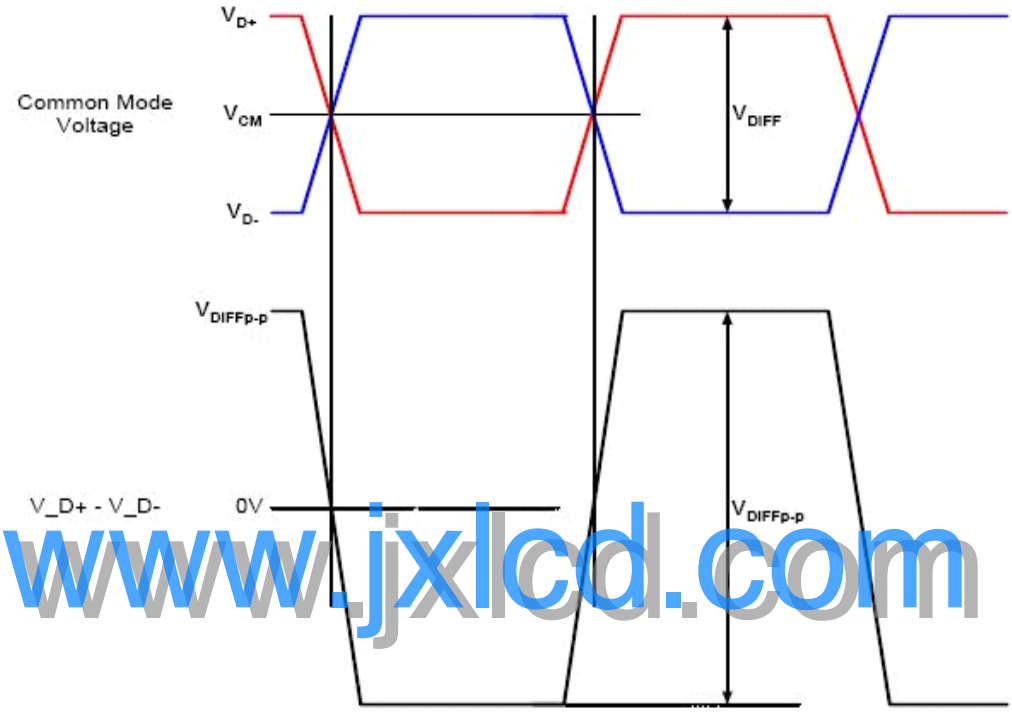
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

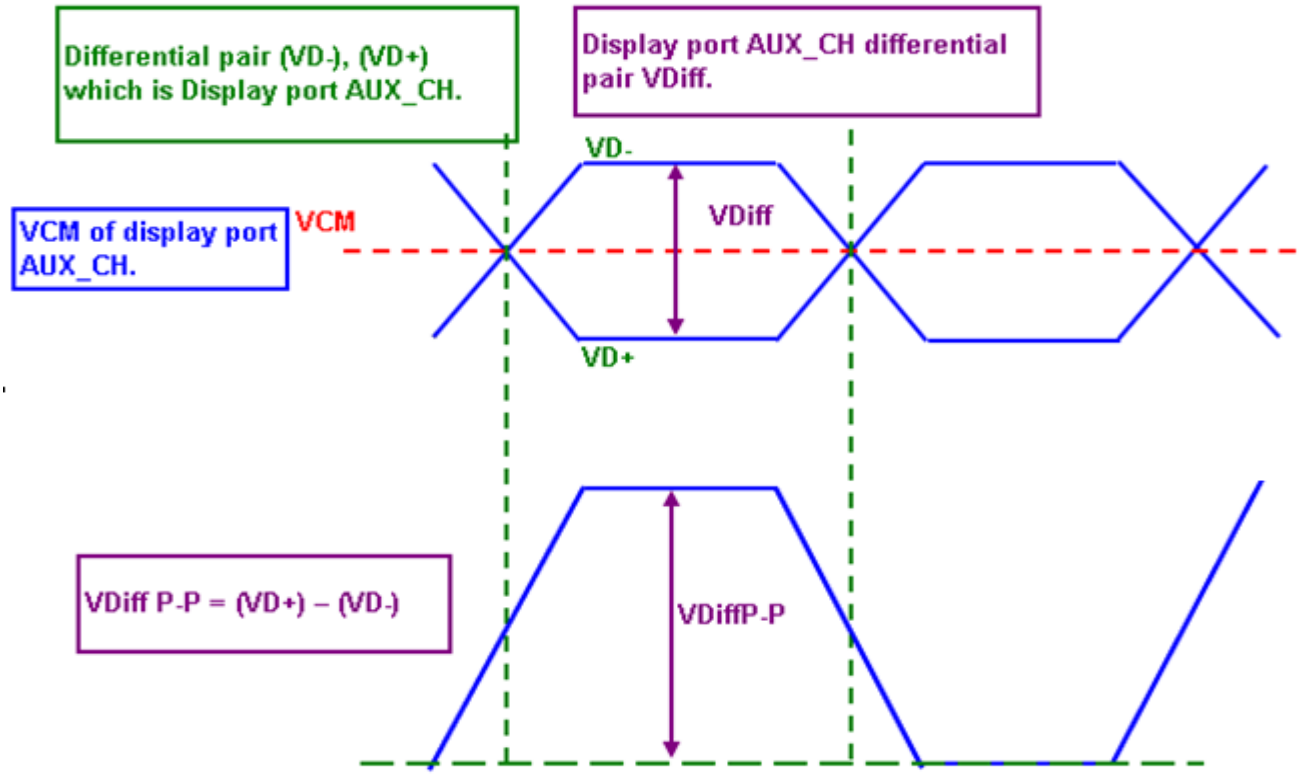
5.1.2.1 Display Port main link signal



Display Port Main Link					
		Min	Typ	Max	Unit
V_{CM}	Differential common mode voltage	0	**0.8**	2	V
VDiffP-P level1	Differential peak to peak voltage level1	0.34	0.4	0.46	V
VDiffP-P level2	Differential peak to peak voltage level2	0.51	0.6	0.68	V
VDiffP-P level3	Differential peak to peak voltage level3	0.69	0.8	0.92	V
VDiffP-P level4	Differential peak to peak voltage level4	1.02	1.2	1.38	V

Remark: Reference VESA eDP standard

5.1.2.2 Display Port AUX_CH signal



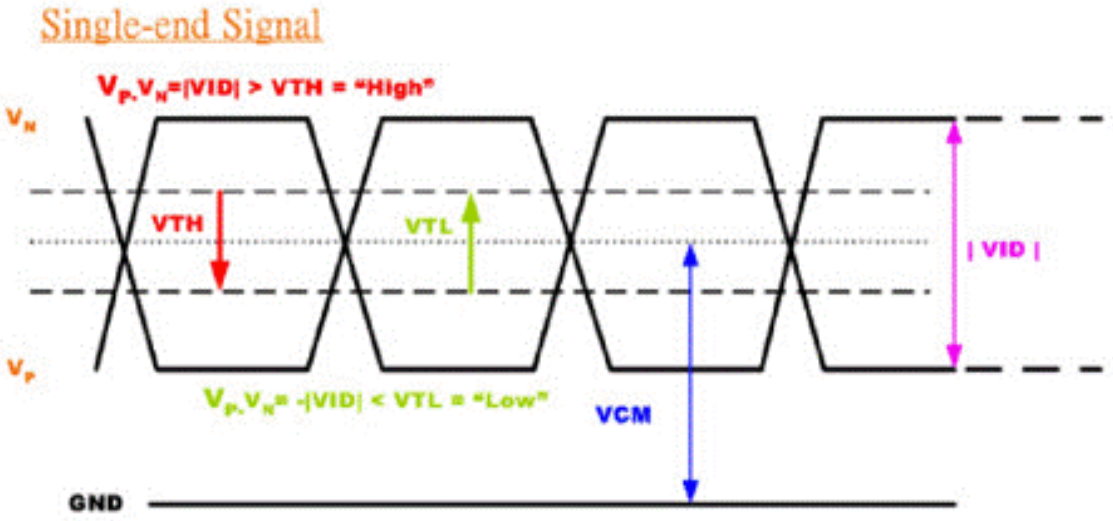
Display Port AUX_CH					
		Min	Typ	Max	Unit
VCM	Differential common mode voltage	0	**0.8**	2	V
VDiff $_{P-P}$	Differential peak to peak voltage	0.39	-	1.38	V

Remark: Reference VESA eDP standard

5.1.2.3 Display Port V_{HPD} signal

Display Port AUX_CH					
		Min	Typ	Max	Unit
V_{HPD}	HPD Voltage	2.25	**-**	3.6	V

Remark: Reference VESA eDP standard



Display Port AUX_CH					
		Min	Typ	Max	Unit
VCM	Differential common mode voltage	0	**0.8**	2	V
VDiff $_{P-P}$	Differential peak to peak voltage	0.39	-	1.38	V

Remark: Reference VESA eDP standard

5.1.2.4 Display Port V_{HPD} signal

Display Port AUX_CH					
		Min	Typ	Max	Unit
V_{HPD}	HPD Voltage	2.25	**-**	3.6	V

Remark: Reference VESA eDP standard

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	4.07	4.4	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	10,000	-	-	Hour	(Ta=25℃), Note 2 I_F=20 mA

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

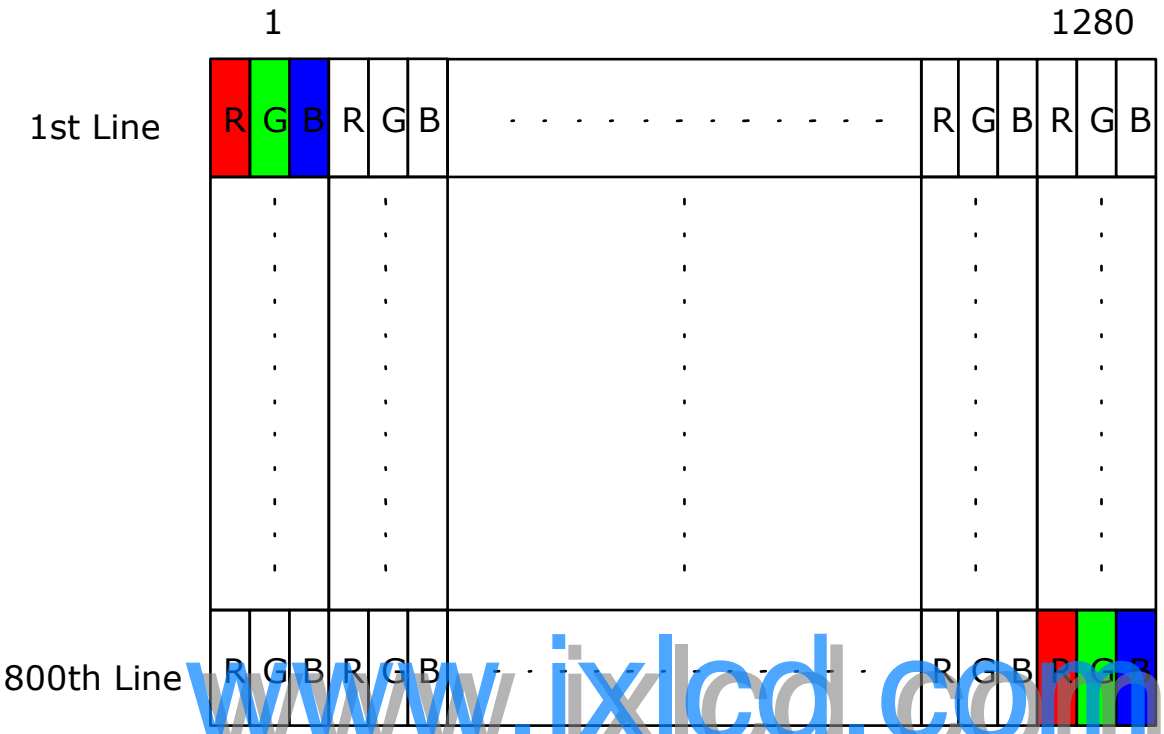
5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	200	--	1K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format

18bbp RGB Mapping to a One Lane Main Link

Lane 0
R0-5:0 | G0-5:4
G0-3:0 | B0-5:2
B0-1:0 | R1-5:0
G1-5:0 | B1-5:4
B1-3:0 | R2-5:2
R2-1:0 | G2-5:0
B2-5:0 | R3-5:4
R3-3:0 | G3-5:2
G3-1:0 | B3-5:0

6.3 Integration Interface Requirement

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

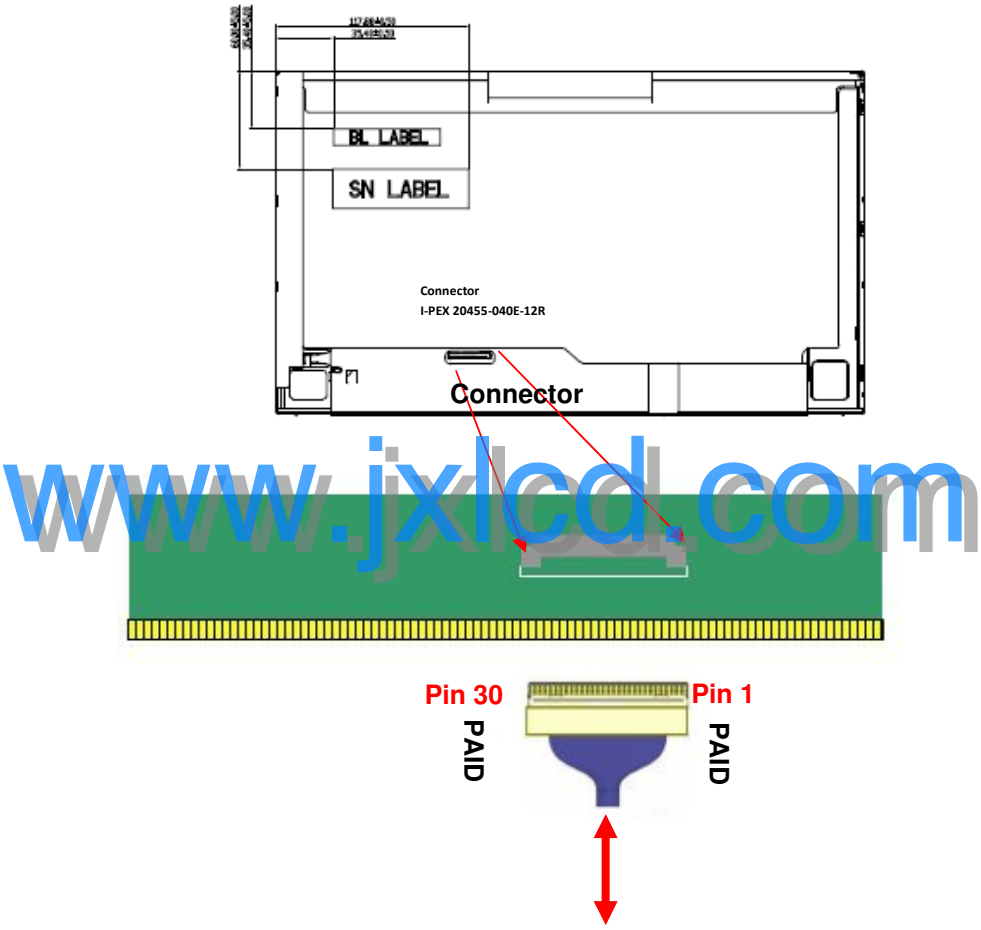
Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20455-030E-12 or compatible
Mating Housing/Part Number	IPEX 20453-030T-11or compatible

6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN#	Signal Name	Description
1	PAID	Conn. Continuity Test
2	H_GND	High Speed Ground
3	Lane1_N	Comp Signal Link Lane 1
4	Lane1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	BIST	LCD Panel Self Test Enable
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight ground
19	BL_GND	Backlight ground
20	BL_GND	Backlight ground
21	BL_GND	Backlight ground
22	NC	No Connection

23	BL_PWM_DIM	System PWM signal input
24	SMBUS_CLK	System PWM Data
25	SMBUS_DATA	No Connection (Reserve)
26	BL_PWR	Backlight power
27	BL_PWR	Backlight power
28	BL_PWR	Backlight power
29	BL_PWR	Backlight power
30	PAID	Conn. Continuity Test



Note1: Input signals shall be low or High-impedance state when VDD is off.

6.4 Interface Timing

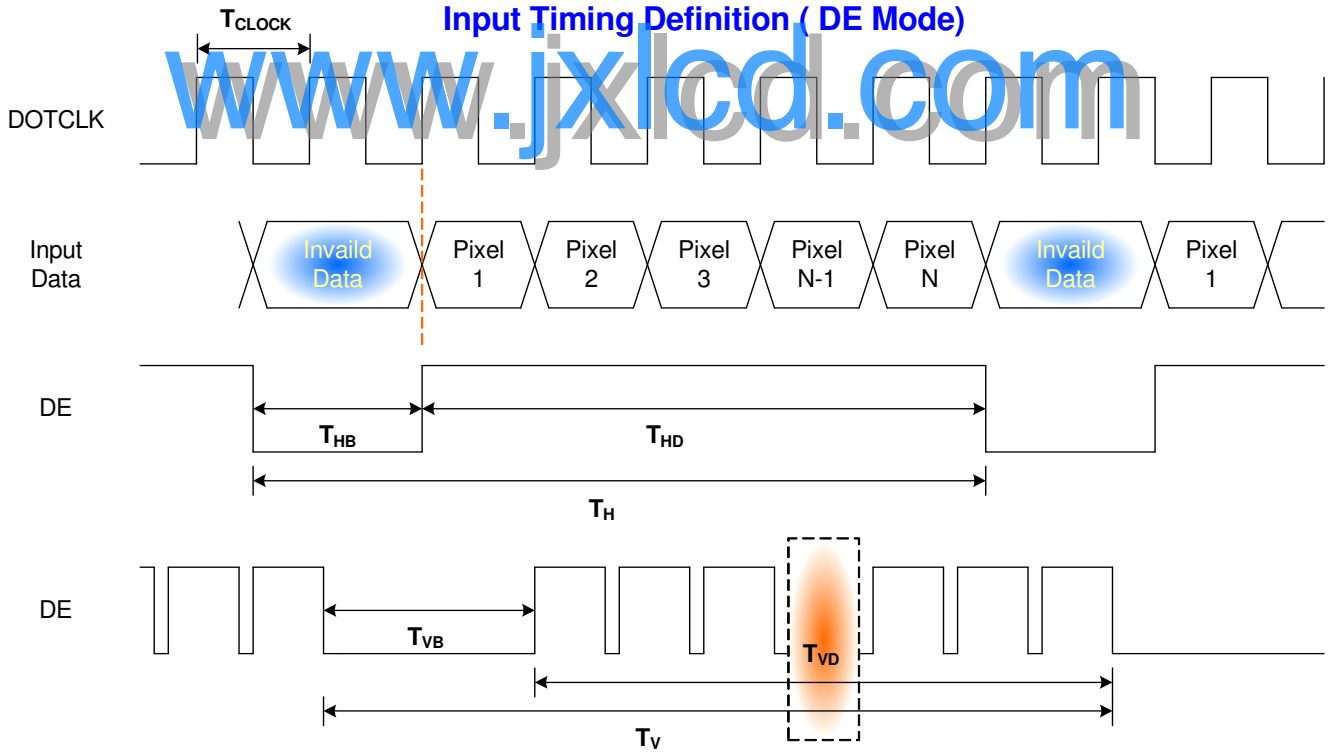
6.4.1 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

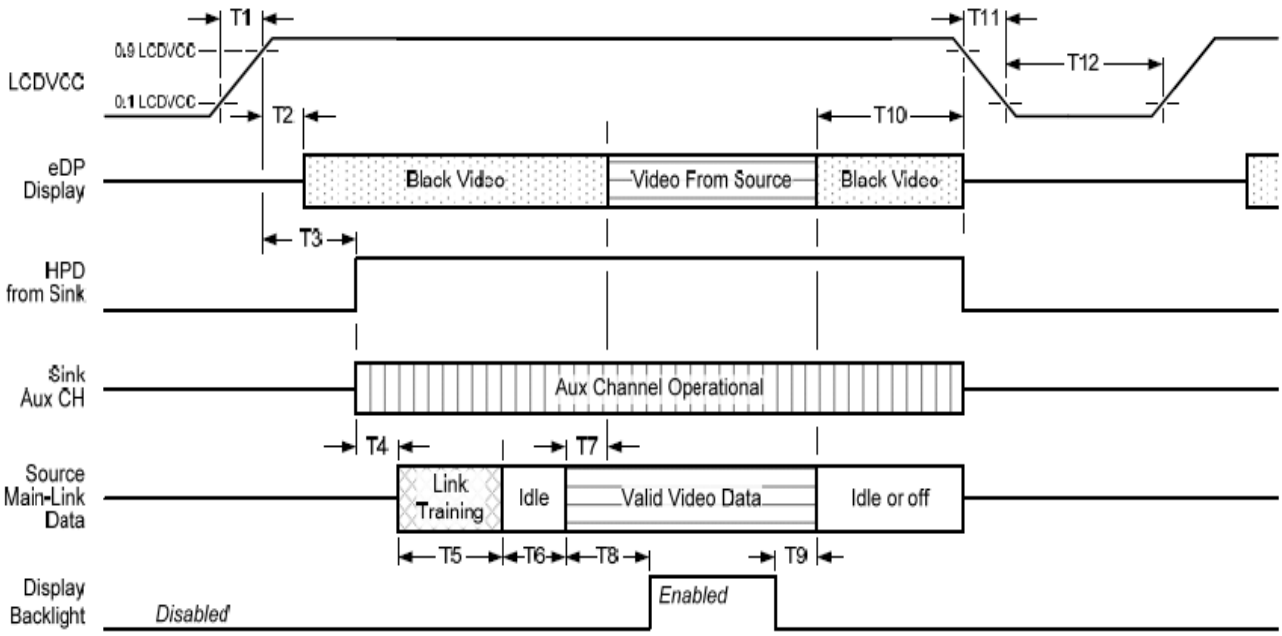
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	40	60	65	Hz
Clock frequency		1/ T_{Clock}	65	69	80	MHz
Vertical Section	Period	T_V	-	806	-	T_{Line}
	Active	T_{VD}	768			
	Blanking	T_{VB}	-	38	-	
Horizontal Section	Period	T_H	-	1426	-	T_{Clock}
	Active	T_{HD}	1366			
	Blanking	T_{HB}	-	160	-	

Note : DE mode only

6.4.2 Timing diagram

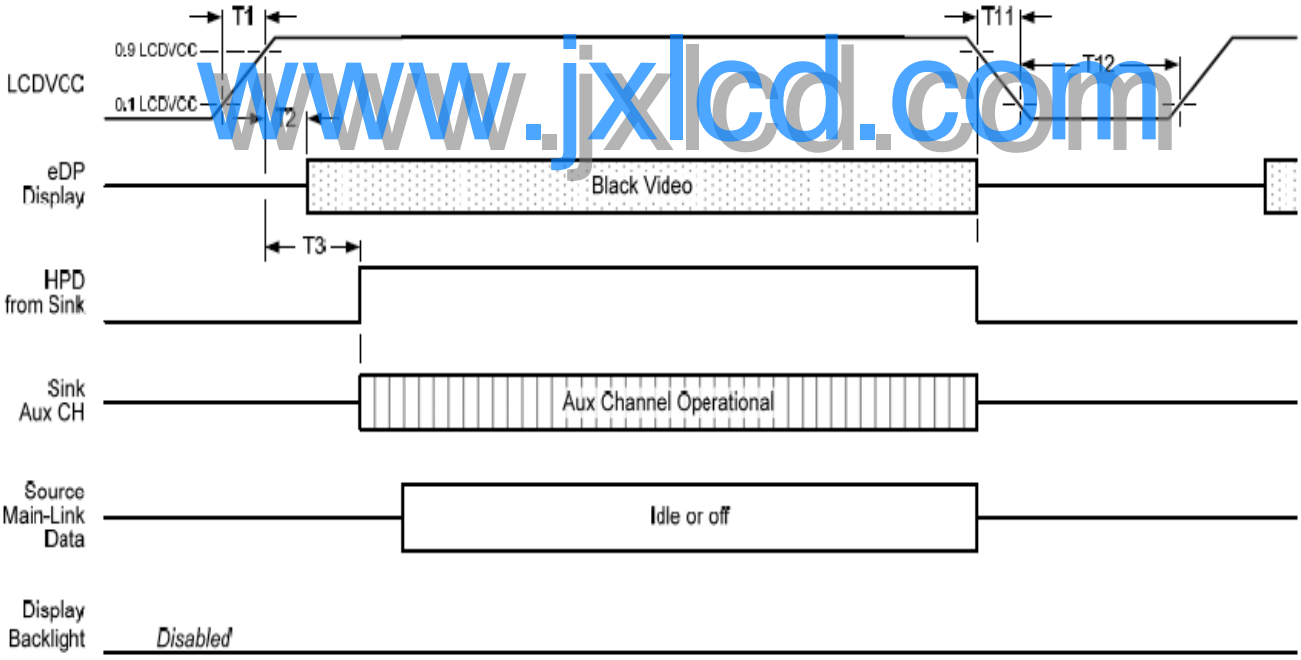


6.5 Power ON/OFF Sequence



Normal system operation.

Display Port AUX_CH transaction only:



AUX_CH transaction only

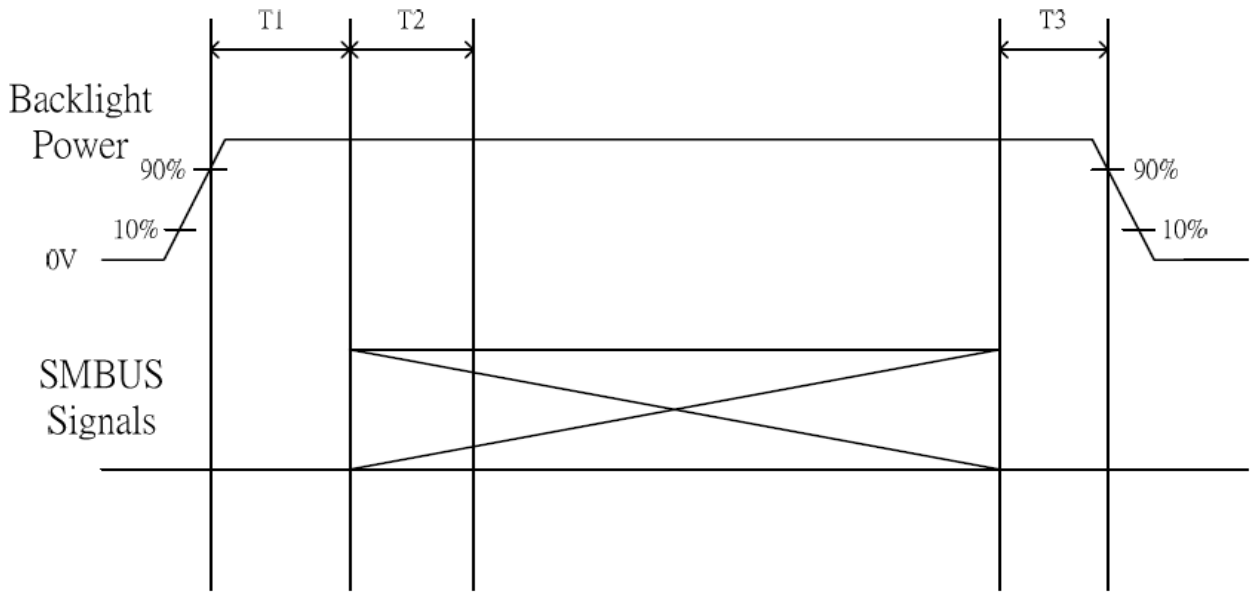
Parameter	Value		Units
	Min.	Max.	
T1	0.5	10	ms
T2	0	200	
T3	200	200	
T4	-	-	
T5	-	-	
T6	-	-	
T7	0	50	
T8	-	-	
T9	-	-	
T10	0	500	
T11	-	10	
T12	500	-	

Note 1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
- upon LCDVDD power on (with in T2 max)
- when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
- when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

LED on/off sequence is as follows. Interface signals are also shown in the chart :

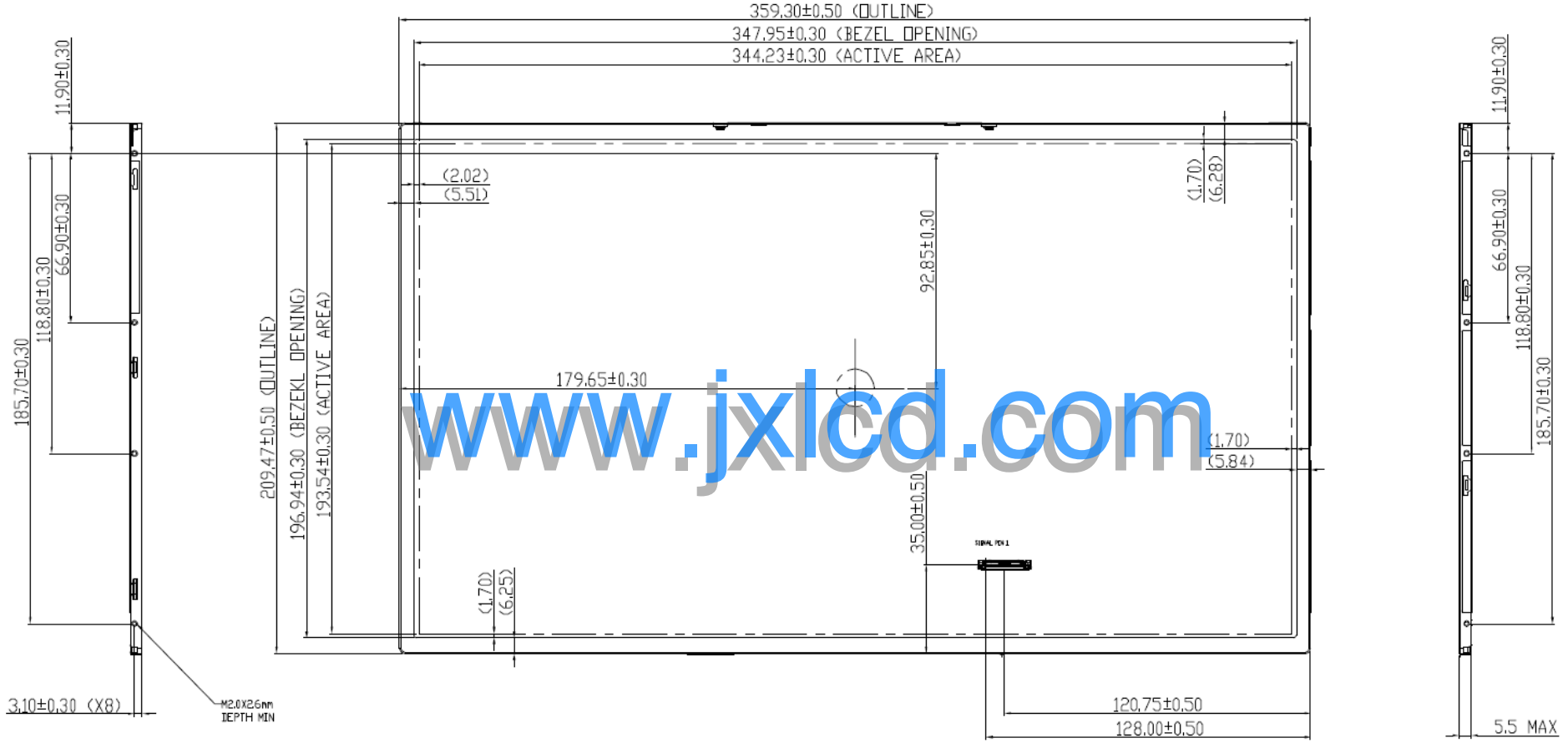


Power Sequence Timing				
Parameter	Value			Units
	Min.	Typ.	Max.	
T1	10	-	-	ms
T2	100	-	-	
T3	10	-	-	

Note: The duty of LED dimming signal should be more than 20% in T2.

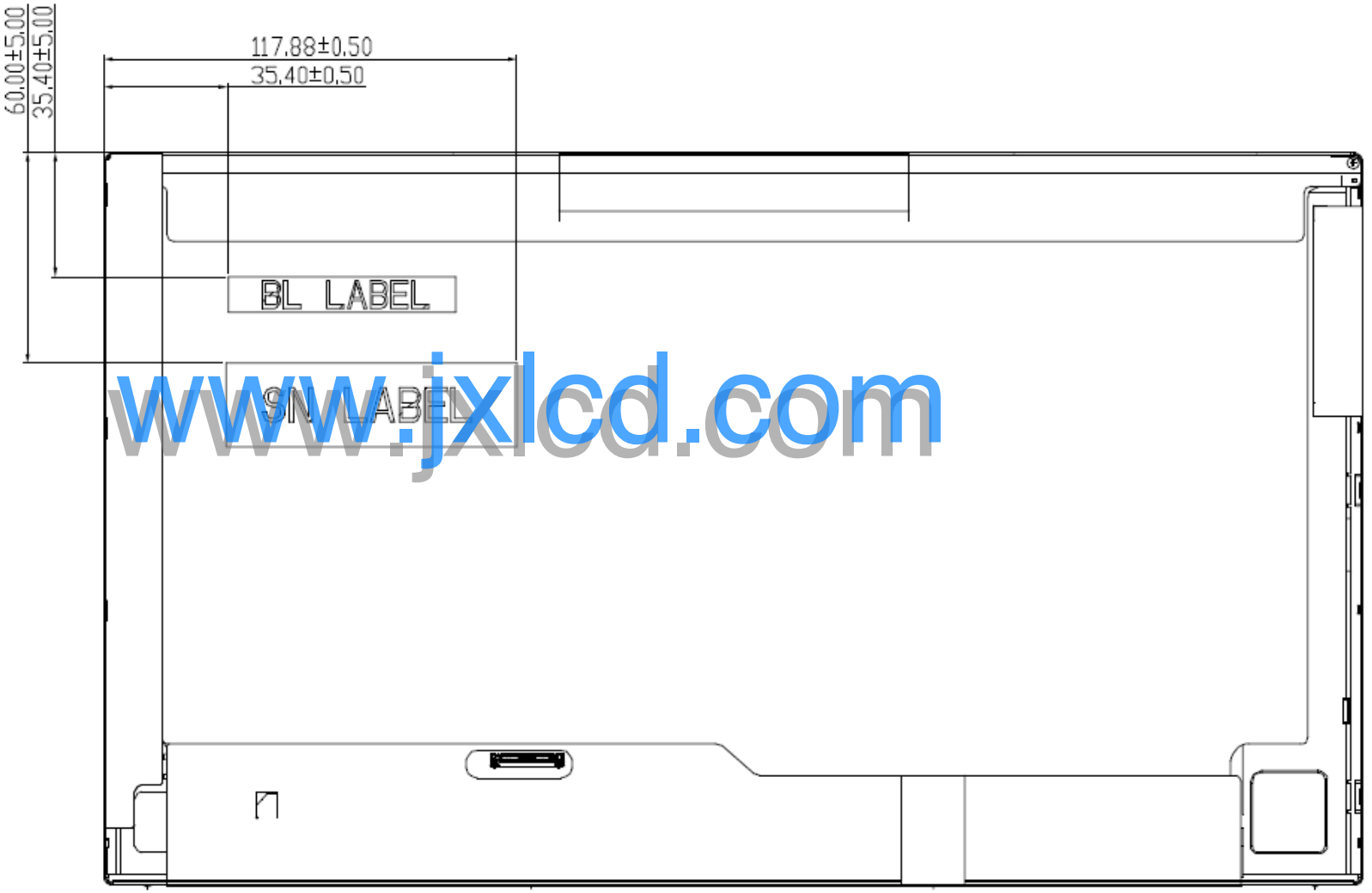
8. Mechanical Characteristics

8.1 LCM Outline Dimension



Front view 2D drawing

Remind RD Solid line and dotted line



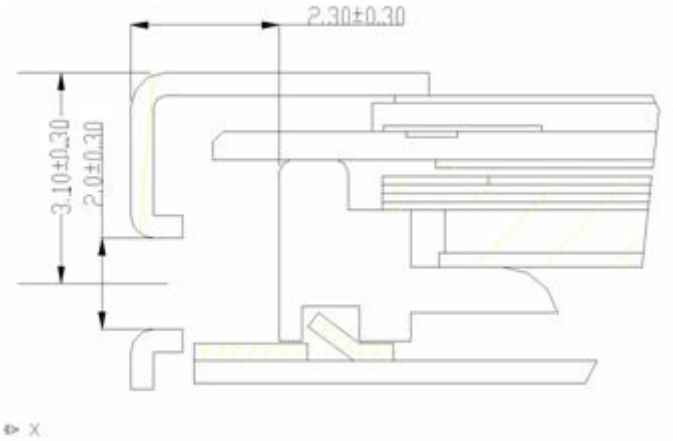
Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

8.2 Screw Hole Depth and Center Position

Maximum Screw penetration from side surface is 2.6 mm

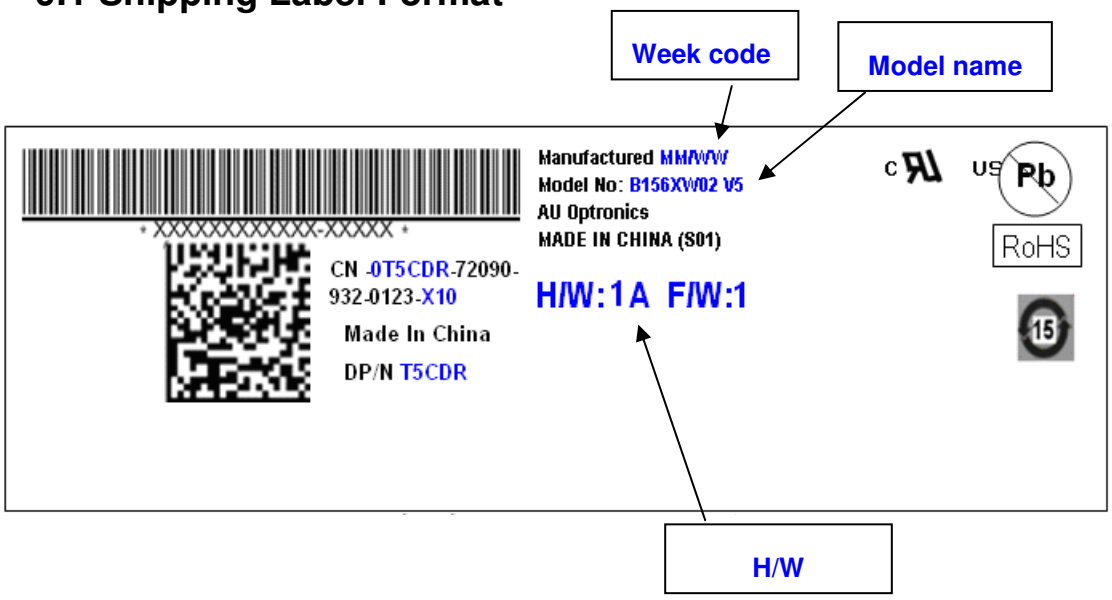
The center of screw hole center location is 3.1 ± 0.3mm from front surface

Screw Torque: Maximum 2.5 kgf-cm



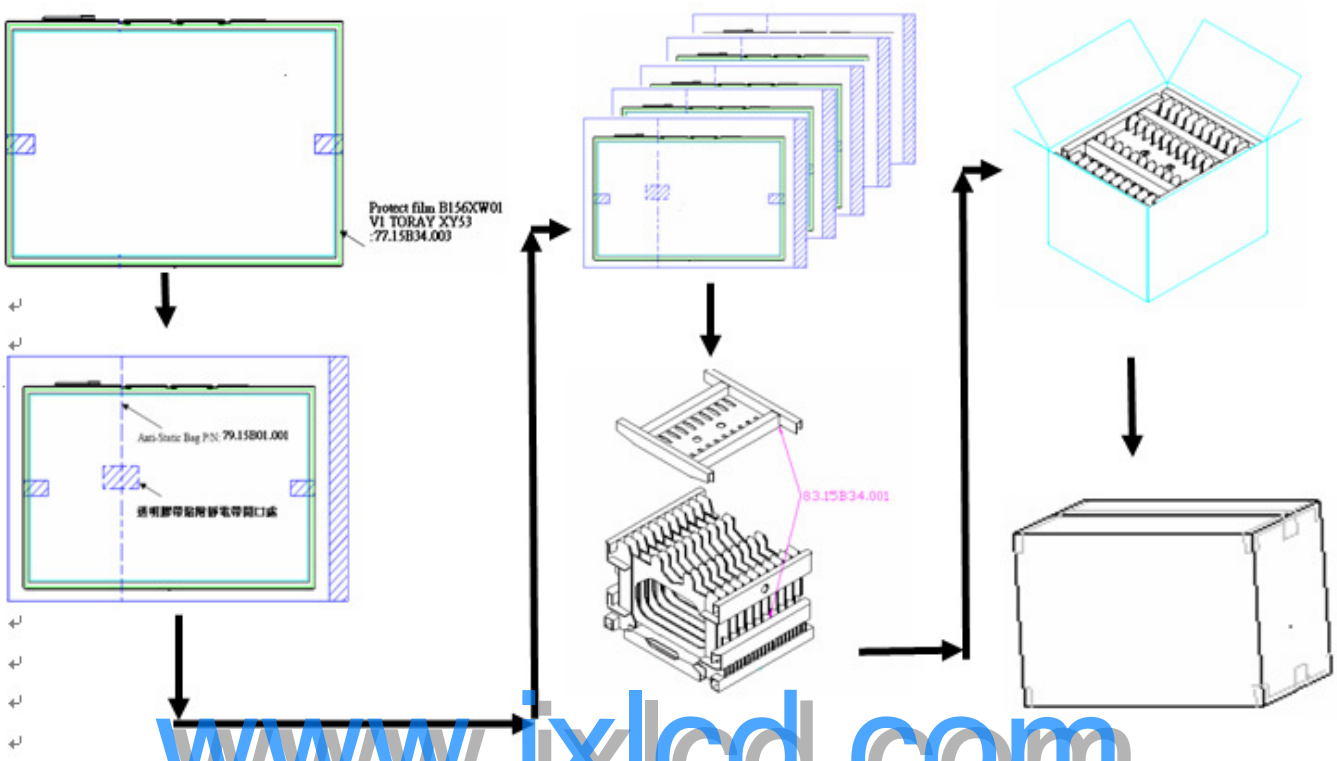
9. Shipping and Package

9.1 Shipping Label Format

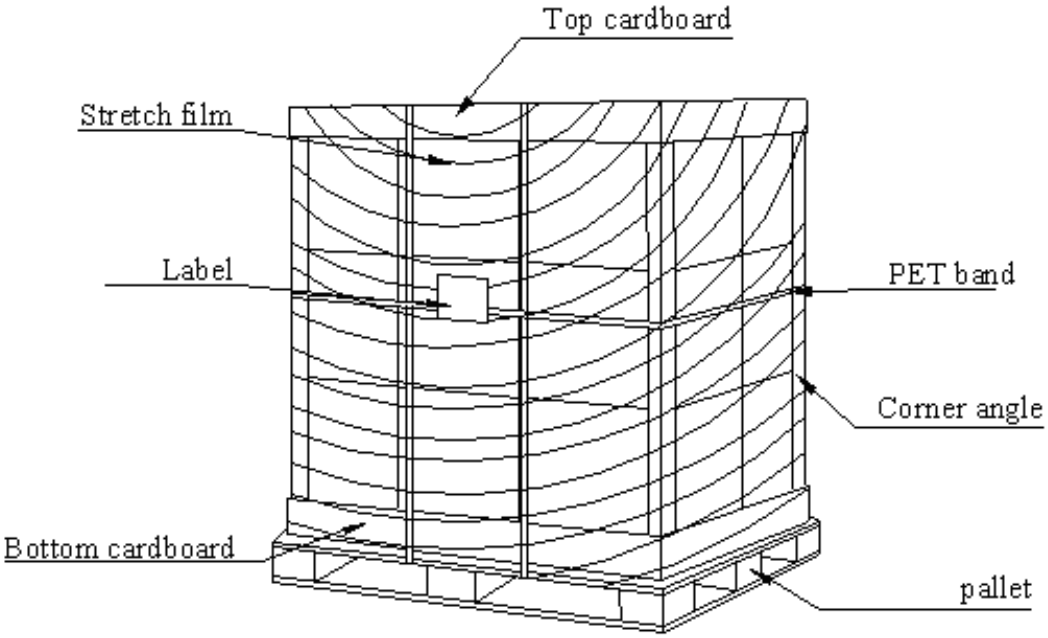


9.2 Carton Package

The outside dimension of carton is 437(L)mm x 369 (W)mm x 313 (H)mm



9.3 Shipping Package of Palletizing Sequence



10. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value
HEX		HEX	BIN	DEC
0	Header	00	00000000	0
1	Header	FF	11111111	255
2	Header	FF	11111111	255
3	Header	FF	11111111	255
4	Header	FF	11111111	255
5	Header	FF	11111111	255
6	Header	FF	11111111	255
7	Header	00	00000000	0
8	EISA manufacture code = 3 Character ID	06	00000110	6
9	EISA manufacture code (Compressed ASCII)	AF	10101111	175
0A	Panel Supplier Reserved – Product Code	EC	11101100	236
0B	Panel Supplier Reserved – Product Code	25	00100101	37
0C	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
0D	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
0E	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
0F	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
10	Week of manufacture	00	00000000	0
11	Year of manufacture	13	00010011	19
12	EDID structure version # = 1	01	00000001	1
13	EDID revision # = 3	04	00000100	4
14	Video I/P definition = Digital I/P (90 (6-bit) or A0 (8-Bit))	95	10010101	149
15	Max H image size = cm (Rounded to cm)	22	00100010	34
16	Max V image size = cm (Rounded to cm)	13	00010011	19
17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120	78	01111000	120
18	Feature support (no DPMS, Active off, RGB, timing BLK 1) ==> fix=0A	02	00000010	2
19	Red/Green Low bit (RxRy/GxGy)	C8	11001000	200
1A	Blue/White Low bit (BxBy/WxWy)	95	10010101	149
1B	Red X Rx =	9E	10011110	158
1C	Red Y Ry =	57	01010111	87
1D	Green X Rx =	54	01010100	84

1E	Green Y Ry =	92	10010010	146
1F	Blue X Rx =	26	00100110	38
20	Blue Y Ry =	0F	00001111	15
21	White X Rx =	50	01010000	80
22	White Y Ry =	54	01010100	84
23	Established timings 1 (00h if not used)	00	00000000	0
24	Established timings 2 (00h if not used)	00	00000000	0
25	Manufacturer's timings (00h if not used)	00	00000000	0
26	Standard timing ID1 (01h if not used)	01	00000001	1
27	Standard timing ID1 (01h if not used)	01	00000001	1
28	Standard timing ID2 (01h if not used)	01	00000001	1
29	Standard timing ID2 (01h if not used)	01	00000001	1
2A	Standard timing ID3 (01h if not used)	01	00000001	1
2B	Standard timing ID3 (01h if not used)	01	00000001	1
2C	Standard timing ID4 (01h if not used)	01	00000001	1
2D	Standard timing ID4 (01h if not used)	01	00000001	1
2E	Standard timing ID5 (01h if not used)	01	00000001	1
2F	Standard timing ID5 (01h if not used)	01	00000001	1
30	Standard timing ID6 (01h if not used)	01	00000001	1
31	Standard timing ID6 (01h if not used)	01	00000001	1
32	Standard timing ID7 (01h if not used)	01	00000001	1
33	Standard timing ID7 (01h if not used)	01	00000001	1
34	Standard timing ID8 (01h if not used)	01	00000001	1
35	Standard timing ID8 (01h if not used)	01	00000001	1
36	Pixel Clock/10,000 (LSB)	12	00010010	18
37	Pixel Clock/10,000 (MSB)	1B	00011011	27
38	Horizontal Active = pixels (lower 8 bits)	56	01010110	86
39	Horizontal Blanking (Thbp) = pixels (lower 8 bits)	5A	01011010	90
3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	50	01010000	80
3B	Vertical Active = lines	00	00000000	0
3C	Vertical Blanking (Tvbp) = lines (DE Blanking typ. for DE only panels)	19	00011001	25
3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000	48

3E	Horizontal Sync, Offset (Thfp) = pixels	30	00110000	48
3F	Horizontal Sync, Pulse Width = pixels	20	00100000	32
40	Vertical Sync, Offset (Tvfp) = 3 lines Sync Width = 1 lines	36	00110110	54
41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
42	Horizontal Image Size = mm	58	01011000	88
43	Vertical image Size = mm	C1	11000001	193
44	Horizontal Image Size / Vertical image size	10	00010000	16
45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
47	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	1A	00011010	26
48	Pixel Clock/10,000 (LSB)	0C	00001100	12
49	Pixel Clock/10,000 (MSB)	12	00010010	18
4A	Horizontal Active = xxxx pixels (lower 8 bits)	56	01010110	86
4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	5A	01011010	90
4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	50	01010000	80
4D	Vertical Active = xxxx lines	00	00000000	0
4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	19	00011001	25
4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000	48
50	Horizontal Sync, Offset (Thfp) = xxxx pixels	30	00110000	48
51	Horizontal Sync, Pulse Width = xxxx pixels	20	00100000	32
52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	36	00110110	54

53	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
54	Horizontal Image Size =xxx mm	58	01011000	88
55	Vertical image Size = xxx mm	C1	11000001	193
56	Horizontal Image Size / Vertical image size	10	00010000	16
57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
59	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	1A	00011010	26
5A	Flag	00	00000000	0
5B	Flag	00	00000000	0
5C	Flag	00	00000000	0
5D	Data Type Tag: Alphanumeric Data String (ASCII) ==> fix=FE	FE	11111110	254
5E	Flag	00	00000000	0
5F	Dell P/N 1st Character	54	01010100	84
60	Dell P/N 2nd Character	35	00110101	53
61	Dell P/N 3rd Character	43	01000011	67
62	Dell P/N 4th Character	44	01000100	68
63	Dell P/N 5th Character	52	01010010	82
64	**EDID Revision** **Bit[6:0] See charts below** **Bit[7] 0: X-rev, 1: A-rev**	0A	00001010	10
65	Manufacturer P/N	42	01000010	66
66	Manufacturer P/N	31	00110001	49
67	Manufacturer P/N	35	00110101	53
68	Manufacturer P/N	36	00110110	54
69	Manufacturer P/N	58	01011000	88
6A	Manufacturer P/N	57	01010111	87
6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	32	00110010	50
6C	Flag	00	00000000	0

6D	Flag	00	00000000	0
6E	Flag	00	00000000	0
6F	Data Type Tag: Manufacturer Specified Data 00 ==>fix=00	00	00000000	0
70	Flag	00	00000000	0
71	SMBUS Value = Nits ==> fix=00(for M09)	00	00000000	0
72	SMBUS Value = Nits ==> fix=00(for M09)	41	01000001	65
73	SMBUS Value = Nits ==> fix=00(for M09)	21	00100001	33
74	SMBUS Value = Nits ==> fix=00(for M09)	19	00011001	25
75	SMBUS Value = Nits ==> fix=00(for M09)	00	00000000	0
76	SMBUS Value = Nits ==> fix=00(for M09)	00	00000000	0
77	SMBUS Value = Nits ==> fix=00(for M09)	00	00000000	0
78	SMBUS Value = Nits ==> fix=00(for M09)	00	00000000	0
79	Bit[1:0] 00: reserved, 01: single LVDS, 10: dual LVDS, 11: reserved Bit[2] 0: No RTC support, 1: RTC support Bit[7:3] Reserved	09	00001001	9
7A	Bit[0] 0: No BIST support, 1: BIST support Bit[7:1] Reserved	01	00000001	1
7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010	10
7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000	0
7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	5C	01011100	92
			SUM	1B00