




Product Specification

AU OPTRONICS CORPORATION

(V) Preliminary Specifications

() Final Specifications

Module	17.3”(17.25”) FHD Color TFT-LCD with LED Backlight design
Model Name	B173HW01 V0 (H/W:0A)
Note ()	<i>LED Backlight with driving circuit design</i>

Customer	Date
Checked & Approved by	Date
_____	_____
<p>Note: This Specification is subject to change without notice.</p>	

Approved by	Date
<u>Beyond Yang</u>	<u>03/20/2009</u>
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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2009/02/24	All	First Edition for Customer		

1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B173HW01 V0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the FHD (1920(H) x 1080(V)) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B173HW01 V0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	17.3W”(17.25)			
Active Area	[mm]	381.888 X 214.812			
Pixels H x V		1920x3(RGB) x1080			
Pixel Pitch	[mm]	0.1989X0.1989			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (ILED=20mA) (Note: ILED is LED current)	[cd/m ²]	300 typ. (5 points average) 270 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points) / 1.35 max. (13 points)			
Contrast Ratio		500 typ			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	9.0 max. (Include Logic and Blu power)			
Weight	[Grams]	590 max.			
Physical Size without inverter, bracket.	[mm]		Min.	Typ.	Max.
		Length	397.6	398.1	398.6
		Width	232.3	232.8	233.3
		Thickness	---	---	6.0
Electrical Interface		2 channel LVDS			
Glass Thickness	[mm]	0.5			
Surface Treatment		Glare, Hardness 4H,			
Support Color		262K colors (RGB 6-bit)			



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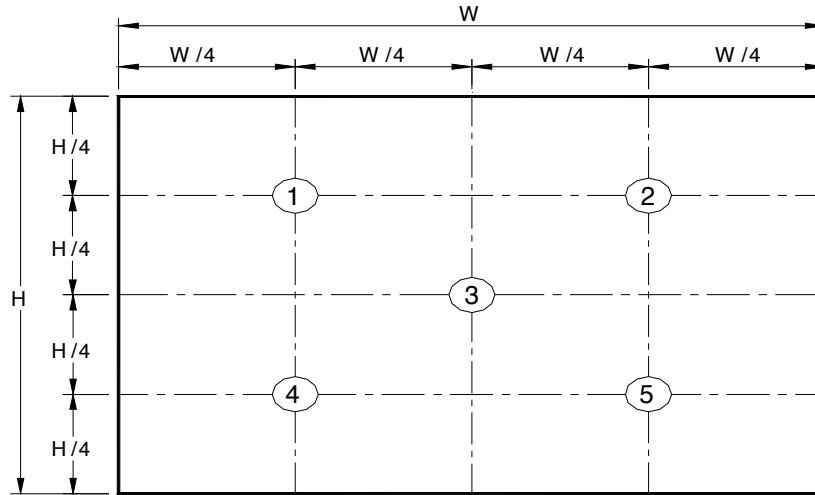
Temperature Range Operating	[°C]	0 to +50
Storage (Non-Operating)	[°C]	-20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note	
White Luminance I _{LED} =20mA		5 points average	270	300	---	cd/m²	1, 4, 5.	
Viewing Angle	θ_R	Horizontal (Right) CR = 10 (Left)	60	70	---	degree	4, 9	
	θ_L		60	70	---			
	ϕ_H	Vertical (Upper) CR = 10 (Lower)	45	60	---			
	ϕ_L		50	60	---			
Luminance Uniformity	δ_{5P}	5 Points	---	---	1.25		1, 3, 4	
Contrast Ratio	CR		400	500	---			4, 6
Cross talk	%				4			4, 7
Response Time	T_r	Rising	---	TBD	---	msec	4, 8	
	T_f	Falling	---	TBD	---			
	T_{RT}	Rising + Falling	---	8	16			
Color / Chromaticity Coodinates	Red	R_x	CIE 1931	---	TBD	---	4	
		R_y		---	TBD	---		
	Green	G_x		---	TBD	---		
		G_y		---	TBD	---		
	Blue	B_x		---	TBD	---		
		B_y		---	TBD	---		
	White	W_x		0.283	0.313	0.343		
		W_y		0.299	0.329	0.359		
NTSC	%		---	72	---			

Note 1: 5 points position (Ref: Active area)

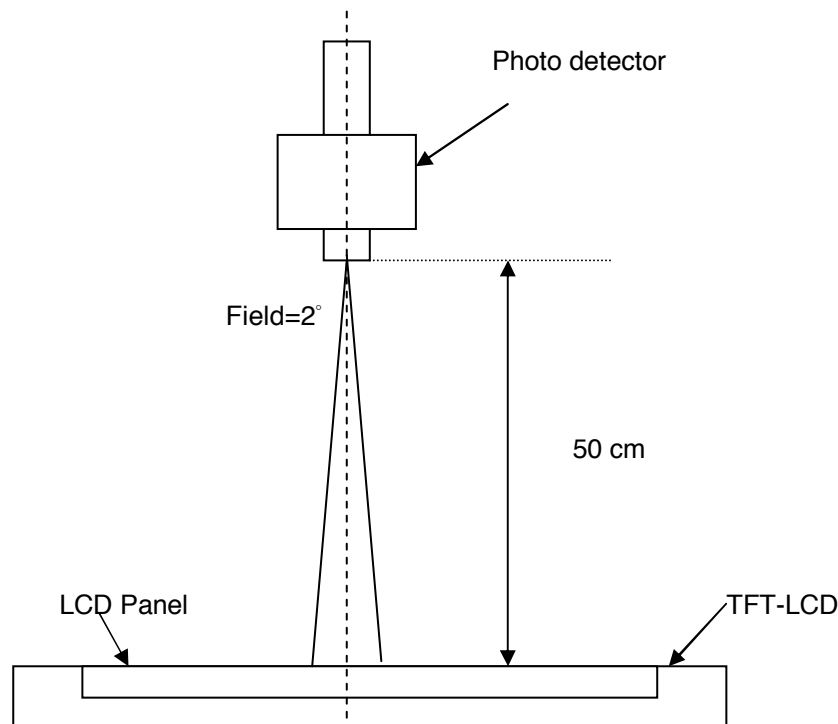


Note 2: The luminance uniformity of 5 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{w5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

Note 3: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 4 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points · $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 5 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

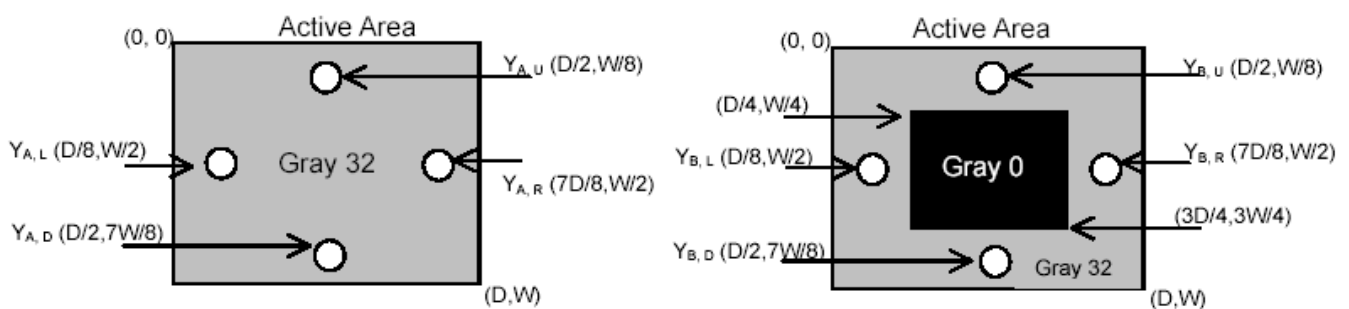
Note 6 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

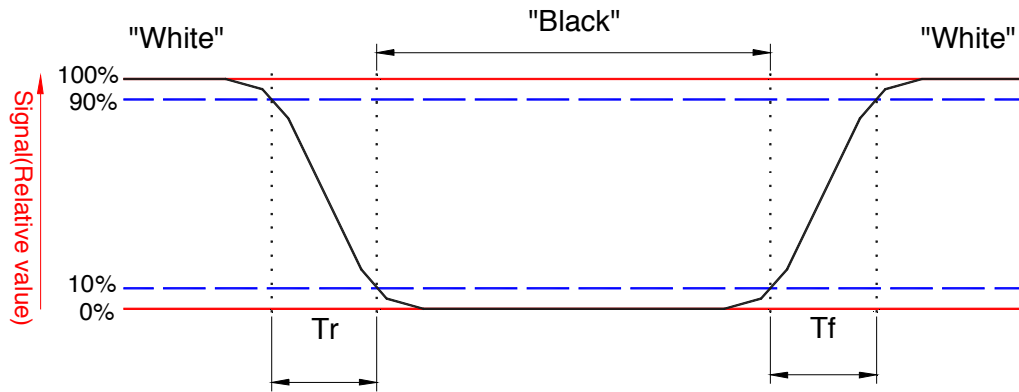
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



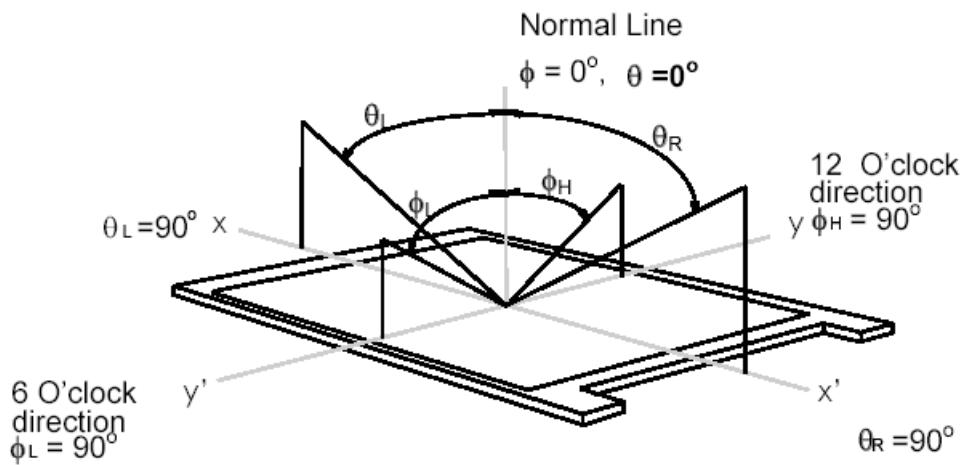
Note 7: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



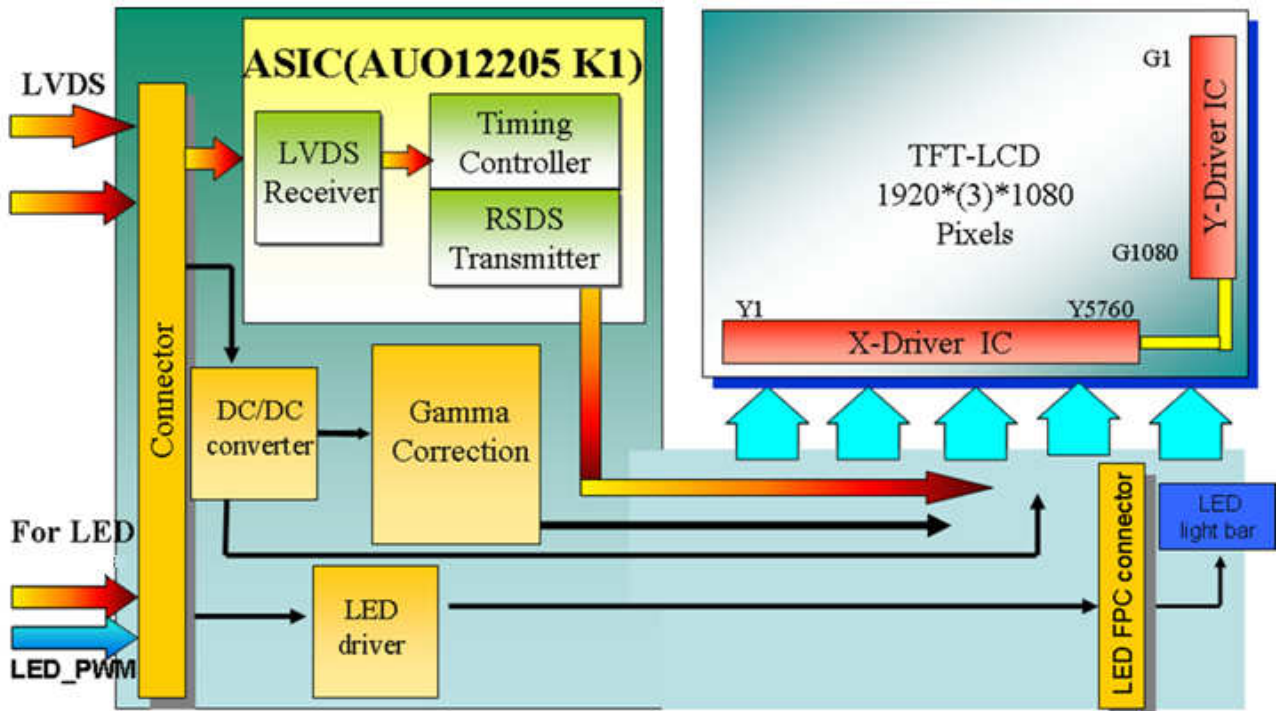
Note 8. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (ϕ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 17.3 inches wide Color TFT/LCD 40 Pin (Two CH/connector Module)



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

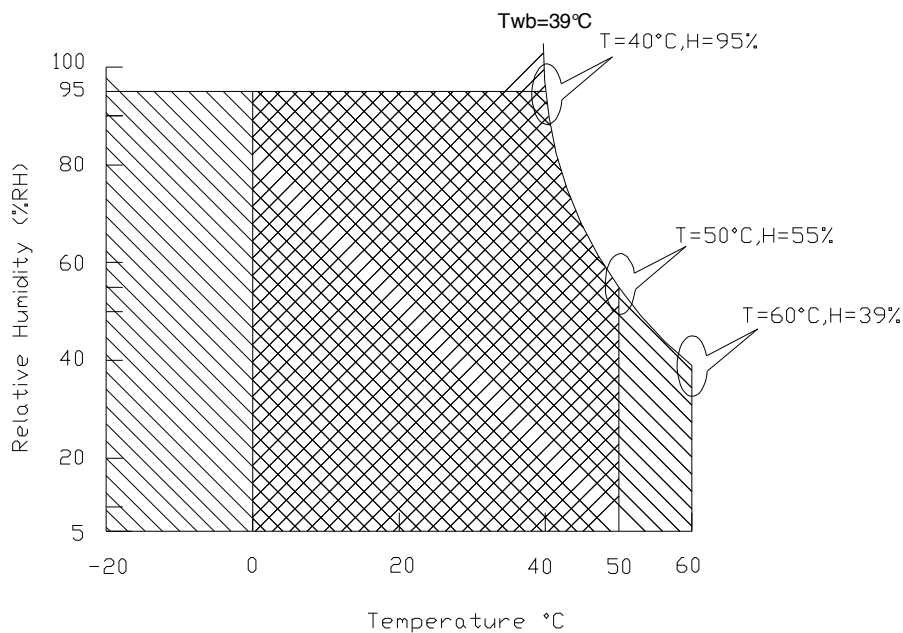
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

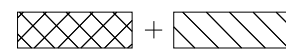
Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range



5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

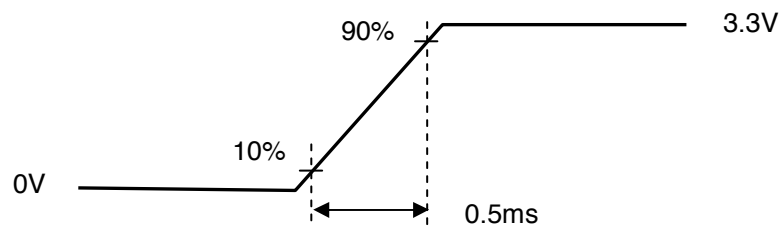
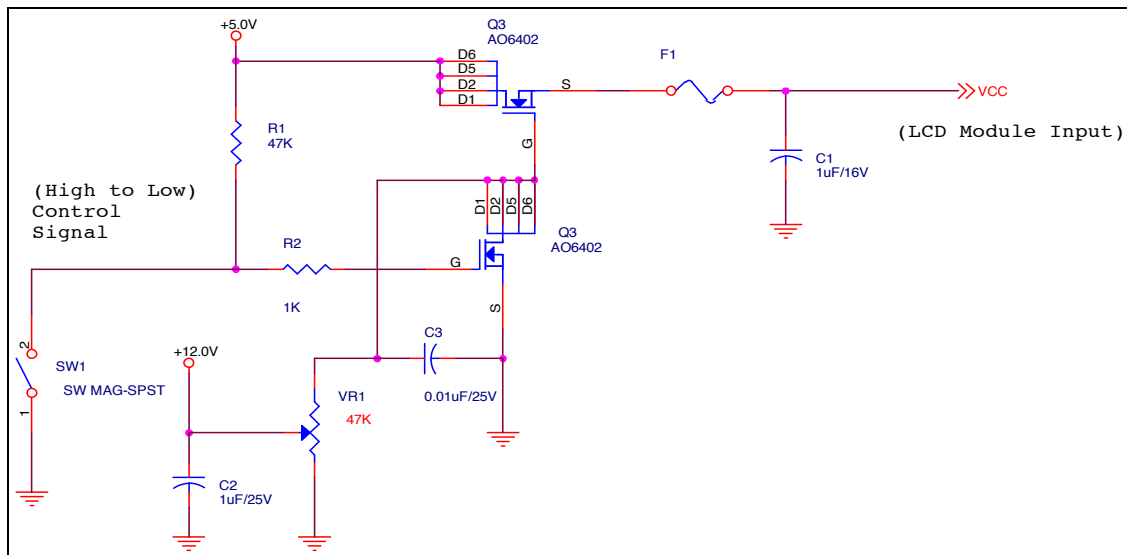
The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	2	[Watt]	Note 1/2
IDD	IDD Current	-	350	600	[mA]	Note 1/2
IRush	Inrush Current	-	-	2000	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern

Note 2 : Typical Measurement Condition: Mosaic Pattern

Note 3 : Measure Condition



Vin rising time

5.1.2 Signal Electrical Characteristics

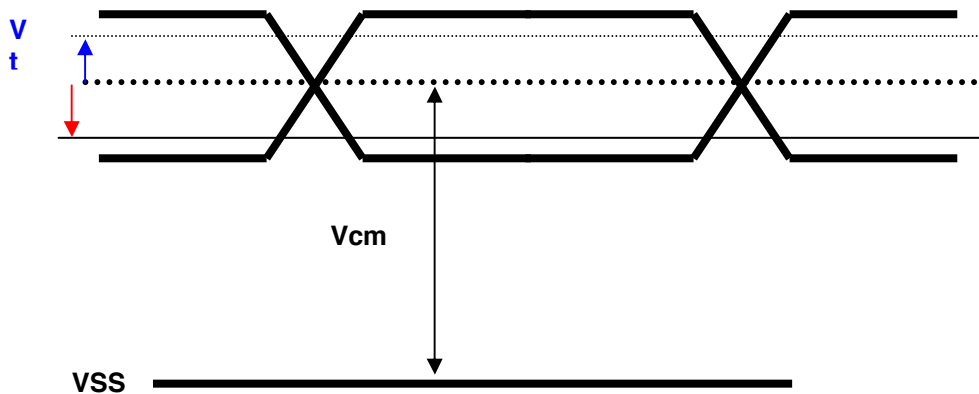
Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of THC63LVDF84A (Thine Electronics Inc.) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)	-	100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100	-	[mV]
Vcm	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform





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5.2 Backlight Unit

LED Parameter guideline for LED driving selection (Ref. Remark 1)

Parameter	Symbol	Min	Typ	Max	Units	Condition
LED Forward Voltage	V_F	3.0	3.2	3.4	[Volt]	(Ta=25°C)
LED Forward Current	I_F		20		[mA]	(Ta=25°C)
LED Power consumption	P_{LED}		6		[Watt]	(Ta=25°C) Note 1
LED Life-Time	N/A	10,000	-	-	Hour	(Ta=25°C) $I_F=20$ mA Note 2
Output PWM frequency	F_{PWM}	100	200	20K	Hz	
Duty ratio	--	5	--	100	%	

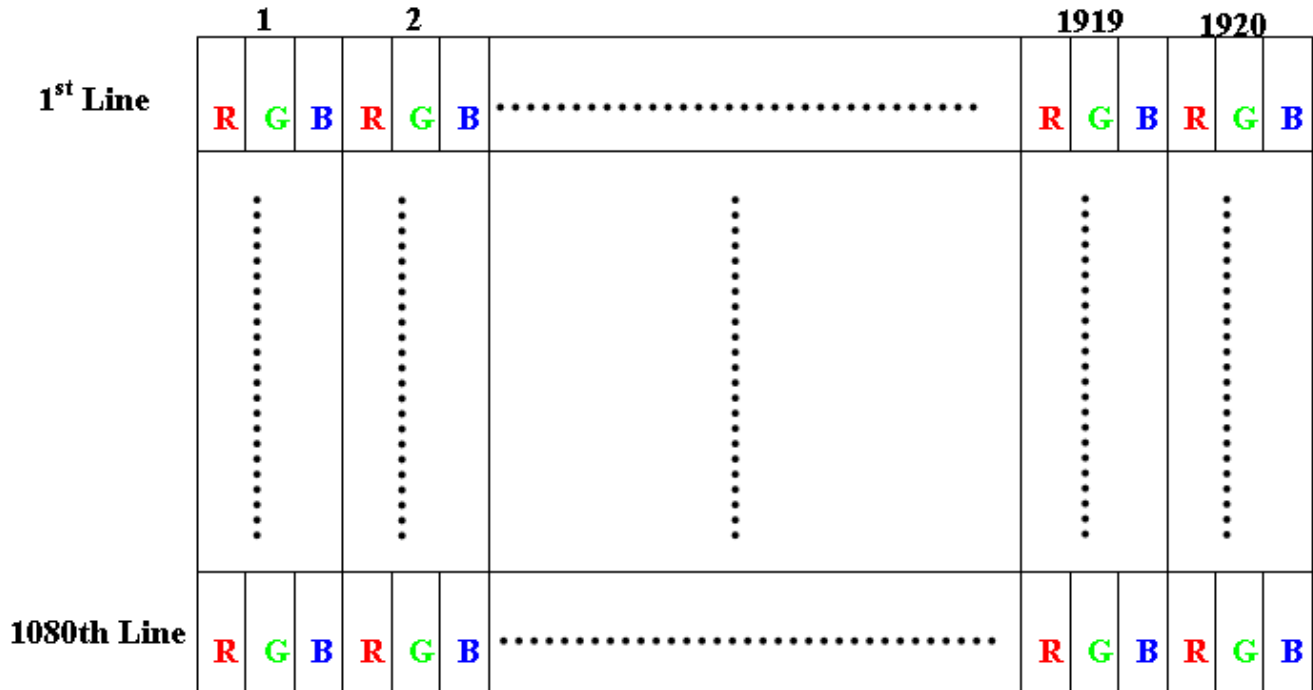
Note 1: Calculator value for reference $P_{LED} = V_F$ (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

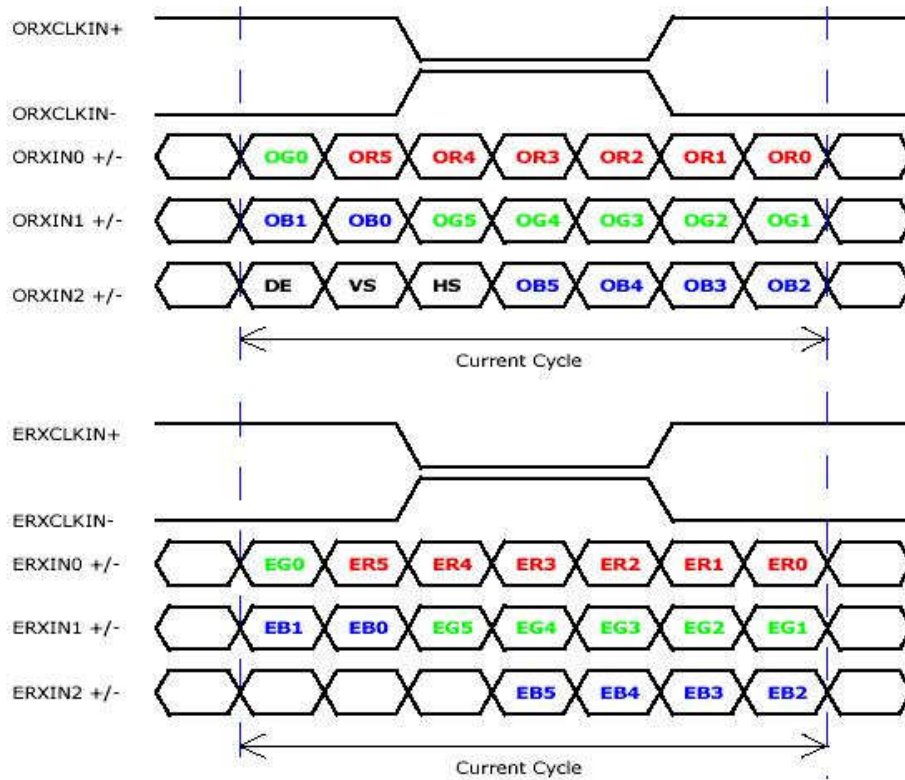
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the



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		falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.



6.3 Integration Interface and Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN#	Signal Name	Description
1	DIAG_LOOP	Pin 1 & 34 must be connected together on the PCB board
2	VDD	Power Supply, 3.3 V (typical)
3	VDD	Power Supply, 3.3 V (typical)
4	V EEDID	DDC 3.3V power
5	TEST	Panel Self Test
6	Clk EEDID	DDC Clock
7	DATA EEDID	DDC Data
8	Odd_Rin0-	- LVDS differential data input (R0-R5, G0) (odd pixels)
9	Odd_Rin0+	+ LVDS differential data input (R0-R5, G0) (odd pixels)
10	VSS	Ground – Shield
11	Odd_Rin1-	- LVDS differential data input (G1-G5, B0-B1) (odd pixels)
12	Odd_Rin1+	+ LVDS differential data input (G1-G5, B0-B1) (odd pixels)
13	VSS	Ground – Shield
14	Odd_Rin2-	- LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
15	Odd_Rin2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
16	VSS	Ground – Shield
17	Odd_ClkIN-	- LVDS differential clock input (odd pixels)
18	Odd_ClkIN+	+ LVDS differential clock input (odd pixels)
19	VSS	Ground – Shield
20	Even_Rin0-	- LVDS differential data input (R0-R5, G0) (even pixels)
21	Even_Rin0+	+ LVDS differential data input (R0-R5, G0) (even pixels)
22	VSS	Ground – Shield
23	Even_Rin1-	- LVDS differential data input (G1-G5, B0-B1) (even pixels)
24	Even_Rin1+	+ LVDS differential data input (G1-G5, B0-B1) (even pixels)
25	VSS	Ground – Shield
26	Even_Rin2-	- LVDS differential data input (B2-B5, HS, VS, DE) (even pixels)
27	Even_Rin2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (even pixels)
28	VSS	Ground – Shield
29	Even_ClkIN-	- LVDS differential clock input (even pixels)
30	Even_ClkIN+	+ LVDS differential clock input (even pixels)
31	VSSLED	Ground – LED
32	VSSLED	Ground – LED
33	VSSLED	Ground – LED
34	DIAG_LOOP	Pin 1 & 34 must be connected together on the PCB board

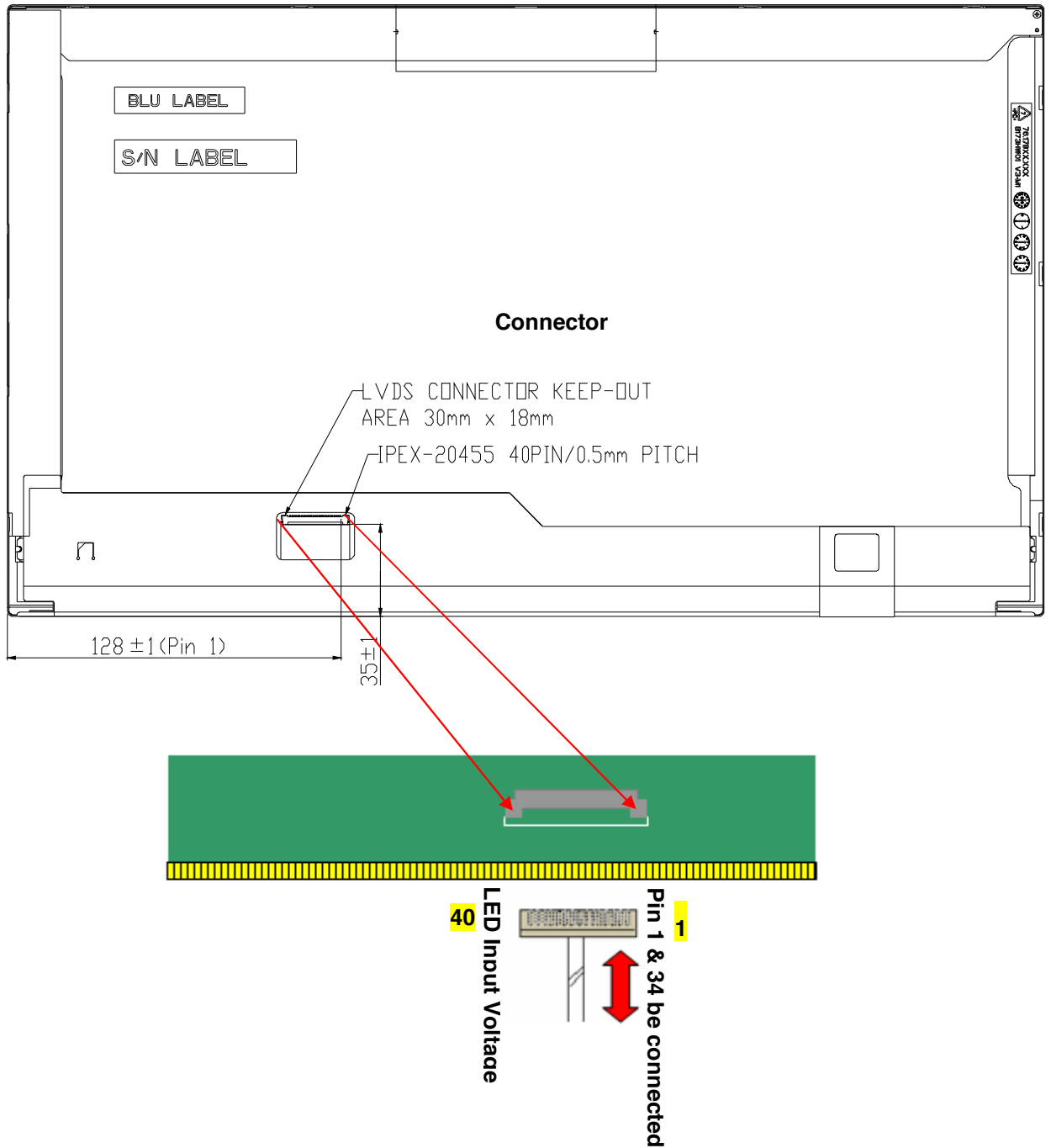


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35	PWM	System PWM Signal Input (+3.3V Swing)
36	LED_EN	LED enable pin (+3.3V Input)
37	NC	NC
38	VDDLED	6V – 21V LED power
39	VDDLED	6V – 21V LED power
40	VDDLED	6V – 21V LED power

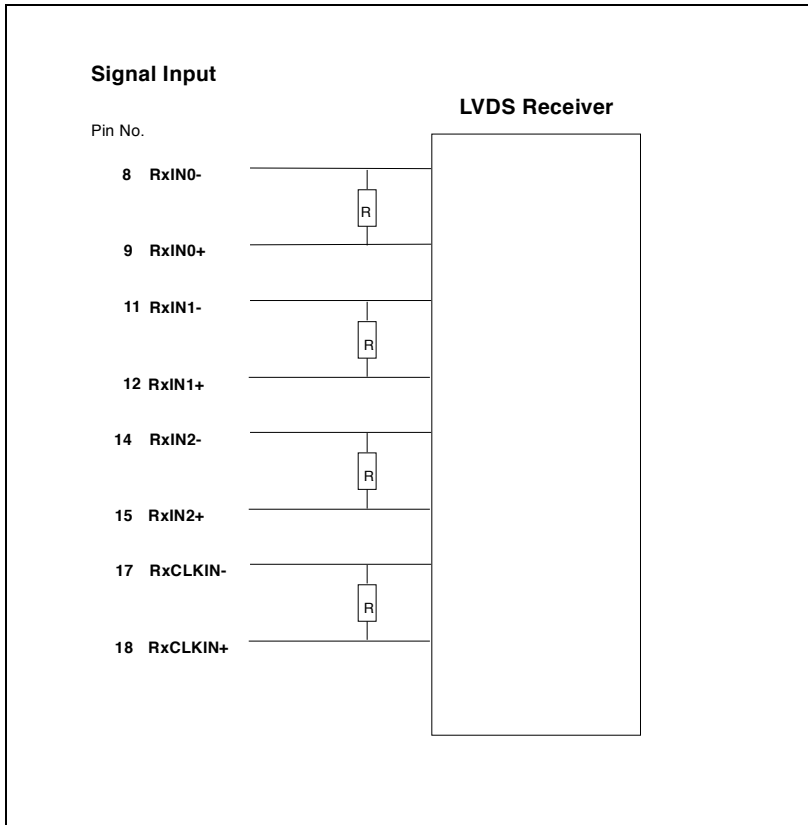
Note1: Start from right side



Note2: Input signals shall be low or High-impedance state when VDD is off.

internal circuit of LVDS inputs are as following.

The module uses a 100ohm resistor between positive and negative data lines of each receiver input



6.4 Interface Timing

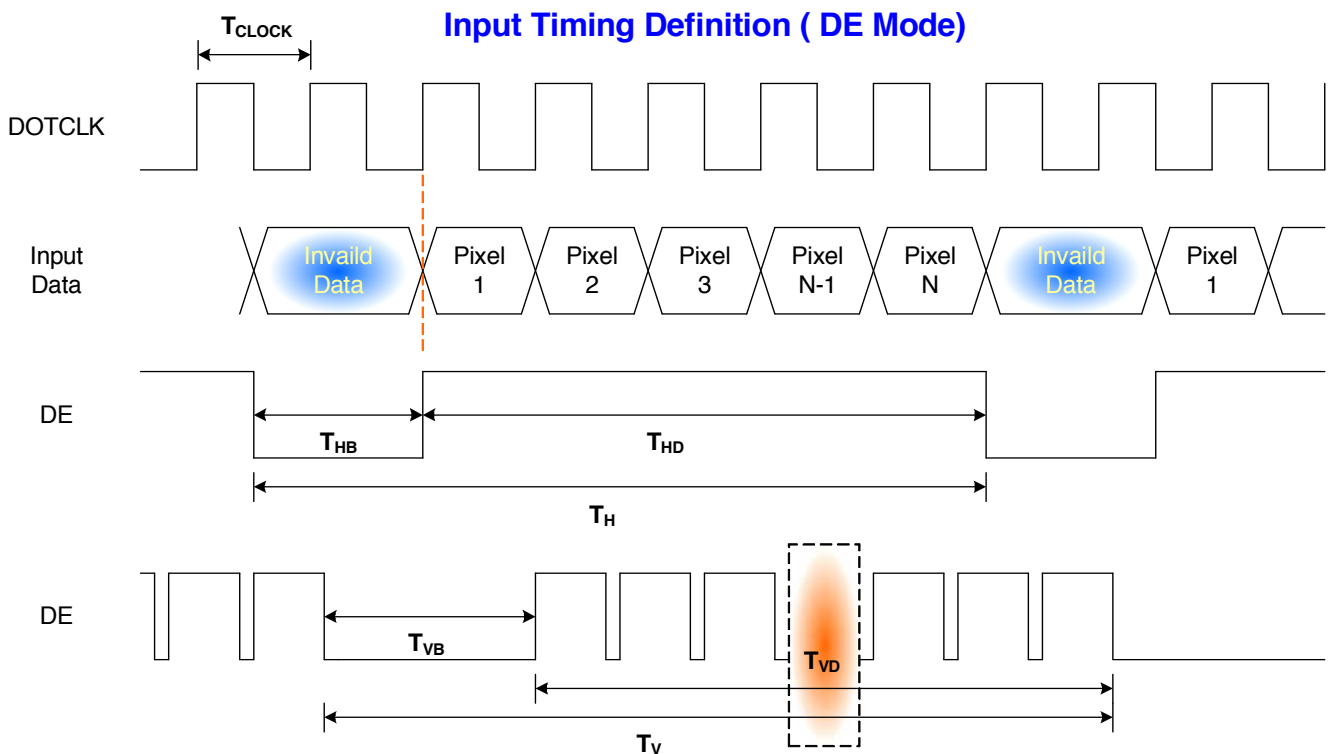
6.4.1 Timing Characteristics

Basically, interface timings should match the 1920X1080 / 60Hz manufacturing guide line timing.

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Frame Rate	-	50	60	-	Hz	
Clock frequency	$1/T_{Clock}$	64.63	71.2	85	MHz	
Vertical Section	Period	T_V	1088	1130	-	T_{Line}
	Active	T_{VD}	1080			
	Blanking	T_{VB}	8	50	-	
Horizontal Section	Period	T_H	990	1050	-	T_{Clock}
	Active	T_{HD}	1920			
	Blanking	T_{HB}	30	90	-	

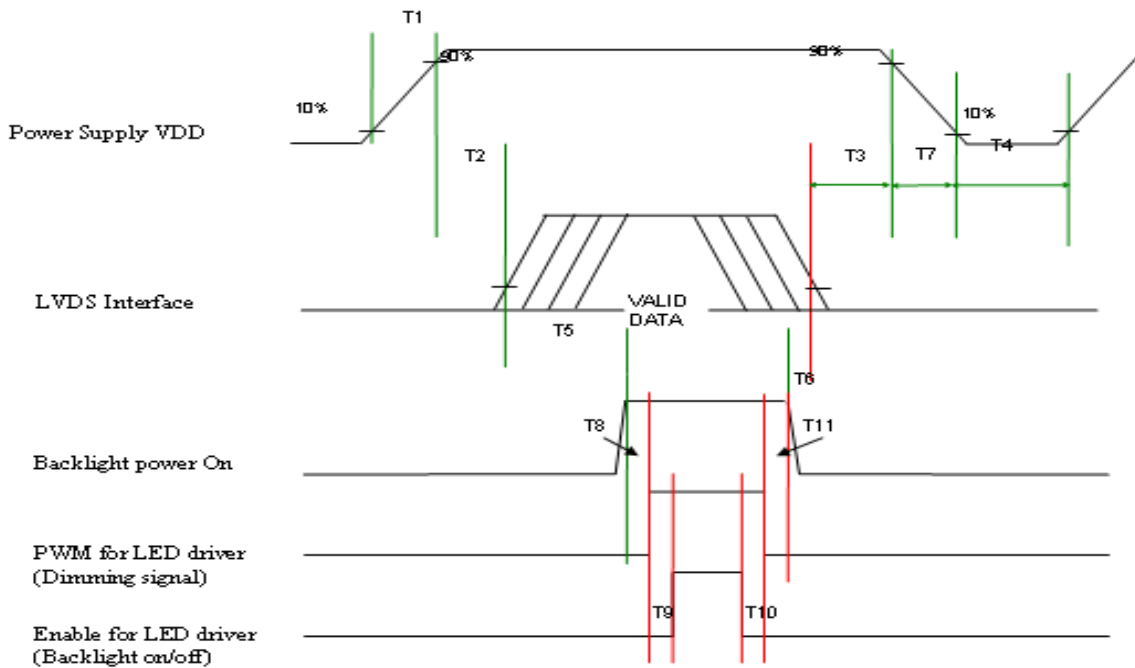
Note : DE mode only

6.4.2 Timing diagram



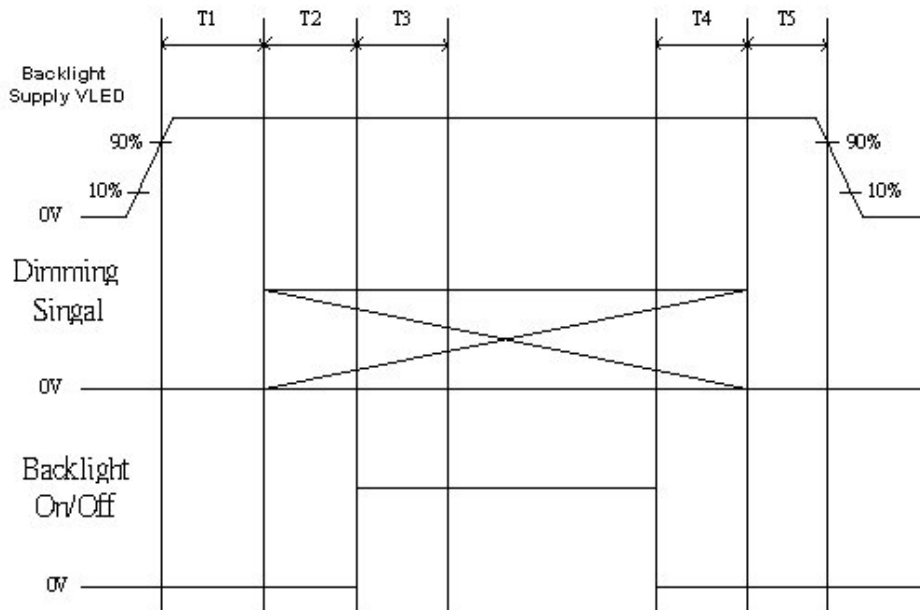
6.5 Power ON/OFF Sequence

VDD power on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	5	-	50	(ms)
T3	0.5	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0.5	-	10	(ms)
T8	10	---	---	(ms)
T9	10	---	---	(ms)
T10	10	---	---	(ms)
T11	10	---	---	(ms)

LED on/off sequence is as follows. Interface signals are also shown in the chart.



Symbol	Values			Unit
	Min	Typ	Max	
T1	10	---	---	ms
T2	10	---	---	
T3	50	---	---	
T4	0	---	---	
T5	10	---	---	

Note: The duty of LED dimming signal should be more than 5% in T2 and T3.



7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or Compatible
Type / Part Number	IPEX 20455-040E-12A or Compatible
Mating Housing/Part Number	IPEX 20453-040T-11 or Compatible



8. LED Driving Specification

8.1 Connector Description

It is an integrative interface and combines into LVDS connector. The type and mating refer to section 7.

8.2 Pin Assignment

Ref. to 6.3



9. Vibration and Shock Test

9.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

9.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side



10. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C, 90%RH, 300h	
High Temperature Operation	Ta= 50°C, Dry, 300h	
Low Temperature Operation	Ta= 0°C, 300h	
High Temperature Storage	Ta= 60°C, 35%RH, 300h	
Low Temperature Storage	Ta= -20°C, 50%RH, 250h	
Thermal Shock Test	Ta=-20°C to 60°C, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost
. Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

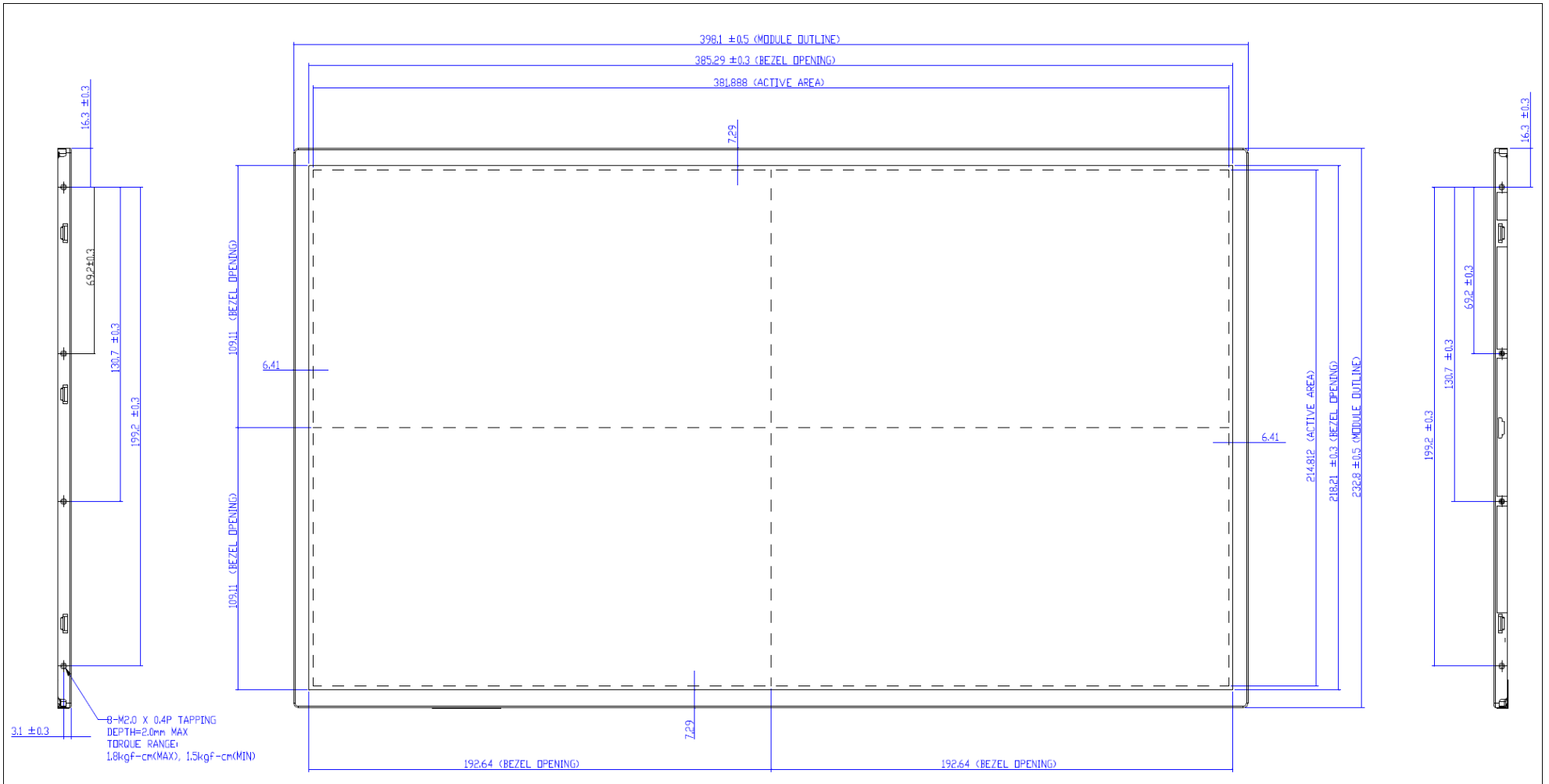


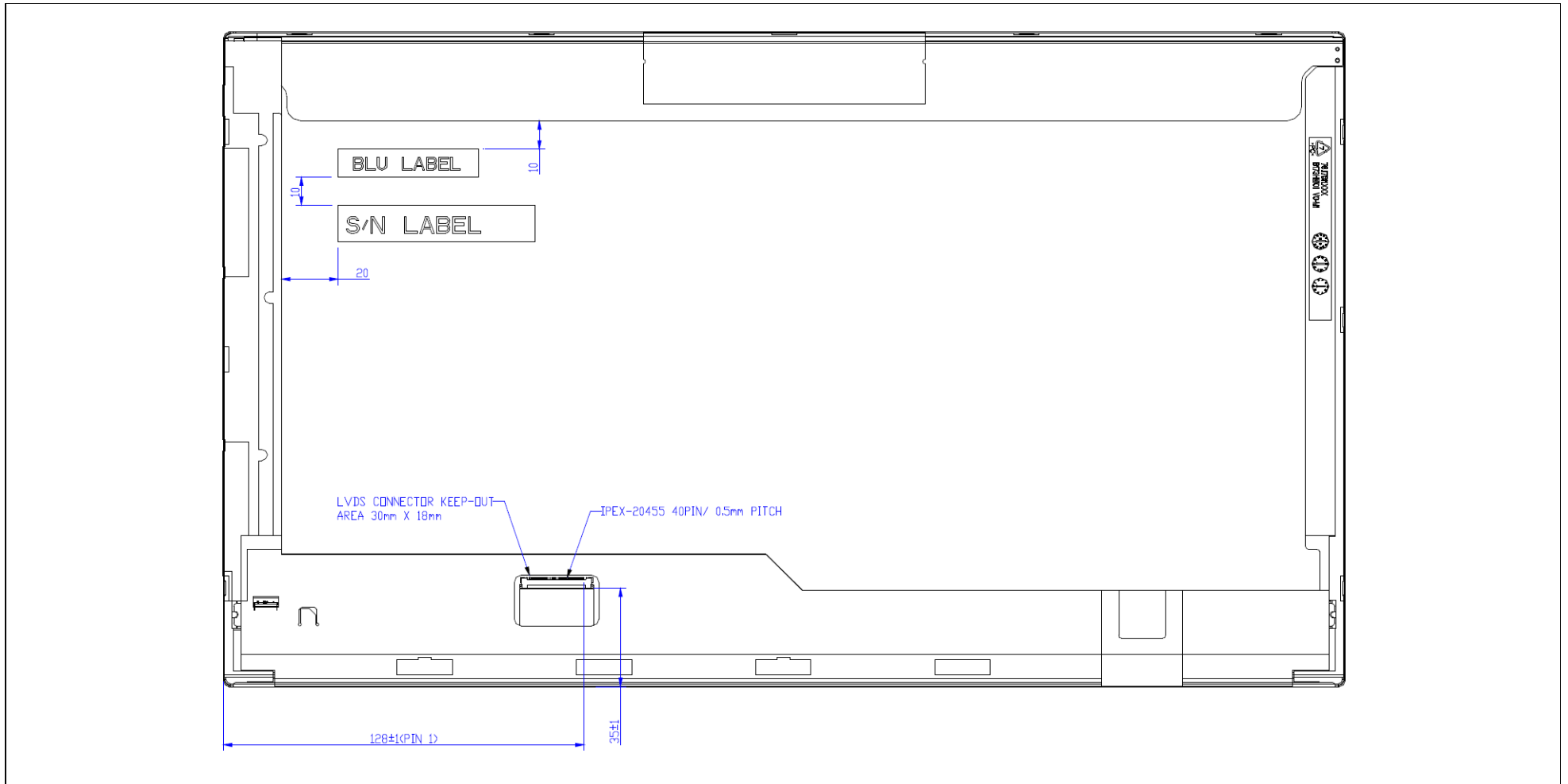
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11. Mechanical Characteristics

11.1 LCM Outline Dimension





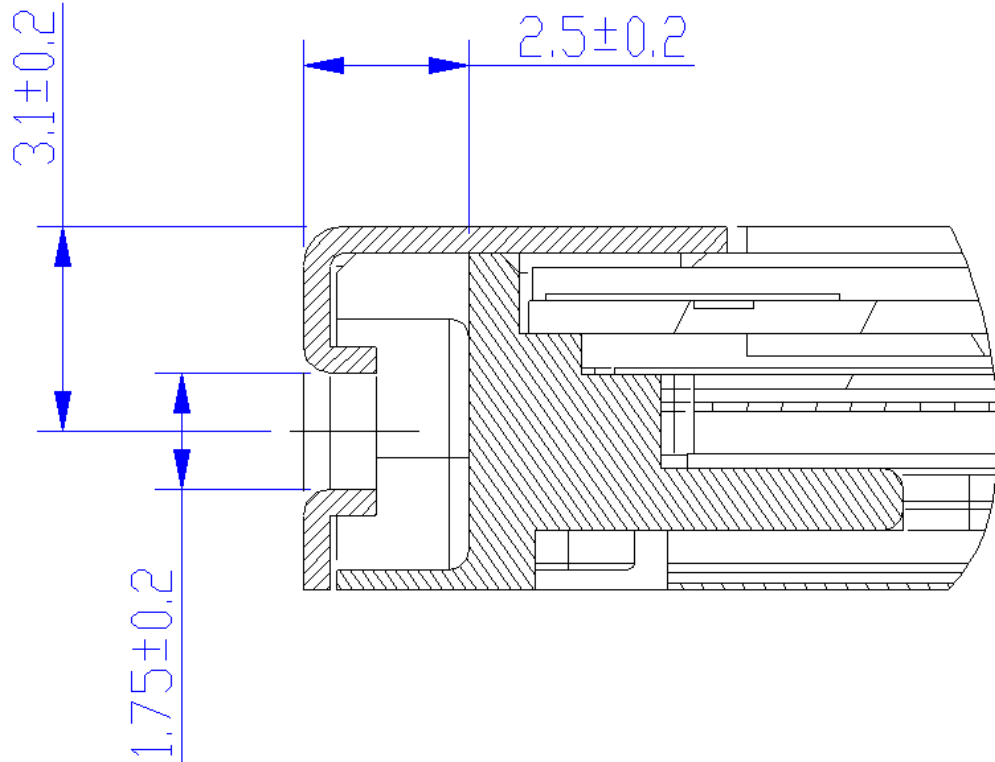
Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

11.2 Screw Hole Depth and Center Position

Screw hole depth, from side surface = 2.5 ± 0.2 mm (See drawing)

Screw hole center location, from front surface = 3.1 ± 0.2 mm (See drawing)

Screw Torque: Maximum 2.5 kgf-cm



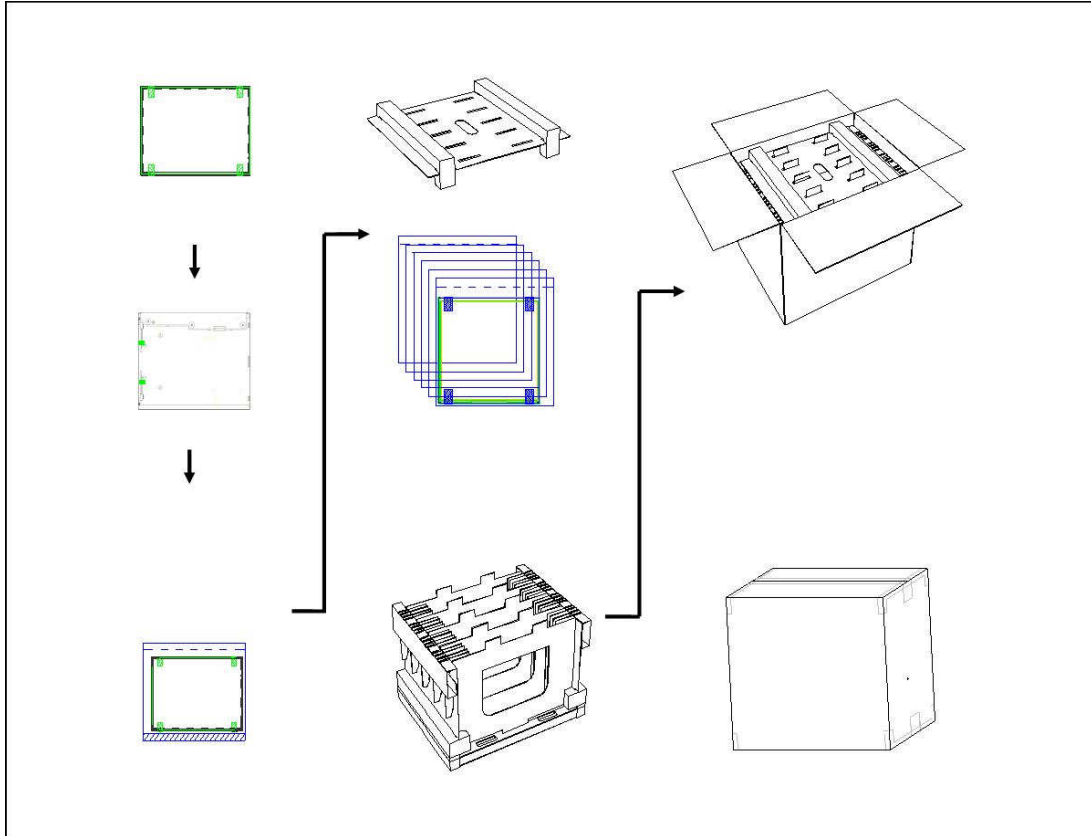
12. Shipping and Package

12.1 Shipping Label Format

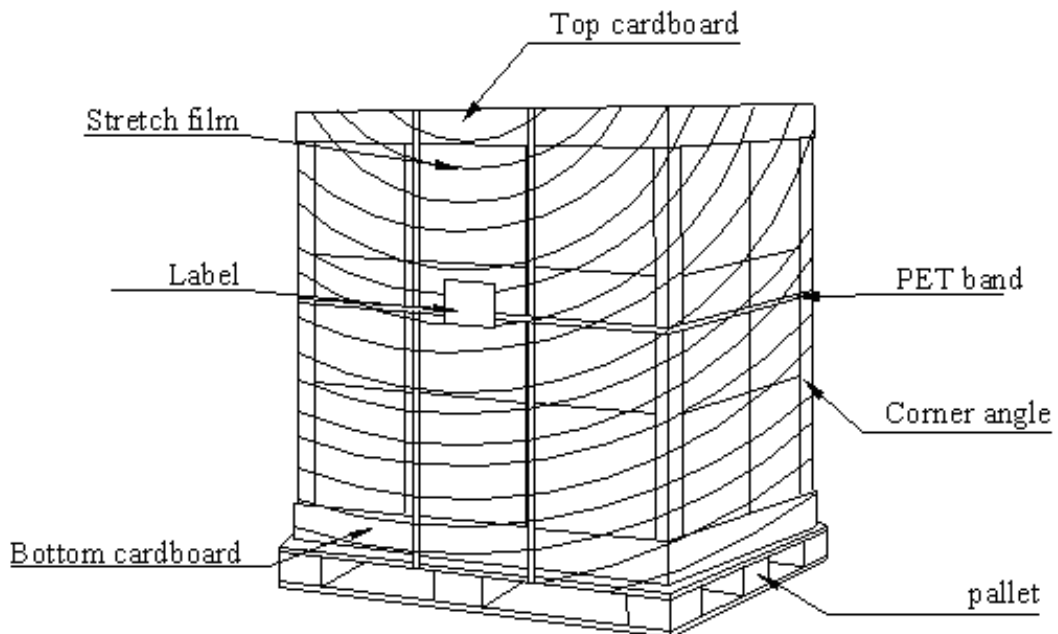


12.2 Carton package

The outside dimension of carton is 480 (L)mm x 373 (W)mm x 311 (H)mm



12.3 Shipping package of palletizing sequence





13. Appendix: EDID description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00			
01		FF			
02		FF			
03		FF			
04		FF			
05		FF			
06		FF			
07		00			
08	EISA Manuf. Code LSB	06			
09	Compressed ASCII	AF			
0A	Product Code	9D			
0B	hex, LSB first	10			
0C	32-bit ser #	00			
0D		00			
0E		00			
0F		00			
10	Week of manufacture	01			
11	Year of manufacture	13			
12	EDID Structure Ver.	01			
13	EDID revision #	03			
14	Video input def. (<i>digital I/P, non-TMDS, CRGB</i>)	90			
15	Max H image size (<i>rojAh d to cm</i>)	26			
16	Max V image size (<i>rounded to cm</i>)	15			
17	Display Gamma (<i>=(gamma*100)-100</i>)	78			
18	Feature support (<i>no DPMS, Active OFF, RGB, tmg Blk#1</i>)	0A			
19	Red/green low bits (Lower 2:2:2:2 bits)	C8			
1A	Blue/white low bits (Lower 2:2:2:2 bits)	95			
1B	Red x (Upper 8 bits)	9E			
1C	Red y/ highER 8 bits	57			
1D	Green x	54			
1E	Green y	92			
1F	Blue x	26			
20	Blue y	0F			
21	White x	50			
22	White y	54			
23	Established timing 1	00			



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24	Established timing 2	00		
25	Established timing 3	00		
26	Standard timing #1	01		
27		01		
28	Standard timing #2	01		
29		01		
2A	Standard timing #3	01		
2B		01		
2C	Standard timing #4	01		
2D		01		
2E	Standard timing #5	01		
2F		01		
30	Standard timing #6	01		
31		01		
32	Standard timing #7	01		
33		01		
34	Standard timing #8	01		
35		01		
36	Pixel Clock/10000 LSB	A0		
37	Pixel Clock/10000 USB	37		
38	Horz active Lower 8bits	80		
39	Horz blanking Lower 8bits	B4		
3A	HorzAct:HorzBlnk Upper 4:4 bits	70		
3B	Vertical Active Lower 8bits	38		
3C	Vertical Blanking Lower 8bits	32		
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	40		
3E	HorzSync. Offset	6C		
3F	HorzSync.Width	30		
40	VertSync.Offset : VertSync.Width	AA		
41	Horz&Vert Sync Offset/Width Upper 2bits	00		
42	Horizontal Image Size Lower 8bits	7D		
43	Vertical Image Size Lower 8bits	D6		
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10		
45	Horizontal Border <i>(zero for internal LCD)</i>	00		
46	Vertical Border <i>(zero for internal LCD)</i>	00		
47	Signal <i>(non-intr, norm, no stero, sep sync, neg pol)</i>	1A		
48	Detailed timing/monitor	A0		
49	descriptor #2	37		
4A		80		



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4B		B4		
4C		70		
4D		38		
4E		32		
4F		40		
50		6C		
51		30		
52		AA		
53		00		
54		7D		
55		D6		
56		10		
57		00		
58		00		
59		1A		
5A	Detailed timing/monitor	00		
5B	descriptor #3	00		
5C		00		
5D		FE		
5E		00		
5F	Manufacture	54		
60	Manufacture	31		
61	Manufacture	39		
62		37		
63		4E		
64		0A		
65		42		
66		31		
67		37		
68		33		
69		48		
6A		57		
6B		31		
6C	Detailed timing/monitor	00		
6D	descriptor #4	00		
6E		00		
6F		00		
70		00		
71	Manufacture P/N	00		



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72	Manufacture P/N	00			
73	Manufacture P/N	00			
74	Manufacture P/N	00			
75	Manufacture P/N	00			
76	Manufacture P/N	00			
77	Manufacture P/N	00			
78	Manufacture P/N	00			
79	Manufacture P/N	02			
7A	Manufacture P/N	01			
7B	Manufacture P/N	0A			
7C		20			
7D		20			
7E	Extension Flag	00			
7F	Checksum	09			