CUSTOMER APPROVAL SHEET

Company Name	
MODEL	**H154QN01 V2**
CUSTOMER APPROVED	**Title :** **Name :**

☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver.____)**
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Product Specification

1.54" COLOR TFT-LCD MODULE

MODEL NAME: H154QN01 V2

< ◆ >Preliminary Specification
< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2010/10/20		First Draft.

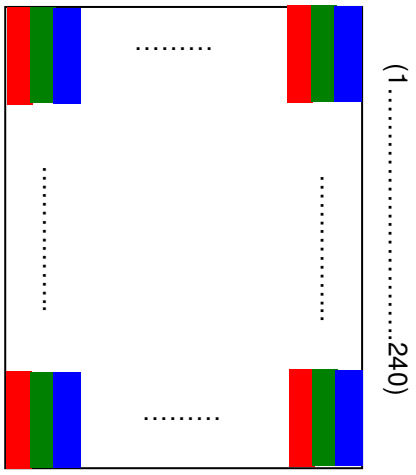
Contents

A. General Information

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	1.54(Diagonal)	
2	Display Resolution	dot	240RGB(H)×240(V)	
3	Overall Dimension	mm	31.82(H) × 33.72(V) × 1.242(T)	Note 1
4	Active Area	mm	27.72(H)×27.72(V)	
5	Pixel Pitch	mm	0.0385(H)×0.1155(V)	
6	Color Configuration	--	R. G. B. Stripe	Note 2
7	Color Depth	--	262k Colors	
8	NTSC Ratio	%	50	
9	Display Mode	--	ECB Normally white	
10	Weight	g	2.4g	
11	Interface		1-Lane MIPI I/F	
12	Viewing angle		CR>10:1 at 50 degree	

Note 1: Not include FPCs extrude stucture.

Note 2: Below figure shows dot stripe arrangement.

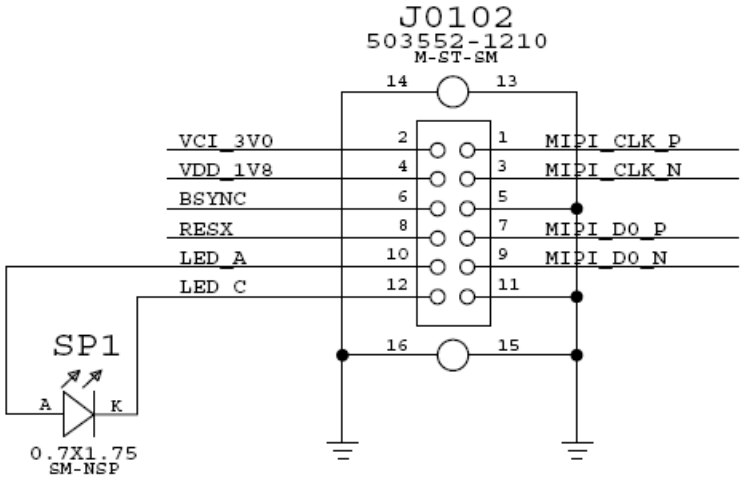


B. Electrical Specifications

1 Pin Assignment

TFT LCD Panel Pin Assignment:

No.	Pin Name	I/O	Description	Remarks
1	DISP_CLK_P	I/O	MIPI Clock	
2	DISP_3V0	-	3.0 V Power Supply	
3	DISP_CLK_N	I/O	MIPI Clock	
4	1V8	-	1.8 V Power Supply	
5	GND	-	MIPI Data Guard	
6	DISP_SYNC	O	Synchronization Pulse Signal	
7	DISP_D0_P	I/O	MIPI Data	
8	DISP_RESET_L	I	Reset	Active Low
9	DISP_D0_N	I/O	MIPI Data	
10	LCD_BL_CA	O	LCD Backlight Anode	
11	GND	-	MIPI Data Guard	
12	LCD_BL_CC	O	LDC Backlight Cathode	



2 Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Notes
Analog Power Supply Voltage	DISP_3V0	-0.3 ~ +5.0	V	
Logic I/O Voltage	1V8	-0.3 ~ +5.0	V	
Logic Input Voltage	VIN	-0.3 ~ (1.8+0.5)	V	1
LED Power Consumption	PLED	425	mW	2
LED Current	ILED	25	mA	2
Operating Temperature	TOP	-20 ~ +70	℃	3
Storage Temperature	TSTG	-30 ~ +80	℃	3
Humidity	H	5% ~ 95%	RH	3
Maximum Pressure		100	N	4

(1)Applies to DISP_D0_N, DISP_D0_P, DISP_CLK_N, DISP_CLK_P, DISP_SYNC, DISP_RESET_L

(2) Applies for each LED individually

(3) See Section 7 for specific temperature and humidity test conditions.

(4) Test with a 10 mm diameter metal cylinder with 2.5 mm rubber tip moving down at 1mm/minute in the center and top left corner without permanent optical change. See section 7 for additional system-level pressure testing.

3 Electrical DC Characteristics

a. Typical Operation Condition (GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Logic I/O Voltage	VDD3-VSS	1.71	1.8	1.89	V	
1.8V Input Current	IVDD3NM	-	-	TBD	mA	1
	IVDD3KEYNOTE					1
	IVDD3SLEEP					1
Analog Power Supply	VCI-VSS	2.85	3	3.15	V	
3.0V Input Current	IVCINM					1

	IVCIKEYNOTE					1
	IVCISLEEP					1
LED Input Current	ILED		10.5	20	mA	
“H” Level Input Voltage	VIH	0.7VDD3	-	VDD3	V	1,2
“L” Level Input Voltage	VIL	0	-	0.3VDD3	V	1,2
“H” Level Output Voltage	VOH	0.8VDD3	-	VDD3	V	Iout = -1mA
“L” Level Output Voltage	VOL	0	-	0.2VDD3	V	Iout = +1mA
“H” Level Input Current	IIH	-	-	10	uA	
“L” Level Input Current	IIL	-10	-	-	uA	
Power, MIPI full refresh	PMIPI	-	-	27.5	mW	1
MIPI Operating Frequency	fMIPI	-	66.5	300	MHz	
Power, Normal mode. MIPI ULPS	PULPS	-	-	19.5	mW	7
Power Consumption, Backlight	PB	-	170	180	mW	3
Power Consumption, Suspend	PS	-	84	-	uW	4

(1) The specified current and power consumption are under the conditions at VCI = V_{DD} = 3.0V, VDD3 = V_{EE} = 1.8V, T = 25℃, and

f_v = 60 Hz, large black/white checker pattern (20-pixel blocks), 240 Mbps MIPI refresh at 30 fps.

(2) Input mode of DISP_RESET_L, MTP, HIFA, DISP_SYNC

(3) LED Backlight assumptions: 3.2 V_f, 10.5 mA, 5 LED’s.

(4) VDD3 and VCI present, MIPI lane ULPS, Deep Sleep In mode

(5) The specified power consumption is under the conditions at VCI = V_{DD} = 3.0V, VDD3 = V_{EE} = 1.8V, T = 25℃, and f_v = 60 Hz, large black/white checker pattern (20-pixel blocks), MIPI in ULPS (LP11 for both CKL and D0)

4 Electrical Timing Characteristics

4.1. MIPI DC Characteristics

MIPI DC characteristics

Item		Parameter	Min	Nom	Max	Units	Notes
LP_TX	Thevenin output high level	V_O	1.1	1.2	1.3	V	
	Thevenin output low level	V	-50		5	mV	
	Output impedance of LP	Z_O	110			Ω	1
HS_RX	Common-mode voltage HS	$V_{CMRX(D}$	7		330	mV	2,3
	Differential input high	V_{ID}			7	mV	
	Differential input low threshold	V_{ID}	-70			mV	
	Single-ended input high	V_{IH}			460	mV	2
	Single-ended input low voltage	V_{IL}	-40			mV	2
	Single-ended threshold for HS termination enable	$V_{TERM-EN}$			450	mV	
	Differential input impedance	Z_I	8	100	125	Ω	
LP_RX	Logic 1 input voltage	V_I	880			mV	
	Logic 0 input voltage, not in ULP	V_I			550	mV	
	Input hysteresis	V_{HYST}	2			mV	
LP_CD	Logic 1 contention threshold	V_{IH}	450			mV	
	Logic 0 contention threshold	V_{IL}			200	mV	

Note1. Even though a maximum value for ZOLP is not specified, the output impedance of the LP transmitter ensures that the TRLP/TFLP specification is met

Note2. Excluding additional RF interference of 100mV peak sine wave beyond 450MHz

Note3. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz.

4.2. High Speed Data-Clock Timing

Host sends a differential clock signal to the S6D04D2 to be used for data sampling. This signal is a DDR (half- rate) clock and has one transition per data bit time. The timing relationship of the DDR Clock differential signal
to the Data differential signal is shown in Figure 1

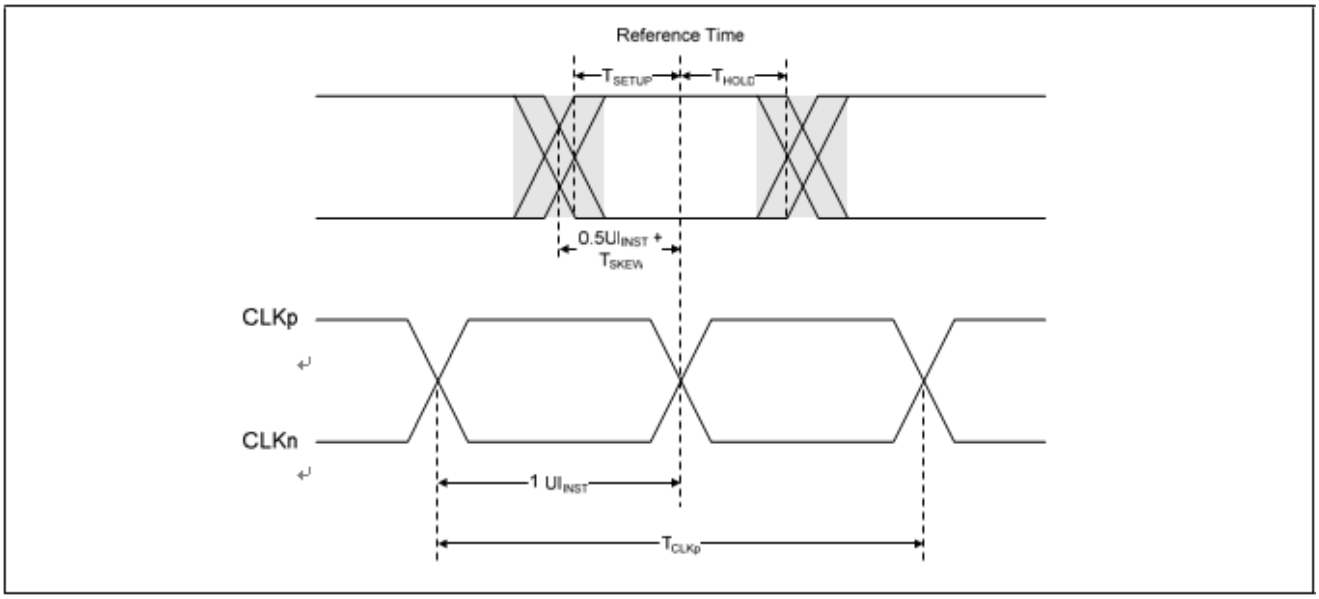


Figure 1. MIPI data to clock timing definitions

MIPI pin characteristic specifications

Clock Parameter	Symbol	# of d-lane	Mi	Typ	Max	Units	Notes
UI instantaneous	UIINST	1	2		12.5	ns	1,2

Note1. This value corresponds to a minimum 80 Mbps data rate.

Note2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

MIPI data-clock timing specifications

Paramet	Symbol	Mi	Typ	Max	Units	Notes
Data to Clock Setup Time	TSETUP[R	0.15			UIINS	2
Clock to Data Hold Time	THOLD[RX	0.15			UIINS	2

Note1. Total silicon and package delay budget of 0.3* UI_{INST}

Note2. Total setup and hold window for receiver of 0.3* UI_{INST}

4.3. Global Operation Timings

This section specifies global operation timings of the MIPI Interface. Detailed timing specifications are in Table 1.

4.3.1. Global Operation Timing Parameters

Table 1 lists the ranges for all timing parameters used in this section. The values in the table require a clock tolerance no worse than ±10% for implementation.

Table 1. Global Operation Timing Parameters

Parameter	Descripti	Mi	Typ	Max	Unit	Notes
$T_{CLK-MISS}$	Detection time that the clock has stopped toggling			60	ns	1
$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated data lane has transitioned to LP mode	60 ns + 52*UI			ns	2
$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8			UI	
$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	50		140	ns	
$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			ns	
$T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting clock	390			ns	
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state			105 ns + n*12*UI	ns	4
$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			ns	
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40 ns + 4*UI		85 ns + 6*UI	ns	
$T_{HS-PREPARE}$ + T_{HS-ZER}	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145 ns + 10*UI			ns	

$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40		55 ns + 4*UI	ns	
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 ns +n*4*UI)			ns	3,4
T_{INIT}	Initialization period	100			µs	
T_{LPX}	Length of any low-power state period	50			ns	5
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	2/3		3/2		
T_{TA-GET}	Time to drive LP-00 by new TX	$5*T_{LPX}$			ns	
T_{TA-GO}	Time to drive LP-00 after turnaround request	$4*T_{LPX}$			ns	
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}		$2*T_{LPX}$	ns	

Note1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates. Note2. UI is the instantaneous unit interval.

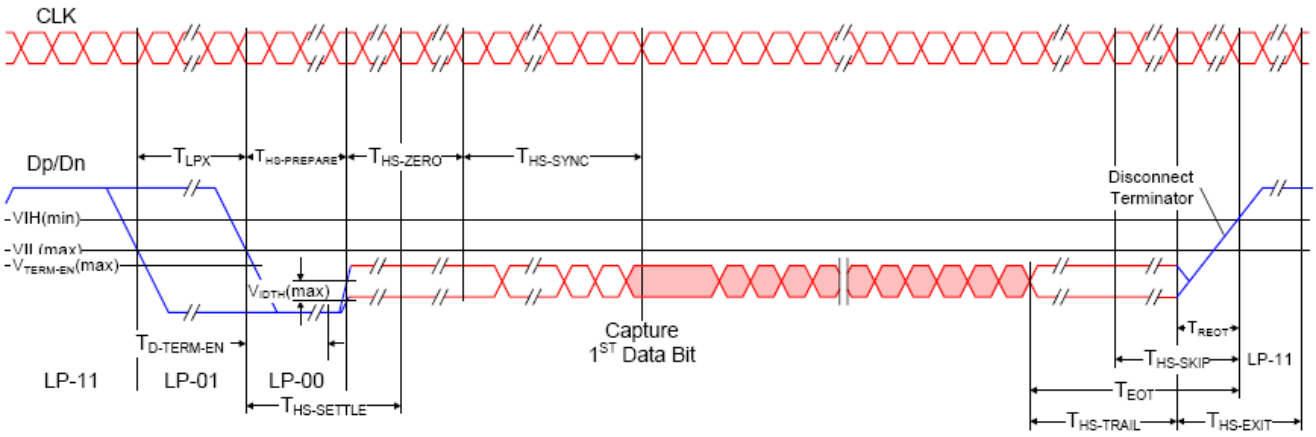
Note3. If a] b then max (a, b) = a otherwise max (a, b) = b

Note4. Where n = 1 for Forward-direction HS mode and n = 4 for reverse-direction HS mode

Note5. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

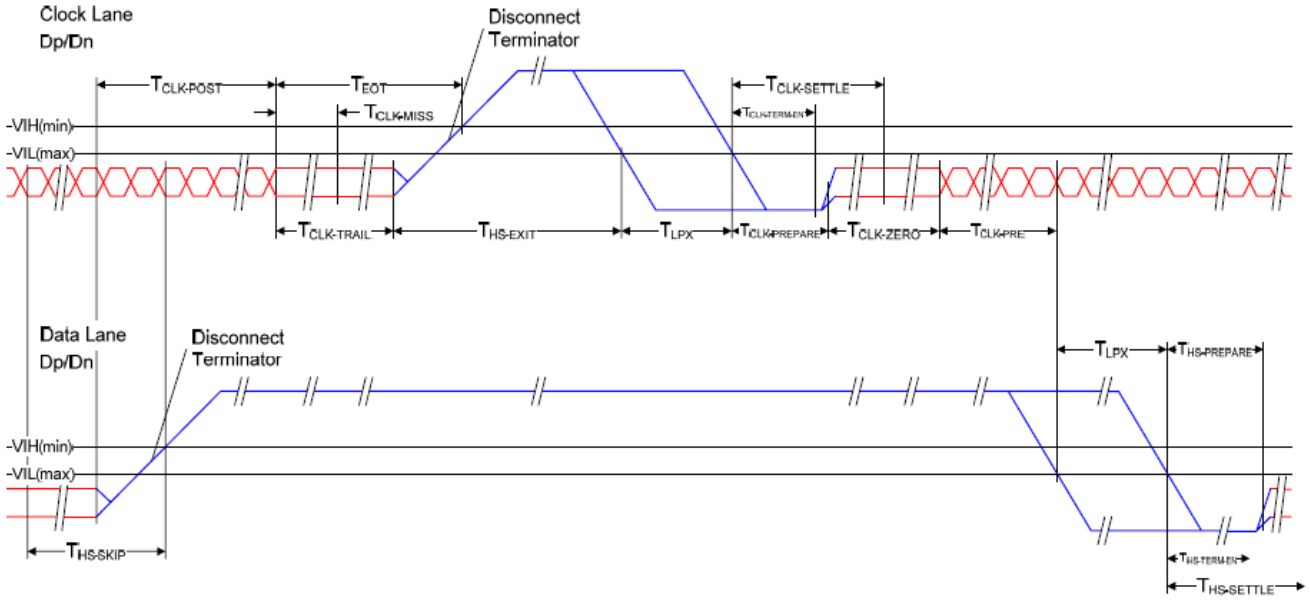
4.3.2. High Speed Data Transmission

The following figure shows the sequence of the high speed data transmission including SoT data.



High-Speed Data Transmission in Bursts

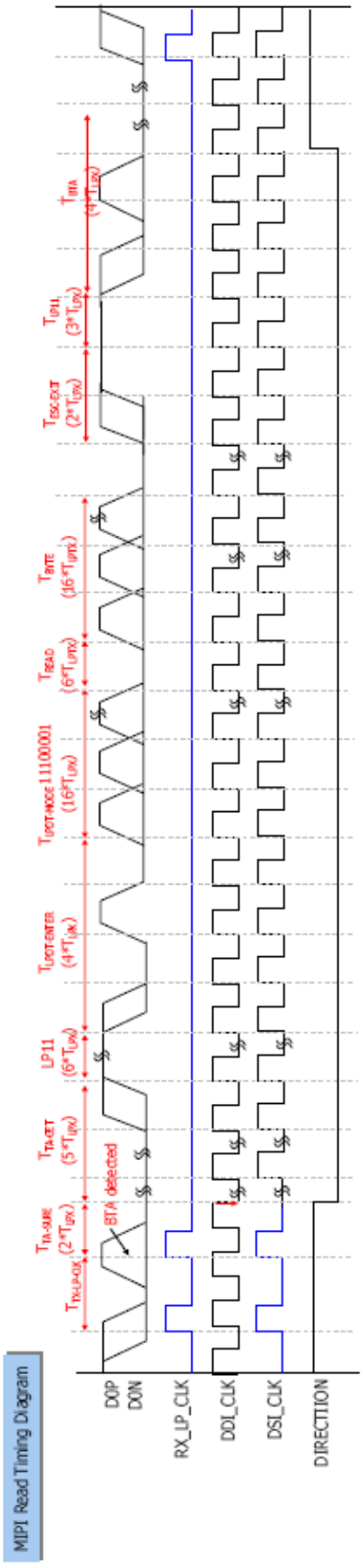
4.3.3. High Speed Clock Transmission



Switching the Clock Lane Between Clock Transmission and Low-Power Mode

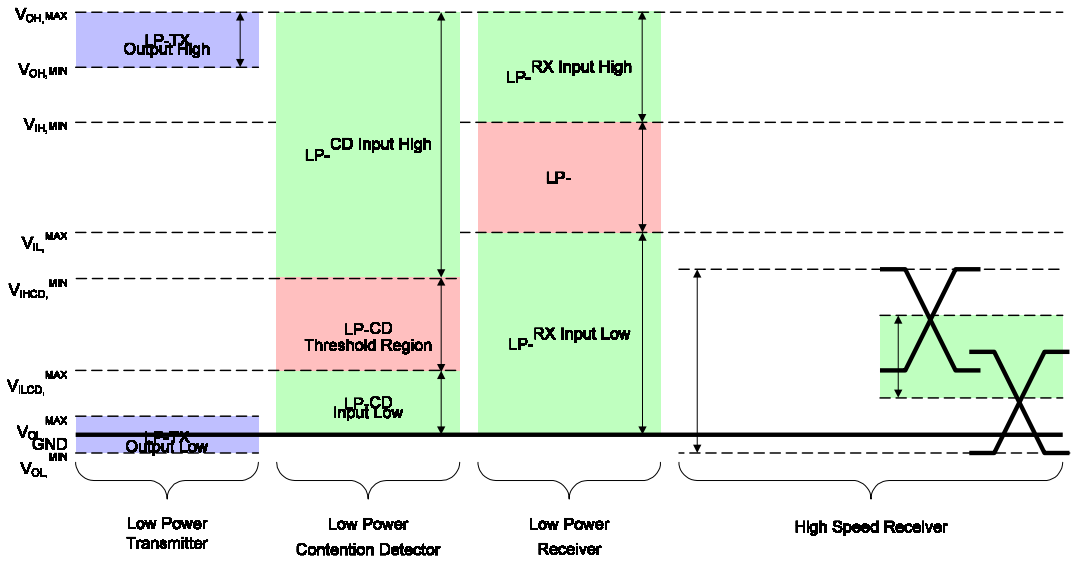
4.3.4. Reverse Transmission Timing Diagram

The MIPI needs BTA procedure to read data from DDI side. The DSI receiver (S6D04D2) gets the ownership of the lane via BTA. The DSI (S6D04D2) receiver starts the low power data transmission for the previous data packet. If the previous packet is read, the S6D04D2 make the read packet including DSI packet header and read data (payload). The entire timing diagram of the read procedure is described in the following figure.



MIPI Read Timing Diagram

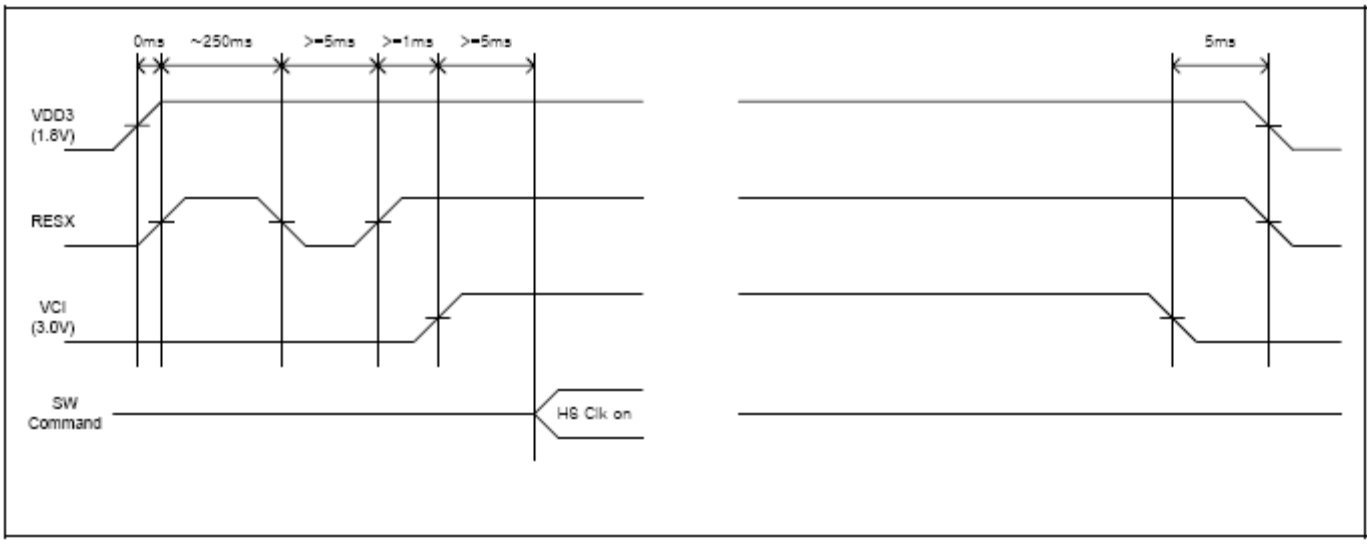
4.4. Line Contention Detection



5 Power On/Off Characteristics

5.1. Hard Power On/Off Sequence

Figure below shows the timing diagram & relationship among VDD3/VCI power, RESX signal & high-speed clock/data lanes in Hard Power On/Off sequence.

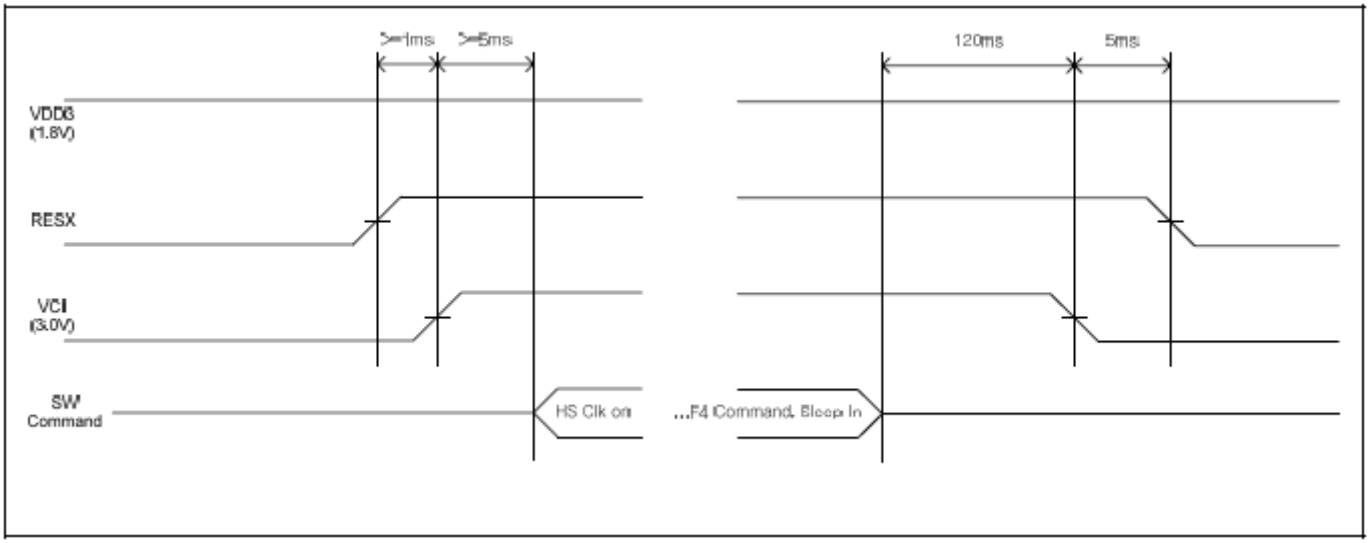


Timing diagram of Hard Power On/Off sequence

Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

5.2. Soft Power On/Off Sequence

Figure below shows the timing diagram & relationship among VDD3/VCI power, RESX signal & high-speed clock/data lanes in Soft Power On/Off sequence



Timing diagram of Soft Power On/Off sequence

Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level

5.3 System Power On and Reset Sequences

Recommended Initial Sequence (State : NVM Written)				
Step	Reg.	Data	Delay	Command
1				VDD3 on (Typ. 1.8V)
			10us	for settlement (up to SET's Power Supplier)
2				H/W reset set to HIGH
			1ms	for DDI's Logic VDD settlement
3				VCI on (Typ. 3.0V)
			5ms	for OSC stabilization & NVM Loading
4				Turn on high-speed clock (HS clock on)
			10us	(up to SET's Clock Driver)
5	0x11			Sleep out
			120ms	
			40ms	wait 2 frames (BLK_OFF set)
6	0x36	0x08		RGB/BGR order chage
7	0x2C	Image		Start to send image data (HS data on)
8	0x29			Display On
9				Turn on Backlight

Power On Sequence

5.4 Power Off or Sleep in

In a normal power off or sleep in sequence the commands and/or register settings in the supplier-specific specification are followed. The sequence for power down or sleep in is shown below.

Recommended Power Off Sequence				
Step	Reg.	Data	Delay	Command
1				Turn off Backlight
			1ms	to prevent white flash
2	0x28			Display off
			5ms	
3	0xF1	0x5A		Enable to Access
		0x5A		
4	0xF4	0x0B		VC(11)
		0x00		-
		0x00		-
		0x00		-
		0x21		SEQ2(2), SEQ1(2)
		0x4F		SEQ4(6), SEQ3(4)
		0x01		SEQ5(1)
		0x02		for making DDI be in Sleep-in status not to activate DDI's discharging circuit for AVDD & VGH
		0x2A		NDC3(2), NDC2(2), NDC0(2)
		0x7F		NGVD(102) = 4.5V
		0x03		NBT(5), VGH, VGL
		0x2A		PIDC3(2), PIDC2(2), PIDC0(2)
		0x00		-
		0x03		PIBT(5), VGH, VGL
5	0xF1	0xA5		Disable to Access
		0xA5		
6	0x10			Sleep In
			120ms	Discharge time
7				Stop to send Image data (HS data off)
8				Turn off high-speed clock (HS clock off)
			10us	
9				VCI Off
			5ms	for settlement (up to SET's Power Supplier)
10				H/W reset set to LOW
			5ms	
11				VDD3 Off
				for settlement (up to SET's Power Supplier)

A mar datory Command which must be issued just before Sleep-in command whenever users want DDI to be in the sleep-in mode.

For the 8th byte, 0x**0E** should be set.

For the other bytes, The **Default values** should be set.

6 Command Register Map

a. Registers programmed by MTP function, automatically loaded into driver IC after Sleeep-Out command.

b. refer to 5.3 power on flow

	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th	13th	14th	15th	16th	17th	
E1h	F3h	10h	1Ch	17h	08h	1Dh												MIPI(FIXED)
F2h	00h	D7h	03h	22h	23h	00h	01h	01h	12h	01h	08h	57h	00h	00h	D7h	22h	23h	TIMING, FIXED(Blank time = 3.71ms, TE_OFF time = 538us, Freq 60Hz [NHW=215, VBP=34, VFP=35, TE_ST=274, TE_ED = 264], HIFA port = BSYNC, B_SYNC port = TE)
F4h	0Bh	00h	00h	00h	21h	4Fh	01h	02h	2Ah	7Fh	03h	2Ah	00h	03h				POWER ON SEQUENCE(FIXED), VCI1, VGH, VGL, BOOSTING FREQ (FIXED)
F5h	00h	30h	49h	XXh	00h	18h	00h	00h	04h	04h								VCOM CONTROL, VCOM OUTPUT AT PORCH PERIOD(GND, FIXED). Note (1)
F6h	02h	01h	06h	00h	02h	04h	02h	84h	06h									SORUCE CONTROL. Notes (2), (3), (4), (5), (6)
F7h	40h																	MADCTL(MIRROR D6XOR, FIXED)
F8h	33h	00h																GATE CONTROL
F9h	00h																	MIPI LPTX SPEED(8Mbps, FIXED)
36h	08h																	BGR → RGB SWAP

E1h	F3h	10h	1Ch	17h	08h	1Dh												MIPI(FIXED)
E2h	C3h	87h	39h	63h	D8h													MIPI(FIXED)
E3h	84h	06h	52h															MIPI(FIXED)
E4h	43h	00h	00h															MIPI(FIXED)

(1) Min VCIR1 setting according to DDI recommended VCIR matrix
(2) Min SVCIR setting of 02h
(3) Min SAP setting of 05h
(4) Max SDT setting of 9h
(5) Min HBLK_SRC setting of 5h
(6) Min DIV_SRC setting of 5h

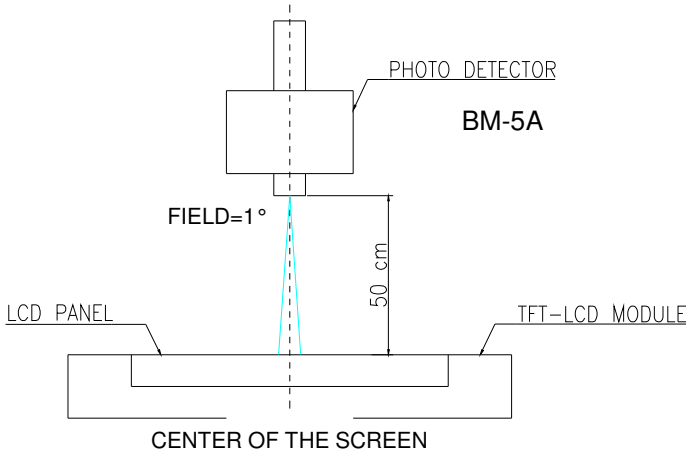
C. Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise Fall		 Tr Tf	θ=0°	 -- --	 6 20	 15 30	 ms ms	Note 3
Contrast ratio		CR	At optimized	100	150	--		Note 4
Viewing Angle	Top		CR≧10	50	60	--	deg.	Note 5
	Bottom			50	60	--		
	Left			50	60	--		
	Right			50	60	--		
High gray level inversion	Top		CR≧10	45	55	--	deg.	Note 5
	Bottom			50	60	--		
	Left			50	60	--		
	Right			25	35	--		
Low gray level inversion	Top		CR≧10	50	60	--	deg.	Note 5
	Bottom			50	60	--		
	Left			50	60	--		
	Right			50	60	--		
Brightness		Bottom	θ=0°	450	500	--	cd/m^2	Note 6
NTSC		Left	θ=0°	--	50	--		
Chromaticity	White	X	θ=0°	0.265	0.296	0.309	0.315	0.341
		Y	θ=0°	0.318	0.279	0.324	0.371	0.329
	Red	X	θ=0°	0.600	0.573	0.610	0.610	0.634
		Y	θ=0°	0.312	0.347	0.345	0.378	0.344
	Green	X	θ=0°	0.298	0.277	0.320	0.335	0.358
		Y	θ=0°	0.516	0.553	0.555	0.595	0.560
	Blue	X	θ=0°	0.150	0.120	0.150	0.153	0.184
		Y	θ=0°	0.079	0.116	0.120	0.150	0.112
Uniformity		ΔY_L	%	--	80	--	%	Note 7

Note 1: Measured under Ambient temperature =25℃, and LED lightbar current I_L = 20mA in the dark room.

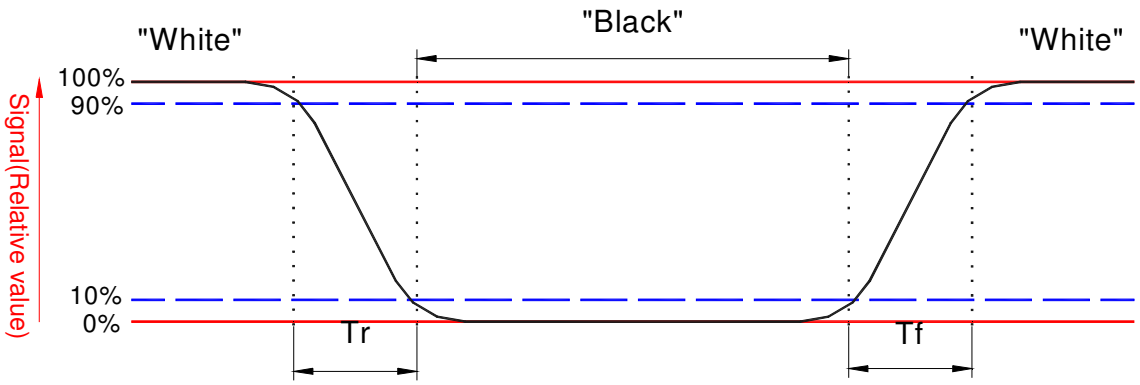
Note 2: To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5A, after 15 minutes operation.



Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white” (falling time) and from “white” to “black” (rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

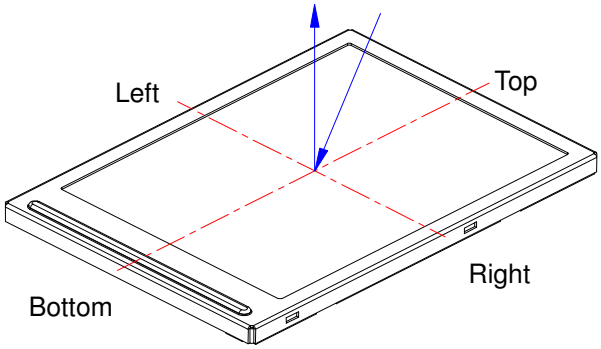


Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

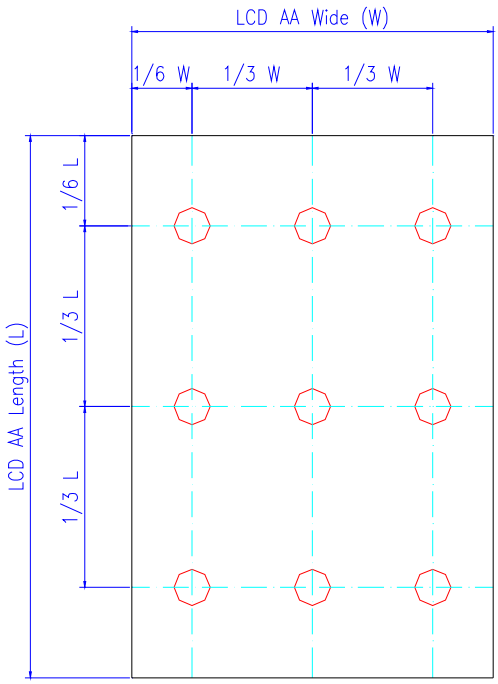
$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

Note 5. Definition of viewing angle, θ, Refer to figure as below.



Note 6: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 7: Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

D. Reliability test items

1. Test items and conditions:

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 80℃ 500H	
2	Low temperature storage	Ta= -30℃ 500H	
3	High temperature operation	Ta= 70℃ 500H	
4	Low temperature operation	Ta= -20℃ 500H	
5	High temperature and high humidity	Ta= 50℃. 90% RH 240H	Operation
6	Heat shock	-30℃~80℃/50 cycles 1H/cycle	Non-operation
7	Electrostatic discharge	±HBM 2KV, once for each terminal in the non-operation mode.	Non-operation

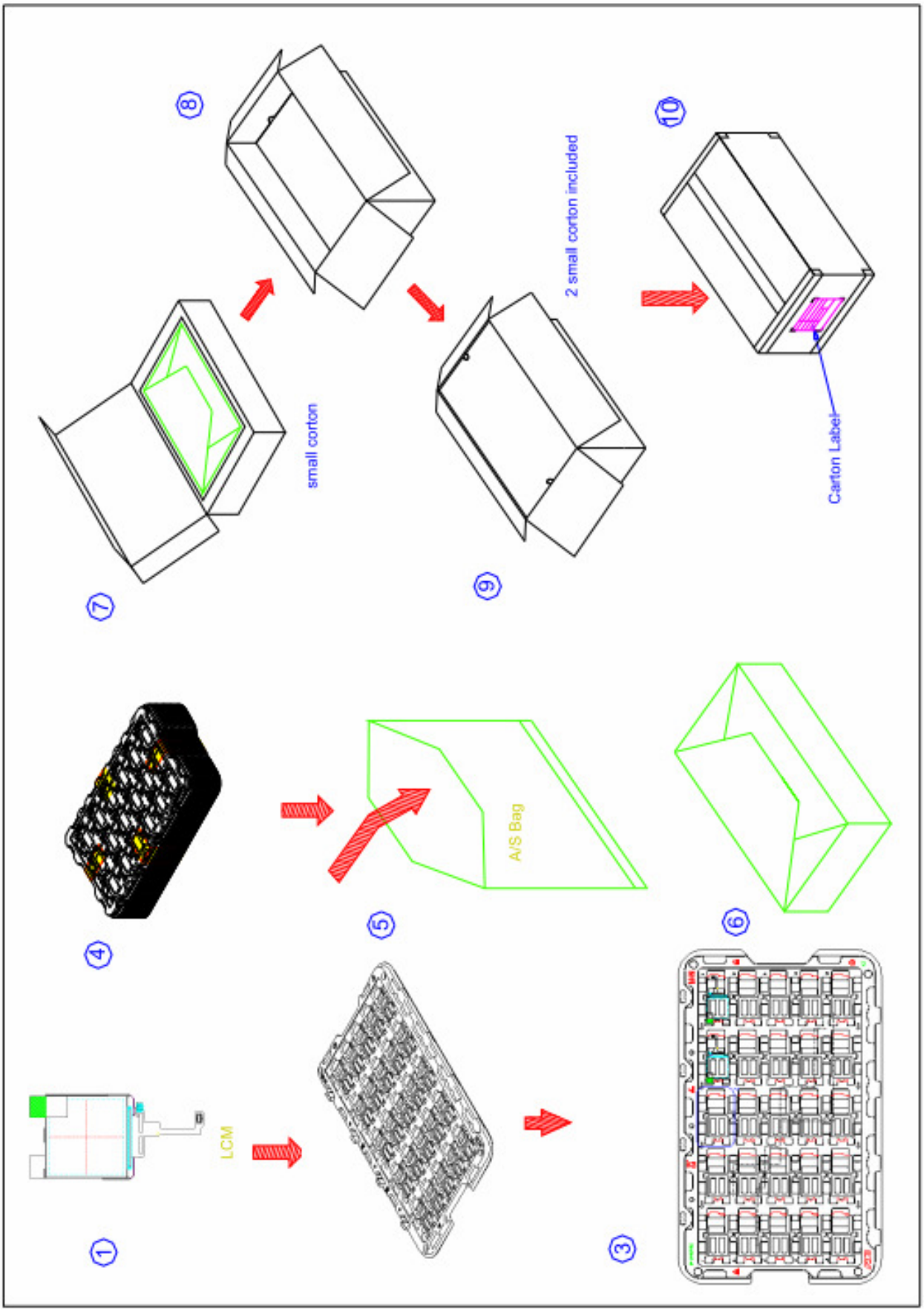
Note: After finishing the test, leave the samples under room temperature and normal humidity for 2 hours, and then this module should work normally.

2. Failure Judgment Criterion:

a. Neither abnormality nor significant visible deterioration should be found on display quality and appearance.

b. There should be no functional abnormalities on display quality.

E. Packing



F. Outline Dimension