(V) Preliminary Specification
( ) Final Specification

Module	20.1” UXGA Color TFT-LCD with LED BL
Model Name	M201UN03 V0

Customer	**Date**	**Checked & Approved by**	**Date**
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Approved by		**Prepared by**	
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Note: This Specification is subject to change without notice.

Desktop Display Business Group /
AU Optronics corporation

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Record of Revision

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V0.1 2006/04/25	All	First edition for customer	All	
V0.2 2006/06/12	5	2.1 Display Characteristics Power Consumption (VDD line + LED line) 55W (typ.) (w/o Inverter, All white pattern)	2.1 Display Characteristics Power Consumption (VDD line + LED line) 50.2W (typ.) (with Driver, All white pattern)	Modified
	11	4. Absolute Maximum Ratings LED Pulse current and LED current	4. Absolute Maximum Ratings Added LED Driver Voltage: Vdd and Vcc	Modified
	12	5.1 TFT LCD Module 5.1.1 Power Specification VDDns	5.1 TFT LCD Module 5.1.1 Power Specification NA	Deleted
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	24	7.2.1 Signal for LED connector Backlight Power: Pin7: Venable Pin8: Vcc	7.2.1 Signal for LED connector Backlight Power: Pin7: Vcc Pin8: Venable	Modified
	27 28	10. Mechanical Characterisitc Old version	10. Mechanical Characterisitc Update 2D drawing	Updated

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.

2) Be sure to turn off power supply when inserting or disconnecting from input connector.

3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.

6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.

7) Do not open nor modify the Module Assembly.

8) Do not press the reflector sheet at the back of the module to any directions.

9) In case if a module has to be put back into the packing container slot after once it was taken out from the container. Instead of pressing at the edge softly. Otherwise the TFT module may be damaged.

10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT module.

11) After installation of the TFT module into an enclosure (Desktop monitor Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT module from outside. Otherwise the TFT module may be damaged.

2. General Description

This specification applies to the 20.1 inch Color TFT-LCD Module M201UN03 v.0.
The display supports the UXGA (1600(H) x 1200(V)) screen format and 16.7M colors (RGB 8-bits data).
All input signals are 2 Channel LVDS interface compatible.
This module contains a driver card for backlight.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

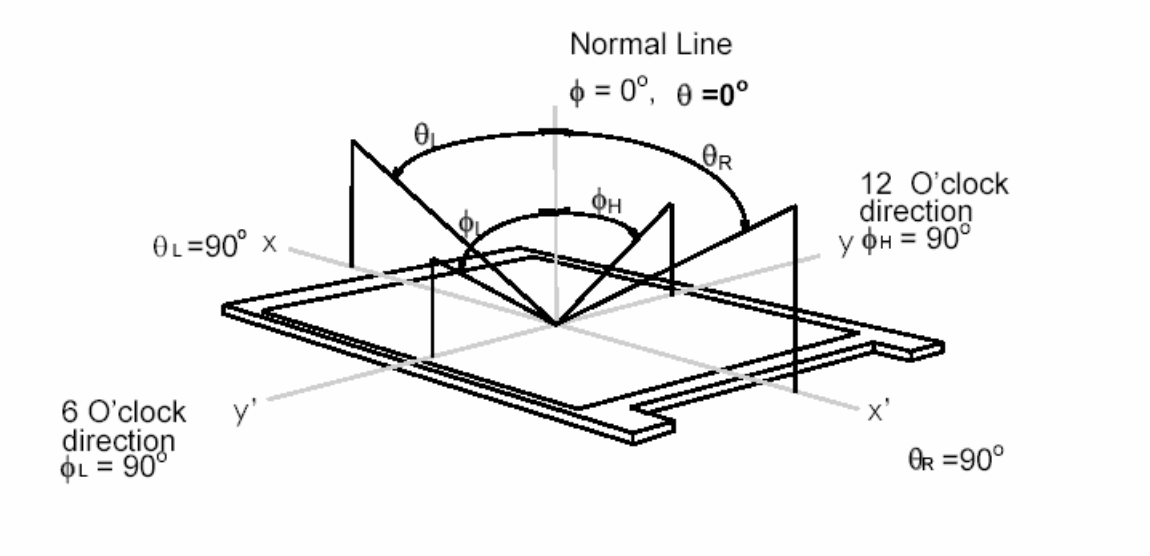
ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	510(20.1")
Active Area	[mm]	408.0 (H) x 306.0 (V)
Pixels H x V		1600(x3) x 1200
Pixel Pitch	[mm]	0.255 (per one triad) x 0.255
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally Black
White Luminance	[cd/m^2]	250 cd/m2 (Typ)
Contrast Ratio		1000 : 1 (Typ)
Optical Response Time (Raising + Falling) (Gray to Gray)	[msec]	 16 (Typ) 8 (Typ)
Nominal Input Voltage VDD	[Volt]	+5.0 V
Power Consumption (VDD line + LED line)	[Watt]	50.2W(typ.) (with Driver, All white pattern)
Weight	[Grams]	3300 (Typ)
Physical Size	[mm]	432(W) x 331.5(H) x 40(D)
Electrical Interface		Even/Odd R/G/B data, 3 sync signal, Clock
Support Color		16.7M colors (RGB 8-bit data)
Surface treatment		Anti-glare (3H)
Temperature Range Operating Storage (Shipping)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

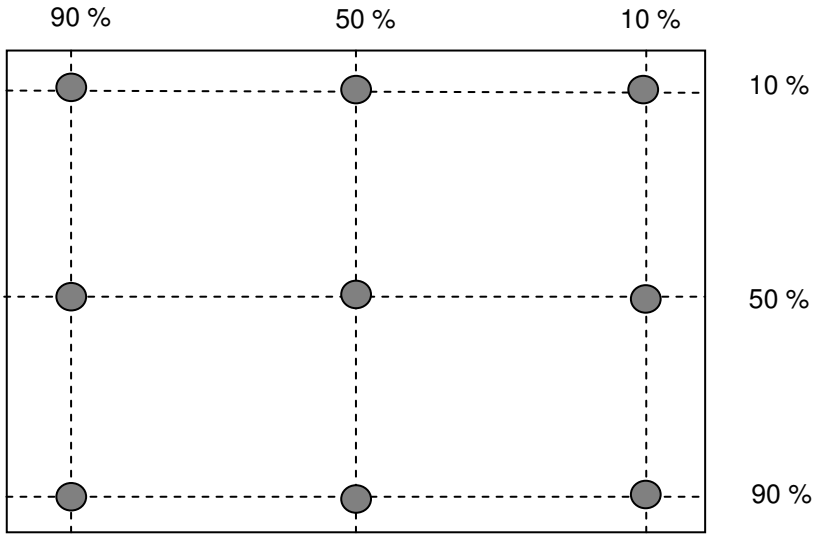
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing Angle	[degree]	Horizontal (Right)	75	89	-	1
	[degree]	CR = 10 (Left)		89	-	
	[degree]	Vertical (Up)	75	89	-	
	[degree]	CR = 10 (Down)		89	-	
Contrast ratio		Normal Direction	700	1000		
Response Time (Note 1)	[msec]	Raising Time	-	11	15	4,6
	[msec]	Falling Time	-	5	7	4,6
	[msec]	Raising + Falling	-	16	22	4,6
	[msec]	Gray to Gray	-	8		4,6
Color / Chromaticity Coordinates (CIE)		Red x	0.661	0.691	0.721	4
		Red y	0.271	0.301	0.331	
		Green x	0.151	0.181	0.211	
		Green y	0.671	0.701	0.731	
		Blue x	0.116	0.146	0.176	
		Blue y	0.053	0.083	0.113	
Color Coordinates (CIE) White		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	
White Luminance at LED (central point)	[cd/m^2]		200	250		
Luminance Uniformity	[%]		75	80	-	4
Crosstalk (in 60Hz) (Note 3)	[%]				1.5	5

Optical Equipment: BM-5A, PR880, SR3, CS1000 or equivalent.
Note 1: Definition of viewing angle
Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



Note 2: 9 points position

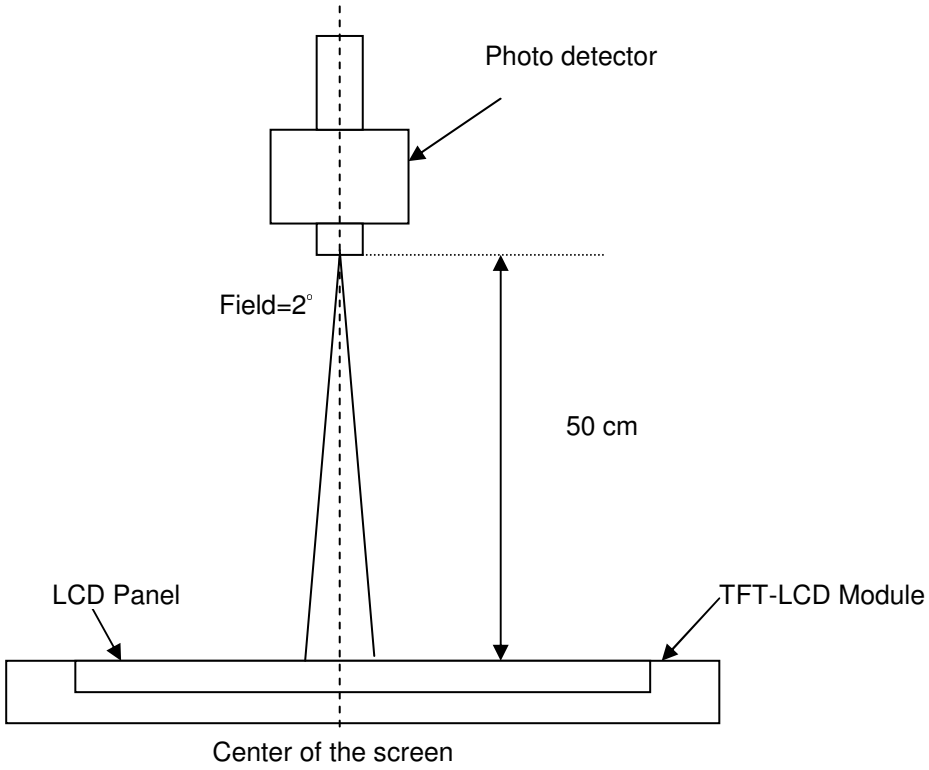


Note 3: The luminance uniformity of 9 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W9} = \frac{\text{Minimum Luminance of 9 points}}{\text{Maximum Luminance of 9 points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



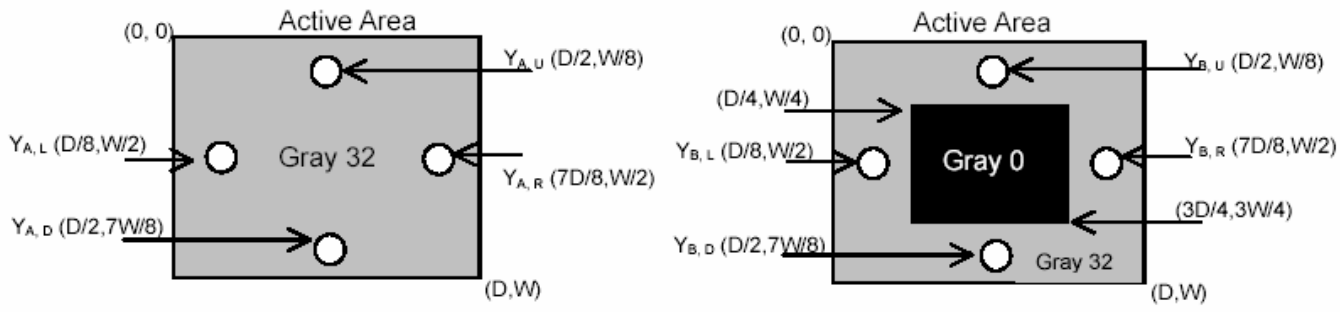
Note 5: Definition of Cross Talk (CT)

CT = | YB – YA | / YA × 100 (%)

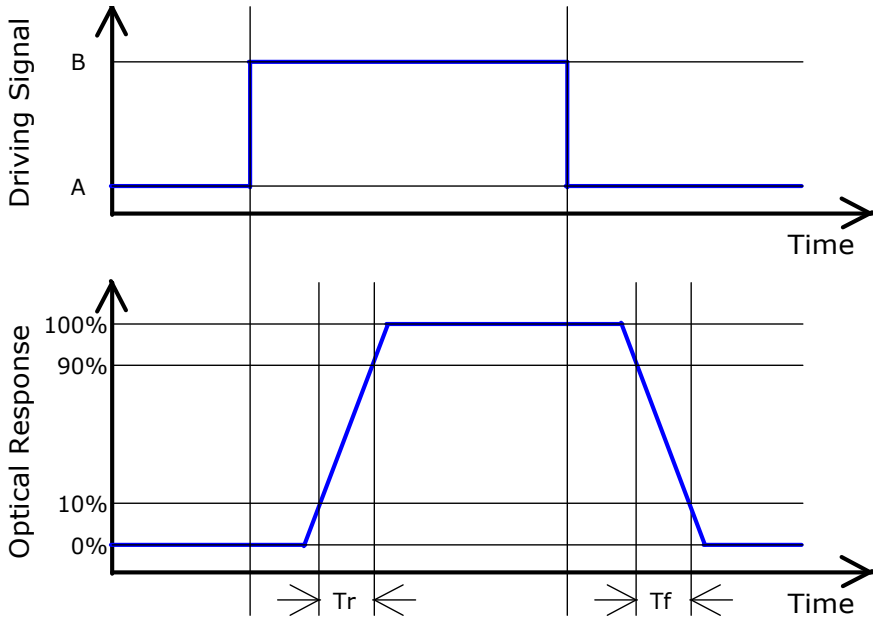
Where

YA = Luminance of measured location without gray level 0 pattern (cd/m2)

YB = Luminance of measured location with gray level 0 pattern (cd/m2)



Note 6: Definition of response time:

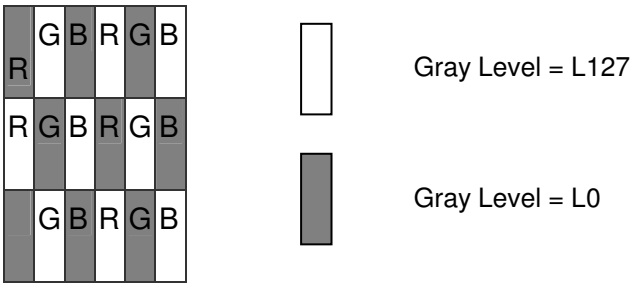


Algorithm:

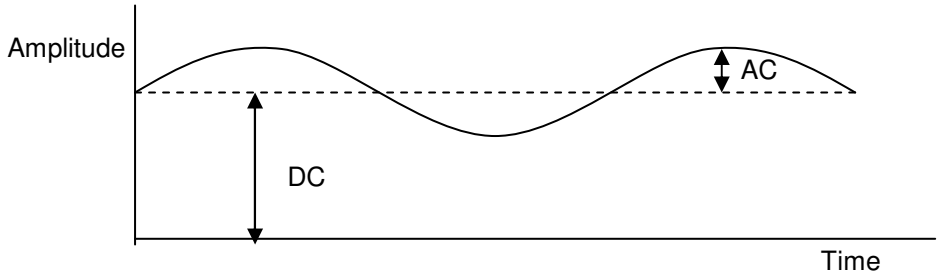
$|\text{Level A} - \text{Level B}| \geq 16$ then the average of Grey-to-Grey response time is 8ms. (F= 60 Hz).

Tr_R(rising time; from “All Black” to “All White”) + Tr_F(Falling time; from “All White” to “All Black”) = 16ms(typ).

Note 7: Subchecker Pattern



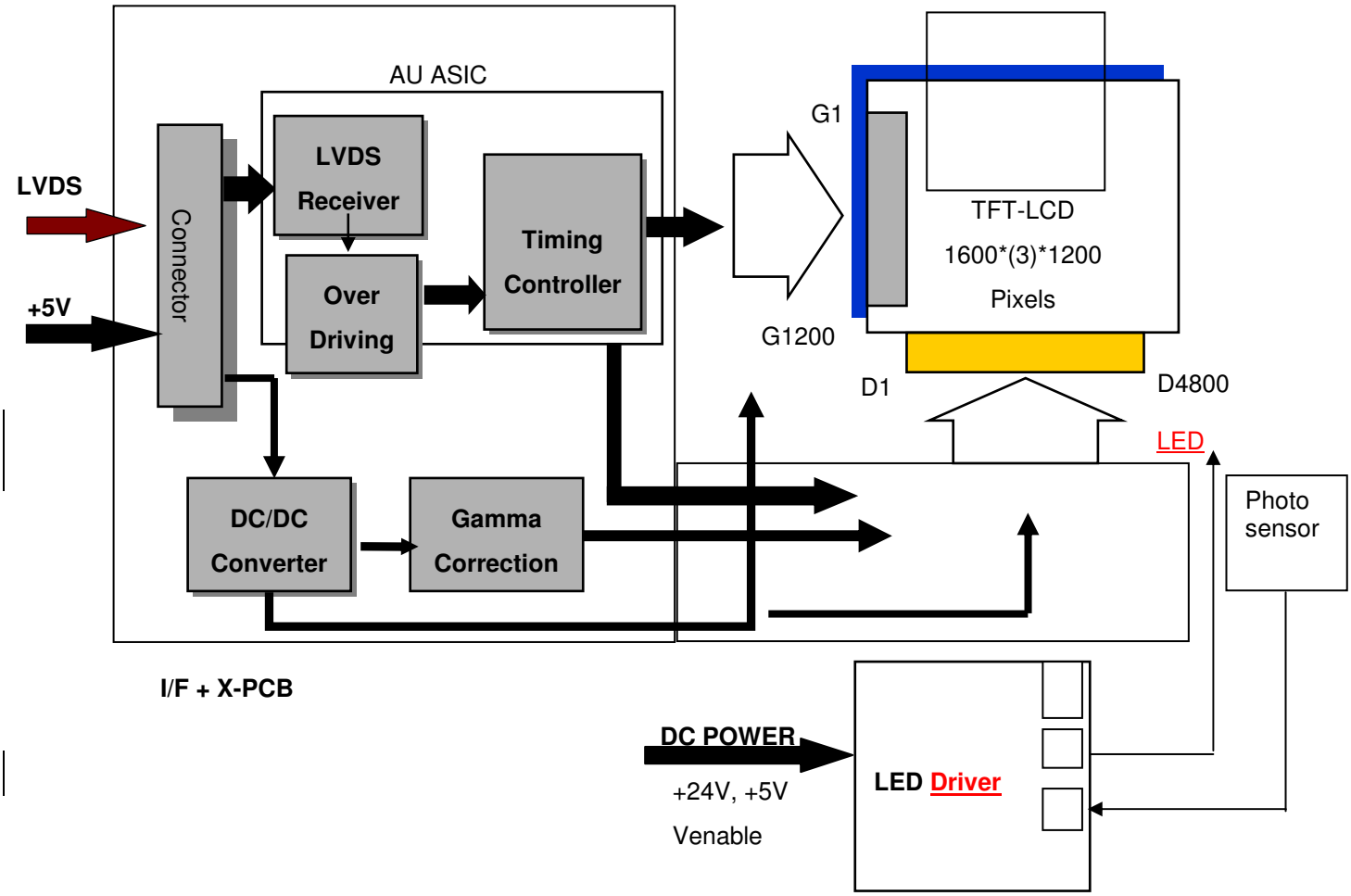
Method: Record dBV & DC value with (WESTAR)TRD-100



$$\text{Flicker (dB)} = 20\log\frac{\text{AC Level(at 30 Hz)}}{\text{DC Level}}$$

3. Functional Block Diagram

The following diagram shows the functional block of the 20.1 inches Color TFT-LCD Module:



4. Absolute Maximum Ratings

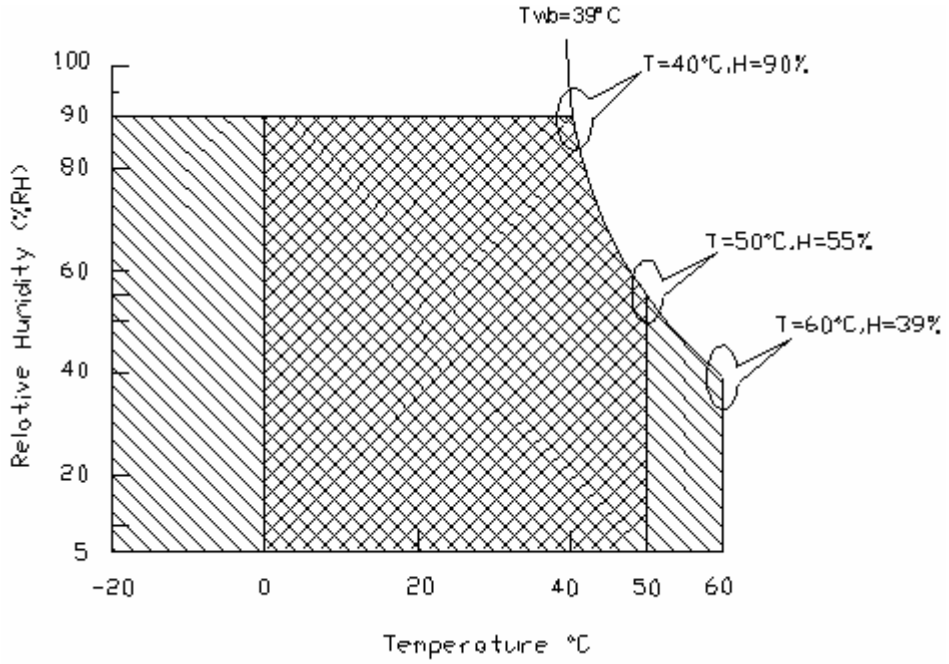
Absolute maximum ratings of the module is as following:

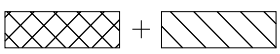
Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+6.0	[Volt]	
Select LVDS data order	SELLVDS	NC	NC	[Volt]	
LED Drive Voltage	Vdd	-0.3	+28.0	[Volt]	Note 1
LED Drive Voltage	Vcc	-0.3	+6.0	[Volt]	
Operating Temperature	TOP	0	+50	[°C]	Note 2,3
Operating Humidity	HOP	8	90	[%RH]	Note 2,3
Storage Temperature	TST	-20	+60	[°C]	Note 2,3
Storage Humidity	HST	8	90	[%RH]	Note 2,3

Note 1: Duration= 0.1 msec.

Note 2: Maximum Wet-Bulb should be 39℃and no condensation.

Note 3: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range  Storage Range 

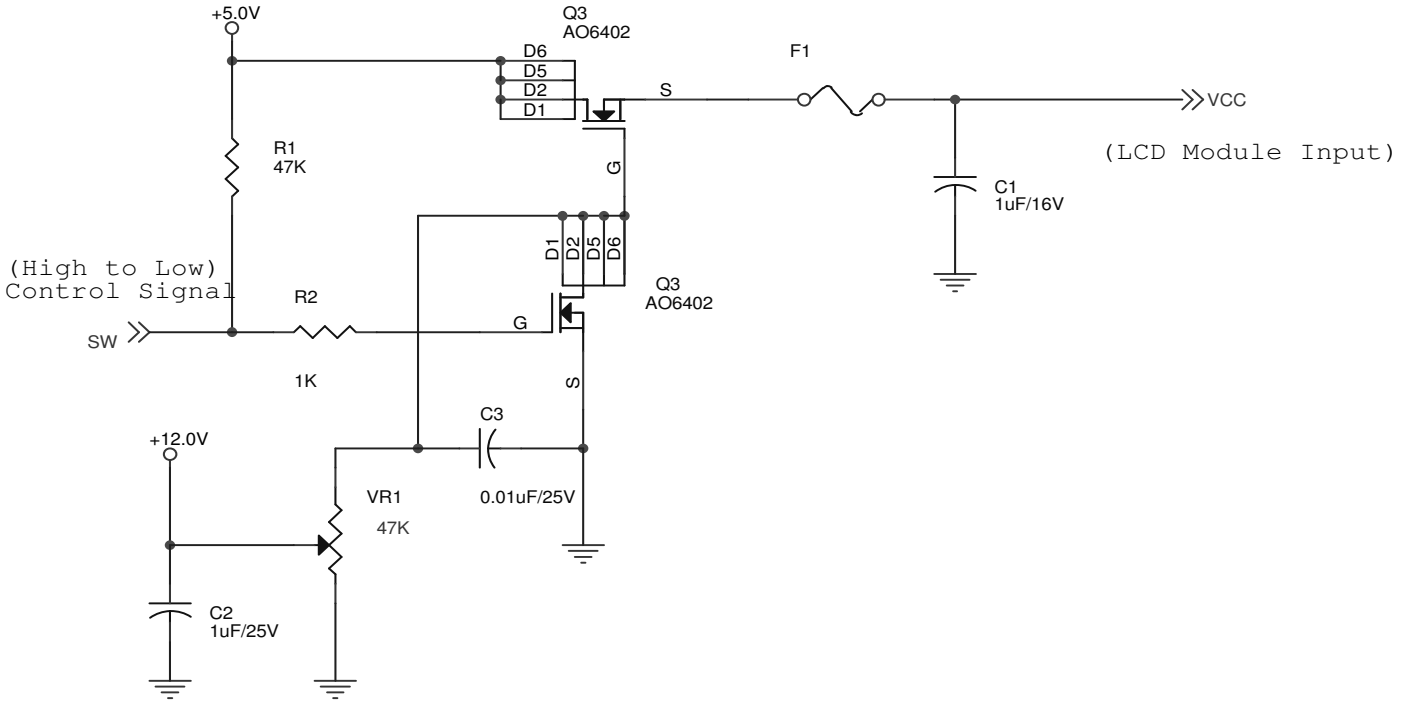
5. Electrical characteristics

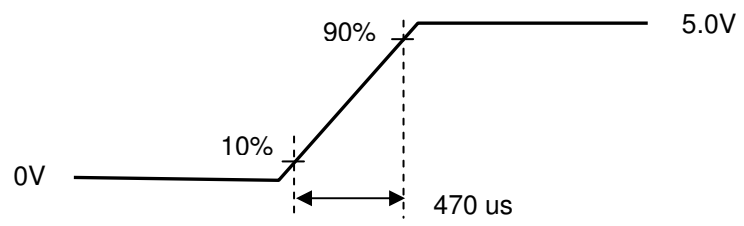
5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows:

Symbol	Parameter	Min	Typ	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	4.5	5	5.5	[Volt]	±10%
IDD	VDD current		1300	1500	[mA]	VDD=5V, All White Pattern
IIDD	Inrush VDD current			7.0	[A]	t < 470us
PDD	VDD Power		6.5	8.3	[Watt]	VDD=5V, All White Pattern
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	





VDD rising time

5.2 Backlight Unit

5.2.1 Power Specification

Parameter guideline for LED driving board is under stable conditions at 25℃ (Room Temperature):

Symbol	Parameter	Min	Typ	Max	Units	Condition
Vdd	Backlight Drive Input Voltage	21.6	24.0	26.4	[Volt]	
IDD1	Vdd current		1800	2400	[mA]	
IIDD1	Inrush Vdd current			8.0	[A]	t < 470us
PDD1	Vdd Power		43.2	55.2	[Watt]	Vdd=24V; Vcc=5V ; Dimming brightness Max.

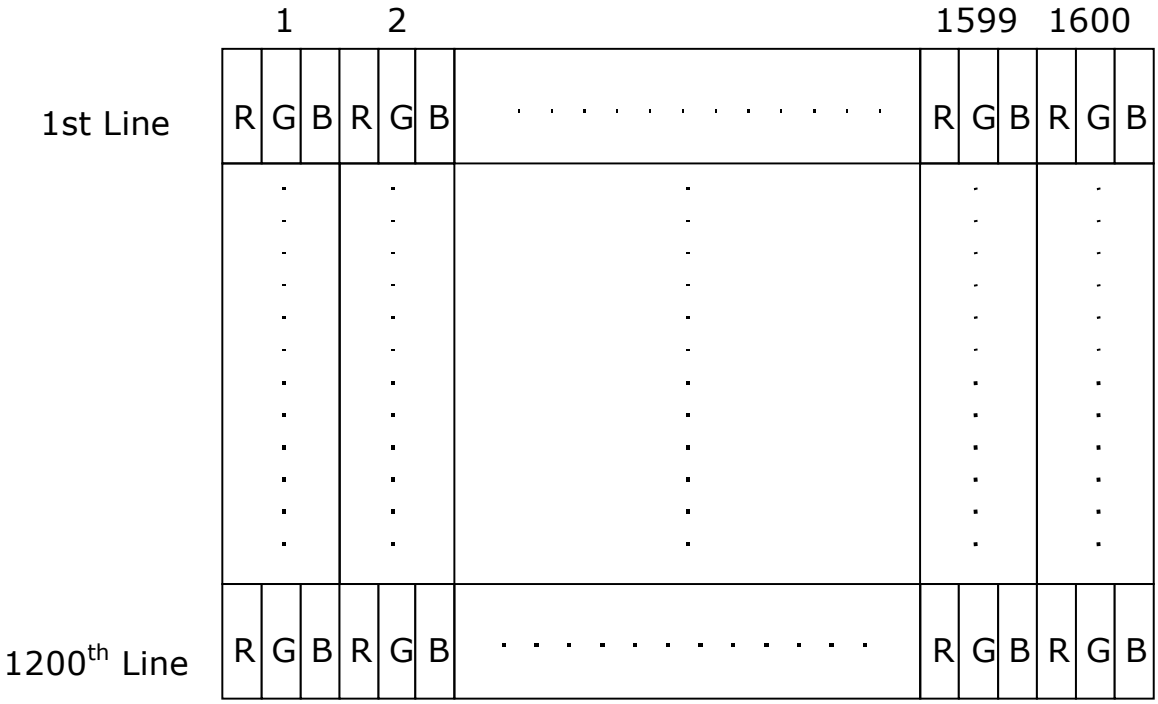
Symbol	Parameter	Min	Typ	Max	Units	Condition
Vcc	Backlight Drive Input Voltage	4.5	5.0	5.5	[Volt]	
IDD2	Vcc current		100	200	[mA]	
IIDD2	Inrush Vcc current			1.0	[A]	t < 470us
PDD2	Vcc Power		0.5	1.0	[Watt]	Vdd=24V; Vcc=5V ; Dimming brightness Max.

Symbol	Parameter	Min	Typ	Max	Units	Condition
Venable	Backlight Drive ON Voltage	1.0	5.0	5.5	[Volt]	Vdd=24V; Vcc=5V

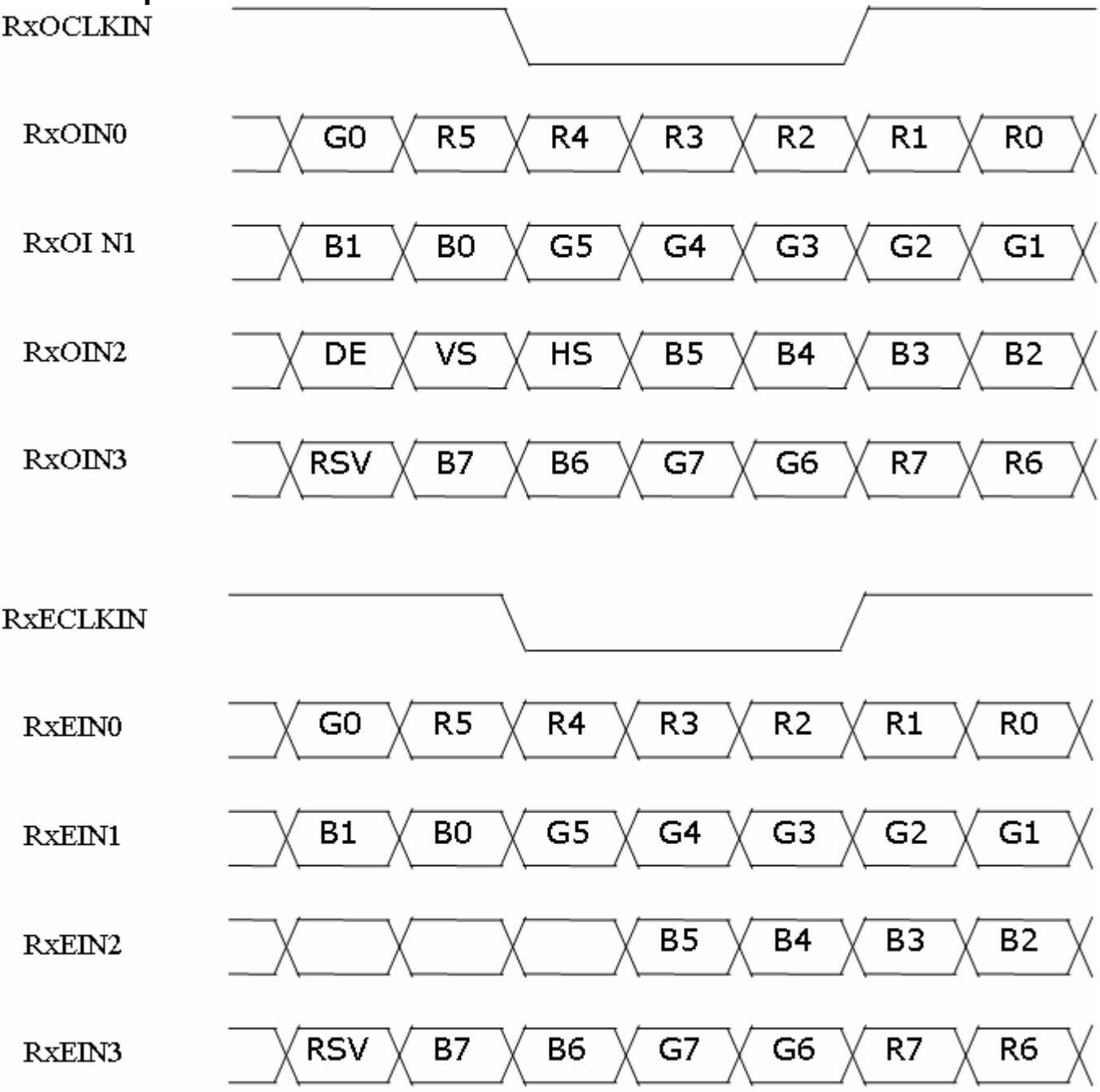
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format



Note: R/G/B data 7:MSB, R/G/B data 0:LSB

O = "First Pixel Data"

E = "Second Pixel Data"

6.3 Signal Description

The module using a pair of LVDS receiver SN75LVDS82(Texas Instruments) or compatible. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS83(negative edge sampling) or compatible. The first LVDS port(RxOxxx) transmits odd pixels while the second LVDS port(RxExxx) transmits even pixels.

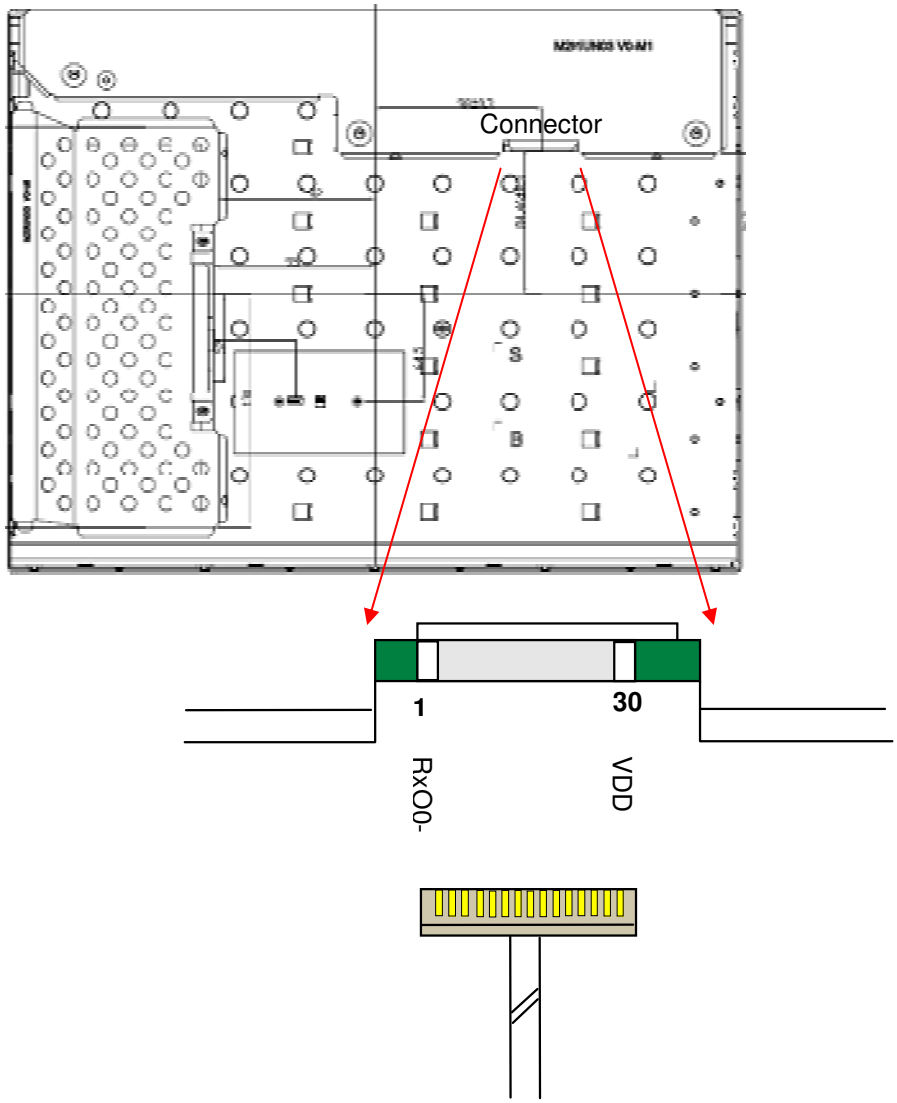
PIN #	SIGNAL NAME	DESCRIPTION
1	RxO0-	Negative LVDS differential data input (Odd data)
2	RxO0+	Positive LVDS differential data input (Odd data)
3	RxO1-	Negative LVDS differential data input (Odd data)
4	RxO1+	Positive LVDS differential data input (Odd data)
5	RxO2-	Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG)
6	RxO2+	Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG)
7	GND	Power Ground
8	RxOC-	Negative LVDS differential clock input (Odd clock)
9	RxOC+	Positive LVDS differential clock input (Odd clock)
10	RxO3-	Negative LVDS differential data input (Odd data)
11	RxO3+	Positive LVDS differential data input (Odd data)
12	RxE0-	Negative LVDS differential data input (Even clock)
13	RxE0+	Positive LVDS differential data input (Even data)
14	GND	Power Ground
15	RxE1-	Positive LVDS differential data input (Even data)
16	RxE1+	Negative LVDS differential data input (Even data)
17	GND	Power Ground
18	RxE2-	Negative LVDS differential data input (Even data)
19	RxE2+	Positive LVDS differential data input (Even data)
20	RxEC-	Negative LVDS differential clock input (Even clock)
21	RxEC+	Positive LVDS differential clock input (Even clock)
22	RxE3-	Negative LVDS differential data input (Even data)
23	RxE3+	Positive LVDS differential data input (Even data)
24	GND	Power Ground
25	NC	-
26	NC	-
27	NC	-
28	POWER	Power
29	POWER	Power
30	POWER	Power

Note: Input signals of odd and even clock shall be the same timing.

LVDS DATA Name	Description
DSP	Display Timing: When the signal is high, the pixel data shall be valid to be displayed
V-S	Vertical Sync: Both Positive and Negative polarity are acceptable
H-S	Horizontal Sync: Both Positive and Negative polarity are acceptable

TI LVDS X'mitter SN75LVDS83	**Module LVDS signal (interface connector pin7)**
Signal Name	**Low(open)**
D0	Red0
D1	Red1
D2	Red2
D3	Red3
D4	Red4
D5	Red7
D6	Red5
D7	Green0
D8	Green1
D9	Green2
D10	Green6
D11	Green7
D12	Green3
D13	Green4
D14	Green5
D15	Blue0
D16	Blue6
D17	Blue7
D18	Blue1
D19	Blue2
D20	Blue3
D21	Blue4
D22	Blue5
D23	NA
D24	H Sync
D25	V Sync
D26	Display Timing
D27	Red6

Note2: Start from left side



6.4 Interface Timing

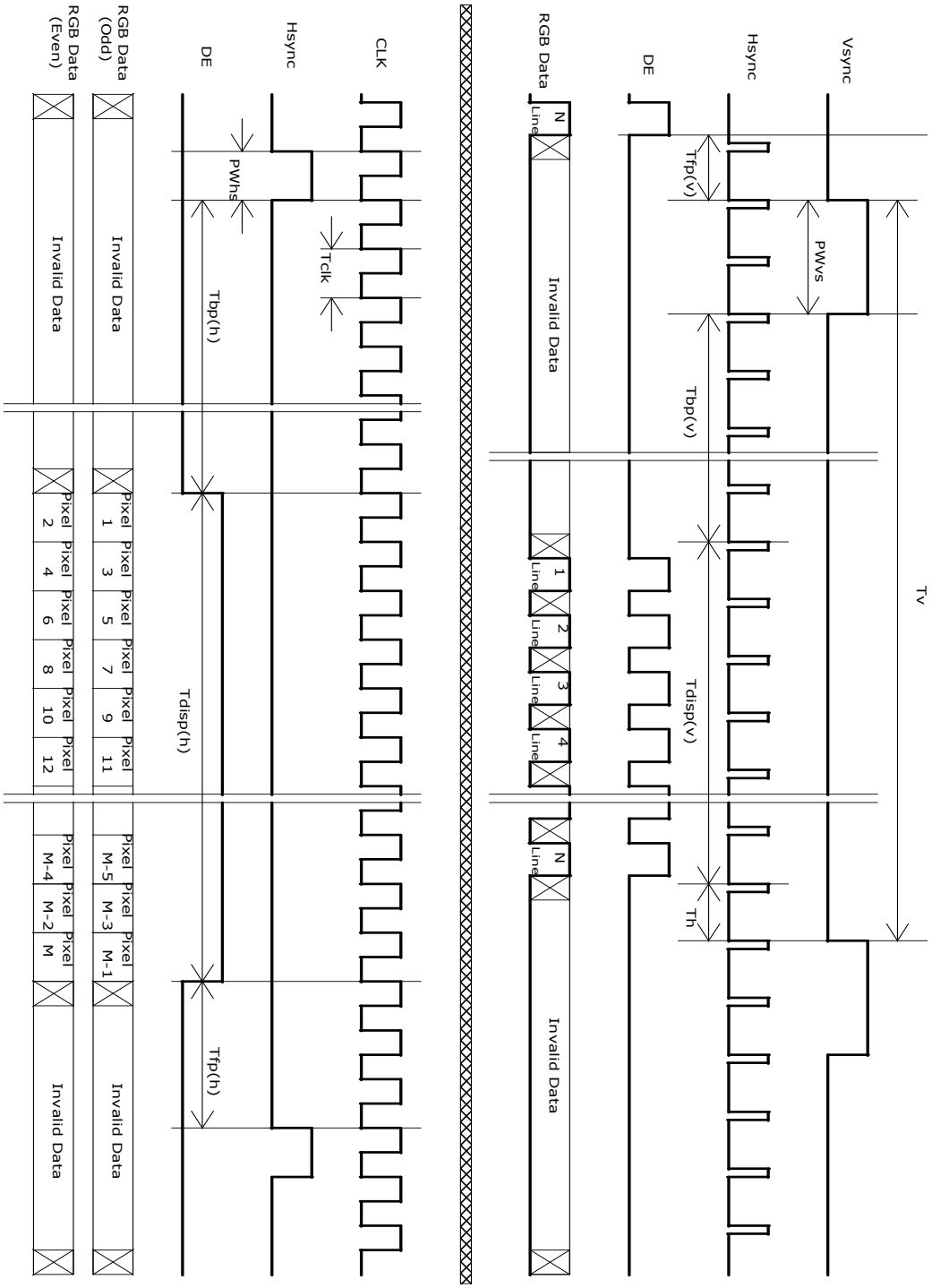
6.4.1 Timing Characteristics

Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS82DGG (Texas Instruments) or equivalent.

Signal	Item	Symbol	Min	Typ	Max	Unit
Vertical Section	Period	Tv	1211	1250	1300	Th
	Active	Tdisp(v)	1200	1200	1200	Th
	Blanking	Tbp(v)+Tfp(v)+PWvs	11	50	100	Th
Horizontal Section	Period	Th	880	1080	1160	Tclk
	Active	Tdisp(h)	800	800	800	Tclk
	Blanking	Tbp(h)+Tfp(h)+PWhs	80	280	360	Tclk
Frame Rate	Frequency	Freq/(Tv x Th)	55	60	75	Hz
Clock	Period	Tclk	12.0	12.3	17.1	ns
	Frequency	Freq	59	81	83	MHz

Note : DE mode only

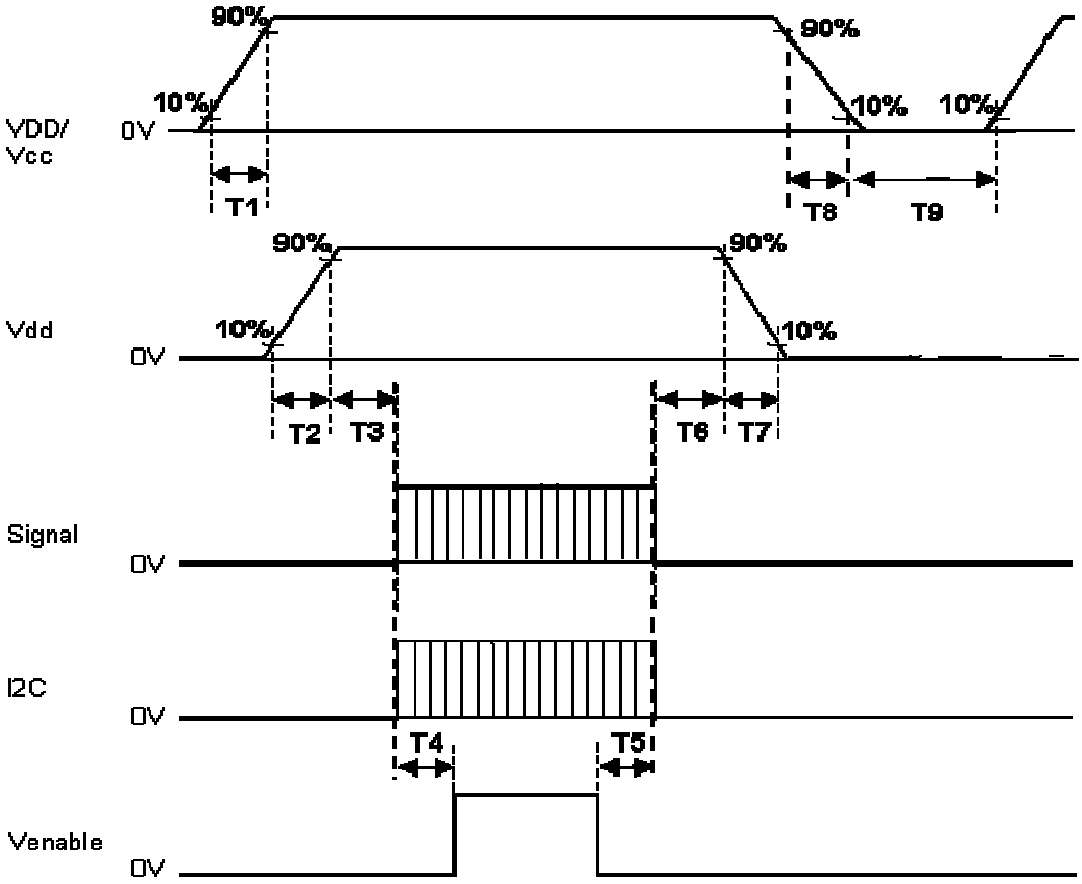
6.4.2 Timing diagram



Note :1600X1200 at 60 Hz (VESA STANDARD)

6.5 Power ON/OFF Sequence

Input power and LED on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when power off.



Power Sequence Timing

Symbol	Values			Unit
	Min	Typ	Max	
T1	0.5	-	10	[ms]
T2	0.5	-	10	[ms]
T3	0.5	40	50	[ms]
T4	400	-	-	[ms]
T5	400	-	-	[ms]
T6	0.5	16	50	[ms]
T7	0.5	-	10	[ms]
T8	0.5	-	10	[ms]
T9	1000	-	-	[ms]

7. Connector & Pin Assignment

Physical interface is described as for the connector on module.These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

7.1.1 Connector

Connector Name / Designation	Interface Connector / Interface card
Manufacturer	JAE or compatible
Type Part Number	FI-XB30SSL-HF15 or MDF76TW-30S-1H58
Mating Housing Part Number	FI-X30S-H

7.1.2 Pin Assignment

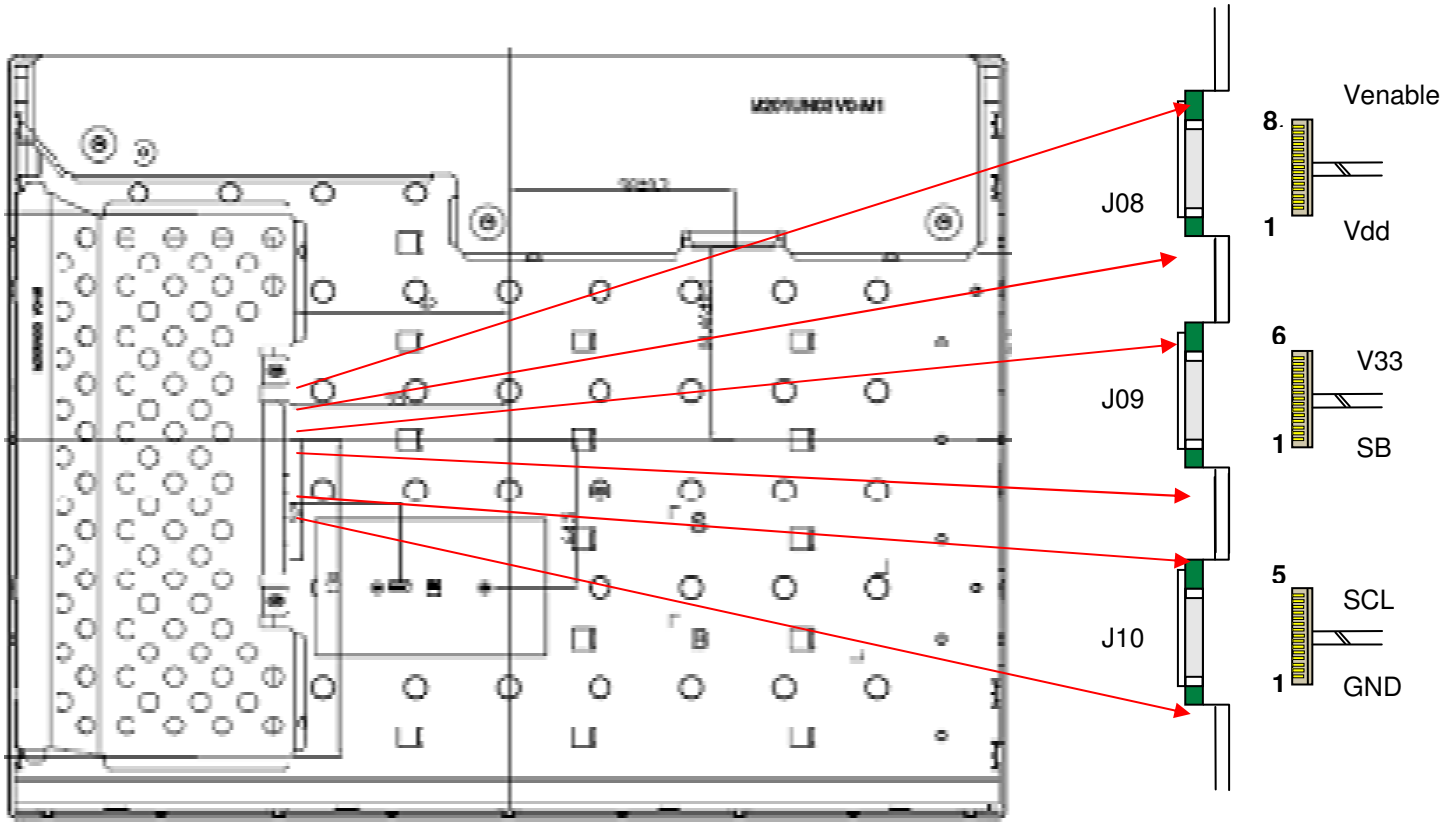
Pin#	Signal Name	Pin#	Signal Name
1	RxO0-	2	RxO0+
3	RxO1-	4	RxO1+
5	RxO2-	6	RxO2+
7	GND	8	RxOC-
9	RxOC+	10	RxO3-
11	RxO3+	12	RxE0-
13	RxE0+	14	GND
15	RxE1-	16	RxE1+
17	GND	18	RxE2-
19	RxE2+	20	RxEC-
21	RxEC+	22	RxE3-
23	RxE3+	24	GND
25	NC	26	NC
27	NC	28	Power
29	Power	30	Power

7.2 Backlight Unit

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

Backlight Power J08	**Connector Name / Designation**	Connector / Backlight Power
	Manufacturer	P-Two
	Type Part Number	CW3084-AAG1Z (8 pins)
	Mating Type Part Number	P24268 (8 pins)
Backlight I2C J10	**Connector Name / Designation**	Connector / Backlight I2C
	Manufacturer	P-Two
	Type Part Number	CW3054-AAG1Z (5 pins)
	Mating Type Part Number	P24265 (5 pins)

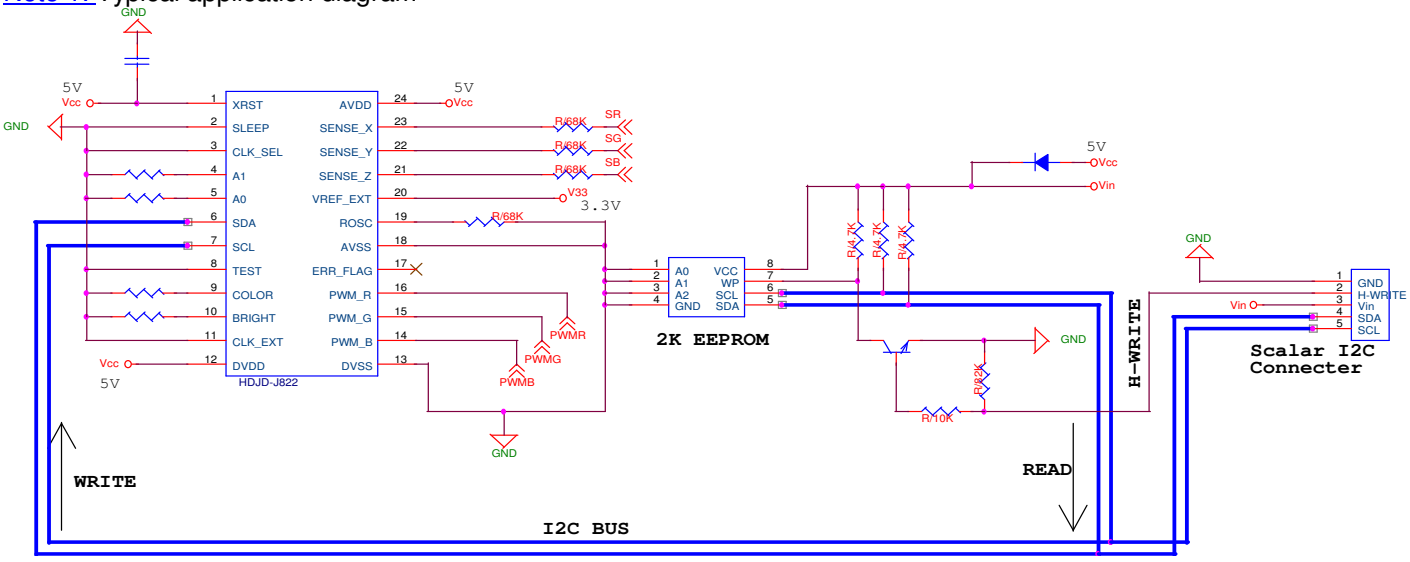
Note1: Start from upper side



7.2.1 Signal for LED connector

Connector No.	Pin No.	Label	Function
Backlight Power	1	Vdd	24V
	2	Vdd	24V
	3	Vdd	24V
	4	GND	GND
	5	GND	GND
	6	GND	GND
	7	Vcc	5V
	8	Venable	5V
LED sensor	1	SB	Analog signal
	2	SR	Analog signal
	3	SG	Analog signal
	4	GND	GND
	5	Vcc	5V
	6	V33	3.3V
Backlight I^2C(Note 1, 2)	1	GND	GND
	2	WP	Write Protect (connect to GND enable)
	3	Vin	5V(connect to Vcc)
	4	SDA	Serial Data Line
	5	SCL	Serial Clock Line

Note 1: Typical application diagram



Note 2: Please refer to AVAGO HDJD-J822 in detail.

8. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50℃, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50℃, 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0℃, 300hours	
High Temperature Storage (HTS)	Ta= 60℃, 300hours	
Low Temperature Storage (LTS)	Ta= -20℃, 300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 G Wave: Random Frequency: 10 - 200 - 10 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Drop Test	Height: 60 cm, package test	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω) 1sec, 8 points, 25 times/ point.	2
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 8 points, 25 times/ point.	
Altitude Test	Operation:10,000 ft Non-Operation:30,000 ft	

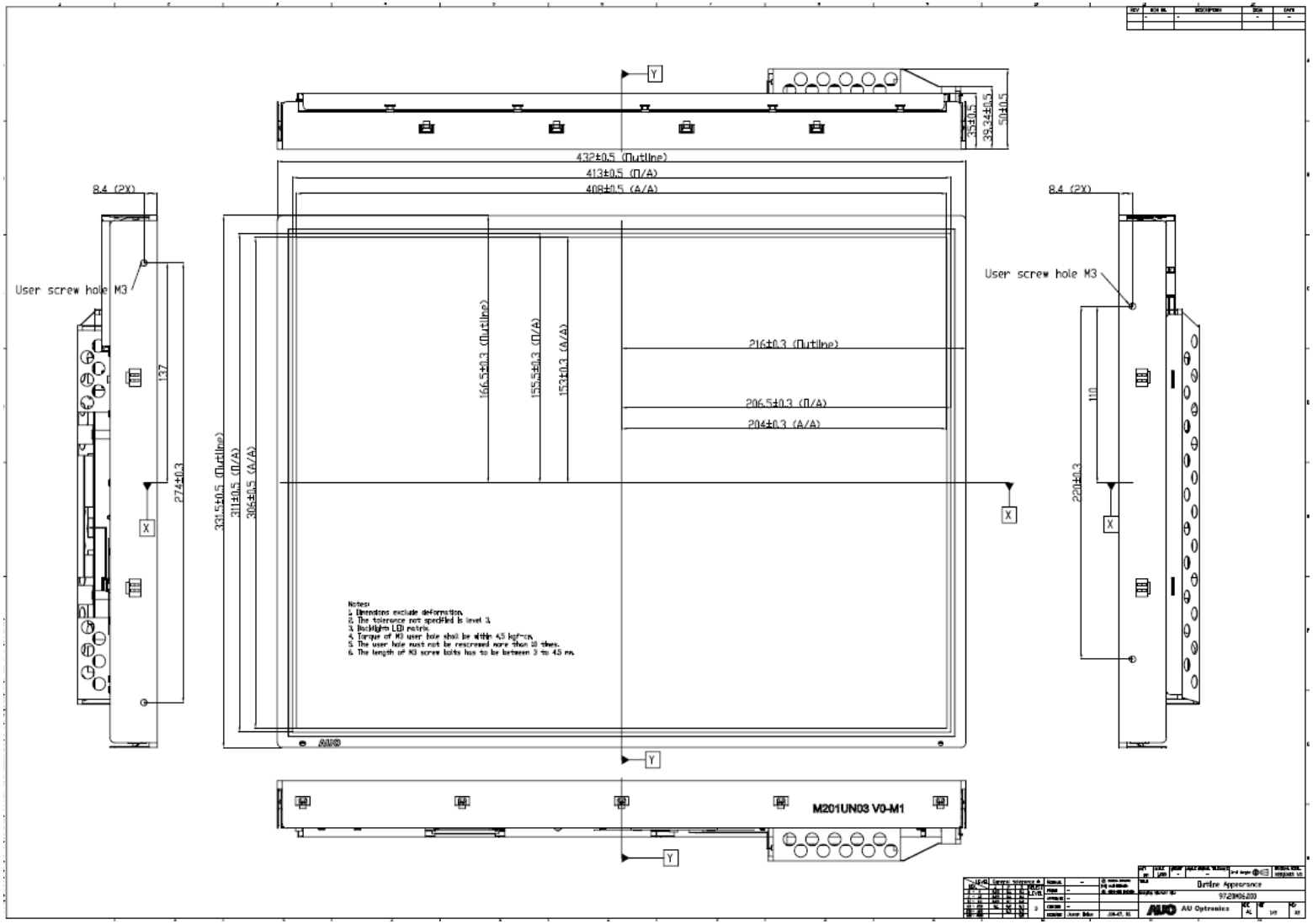
Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20℃ to 60℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

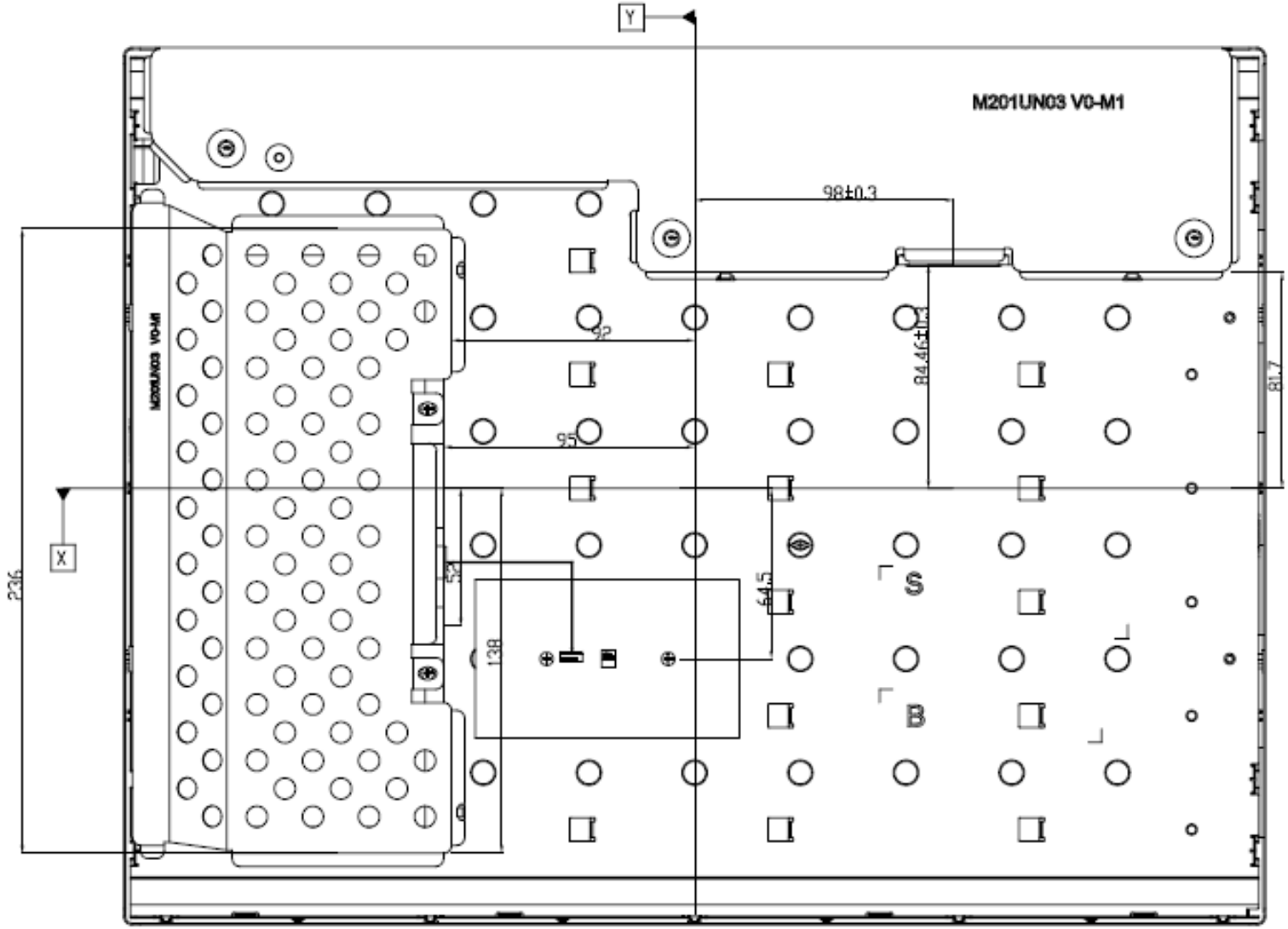
Note 2: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

9. Shipping Label

The shipping label format is shown as below.

10. Mechanical Characteristic




Y
X
M201UN03 V0-M1
98±0.3
92
95
84.46±0.3
81.7
236
52
64.5
138
S
B
L