TITLE : HV080X01-100

Product Specification

HYDIS Technologies
## REVISION HISTORY

<table>
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<th>REV.</th>
<th>ECN NO.</th>
<th>DESCRIPTION OF CHANGES</th>
<th>DATE</th>
<th>PREPARED</th>
</tr>
</thead>
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<tr>
<td>0</td>
<td></td>
<td>Initial Release</td>
<td>11. 11. 21</td>
<td>S.H.Han</td>
</tr>
</tbody>
</table>
| A    | E1202-F003 | 4.2 Optical Specifications  
|      |          | 4.3 Optical Measurements                                  | 12. 02. 13 | S.T.KO |

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**SPEC. NUMBER**  
S864-1458

**SPEC TITLE**  
HV080X01-100 Product Specification

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B2005-C001-D (2/3)  
A4(210 X 297)
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1.0 GENERAL DESCRIPTION

1.1 Introduction
HV080X01-100 is a color active matrix TFT LCD module using amorphous silicon TFT’s (Thin Film Transistors) as an active switching devices. This module has a 8.01 inch diagonally measured active area with XGA resolutions (768 horizontal by 1024 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical Stripe and this module can display 16.7M colors. The TFT-LCD panel used for this module is a low reflection and higher color type.

1.2 Features
- 3.3 V & 1.8V Logic Power
- MIPI Interface (DSI 1.01 D-PHY 1.0. Video mode only)
- 16.7M Colors (6bit + HFRC)
- Data Enable Signal Mode
- SMD LED (28EA) Array (Left Side)
- Green Product (RoHS) & Halogen free
1.3 Application
  • Slate

1.4 General Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
<th>Unit</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active area</td>
<td>122.112(H) × 162.816(V)</td>
<td>mm</td>
<td></td>
</tr>
<tr>
<td>Number of pixels</td>
<td>768(H) × RGB X 1024(V)</td>
<td>pixels</td>
<td></td>
</tr>
<tr>
<td>Pixel pitch</td>
<td>0.159 × 0.159</td>
<td>mm</td>
<td></td>
</tr>
<tr>
<td>Pixel arrangement</td>
<td>RGB Vertical Stripe</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Display colors</td>
<td>16.7M (6bit + HFRC)</td>
<td>colors</td>
<td></td>
</tr>
<tr>
<td>Display mode</td>
<td>Normally Black</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Outline dimension</td>
<td>130.412±0.15(H) × 171.916±0.15(V) × 2.4 ±0.1(D)</td>
<td>mm</td>
<td>Note 1</td>
</tr>
<tr>
<td>Weight</td>
<td>90g Typ. / 100g Max</td>
<td>g</td>
<td></td>
</tr>
<tr>
<td>Back-light</td>
<td>Left edge side, 28-LEDs type</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: at without component
2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit.

< Table 2. Absolute Maximum Ratings >

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Power Supply Voltage</td>
<td>(V_{\text{DD}})</td>
<td>-0.3</td>
<td>4.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Logic Power Supply Voltage</td>
<td>(V_{\text{CC}})</td>
<td>-0.3</td>
<td>2.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Back-light Power Supply Voltage</td>
<td>(H_{V_{\text{DD}}})</td>
<td>-0.3</td>
<td>40</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Back-light LED Current</td>
<td>(I_{\text{LED}})</td>
<td>-</td>
<td>30</td>
<td>mA</td>
<td>Note 1</td>
</tr>
<tr>
<td>Back-light LED Reverse Voltage</td>
<td>(V_{\text{R}})</td>
<td>-</td>
<td>5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>(T_{\text{OP}})</td>
<td>-20</td>
<td>+60</td>
<td>°C</td>
<td>Note 1,</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>(T_{\text{SP}})</td>
<td>-30</td>
<td>+70</td>
<td>°C</td>
<td>Note 2</td>
</tr>
</tbody>
</table>

Note 1. Ambient temperature vs allowable forward current are shown in the figure below.

Note 2. Temperature and relative humidity range are shown in the figure below.

90% RH Max. (40°C ≥ Ta)
Maximum wet-bulb temperature at 39°C or less. (> 40°C) No condensation.
3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

< Table 3. Electrical Specifications >

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Power Supply Voltage</td>
<td>V_{DD}</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Logic Power Supply Current</td>
<td>I_{DD}</td>
<td>-</td>
<td>105</td>
<td>-</td>
<td>mA Vd=3.3V, 25°C Note 1</td>
</tr>
<tr>
<td>Logic Power Supply Voltage</td>
<td>V_{CC}</td>
<td>1.65</td>
<td>1.8</td>
<td>1.95</td>
<td>V</td>
</tr>
<tr>
<td>Logic Power Supply Current</td>
<td>I_{CC}</td>
<td>-</td>
<td>23</td>
<td>-</td>
<td>mA Vcc=1.8V, 25°C Note 1</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>P_{DD}</td>
<td>-</td>
<td>0.35</td>
<td>-</td>
<td>W Vdd=3.3V, 25°C Note 1</td>
</tr>
<tr>
<td></td>
<td>P_{CC}</td>
<td>-</td>
<td>0.04</td>
<td>-</td>
<td>W Vcc=1.8V, 25°C Note 1</td>
</tr>
<tr>
<td></td>
<td>P_{total}</td>
<td>-</td>
<td>0.39</td>
<td>-</td>
<td>W</td>
</tr>
<tr>
<td>Back-light LED Voltage</td>
<td>V_{LED}</td>
<td>2.8</td>
<td>3.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Back-light LED Current</td>
<td>I_{LED}</td>
<td>-</td>
<td>20.0</td>
<td>-</td>
<td>mA</td>
</tr>
</tbody>
</table>

Notes: 1. The supply voltage is measured and specified at the interface connector of LCM.
(Image pattern : White)
3.2 PWM Duty Ratio vs Brightness

![Graph showing the relationship between duty ratio and relative brightness.](image)

Notes:
- In case of duty ratio 0%, LED can’t illuminate itself so this state is LED off.
- In case of duty ratio 100%, the brightness of LED is maximum and the state is LED on.
## 3.2 MIPI Interface DC Characteristic

< Table 4. MIPI Interface DC Characteristic >

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-ended input low voltage</td>
<td>$V_{ILHS}$</td>
<td>-40</td>
<td>-</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Single-ended input high voltage</td>
<td>$V_{IHHS}$</td>
<td>-</td>
<td>460</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Common-mode voltage</td>
<td>$V_{CMRXDC}$</td>
<td>70</td>
<td>-</td>
<td>330</td>
<td>mV</td>
</tr>
<tr>
<td>Differential input impedance</td>
<td>$Z_{ID}$</td>
<td>80</td>
<td>100</td>
<td>125</td>
<td>ohm</td>
</tr>
<tr>
<td>HS transmit differential voltage</td>
<td>$I_{VODI}$</td>
<td>140</td>
<td>200</td>
<td>250</td>
<td>mV</td>
</tr>
<tr>
<td>Pad signal voltage range</td>
<td>$V_i$</td>
<td>-50</td>
<td>-</td>
<td>1350</td>
<td>mV</td>
</tr>
<tr>
<td>Ground shift</td>
<td>$V_{GNDSH}$</td>
<td>-50</td>
<td>-</td>
<td>50</td>
<td>mV</td>
</tr>
<tr>
<td>Logic 0 input threshold</td>
<td>$V_{IL}$</td>
<td>0</td>
<td>-</td>
<td>550</td>
<td>mV</td>
</tr>
<tr>
<td>Logic 1 input threshold</td>
<td>$V_{IH}$</td>
<td>880</td>
<td>-</td>
<td>1350</td>
<td>mV</td>
</tr>
<tr>
<td>Input hysteresis</td>
<td>$V_{HYST}$</td>
<td>25</td>
<td>-</td>
<td>-</td>
<td>mV</td>
</tr>
<tr>
<td>Output low level</td>
<td>$V_{OL}$</td>
<td>-50</td>
<td>-</td>
<td>50</td>
<td>mV</td>
</tr>
<tr>
<td>Output high level</td>
<td>$V_{OH}$</td>
<td>1.1</td>
<td>1.2</td>
<td>1.3</td>
<td>V</td>
</tr>
<tr>
<td>Output impedance of Low power transmitter</td>
<td>$Z_{OLP}$</td>
<td>80</td>
<td>100</td>
<td>125</td>
<td>ohm</td>
</tr>
<tr>
<td>Logic 0 contention threshold</td>
<td>$V_{ILCD.MAX}$</td>
<td>-</td>
<td>-</td>
<td>200</td>
<td>mV</td>
</tr>
<tr>
<td>Logic 0 contention threshold</td>
<td>$V_{ILCD.MIN}$</td>
<td>450</td>
<td>-</td>
<td>-</td>
<td>mV</td>
</tr>
</tbody>
</table>

![Diagram of MIPI Interface DC Characteristic](image)
### 3.3 MIPI Interface AC Characteristic

#### 3.3.1 LP Transmission

<Table 5. LP Transmitter AC Specifications>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>15%~85% rise time and fall time</td>
<td></td>
<td></td>
<td>25</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>30%~85% rise time and fall time</td>
<td></td>
<td></td>
<td>35</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Pulse width of the LP exclusive-OR clock</td>
<td></td>
<td></td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>First LP exclusive-OR Clock pulse after STOP state or last pulse before stop state</td>
<td></td>
<td></td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Period of the LP exclusive-OR clock</td>
<td></td>
<td></td>
<td>90</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Slew Rate @ ( C_{LOAD} = 0 \text{pF} )</td>
<td>30</td>
<td>-</td>
<td>500</td>
<td>mV/ns</td>
<td></td>
</tr>
<tr>
<td>Slew Rate @ ( C_{LOAD} = 5 \text{pF} )</td>
<td>30</td>
<td>-</td>
<td>200</td>
<td>mV/ns</td>
<td></td>
</tr>
<tr>
<td>Slew Rate @ ( C_{LOAD} = 20 \text{pF} )</td>
<td>30</td>
<td>-</td>
<td>150</td>
<td>mV/ns</td>
<td></td>
</tr>
<tr>
<td>Slew Rate @ ( C_{LOAD} = 70 \text{pF} )</td>
<td>30</td>
<td>-</td>
<td>100</td>
<td>mV/ns</td>
<td></td>
</tr>
<tr>
<td>Load Capacitance</td>
<td></td>
<td></td>
<td>70</td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

![Diagram of LP and DP signals with timing measurements](image-url)
3.3.2 Turnaround Procedure

<Table 6. Turnaround Procedure Operation Timing Parameters>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length of any Low-Power state period : Master side</td>
<td>50</td>
<td>-</td>
<td>75</td>
<td>ns</td>
</tr>
<tr>
<td>Length of any Low-Power state period : Slave side</td>
<td>50</td>
<td>55.56</td>
<td>58.34</td>
<td>ns</td>
</tr>
<tr>
<td>Ratio of T_{LPX}(MASTER)/ T_{LPX}(SLAVE) between Master and Slave side</td>
<td>2/3</td>
<td>-</td>
<td>3/2</td>
<td>-</td>
</tr>
<tr>
<td>Time-out before new TX side start driving</td>
<td>T_{TA-SURE}</td>
<td>T_{LPX}</td>
<td>-</td>
<td>2T_{LPX}</td>
</tr>
<tr>
<td>Time to drive LP-00 by new TX</td>
<td>T_{TA-GET}</td>
<td>-</td>
<td>2T_{LPX}</td>
<td>-</td>
</tr>
<tr>
<td>Time to drive LP-00 after Turnaround Request</td>
<td>T_{TA-GO}</td>
<td>-</td>
<td>4T_{LPX}</td>
<td>-</td>
</tr>
</tbody>
</table>
### 3.3.3 High Speed Transmission

< Table 7. Data-Clock Timing Specifications>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>UI instantaneous</td>
<td>UIINST</td>
<td>2</td>
<td>-</td>
<td>12.5</td>
<td>ns</td>
</tr>
<tr>
<td>Data to Clock Skew [measure at transmitter]</td>
<td>TSKEW[TX]</td>
<td>-0.15</td>
<td>-</td>
<td>0.15</td>
<td>UIINST</td>
</tr>
<tr>
<td>Data to Clock Setup Time [measure at receiver]</td>
<td>TSETUP[RX]</td>
<td>0.15</td>
<td>-</td>
<td>-</td>
<td>UIINST</td>
</tr>
<tr>
<td>Data to Clock Hold Time [measure at receiver]</td>
<td>THOLD[RX]</td>
<td>0.15</td>
<td>-</td>
<td>-</td>
<td>UIINST</td>
</tr>
<tr>
<td>20%~80% rise and fall time</td>
<td>tr / tr</td>
<td>150</td>
<td>-</td>
<td>--</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-</td>
<td>0.3</td>
<td>UIINST</td>
<td></td>
</tr>
</tbody>
</table>

* note
1. This value corresponds to a minimum 80Mbps data rate
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
3. Total silicon and package delay budget of 0.3*UIINST
4. Total setup and hold window for receiver of 0.3*UIINST

![Diagram of data-clock timing specifications]
### 3.3.4 High Speed Data Transmission in Burst

< Table 8. High-Speed Data Transmission Operation Timing Parameters>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time to drive LP-00 to prepare for HS transmission</td>
<td>T_HS-PREPARE</td>
<td>40+4UI</td>
<td>-</td>
<td>85+6UI ns</td>
</tr>
<tr>
<td>Time from start of T_HS-TRAIL of tCLK-TRAIL period to start of LP-11 state</td>
<td>T_EOT</td>
<td>-</td>
<td>-</td>
<td>105+12UI ns</td>
</tr>
<tr>
<td>Time to enable Data Lane receiver line termination measured from when Dn cross V_{IL_MAX}</td>
<td>T_HS-TERM-EN</td>
<td>-</td>
<td>-</td>
<td>35+4UI ns</td>
</tr>
<tr>
<td>Time to drive flipped differential state after last payload data bit of a HS transmission burst</td>
<td>T_HS-TRAIL</td>
<td>60+4UI</td>
<td>-</td>
<td>- ns</td>
</tr>
<tr>
<td>Time-out at RX to ignore transition period of EoT</td>
<td>T_HS-SKIP</td>
<td>40</td>
<td>-</td>
<td>55+4UI ns</td>
</tr>
<tr>
<td>Time to drive LP-11 after HS burst</td>
<td>T_HS-EXIT</td>
<td>100</td>
<td>-</td>
<td>- ns</td>
</tr>
<tr>
<td>Length of any Low-Power state period</td>
<td>T_LPX</td>
<td>50</td>
<td>-</td>
<td>- ns</td>
</tr>
<tr>
<td>Sync sequence period</td>
<td>T_HS-SYNC</td>
<td>-</td>
<td>8UI</td>
<td>- ns</td>
</tr>
<tr>
<td>Minimum lead HS-0 drive period before the sync sequence</td>
<td>T_HS-ZERO</td>
<td>105+6UI</td>
<td>-</td>
<td>- ns</td>
</tr>
</tbody>
</table>

*note*
1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the support rates.
2. UI means Unit Interval, equal to one half HS the clock period on the Clock Lane.
3. T_LP is internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise an fall times.
### 3.3.5 High Speed Clock Transmission

< Table 9. Switching the Clock Lane Operation Timing Parameters>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode</td>
<td>T_CLK-POST</td>
<td>60+52UI</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Detection time that the clock has stopped toggling</td>
<td>T_CLK-MISS</td>
<td>-</td>
<td>-</td>
<td>60 ns</td>
</tr>
<tr>
<td>Time to drive LP-00 to prepare for HS clock transmission</td>
<td>T_CLK-PREPARE</td>
<td>38</td>
<td>-</td>
<td>95 ns</td>
</tr>
<tr>
<td>Minimum lead HS-0 drive period before starting Clock</td>
<td>T_CLK-PREPAR + T_CLK-ZERO</td>
<td>300</td>
<td>-</td>
<td>- ns</td>
</tr>
<tr>
<td>Time to enable Clock Lane receiver line termination measured from when Dn cross VIL.MAX</td>
<td>T_HS-TERM-EN</td>
<td>-</td>
<td>-</td>
<td>38 ns</td>
</tr>
<tr>
<td>Minimum time that the HS clock must be set prior to any associated data lane beginning the transmission from LP to HS mode</td>
<td>T_CLK-PRE</td>
<td>8</td>
<td>-</td>
<td>- ns</td>
</tr>
<tr>
<td>Time to drive HS differential state after last payload clock bit of a HS transmission burst</td>
<td>T_CLK-TRAIL</td>
<td>60</td>
<td>-</td>
<td>- ns</td>
</tr>
</tbody>
</table>

* note

The DSI host processor shall support continuous clock on the Clock Lane for NT51012 chip that require it. So the host processor needs to keep the HS-serial clock running.

---

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3.3.6 LP11 timing request between data transformation

When Clock lane of DSI TX chip always keeps High speed mode, then Clock lane never go back to Low power mode. If Date lane of TX chip needs to transmit the next new data transmission or sequence, after the end of Low power mode or High speed mode or BTA. Then TX chip needs to keep LP-11 stop state before the next new data transmission, no matter in Low power mode or High speed mode or BTA. The LP-11 minimum BTA – BTA, LP – BTA, BTA – LP, HS – BTA, and BTA – HS. This rule is suitable for short or long packet between TX and RX data transmission.

(1) Timing between LP – LP command

![Diagram of LP11 timing request between data transformation]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>LP-11 delay to a start of the new Escape Mode Entry</td>
<td>$T_{DEE}$</td>
<td>150</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>

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(2) Timing between LP – HS command

Parameter | Min. | Typ. | Max. | Unit
--- | --- | --- | --- | ---
LP-11 delay to a start of the Entering High Speed Mode | T\textsubscript{DEH} | Max(150,32UI) | - | ns

(3) Timing between HS - LP command

Parameter | Min. | Typ. | Max. | Unit
--- | --- | --- | --- | ---
LP-11 delay to a start of the Entering High Speed Mode | T\textsubscript{DEH} | Max(150,32UI) | - | ns
(4) Timing between HS – HS command

![Diagram of timing between HS – HS command]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>LP-11 delay to a start of the Entering High Speed Mode</td>
<td>$T_{DHH}$</td>
<td>Max(150,32UI)</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>

(5) Timing between BTA - BTA command

![Diagram of timing between BTA - BTA command]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>LP-11 delay to a start of the new BTA</td>
<td>$T_{DBB}$</td>
<td>150</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>
(6) Timing between LP – BTA command

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>LP-11 delay to a start of the BTA</td>
<td></td>
<td>TDEB</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Max(150,32UI)

(7) Timing between BTA - LP command

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>LP-11 delay to a start of the Escape Mode Entry</td>
<td></td>
<td>TDBE</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

150
### (8) Timing between HS – BTA command

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>LP-11 delay to a start of the BTA</td>
<td>( T_{DBH} )</td>
<td>Max(150,32UI)</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>

### (9) Timing between BTA - HS command

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>LP-11 delay to a start of the Escape Mode Entry</td>
<td>( T_{DBH} )</td>
<td>Max(150,32UI)</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>
### 4.0 OPTICAL SPECIFICATIONS

#### 4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2°C) with the equipment of Luminance meter system (Goniometer system and TOPCON BM-5A) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and φ equal to 0°. We refer to $\theta_{\phi=0}$ (= θ 3 ) as the 3 o’clock direction (the “right”), $\theta_{\phi=90}$ (= θ 12 ) as the 12 o’clock direction (“upward”), $\theta_{\phi=180}$ (= θ 9 ) as the 9 o’clock direction (“left”) and $\theta_{\phi=270}$ (= θ 6 ) as the 6 o’clock direction (“bottom”). While scanning θ and/or φ, the center of the measuring spot on the Display surface shall stay fixed. The backight should be operating for 30 minutes prior to measurement. $V_{DD}$ shall be 3.3+/− 0.3V at 25°C.

#### 4.2 Optical Specifications

<Table 10. Optical Specifications>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Viewing Angle range</td>
<td>$\Theta_3$</td>
<td></td>
<td>-</td>
<td>85</td>
<td>Deg.</td>
<td></td>
<td>Note 1</td>
</tr>
<tr>
<td></td>
<td>$\Theta_9$</td>
<td></td>
<td>-</td>
<td>85</td>
<td>Deg.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$\Theta_{12}$</td>
<td></td>
<td>-</td>
<td>85</td>
<td>Deg.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$\Theta_6$</td>
<td></td>
<td>-</td>
<td>85</td>
<td>Deg.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Luminance Contrast ratio</td>
<td>CR</td>
<td>$\theta = 0°$</td>
<td>600</td>
<td>800</td>
<td>-</td>
<td>cd/m²</td>
<td>Note 2</td>
</tr>
<tr>
<td>Luminance of White</td>
<td>$Y_w$</td>
<td>$\theta = 0°$</td>
<td>360</td>
<td>450</td>
<td>-</td>
<td></td>
<td>Note 3</td>
</tr>
<tr>
<td>White Luminance uniformity</td>
<td>$\Delta Y$</td>
<td>$\theta = 0°$</td>
<td>70</td>
<td>80</td>
<td>-</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>White Chromaticity</td>
<td>$W_x$</td>
<td>$\theta = 0°$</td>
<td>0.270</td>
<td>0.300</td>
<td>0.330</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$W_y$</td>
<td></td>
<td>0.290</td>
<td>0.320</td>
<td>0.350</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reproduction of color</td>
<td>$R_x$</td>
<td>$\theta = 0°$</td>
<td>0.574</td>
<td>0.604</td>
<td>0.634</td>
<td></td>
<td>Note 3</td>
</tr>
<tr>
<td></td>
<td>$R_y$</td>
<td></td>
<td>0.309</td>
<td>0.339</td>
<td>0.369</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$G_x$</td>
<td>$\theta = 0°$</td>
<td>0.286</td>
<td>0.316</td>
<td>0.346</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$G_y$</td>
<td></td>
<td>0.595</td>
<td>0.625</td>
<td>0.655</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$B_x$</td>
<td>$\theta = 0°$</td>
<td>0.134</td>
<td>0.164</td>
<td>0.194</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$B_y$</td>
<td></td>
<td>0.114</td>
<td>0.144</td>
<td>0.174</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Response Time Total $T_{r+d}$</td>
<td>$T_a= 25° C$</td>
<td>$\theta = 0°$</td>
<td>-</td>
<td>30</td>
<td>-</td>
<td>ms</td>
<td>Note 5</td>
</tr>
<tr>
<td>Cross Talk</td>
<td>CT</td>
<td>$\theta = 0°$</td>
<td>-</td>
<td>-</td>
<td>2.0</td>
<td>%</td>
<td>Note 6</td>
</tr>
</tbody>
</table>
Notes:

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o’clock direction and the vertical or 6, 12 o’clock direction with respect to the optical axis which is normal to the LCD surface (see Figure1).

2. Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state (see Figure1). Luminance Contrast Ratio (CR) is defined mathematically as $CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$.

3. Reference only / Standard Front Surface Treatment Measured with green cover glass. The color chromaticity coordinates specified in Table 10 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
4.3 Optical Measurements

Figure 1. Measurement Set Up

![Diagram showing measurement setup]

Center of the screen
Optical characteristics measurement setup

Figure 2. White Luminance and Uniformity Measurement Locations (9 points)

![Diagram showing measurement locations]

Note 4.
The White luminance uniformity on LCD surface is then expressed as:
\[ \Delta Y = \left( \frac{\text{Minimum Luminance of 9 points}}{\text{Maximum Luminance of 9 points}} \right) \times 100 \]
(See Figure 2)

* LED Condition = (Duty Ratio 100%, LED current 20.0mA)
Figure 3. Response Time Testing

![Response Time Testing Diagram](image-url)
Figure 4. Cross Modulation Test Description

\[ \text{Cross-Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_B} \right| \times 100 \]

Where:
- \( Y_A \) = Initial luminance of measured area (cd/m\(^2\))
- \( Y_B \) = Subsequent luminance of measured area (cd/m\(^2\))

The location measured will be exactly the same in both patterns

Note 5.
The electro-optical response time measurements shall be made as Figure 4 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is \( T_r \), and 90% to 10% is \( T_d \).

Note 6.
Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance \( (Y_A) \) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance \( (Y_B) \) of that same area when any adjacent area is driven dark (Refer to Figure 4).
5.0 INTERFACE CONNECTIONS
5.1 Electrical Interface Connection

CN1
- HYDIS side connector: LS mtron / GB042-34S-H10
- User side connector: LS mtron / GB042-34P-H10

<Table 11, Electrical Interface Connection>

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ID</td>
<td>LCD ID</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>3</td>
<td>MIPI_D0_N</td>
<td>MIPI Data Input</td>
</tr>
<tr>
<td>4</td>
<td>MIPI_D1_P</td>
<td>MIPI Data Input</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>6</td>
<td>MIPI_D1_N</td>
<td>MIPI Data Input</td>
</tr>
<tr>
<td>7</td>
<td>MIPI_D1_P</td>
<td>MIPI Data Input</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>9</td>
<td>MIPI_CLK_N</td>
<td>MIPI Clock Input</td>
</tr>
<tr>
<td>10</td>
<td>MIPI_CLK_P</td>
<td>MIPI Clock Input</td>
</tr>
<tr>
<td>11</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>12</td>
<td>MIPI_D2_N</td>
<td>MIPI Data Input</td>
</tr>
<tr>
<td>13</td>
<td>MIPI_D2_P</td>
<td>MIPI Data Input</td>
</tr>
<tr>
<td>14</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>15</td>
<td>MIPI_D3_N</td>
<td>MIPI Data Input</td>
</tr>
<tr>
<td>16</td>
<td>MIPI_D3_P</td>
<td>MIPI Data Input</td>
</tr>
<tr>
<td>17</td>
<td>GND</td>
<td>Ground</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>VDD</td>
<td>Power Supply +3.3V</td>
</tr>
<tr>
<td>23</td>
<td>VDD</td>
<td>Power Supply +3.3V</td>
</tr>
<tr>
<td>22</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>21</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>20</td>
<td>VCC</td>
<td>Power Supply +1.8V</td>
</tr>
<tr>
<td>19</td>
<td>VCC</td>
<td>Power Supply +1.8V</td>
</tr>
<tr>
<td>18</td>
<td>GND</td>
<td>Ground</td>
</tr>
</tbody>
</table>

**Legend:**
- LCD ID
- MIPI Data Input
- MIPI Clock Input
- Power Supply
- Ground

LCD Module Rear View

**SPEC. NUMBER:** S864-1458
**SPEC TITLE:** HV080X01-100 Product Specification
5.2 Data Input Format

1 Pixel = 3 Dots

RGBRGB RGBRGB
1 Pixel = 3 Dots
RGBRGB RGBRGB
RGBRGB RGBRGB
RGBRGB RGBRGB
6.0. SIGNAL TIMING SPECIFICATIONS

6.1 The HV080X01 LCM is operated by the only DE (Data enable) mode

< Table 12, Signal Timing >

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frame Period</td>
<td>T1</td>
<td>1029</td>
<td>1032</td>
<td>1254</td>
<td>Lines</td>
<td></td>
</tr>
<tr>
<td>Vertical Display Period</td>
<td>T2</td>
<td>-</td>
<td>1024</td>
<td>-</td>
<td>Lines</td>
<td></td>
</tr>
<tr>
<td>One line Scanning Period</td>
<td>T3</td>
<td>828</td>
<td>832</td>
<td>1312</td>
<td>Clocks</td>
<td></td>
</tr>
<tr>
<td>Horizontal Display Period</td>
<td>T4</td>
<td>-</td>
<td>768</td>
<td>-</td>
<td>Clocks</td>
<td></td>
</tr>
<tr>
<td>Clock Frequency</td>
<td>T5</td>
<td>30</td>
<td>51.52</td>
<td>85</td>
<td>MHz</td>
<td>Note 1</td>
</tr>
</tbody>
</table>

Note 1. This value only guarantee for the circuit–operation
(NO guarantee of display quality)

7.0 SIGNAL TIMING WAVEFORMS

7.1 Timing Waveforms of Interface Signal

![Timing Waveforms Diagram]

Valid display data (768 Clocks)
8.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

A total of 16.7M colors are displayed with dither & HFRC using 64 gray from 8bit input.
9.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below

Notes:
1. When the power supply VDD/ VCC is 0V, Keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on.
3. Back Light must be turn on after power for logic and interface signal are valid.
10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

Figure 6 & 7 (located in 11.0) shows mechanical outlines for the model.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active Area</td>
<td>122.112(H) × 162.816(V)</td>
<td>mm</td>
</tr>
<tr>
<td>Number of pixels</td>
<td>768(H) X 1024(V) (1 pixel = R + G + B dots)</td>
<td></td>
</tr>
<tr>
<td>Pixel pitch</td>
<td>0.159(H) X 0.159(V)</td>
<td>mm</td>
</tr>
<tr>
<td>Pixel arrangement</td>
<td>RGB Vertical stripe</td>
<td></td>
</tr>
<tr>
<td>Display colors</td>
<td>16.7M (6bit + HFRC)</td>
<td></td>
</tr>
<tr>
<td>Display mode</td>
<td>Normally Black</td>
<td></td>
</tr>
<tr>
<td>Outline dimension</td>
<td>130.412(H) × 171.916(V) × 2.4(D) (Typ.)</td>
<td>mm</td>
</tr>
<tr>
<td>Weight</td>
<td>90g Typ. / 100g Max</td>
<td>g</td>
</tr>
<tr>
<td>Back-light</td>
<td>Edge side 28-LEDs type (4 X 7 Array)</td>
<td></td>
</tr>
</tbody>
</table>

10.2 LR and Polarizer Hardness.
The surface of the LCD has an Low reflection coating and a coating to reduce scratching.

10.3 Light Leakage
There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 150lux. The manufacture shall furnish limit samples of the panel showing the light leakage acceptable.
11.0 Mechanical Drawing

Figure 6. TFT-LCD Module Outline Dimension (Front View)
Figure 7. TFT-LCD Module Outline Dimensions (Rear view)

NOTE:
1. CN1: GB042-34S-H10
2. CRITICAL POINT: \( \times \times \)
3. WEIGHT SPEC: 90g typ /100g Max.
4. BENDING ALLOWANCE SPEC: \( \pm 0.47-0.24 \)
5. GENERAL TOLERANCE: \( \pm 0.5 \)
12.0 RELIABILITY TEST
The Reliability test items and its conditions are shown in below.

< Table14, Reliability Test >

<table>
<thead>
<tr>
<th>No</th>
<th>Test Item</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>High temperature Storage test</td>
<td>Ta = 80 °C, 48 hrs</td>
</tr>
<tr>
<td>2</td>
<td>Low temperature Storage test</td>
<td>Ta = -30 °C, 48 hrs</td>
</tr>
<tr>
<td>3</td>
<td>High temperature &amp; high humidity Storage test</td>
<td>Ta = 60 °C, 90%RH, 88hrs</td>
</tr>
<tr>
<td>4</td>
<td>High temperature Operation test</td>
<td>Ta = 70 °C, 24 hrs</td>
</tr>
<tr>
<td>5</td>
<td>Low temperature Operation test</td>
<td>Ta = -20 °C, 24 hrs</td>
</tr>
<tr>
<td>6</td>
<td>High temperature &amp; high humidity Operation test</td>
<td>Ta = 50 °C, 80%RH, 88hrs</td>
</tr>
<tr>
<td>7</td>
<td>Thermal shock</td>
<td>Ta = -30 °C ↔ 70 °C (30min), 50 cycle</td>
</tr>
<tr>
<td>8</td>
<td>Electro-static discharge test (non-operating)</td>
<td>Air : 150pF, 330ohm, 8KV Contact : 150pF, 330ohm, 6KV</td>
</tr>
</tbody>
</table>

13.0 HANDLING & CAUTIONS
13.1 Cautions when taking out the module
- Pick the pouch only, when taking out module from a shipping package.

13.2 Cautions for handling the module
- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back-light element are made from fragile glass (epoxy) material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.
13.3 Cautions for the operation
- When the module is operating, do not lose MCLK, DE signals. If any one of these signals were lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

13.4 Cautions for the atmosphere
- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

13.5 Cautions for the module characteristics
- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

13.6 Cautions for the digitizer assembly
- When assembling FPC connector, do not flip connector past 90° due to possible damage to connector.
- When positioning digitizer underneath driver IC, do not lift driver IC past 90° due to possible damage to drive IC pattern.
- Please be warned that during assembly of digitizer, the opening or closing of FPC will result in possible electrostatic discharge damage to the LED.

13.7 Other cautions
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc., Please pack the module not to be broken. We recommend to use the original shipping packages.
14.0 LABELS

14.1 Product Marking Table

- Barcode (Printed on back cover)

<table>
<thead>
<tr>
<th>No</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Control Number</td>
</tr>
<tr>
<td>2</td>
<td>Grade</td>
</tr>
<tr>
<td>3</td>
<td>Supplier code</td>
</tr>
<tr>
<td>4</td>
<td>Year</td>
</tr>
<tr>
<td>5</td>
<td>Month (1, 2, 3, ..., X, Y, Z)</td>
</tr>
<tr>
<td>6</td>
<td>Day</td>
</tr>
<tr>
<td>7</td>
<td>Revision code</td>
</tr>
<tr>
<td>8</td>
<td>Serial Number</td>
</tr>
</tbody>
</table>
14.2 Packing Label

Label Size: 108 mm (L) × 56 mm (W)
Contents
Model: HV080X01-100
Q’ty: Module Q’ty in one box
Serial No.: Box Serial No. See next figure for detail description.
Date: Packing Date
FG Code: FG Code of Product
15.0 PACKING INFORMATION

15.1 Packing order

Each tray must be loaded with 180° rotation respectively

8EA(7+1) Trays (With Cover-Tray)

2EA Module per Tray

Packing (Anti Static Packing BAG)

Cushion – 2EA per Inner-Box

Inner-Box

5ea per Outer-Box

Box Label

14EA Module per Inner-Box

Box Label

Notes:
1. Box Dimension: 333mm(W) X 333mm(D) X 435mm(H)
2. Package Quantity in one Box : 70pcs
15.2 Pallet Packing

* Note
- Pallet Dimension: 1100 mm (L) x 1100 mm (W) x 120 mm (H)
- Package Quantity in one Box: 70pcs
- Box Quantity in one Pallet: 18box