

Product Specifications

Customer	
Description	2.36" TFT LCD Module
Model Name	LQ024AC112
Date	2006/04/13
Doc. No.	
Revision	01

Customer Approval	
Date	
The above signature represents that the product specifications, testing regulation, and warranty in the specifications are accepted	

		Engineering		
		Approval	Check	Design
		宋三 4/13	宋三 4/13	王頌 4/13

4/13

CONETNTS

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RECORD OF REVISIONS

Revision No.	Revision Date	Page	Summary
01	2006/4/13	all	New Creation

1. SUMMARY

This technical specification applies to 2.36" color TFT-LCD panel. The 2.36" color TFT-LCD panel is designed for camcorder, digital camera application and other electronic products which require high quality flat panel displays.

2. FEATURES

High Resolution :112,320 Dots (480 x 234) . Image Reversion: Up/Down and Left/Right.

3. GENERAL SPECIFICATIONS

Parameter		Specifications	Unit
Screen size		2.36(Diagonal)	inch
Display Format		480 x 234	Dot
Active area		48.0(H) x 35.685(V)	mm
Dot pitch		0.1(H) x 0.1525(V)	mm
Surface treatment		Anti-glare	
Pixel Configuration		RGB-Delta	
Outline dimension		55.2(W) x 47.55(H) x 2.9(D)	mm
Weight		16	g
View Angle direction		6 o'clock	
Temperature Range	Operation	-10~60	°C
	Storage	-20~70	°C

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power Voltage	V _{DD}	GND=0	-0.3	7.0	V	
	AV _{DD}		-0.3	7.0		
	V _{GH}	GND=0	-0.3	32.0	V	
	V _{GL}	GND=0	-22.0	0.3	V	
	V _{GH} -V _{GL}	GND=0	-0.3	+45.0	V	
Input Signal Voltage	V _{in}	GND=0	-0.3	V _{DD} +0.3	V	
Logic Output Voltage	V _{OUT1}	GND=0	-0.3	+0.7	V	

Note : Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

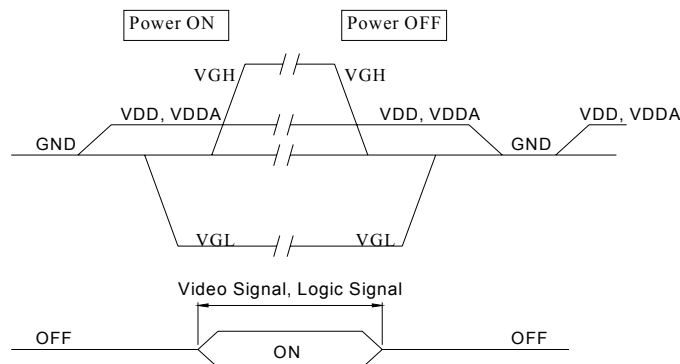
5. ELECTRICAL CHARACTERISTICS

5.1. Operating conditions :

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Power Voltage	V _{DD}	3.0	3.3	3.6	V	
	AV _{DD}	4.5	5	5.5	V	
	V _{GH}	10	15	20	V	
	V _{GL}	-15	-10	-5	V	
Low level input voltage	V _{IL}	0	-	0.3 V _{DD}	V	CLKIN, HSD, VSD, DIN[7:0], SPCK, SPDA, SPENA
High level input voltage	V _{IH}	0.7 V _{DD}	-	V _{DD}	V	CLKIN, HSD, VSD, DIN[7:0], SPCK, SPDA, SPENA
Output current	I _{OH}	20	40	-	uA	S1~S480, V _O =4.9V v.s 4.0V, V _{DDA} =5V
Output current	I _{OL}	20	40	-	uA	S1~S480, V _O =0.1V v.s 1.0V, V _{DDA} =5V
Analog operating current	I _{AVDD}	-	-	TBD	mA	f _{CLKIN} =27MHz, f _{OEH} =15.7KHz, V _{DDA} =5V

5.2 Power Sequence

Sequence for power on/off and Signal on/off



To prevent the device from damage due to latch-up, the power ON/OFF sequence shown below must be followed.

Power ON : V_{DD}, V_{DDA} → V_{GL} → Input Signals → V_{GH}

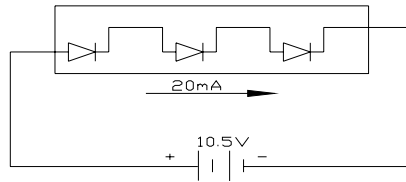
Power OFF : V_{GH} → Input Signals → V_{GL} → V_{DD}, V_{DDA}

5.3 LED driving conditions

T_a = 25°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	I _L	—	20	30	mA	Note
LED voltage	V _L	9.6	10.5	11.4	V	Note

Note:



6. AC Characteristics

6.1. Input signal characteristics

6.1.1. Digital RGB interface

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
CLK period	T_{OSC}	94	104	114	ns
Data setup time	T_{SU}	12	-	-	ns
Data hold time	T_{HD}	12	-	-	ns
HSD period	T_H	61.5	63.5	65.5	us
HSD pulse width	T_{HS}	4	4.7	5.4	us
HSD rising time	T_{Cr}	-	-	700	ns
HSD falling time	T_{Cf}	-	-	300	ns
VSD pulse width	T_{VS}	1	3	5	T_H
VSD rising time	T_{Vr}	-	-	700	ns
VSD falling time	T_{Vf}	-	-	1.5	us
HSD falling to VSD falling time for odd field	T_{HVO1}	0.3	-	-	us
VSD falling to HSD rising time for odd field	T_{HVO2}	1	-	-	us
HSD rising to VSD fallinr time for even field	T_{HVE}	1	-	-	us
VSD-DEN time	NTSC	T_{VSE}	-	15	T_H
	PAL		-	24	
HSD-DEN time	T_{HF}	75	-	120	T_{OSC}
DEN pulse width	T_{EP}	-	480	-	T_{OSC}
DEN-STH time	T_{DES}	-	3	-	T_{OSC}
VSD period	NTSC	T_{VSI}	-	262.5	T_H
	PAL		-	312.5	

PS. when SYNC mode is used, 1st data start from 106th clock after HSD falling.

6.1.2. CCIR601 Interface

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
CLK period	T_{OSC}	-	37	-	ns
Data setup time	T_{SU}	12	-	-	ns
Data hold time	T_{HD}	12	-	-	ns
HSD data blanking pulse width	NTSC	T_{HL}	-	276	T_{OSC}
	PAL		-	288	

6.1.3. CCIR656 Interface

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
CLK period	T_{OSC}	-	37	-	ns
Data setup time	T_{SU}	12	-	-	ns
Data hold time	T_{HD}	12	-	-	ns

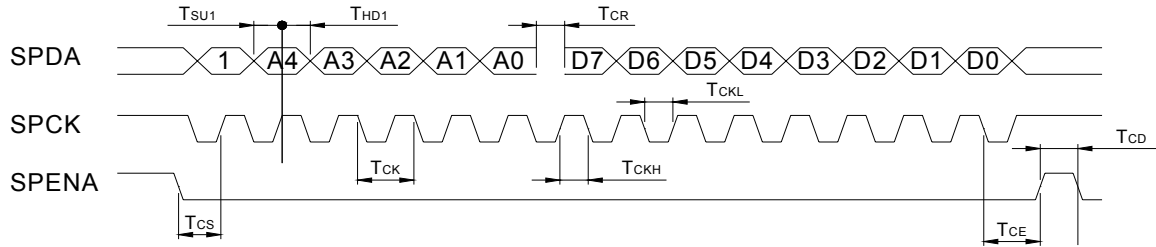
6.2. Output signal characteristics for Digital RGB mode

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.	
Rising time	T_r	-	-	10	ns	
Falling time	T_f	-	-	10	ns	
Clock pulse duty cycle	T_{CWH}	40	50	60	%	
Internal STH setup time	T_{SUS}	12	-	-	ns	
Internal STH hold time	T_{HDS}	12	-	-	ns	
Internal data setup time	T_{SUD}	12	-	-	ns	
Internal data hold time	T_{HDD}	12	-	-	ns	
OEH pulse width	T_{OEH}	-	18	-	T_{OSC}	
OEV pulse width	T_{OEV}	-	15	-	T_{OSC}	
CKV pulse width	T_{CKV}	-	84	-	T_{OSC}	
HSD-OEH time	T_1	-	33	-	T_{OSC}	
HSD-CKV time	T_2	-	18	-	T_{OSC}	
HSD-OEV time	T_3	-	6	-	T_{OSC}	
STV setup time	T_{SUV}	-	12	-	T_{OSC}	
STV pulse width	T_{STV}	-	1	-	T_H	
VSD-STVD time	NTSC PAL	T_{VS1}	-	16	-	T_H
		-	-	25	-	T_H
OEH-STV time	T_{OES}	-	2	-	T_H	
Output settling time	T_{ST}	-	12	20	us	

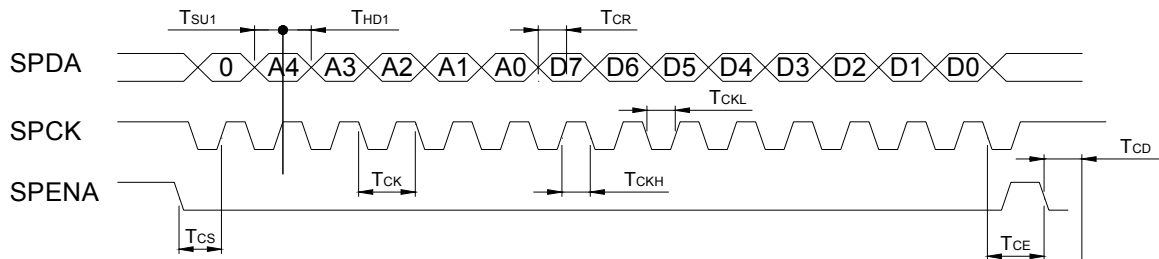
6.3. SPI timing characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
SPCK period	T_{CK}	60	-	-	ns
SPCK high width	T_{CKH}	30	-	-	ns
SPCK low width	T_{CKL}	30	-	-	ns
Data setup time	T_{SU1}	12	-	-	ns
Data hold time	T_{HD1}	12	-	-	ns
SPENA to SPCK setup time	T_{CS}	20	-	-	ns
SPENA to SPDA hold time	T_{CE}	20	-	-	ns
SPENA high pulse width	T_{CD}	50	-	-	ns
SPDA output latency	T_{CR}	-	1/2	-	T_{CK}

● SPI "read" timing



● SPI "write" timing



6.4. Hardware reset timing

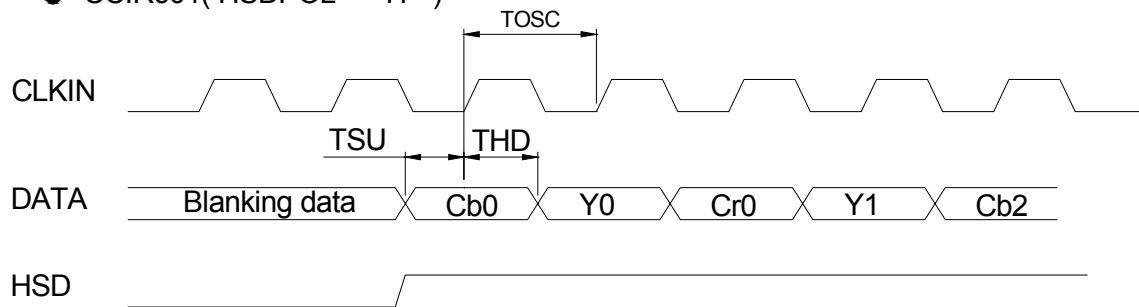
PARAMETER	Symbol	Min.	Typ.	Max.	Unit.
RESETB low pulse width	T_{RSB}	200	-	-	ns

7. Waveform

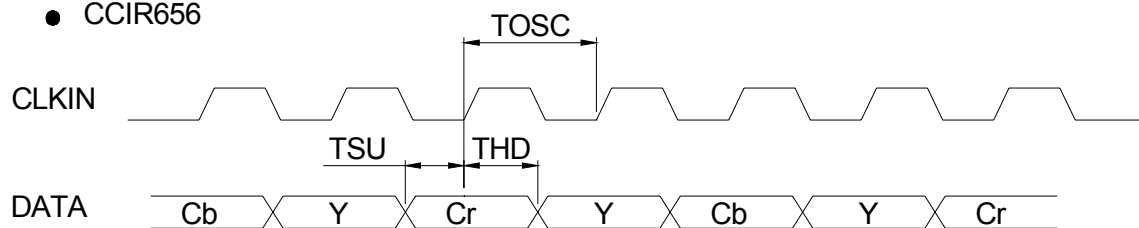
7.1. Timing Controller Timing Chart

7.1.1. Clock and Data waveform

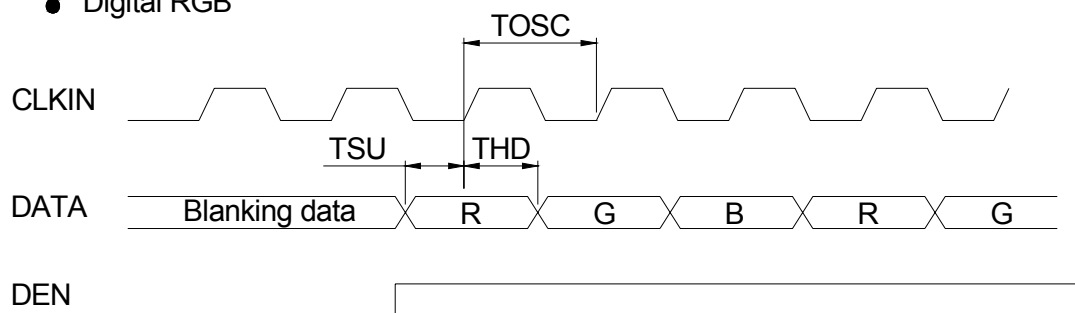
- CCIR601(HSDPOL = " H ")



- CCIR656



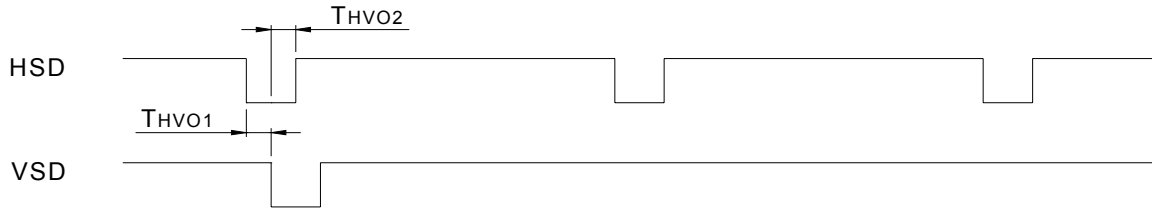
- Digital RGB



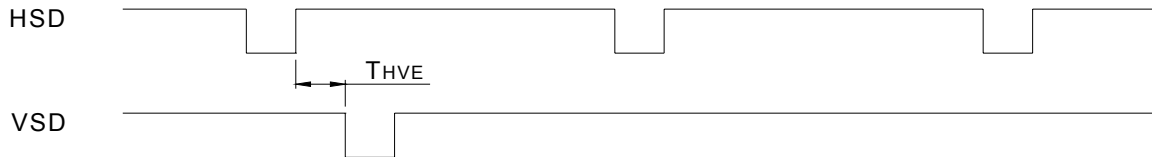
7.1.2. Digital RGB timing waveform

7.1.2.1. HSD and VSD timing for digital RGB mode

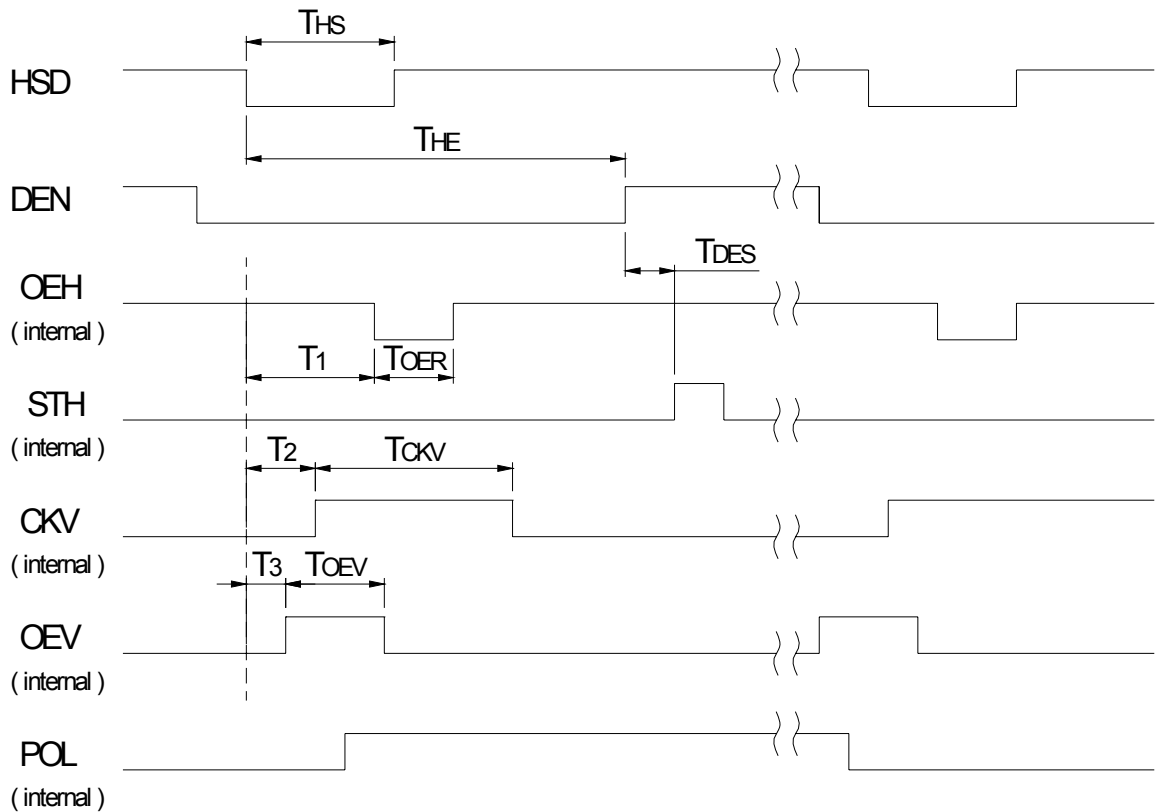
● Odd field



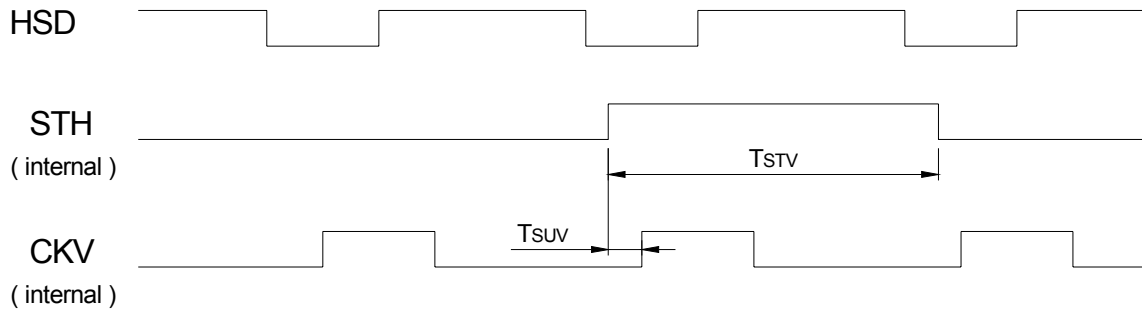
● Even field



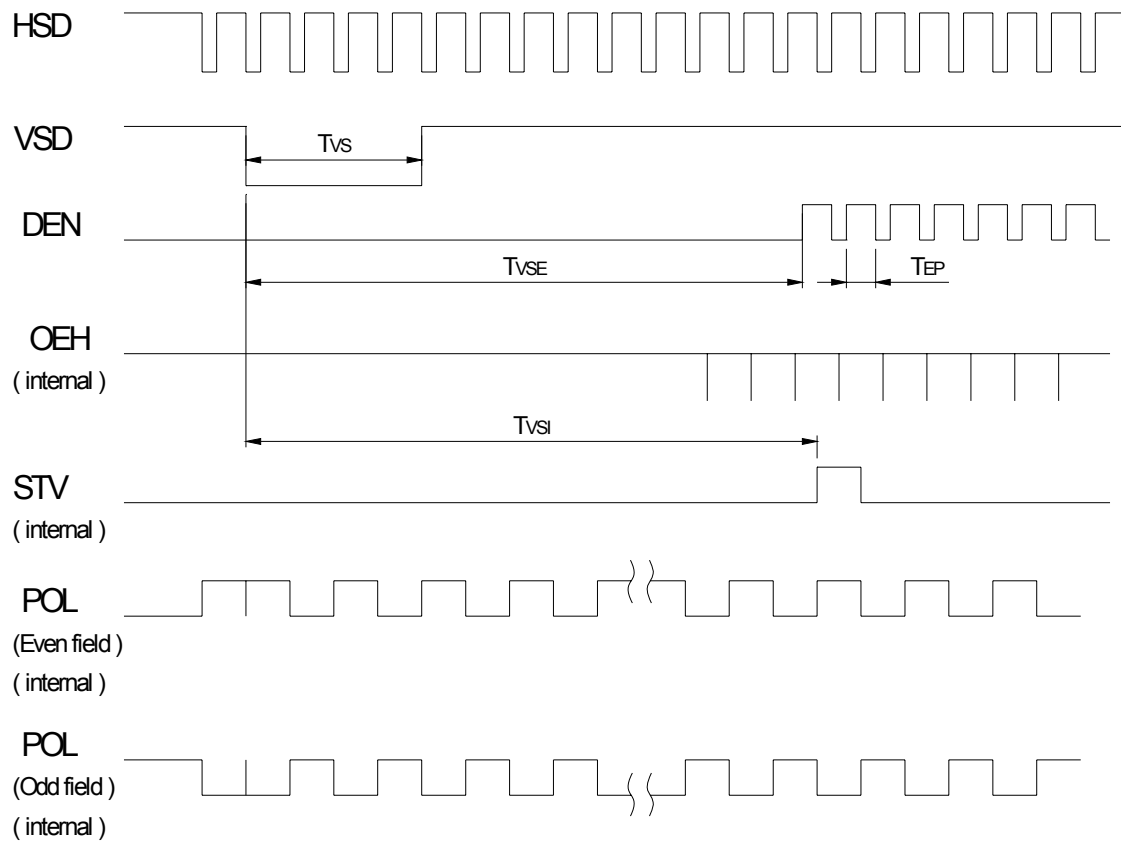
7.1.2.2. HSD and horizontal control timing waveform for digital RGB mode



7.1.2.3. HSD and vertical shift clock timing waveform

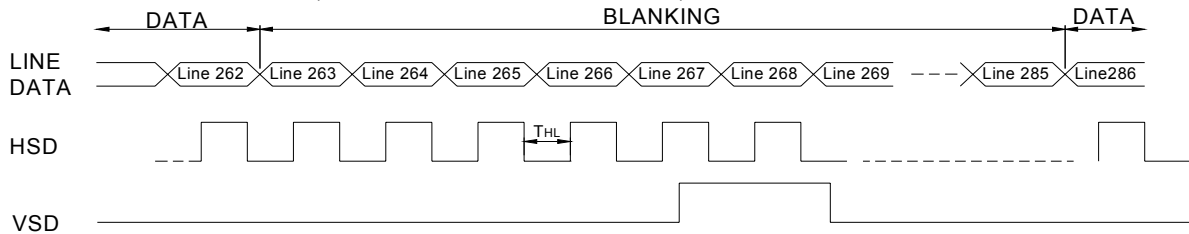


7.1.2.4. HSD and vertical control timing waveform

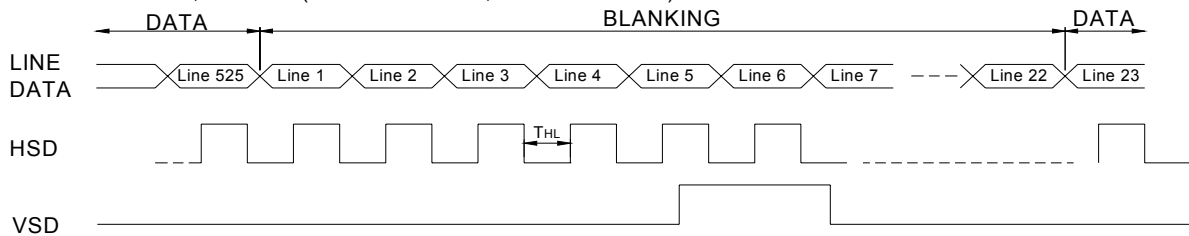


7.1.3. CCIR601 timing waveform

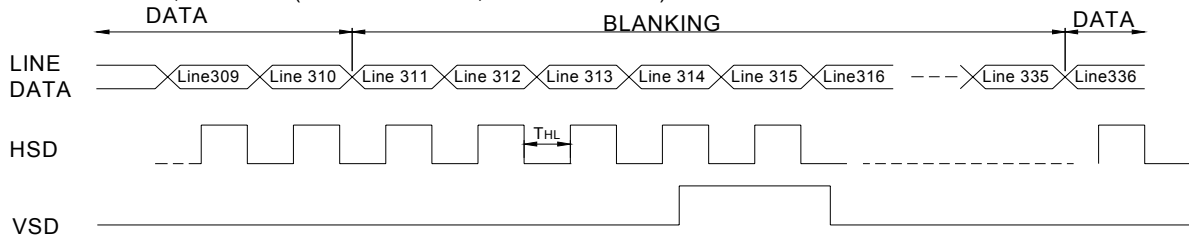
- NTSC mode, even field (HSDPOL = " H ", VSDPOL = " H ")



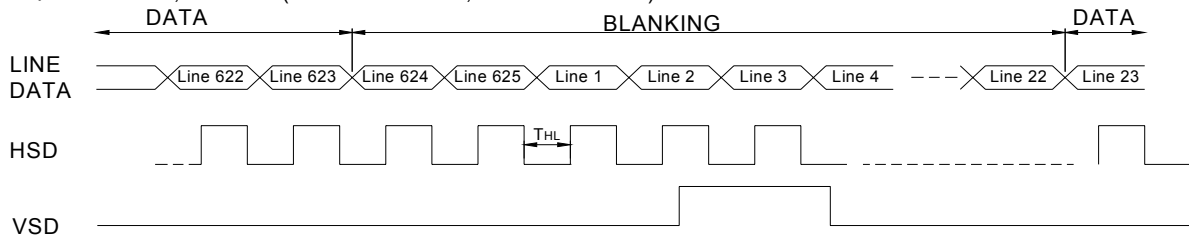
- NTSC mode, odd field (HSDPOL = " H ", VSDPOL = " H ")



- PAL mode, even field (HSDPOL = " H ", VSDPOL = " H ")

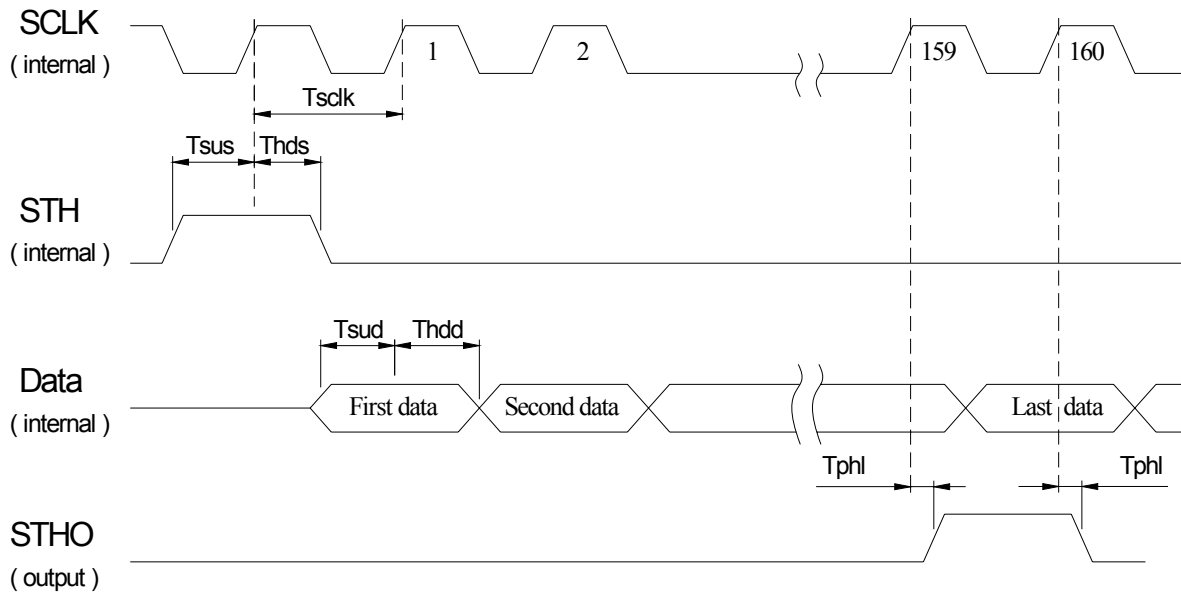


- PAL mode, odd field (HSDPOL = " H ", VSDPOL = " H ")

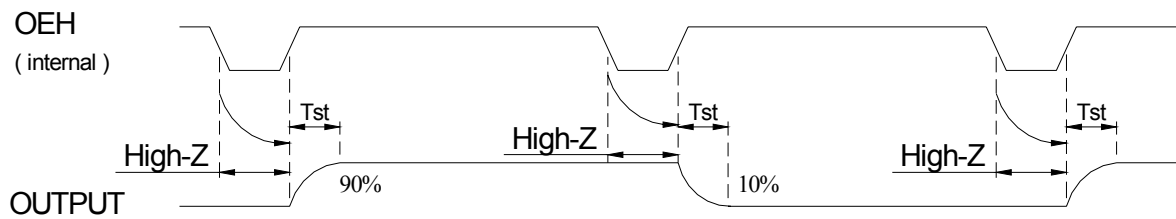


7.2. Source Driver Timing Chart

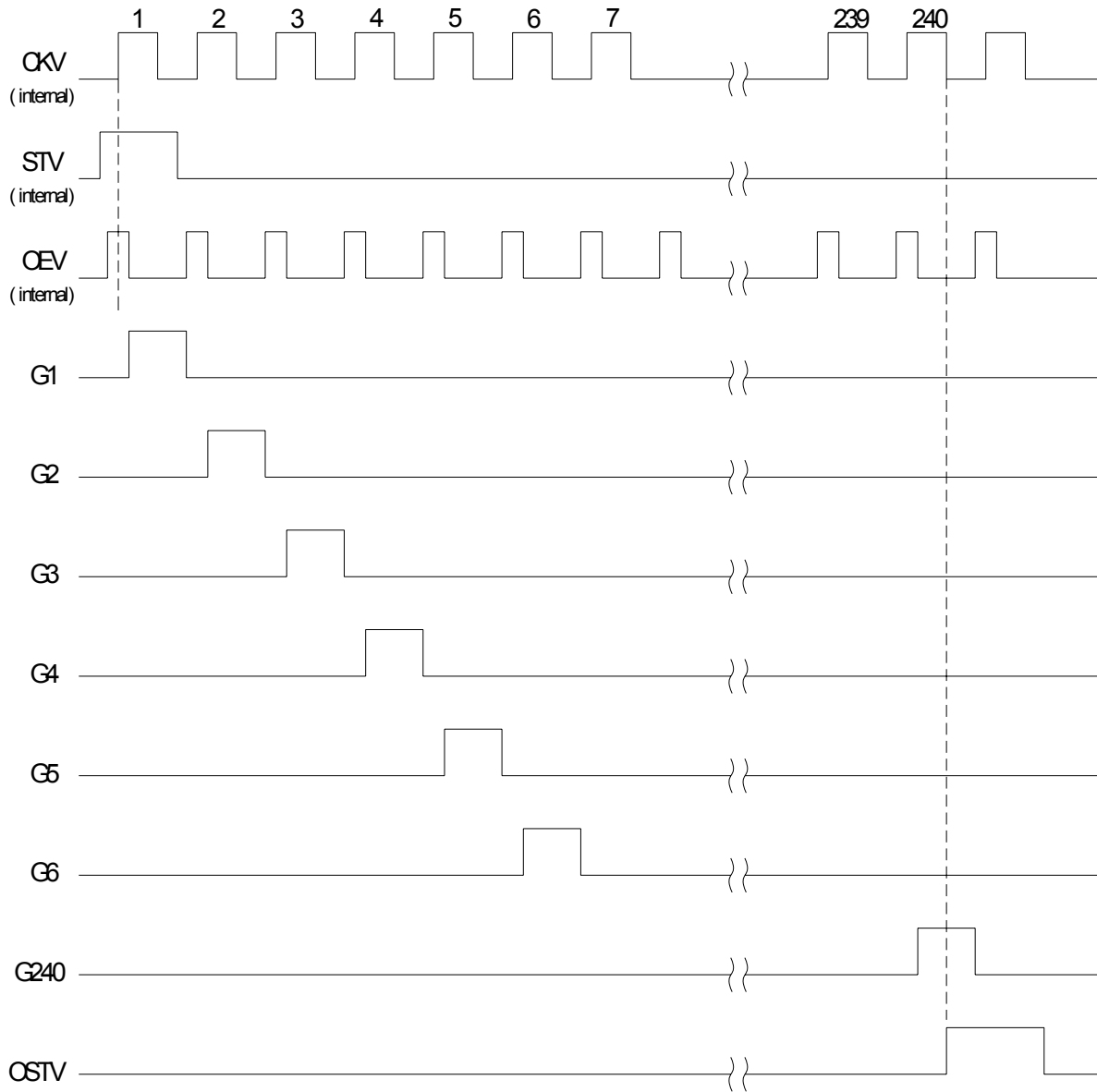
7.2.1. Clock and Start Pulse timing waveform



7.2.2. OEH and Data Output timing waveform



7.3. Gate Driver Timing Chart



8. Optical Characteristics

 $T_a=25\pm 2^{\circ}\text{C}$, ILED=20mA

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	
Response time	Tr	$\theta=0^{\circ}$	-	15	30	ms	Note 3,5	
	Tf		-	35	50	ms		
Contrast ratio	CR	At optimized viewing angle	150	200			Note 4,5	
Color Chromaticity	White	$\theta=0^{\circ}$	Wx	(0.25)	(0.30)	(0.35)		Note 2,6,7
			Wy	(0.27)	(0.32)	(0.37)		
Viewing angle	Hor.	CR ≥ 10	θ_R	-	40	-	Deg.	Note 1
			θ_L	-	40	-		
	Ver.		θ_T	-	10	-		
			θ_B	-	30	-		
Uniformity	U	-	(75)	(80)	-	%		
Brightness	-	-	(200)	(250)	-	cd/m ²	CENTER	

Note 1: Definition of viewing angle range

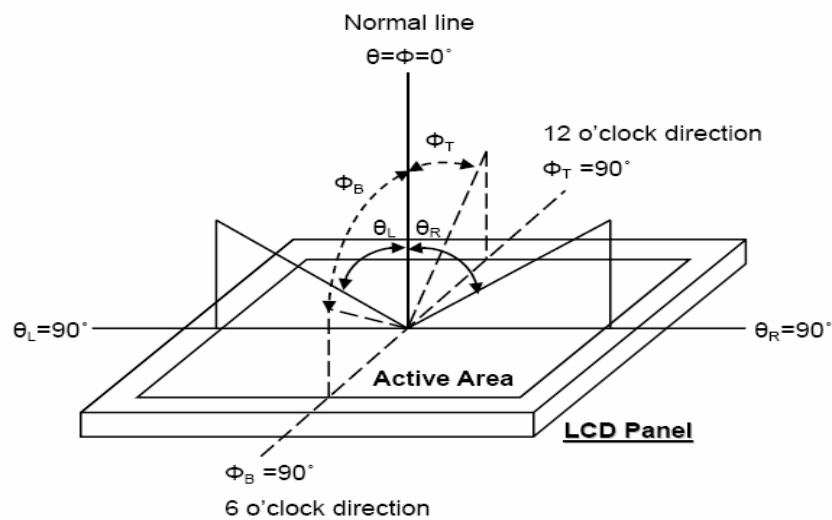


Fig. 8-1 Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

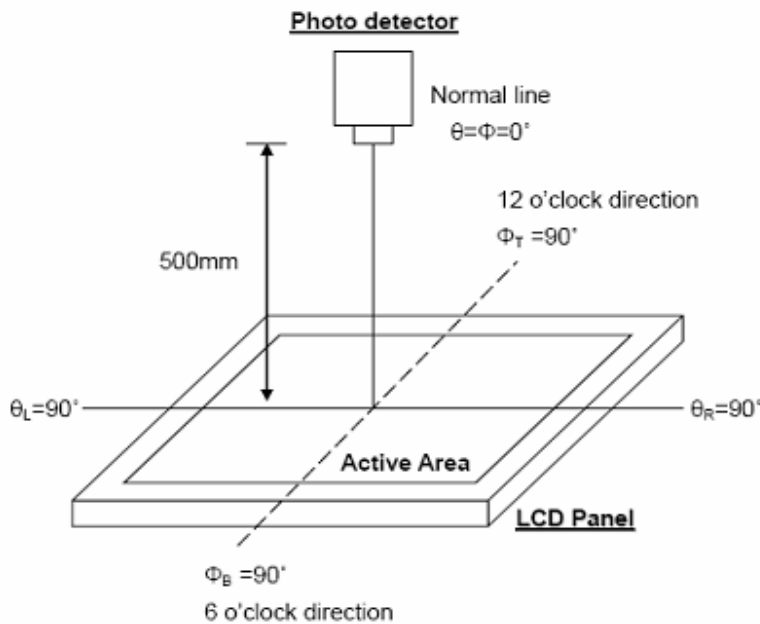


Fig. 8-2 Optical measurement system setup

Note 3: Definition of Response time:

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time, T_r , is the time between photo detector output intensity changed from 90% to 10%. And fall time, T_f , is the time between photo detector output intensity changed from 10% to 90%.

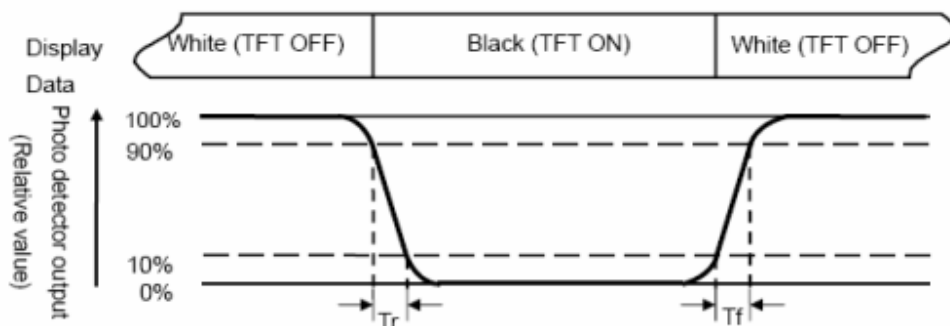


Fig. 3-3 Definition of response time

Note 4: Definition of contrast ratio:

The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: White $V_i = V_{i50} \pm 1.5V$

Black $V_i = V_{i50} \pm 2.0V$

“±” means that the analog input signal swings in phase with VCOM signal.

“±” means that the analog input signal swings out of phase with VCOM signal.

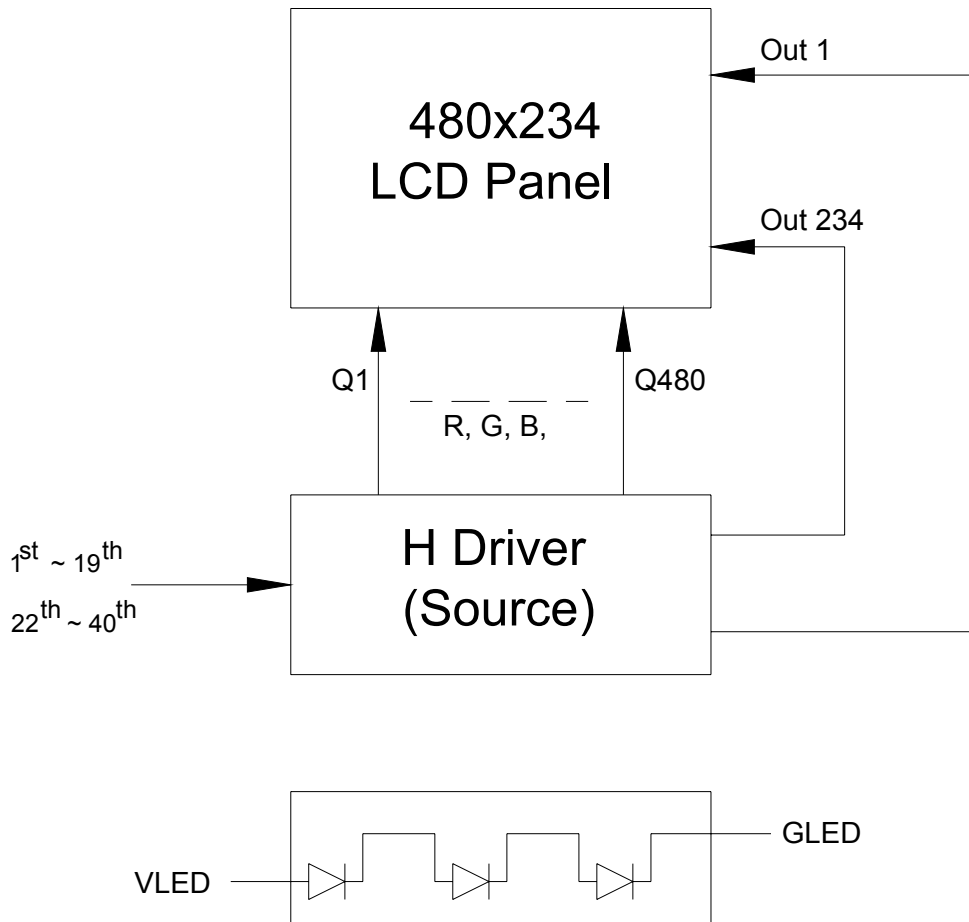
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 6: Definition of color chromaticity (CIE 1931)

Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

9. BLOCK DIAGRAM



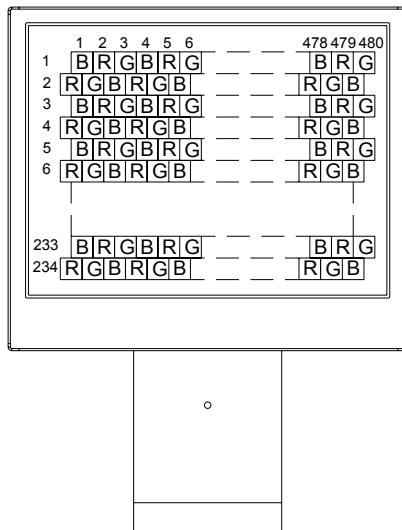
10. Input / Output Terminals

10.1. PIN Connections

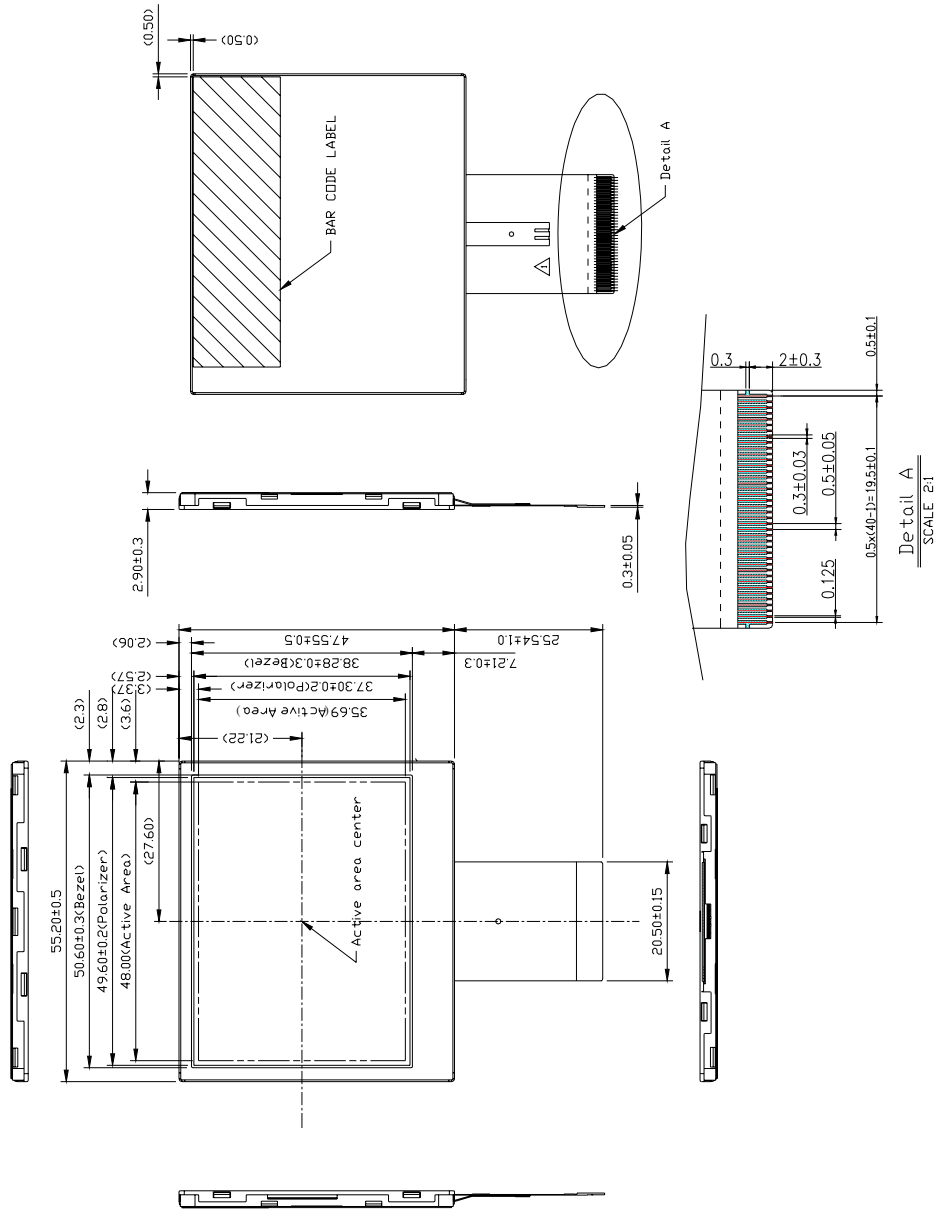
Pin No	Symbol	I/O	Description	Remark
1	NC	-	NC	
2	NC	-	NC	
3	V _{com}	I	Common Electrode Voltage.	
4	V _{COMOUT}	O	V _{COM} output voltage.	
5	VFB	I	PWM feedback reference voltage. Default is 1.2V	
6	DRV	O	PWM drive output signal	
7	V _{COM_L}	IO	V _{COM} reference low level voltage. Connect 1 μ F capacitor to AV _{SS} .	
8	V _{COM_H}	IO	V _{COM} reference high level voltage. Connect 1 μ F capacitor to AV _{SS} .	
9	V _{COM}	I	V _{com} input signal if V _{COMOUT} function is disable	
10	V _{GH}	VI	Gate output High Voltage.	
11	V _{GL}	VI	Gate output Low Voltage.	
12	V _{EE}	VI	Negative power voltage. If Cs-on-common is implemented, short to V _{GL} .	
13	AV _{DD}	VI	Analog power supply. This power connects to Source Driver, Bandgap Reference, and Gamma resistor.	
14	AV _{SS}	VI	Analog GND. This power connects to Source Driver, Bandgap Reference, and Gamma.	
15	V _{SS}	VI	Digital GND.	
16	POLB	O	Polarizer output signal	
17	RESETB	I	Active low global reset signal input. Normally pull high.	
18	SPENA	I	Serial port Data Enable Signal.	
19	SPCK	I	Serial port Clock.	
20	GLED		Ground of LED.	
21	VLED		Voltage of LED.	
22	SPDA	I/O	Serial port Data input/output.	
23	HSD	I	Horizontal sync input with negative polarity.	
24	VSD	I	Vertical sync input with negative polarity.	
25	DEN	I	Input data enable control. Normally pull low.	
26	DIN7	I	Digital image data input.	
27	DIN6	I	Digital image data input.	
28	DIN5	I	Digital image data input.	
29	DIN4	I	Digital image data input.	
30	DIN3	I	Digital image data input.	

31	DIN2	I	Digital image data input.	
32	DIN1	I	Digital image data input.	
33	DIN0	I	Digital image data input.	
34	CLKIN	I	Input data sampling clock at rising edge.	
35	VDD	VI	Digital power voltage	
36	VCOMOUT	O	VCOM output voltage.	
37	VGL	VI	Gate output Low Voltage.	
38	Vcom	I	Common Electrode Voltage.	
39	NC	-	NC	
40	NC	-	NC	

10.2. Pixel Arrangement and Input Connector Pin Number



11. Outline Drawing



Note 1 : There is a protective film on the upper polarizer, customer must peel it off before assembly to machine.

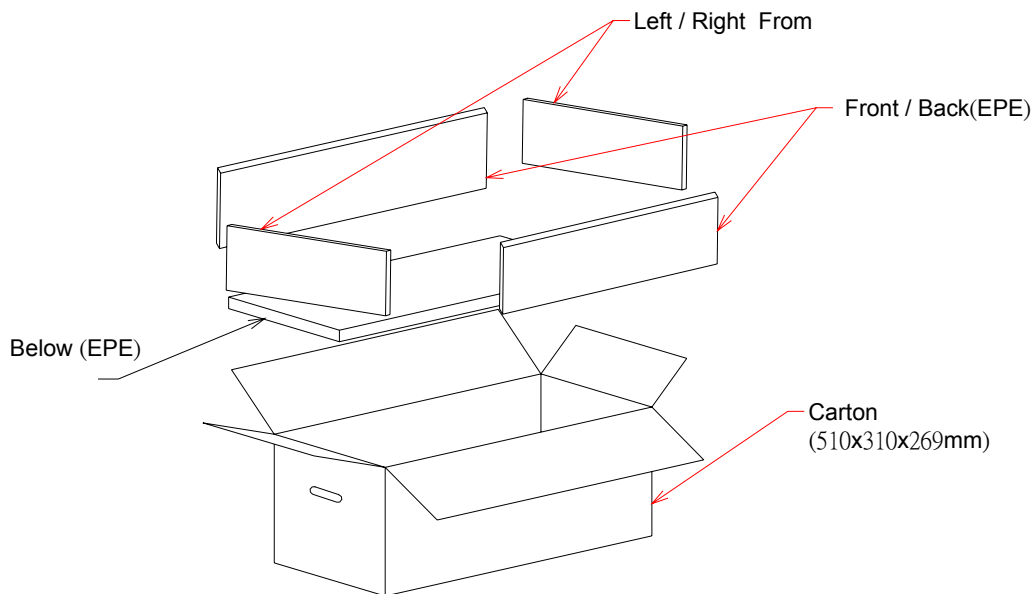
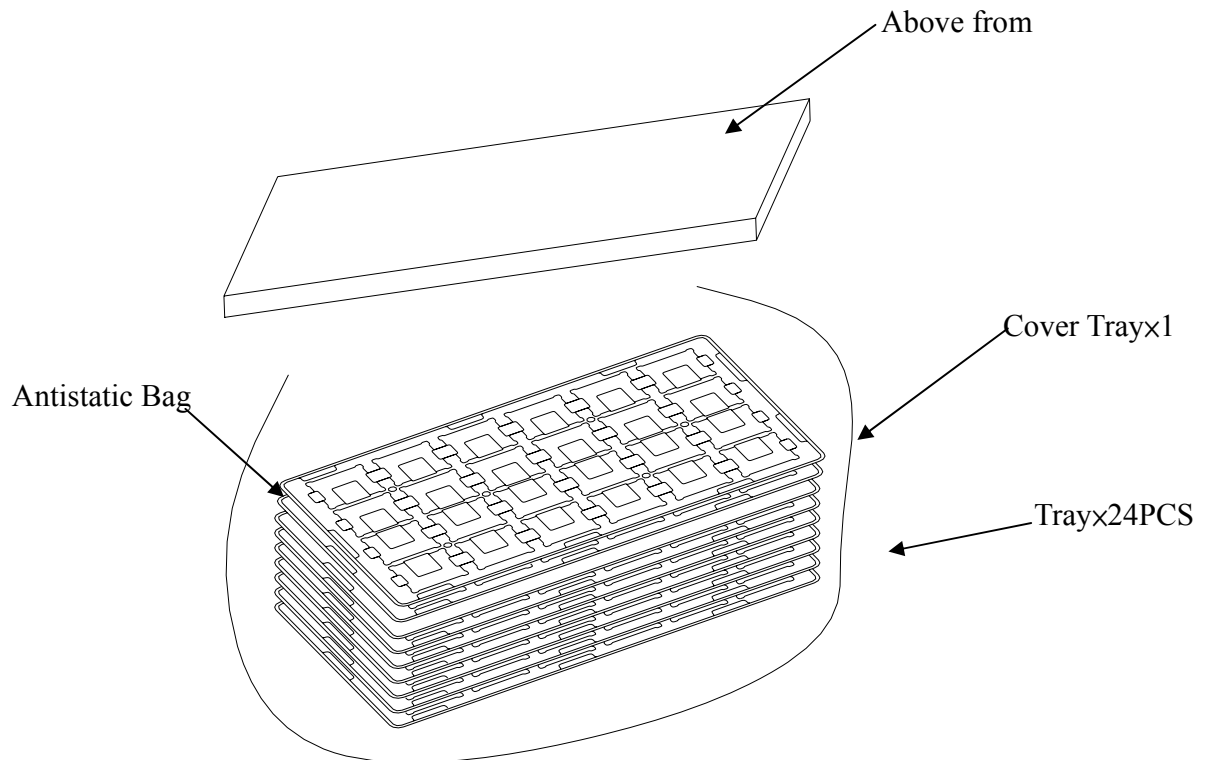
Note 2 : Unmark tolerance : $\pm 0.5\text{mm}$

12. QUALITY ASSURANCE

No.	Test Items	Test Condition	REMARK
1	High Temperature Storage Test	Ta=70°C 240h	
2	Low Temperature Storage Test	Ta=-20°C 240h	
3	High Temperature Operation Test	Ta=60°C 240h	
4	Low Temperature Operation Test	Ta=-10°C 240h	
5	High Temperature and High Humidity Operation Test	Ta=60°C 90%RH 240h	
6	Electro Static Discharge Test	-Panel Surface/Top_Case: 150pF ±15kV 150Ω (direct discharge, five times) -FPC input terminal : 100pF ±200V 0Ω	
7	Shock Test (non-operating)	Half sine wave, 180G, 2ms one shock of each six faces (I.e. run 180G 2ms for all six faces)	
8	Vibration Test (non-operating)	Sine wave, 10 ~ 500 ~ 10Hz, 1.5G, 0.37oct/min 3 axis, 1hour/axis	
9	Thermal Shock Test	-20°C(0.5h) ~ 70°C(0.5h) / 100 cycles	

***** Ta= Ambient Temperature

13. PACKAGE



1 tray = 24pcs
1 Carton = 24(pcs/Layer) x 23(Layer) = 552 pcs
Remove display protective film before use it.