Doc. Number:

■ Tentative Specification
☐ Preliminary Specification
☐ Approval Specification

MODEL NO.: N173HHF
SUFFIX: E21

Customer:

APPROVED BY **SIGNATURE**

Name / Title
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
黃崑峰 2010-11-02 12:57:53 CST	張伯豪 2010-10-26 19:32:21 CST	莊家銘 2010-09-24 09:52:07 CST

CONTENTS

REVISION HISTORY

Version	Date	Page	Description
0.0	Sep.10, 2010	All	Spec Ver.0.0 was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N173HHF-E21 is a 17.3" TFT Liquid Crystal Display module with LED Backlight unit and 40 pins display port interface. This module supports 1920 x 1080 FHD mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction.

1.2 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Screen Size	17.3" diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch	0.1989 (H) x 0.1989 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), Anti-Glare	-	-
Luminance, White	400	Cd/m2	
Power Consumption	Total (TBD)W (Max.) @ cell (TBD)W (Max.), BL (TBD)W (Max.)		(1)

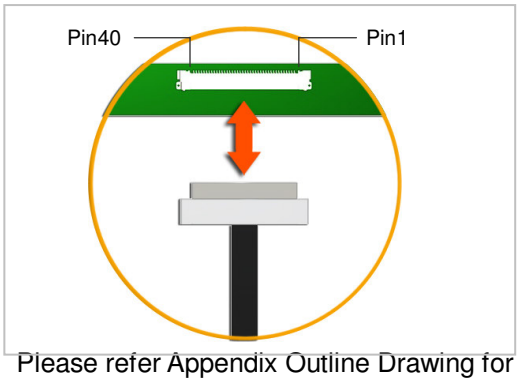
Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 60 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 ºC, whereas mosaic pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	397.6	398.1	398.6	mm	(1)
	Vertical (V)	232.3	232.8	233.3	mm	
	Thickness (T)	-	(TBD)	6.5	mm	
Bezel Area	Horizontal	385.88	386.18	386.48	mm	
	Vertical	218.55	218.85	219.15	mm	
Active Area	Horizontal	-	381.888	-	mm	
	Vertical	-	214.812	-	mm	
Weight		-	(TBD)	650	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE



Please refer Appendix Outline Drawing for detail design.

Connector Part No.: Starconn 111A40-0000RA-G3, Tyco# 5-2069716-3, or equivalent

User's connector Part No: Starconn 111B40-0000RA-G3, Tyco#5-2069715-3, or equivalent

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

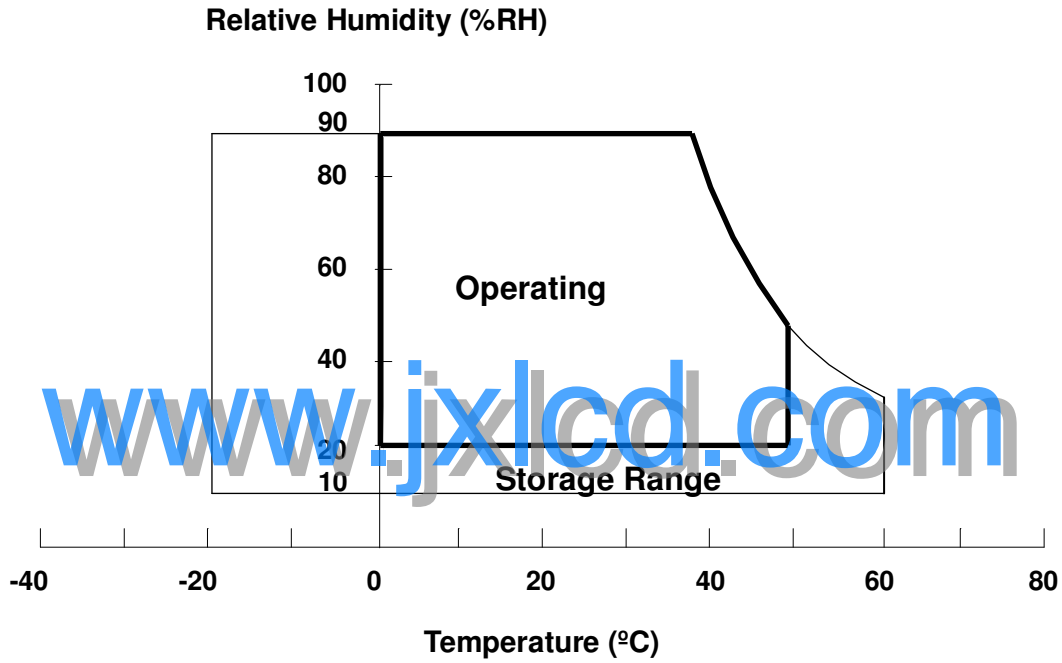
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)

Note (1) (a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 60 ºC max.



3.2 ELECTRICAL ABSOLUTE RATINGS

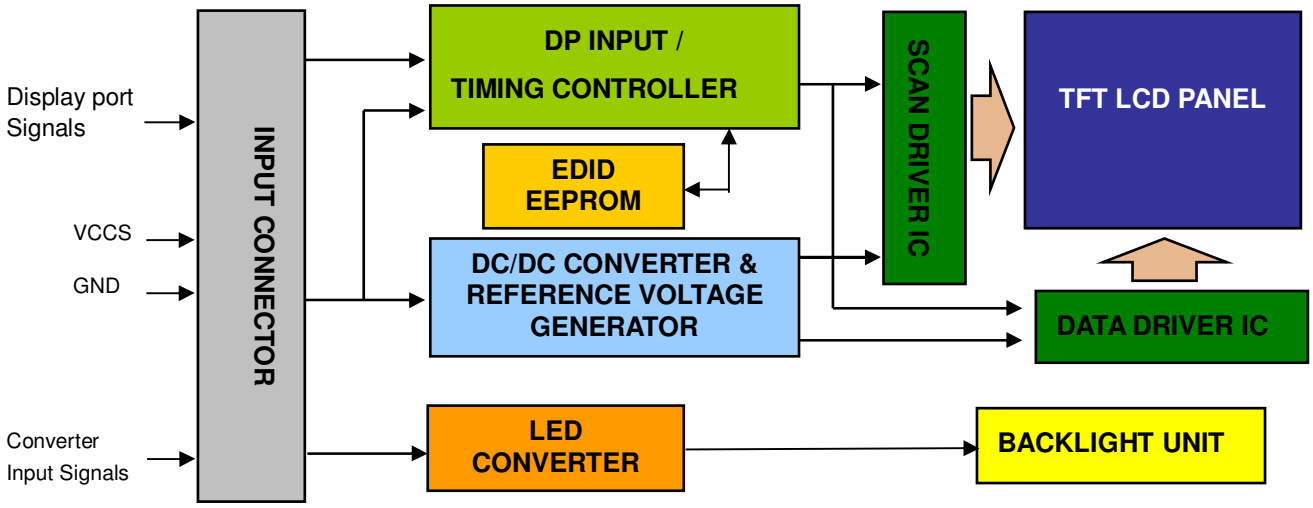
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+6.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	VCCS+0.3	V	
Converter Input Voltage	LED_VCCS	-0.3	25	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	6	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	6	V	(1)

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM

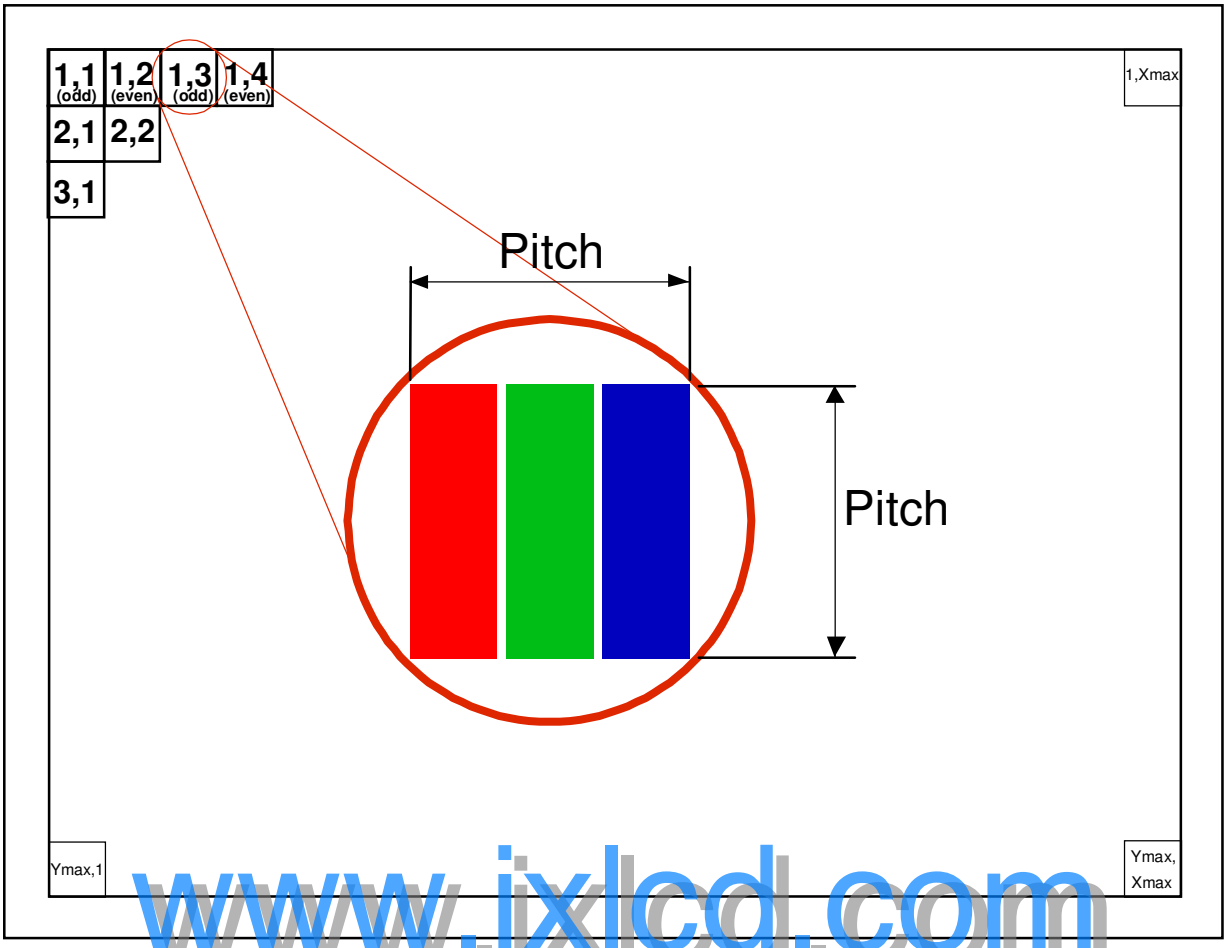


4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved)	
2	H_GND	High Speed Ground	
3	ML3-	Complement Signal-Lane 3	
4	ML3+	True Signal-Main Lane 3	
5	H_GND	High Speed Ground	
6	ML2-	Complement Signal-Lane 2	
7	ML2+	True Signal-Main Lane 2	
8	H_GND	High Speed Ground	
9	ML1-	Complement Signal-Lane 1	
10	ML1+	True Signal-Main Lane 1	
11	H_GND	High Speed Ground	
12	ML0-	Complement Signal-Lane 0	
13	ML0+	True Signal-Main Lane 0	
14	H_GND	High Speed Ground	
15	AUX+	True Signal-Auxiliary Channel	
16	AUX-	Complement Signal-Auxiliary Channel	
17	H_GND	High Speed Ground	
18	VCCS	Power Supply +5 V (typical)	
19	VCCS	Power Supply +5 V (typical)	
20	VCCS	Power Supply +5 V (typical)	
21	VCCS	Power Supply +5 V (typical)	
22	BIST	Built-In Self Test (active high)	
23	GND	Ground	
24	GND	Ground	
25	GND	Ground	
26	GND	Ground	
27	HPD	Hot Plug Detect	
28	BL_GND	BL Ground	
29	BL_GND	BL Ground	
30	BL_GND	BL Ground	
31	BL_GND	BL Ground	
32	LED_EN	BL_Enable Signal of LED Converter	
33	LED_PWM	PWM Dimming Control Signal of LED Converter	
34	NC	No Connection (CMO Reserved)	
35	NC	No Connection (CMO Reserved)	
36	LED_VCCS	BL Power	
37	LED_VCCS	BL Power	
38	LED_VCCS	BL Power	
39	LED_VCCS	BL Power	
40	NC	No Connection (Reserved)	

Note (1) The first pixel is odd as shown in the following figure.



4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

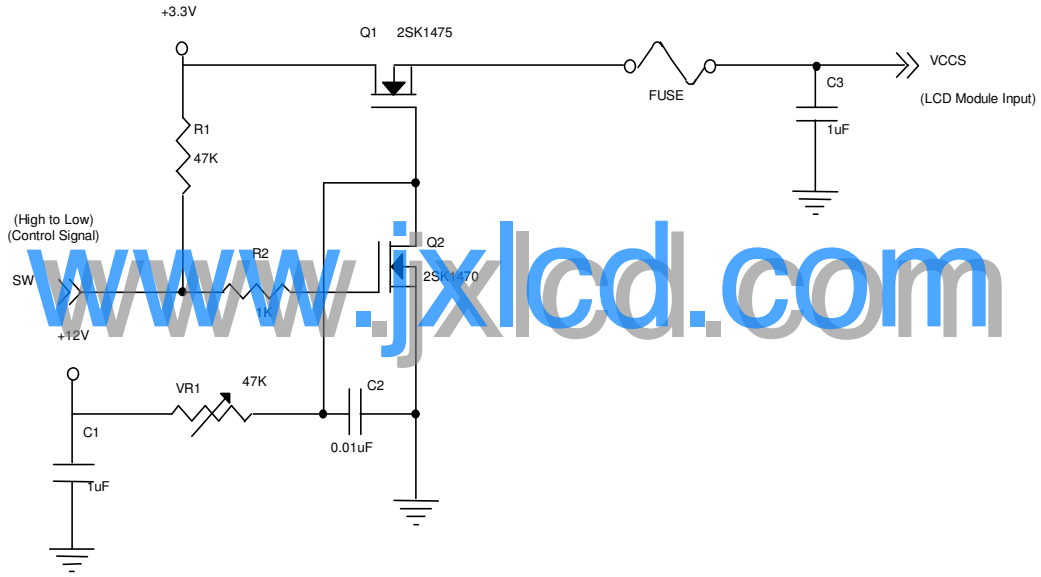
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	4.5	5.0	5.5	V	(1)-
Ripple Voltage		V_{RP}	-	50	-	mV	(1)-
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	Icc	-	TBD	TBD	mA	(3)a
	Black		-	TBD	TBD	mA	(3)b

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

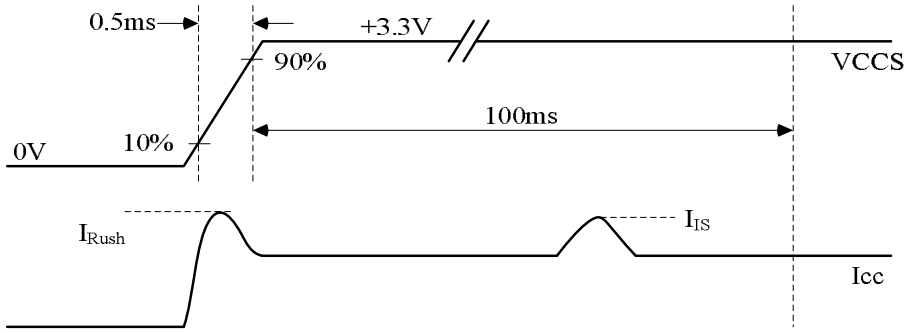
Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black..

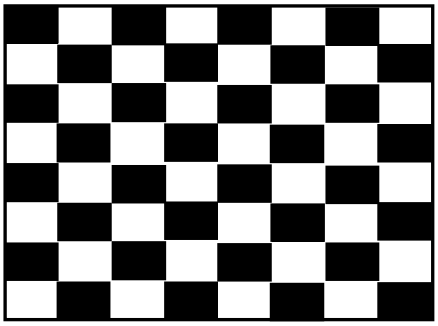


VCCS rising time is 0.5ms



Note (3) The specified power supply current is under the conditions at VCCS = 5 V, Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

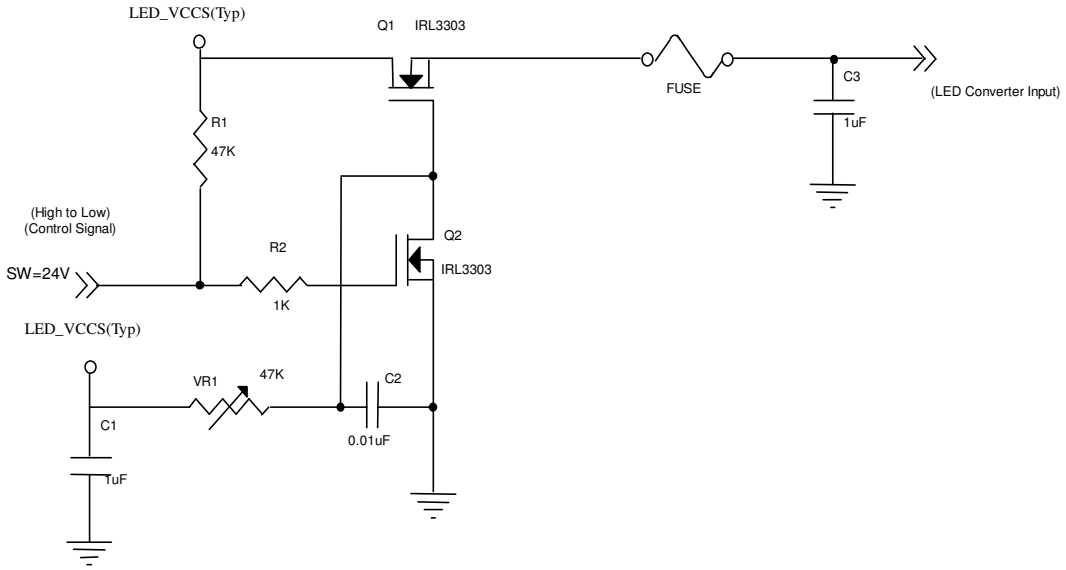
b. Black Pattern

Active Area

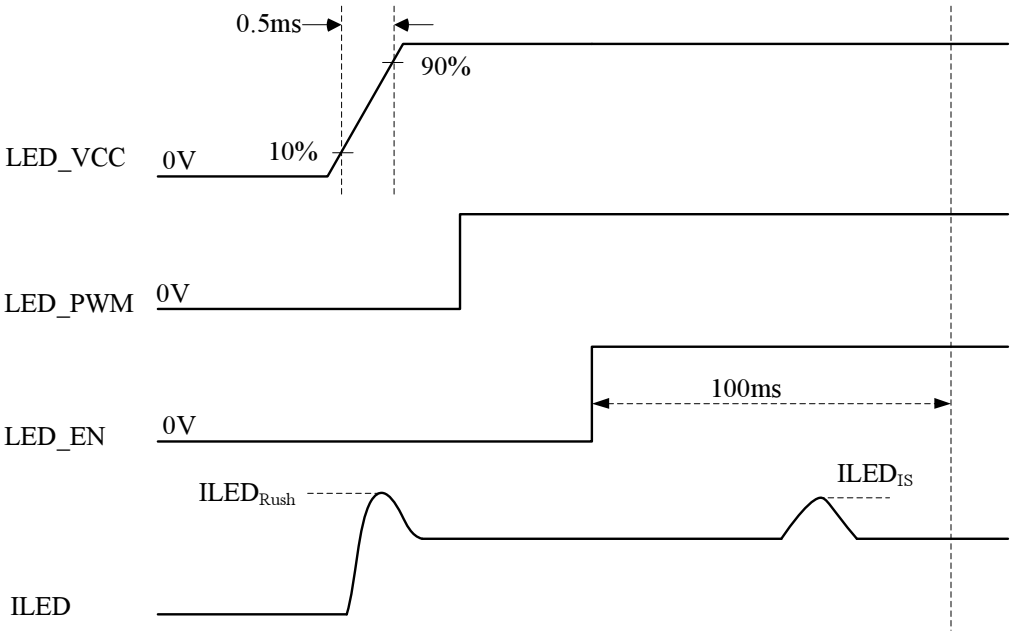
4.3.2 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	(7.5)	(12.0)	(21.0)	V	
Converter Inrush Current		$ILED_{RUSH}$	-	-	(1.5)	A	(1)
EN Control Level	Backlight On		(2.3)	-	(5.0)	V	
	Backlight Off		0	-	(0.5)	V	
PWM Control Level	PWM High Level		(2.3)	-	(5.0)	V	
	PWM Low Level		0	-	(0.5)	V	
PWM Control Duty Ratio			(10)	-	100	%	
			(5)	-	100	%	(2)
PWM Control Permissive Ripple Voltage		V_{PWM_pp}	-	-	100	mV	
PWM Control Frequency		f_{PWM}	(190)	-	(2K)	Hz	(3)
LED Power Current	LED_VCCS =Typ.	ILED	TBD	TBD	TBD	mA	(4)

Note (1) $ILED_{RUSH}$: the maximum current when LED_VCCS is rising,
$ILED_S$: the maximum current of the first 100ms after power-on.
Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.



VLED rising time is 0.5ms



Note (2) If the PWM control duty ratio is less than 10%, there is some possibility that acoustic noise or backlight flash can be found. And it is also difficult to control the brightness linearity.

Note (3) If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

$$(N+0.33)*f \leq f_{PWM} \leq (N+0.66)*f$$

N : Integer $(N \geq 3)$

f : Frame rate

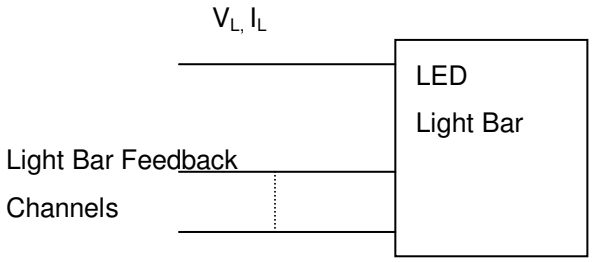
Note (4) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	30.8	35.2	37.4	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	174.8	184	193.2	mA	
Power Consumption	P_L	5.38	6.47	7.22	W	(3)
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

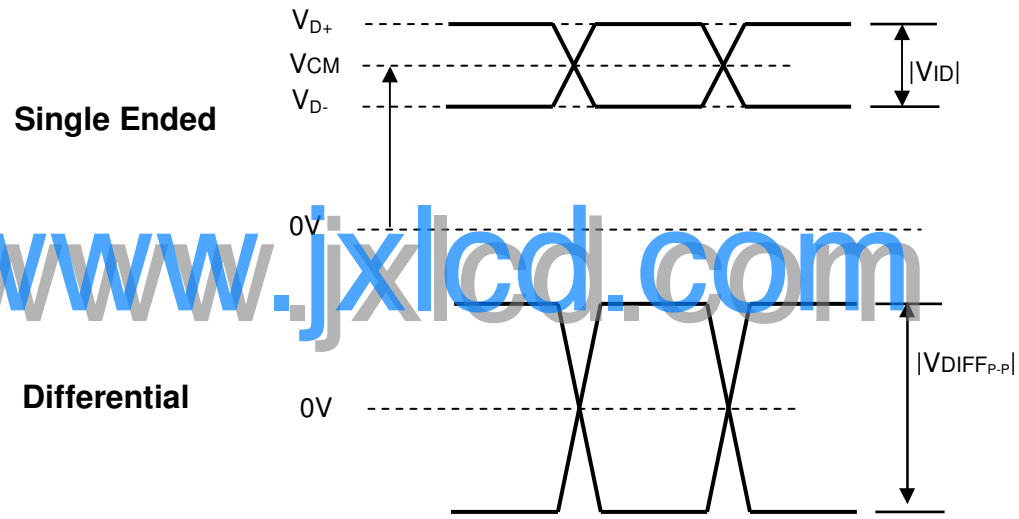
Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 °C and I_L = 23 mA(Per EA) until the brightness becomes ≦ 50% of its original value.

4.4 DISPLAY PORT INPUT SIGNAL TIMING SPECIFICATIONS

4.4.1 ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
MainLink Input Signal Peak-to-peak Voltage	$\|VDIFF_{P-P}\|_{(MainLink)}$	(120)	-	-	mV	High bit rate
		(40)	-	-	mV	Reduced bit rate
AUX Differential Input Voltage	$\|V_{ID}\|_{(AUX)}$	(160)	-	(680)	mV	
Differential Signal Common Mode Voltage	VCM	(0)		(2)	V	
AUX AC Coupling Capacitor	C_{AUX}	(75)		(200)	nF	
Lane Intra-pair Skew	$V_{RX-SKEW-INTRA\_PAIR}$	-	-	(100)	ps	High bit rate
		-	-	(300)		Reduced bit rate

Note (1) Display port interface related AC coupled signals are following VESA Display Port Standard V1.1a



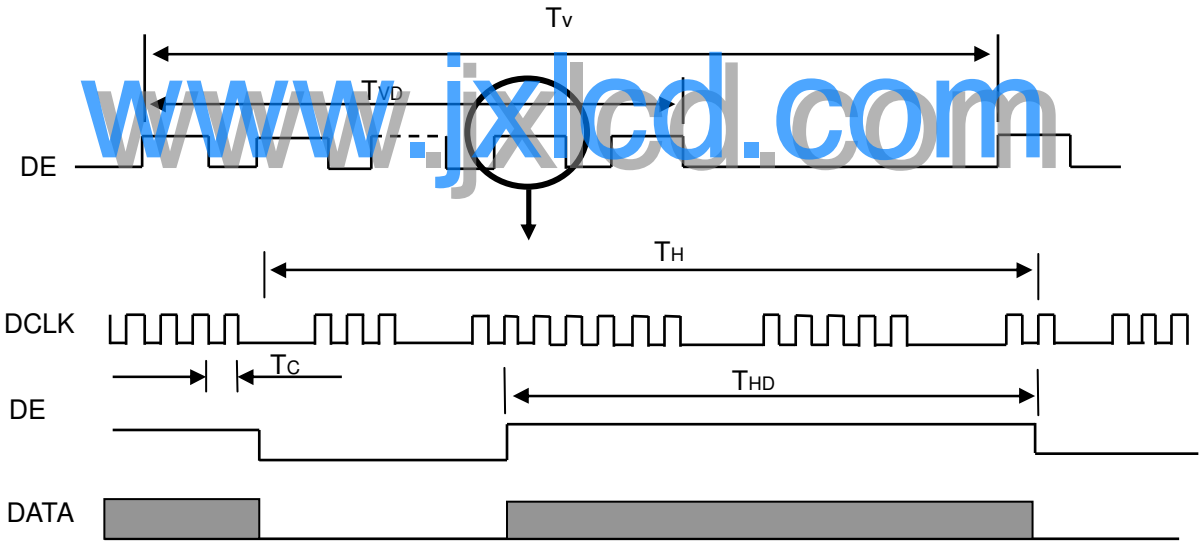
4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

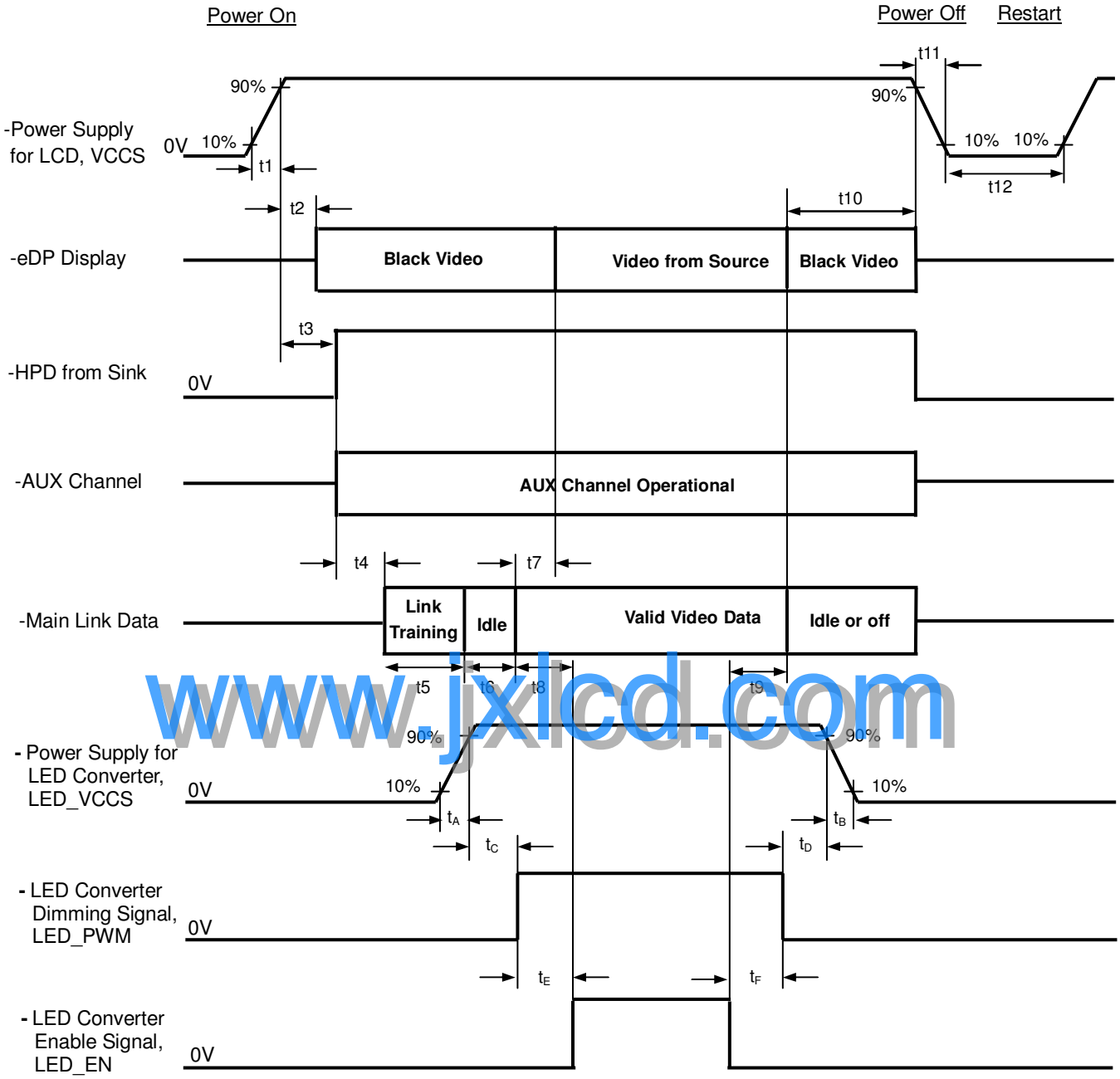
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	TBD	138.5	TBD	MHz	-
DE	Vertical Total Time	TV	TBD	1110	TBD	TH	-
	Vertical Active Display Period	TVD	1080	1080	1080	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	30	TV-TVD	TH	-
	Horizontal Total Time	TH	TBD	2080	TBD	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	-

Note (1) Display timing signal should be contained and transferred by Display Port Main Link stream data packing described in VESA Display Port Standard V1.1a

DISPLAY SIGNAL TIMING DIAGRAM



4.6 POWER ON/OFF SEQUENCE



Timing Specifications: Follow VESA Embedded Display Port Standard Version 1

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	-
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	-
t4	Delay from HPD high to link training initialization	Source	-	-	ms	-
t5	Link training duration	Source	-	-	ms	-
t6	Link idle	Source	-	-	ms	-
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	-
t8	Delay from valid video data from Source to backlight on	Source	-	-	ms	-
t9	Delay from backlight off to end of valid video data	Source	-	-	ms	-
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	-
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-
t12	VCCS Power off time	Source	500	-	ms	-
t_A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t_B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
t_C	Delay from LED power rising to LED dimming signal	Source	10	-	ms	-
t_D	Delay from LED dimming signal to LED power falling	Source	10	-	ms	-
t_E	Delay from LED dimming signal to LED enable signal	Source	10	-	ms	-
t_F	Delay from LED enable signal to LED dimming signal	Source	10	-	ms	-

Note (1) Please follow the power on/off sequence described above. Otherwise, the LCD module might abnormal display or be damaged.

Note (2) Please avoid floating state of interface signal at invalid period. When the interface signal is invalid, be sure to pull down the power supply of LCD VCCS to 0 V.

Note (3) The backlight must be turned on after the power supply for the logic and the interface signal is valid. The backlight must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Please follow the LED backlight power sequence as above. If the customer could not follow, it might cause backlight flash issue during display ON/OFF or damage the LED backlight controller

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

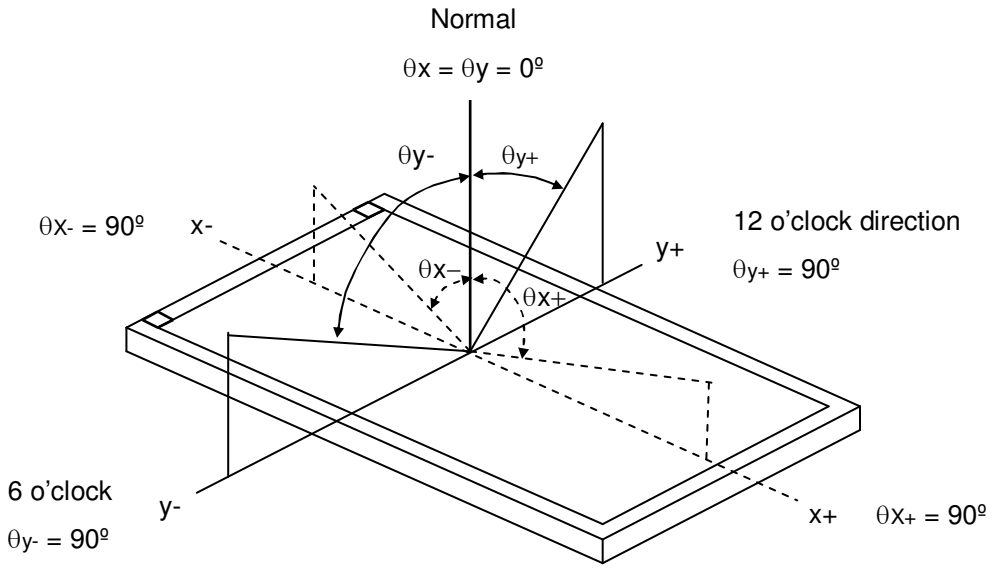
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	184	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	500	650	-	-	(2), (5) ,(7)
Response Time		T_R		-	(1)	(3)	ms	(3) ,(7)
		T_F		-	(5)	(7)	ms	
Average Luminance of White		L_{AVE}		340	400	-	cd/m^2	(4), (6) ,(7)
Color Chromaticity	Red	Rx		Typ – 0.03	(0.640)	Typ + 0.03	-	(1) ,(7)
		Ry			(0.333)		-	
	Green	Gx			(0.303)		-	
		Gy			(0.613)		-	
	Blue	Bx			(0.154)		-	
		By			(0.060)		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	60	70		Deg.	(1),(5) , (7)
		θ_x-		60	70	-		
	Vertical	θ_Y+		50	60	-		
		θ_Y-		50	60	-		
White Variation of 5 Points		δW_{5p}	θ_x=0°, θ_Y =0°	80	-	-	%	(5),(6) , (7)

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

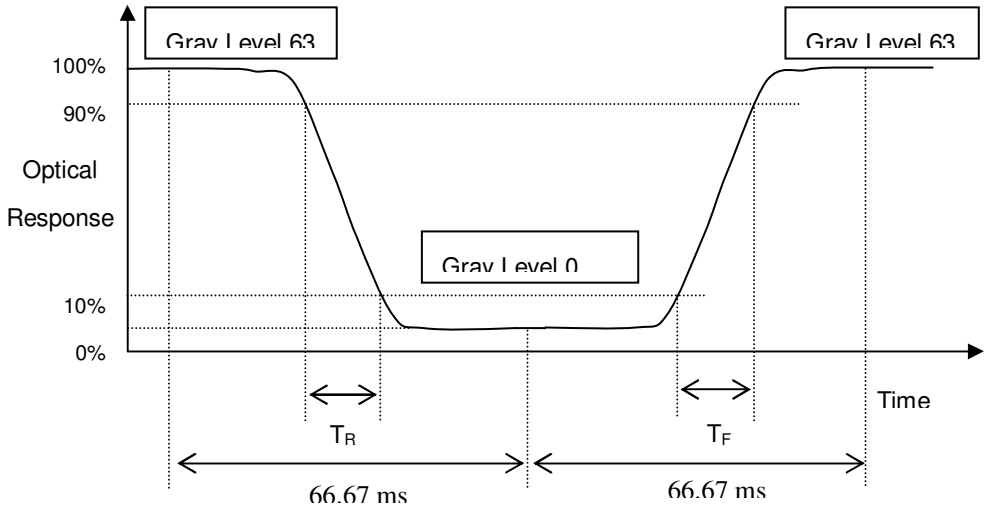
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

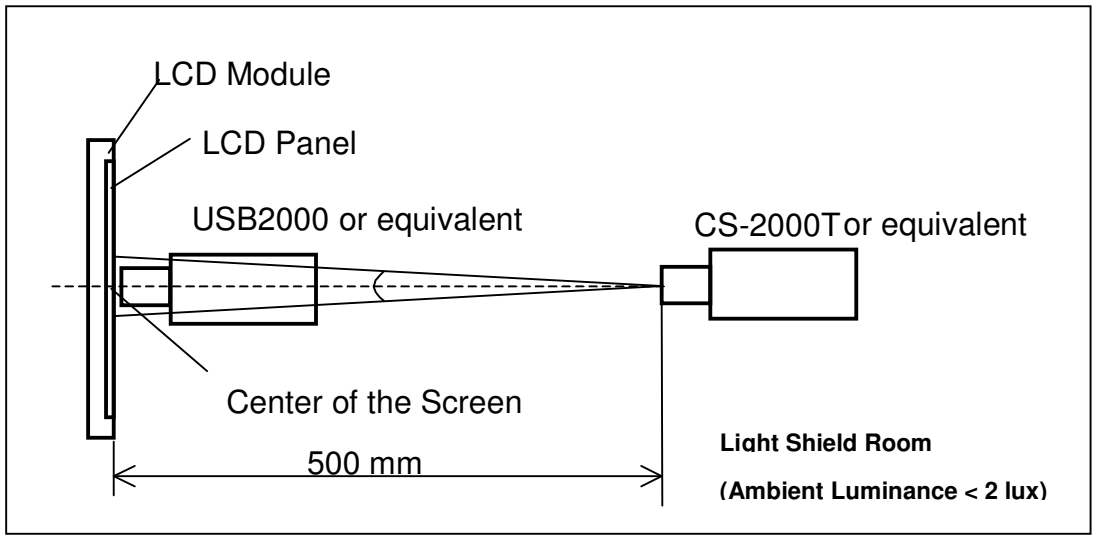
Measure the luminance of gray level 63 at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

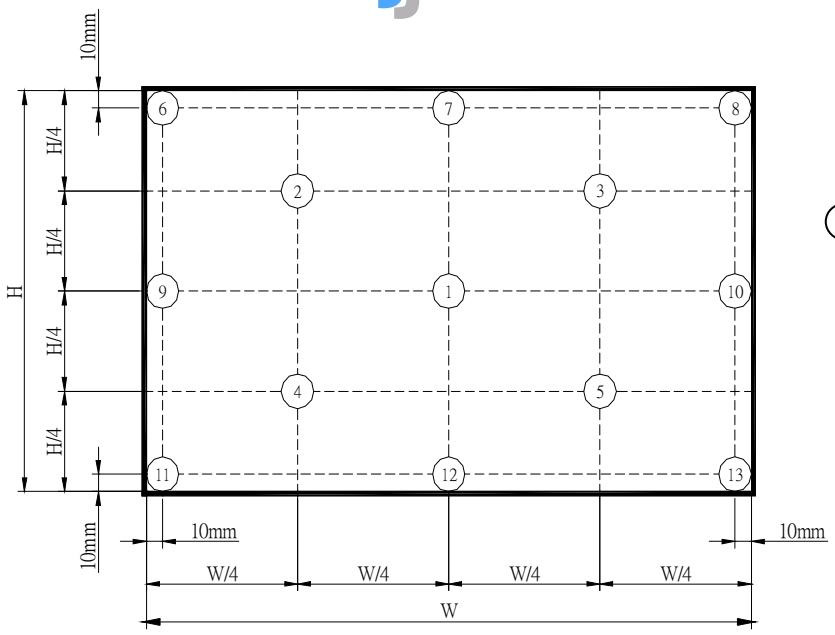
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

δW_{5p} = {Minimum [L (1) ~ L (5)] / Maximum [L (1) ~ L (5)]}*100%



Ⓧ : Test Point

X=1 to 13

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour←→60℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50ºC, 240 hours	
Low Temperature Operation Test	0ºC, 240 hours	
High Temperature & High Humidity Operation Test	50ºC, RH 80%, 240hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. PACKING

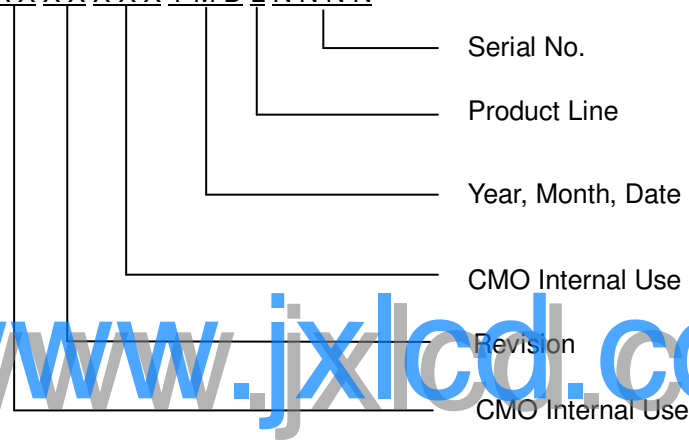
7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Model Name: N173HHF-E21

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

7.2 CARTON

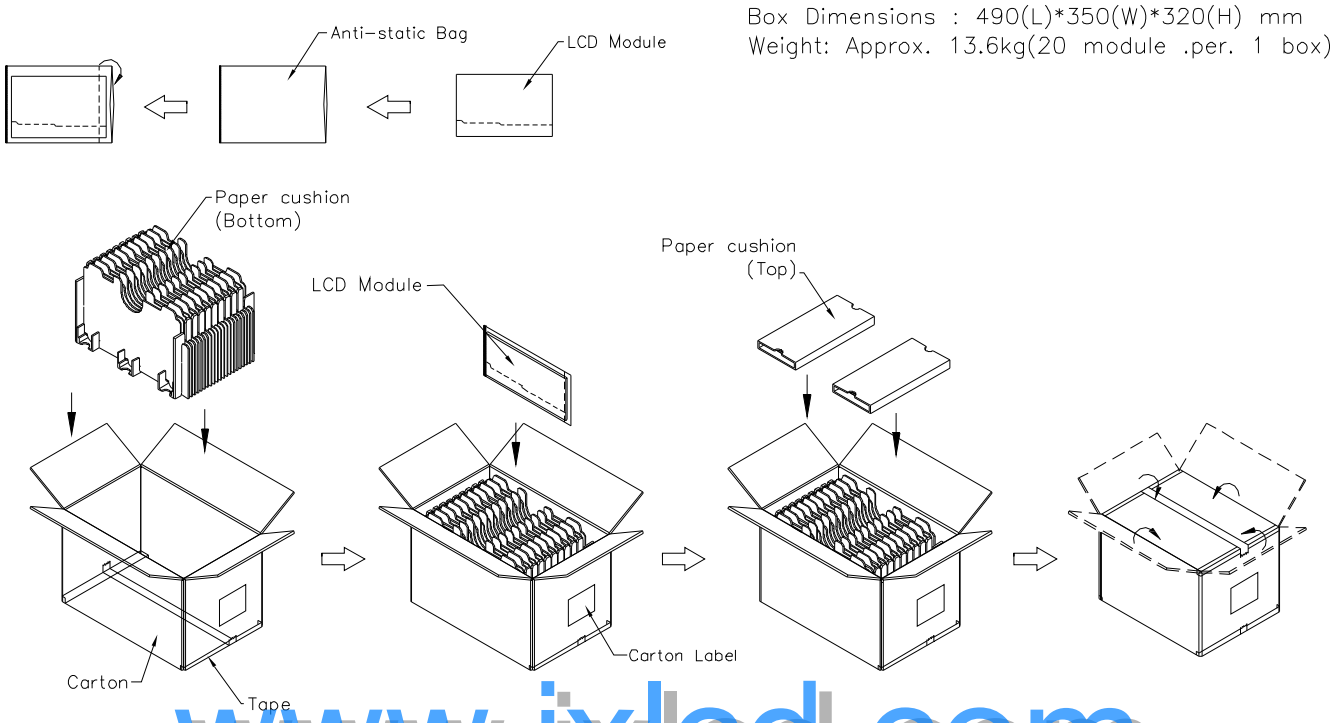


Figure. 7-2 Packing Method

7.3 PALLET

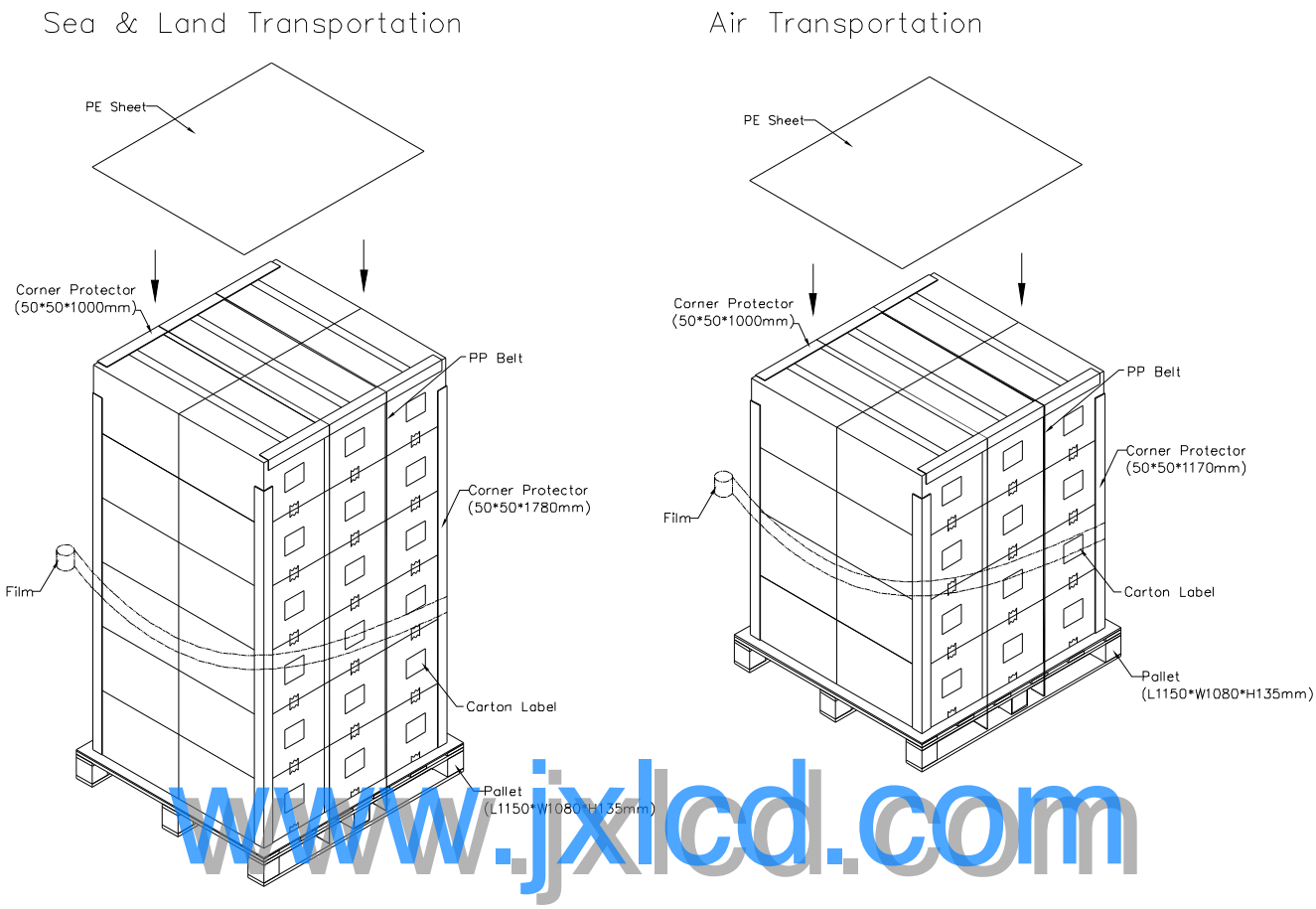


Figure. 7-3 Packing Method

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

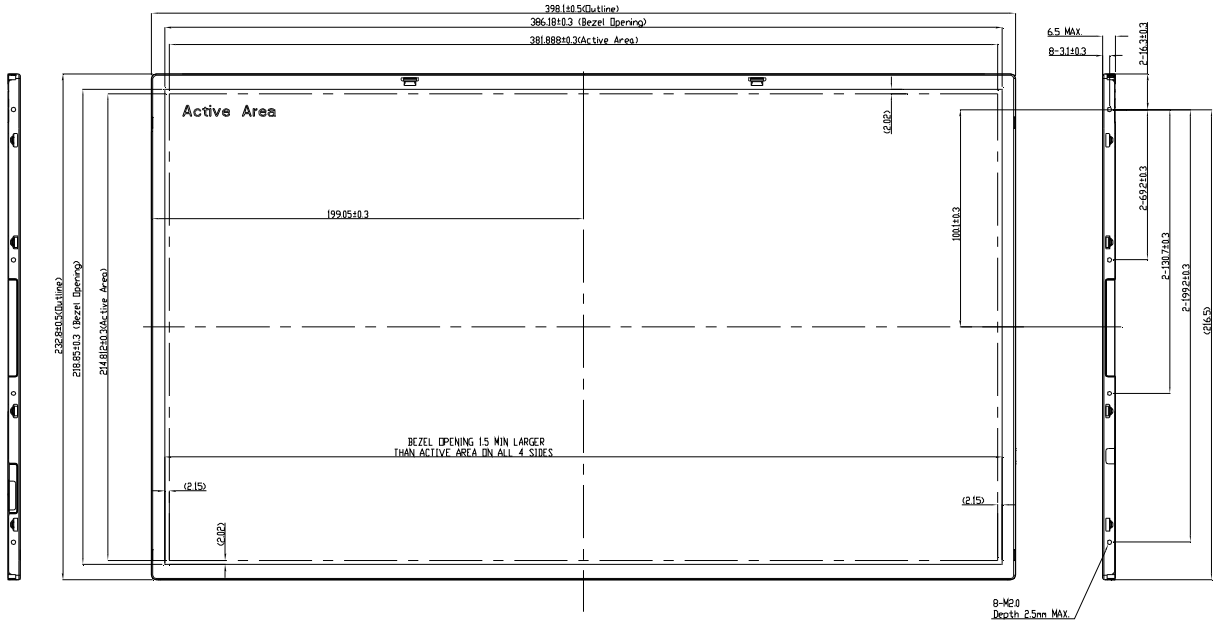
The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte #(decimal)	Byte #(hex)	Field Name and Comments	Value(hex)	Value(binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name (“CMO”)	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AF	10101111
10	0A	ID product code (N173HHF-E11)	23	00100011
11	0B	ID product code (hex LSB first; N173HHF-E11)	17	00010111
12	0C	ID S/N (fixed “0”)	00	00000000
13	0D	ID S/N (fixed “0”)	00	00000000
14	0E	ID S/N (fixed “0”)	00	00000000
15	0F	ID S/N (fixed “0”)	00	00000000
16	10	Week of manufacture (fixed week code)	02	00000010
17	11	Year of manufacture (fixed year code)	15	00010101
18	12	EDID structure version # (“1”)	01	00000001
19	13	EDID revision # (“4”)	04	00000100
20	14	Vedio Input Definition	95	10010101
21	15	Max H image size (“38.189cm”)	26	00100110
22	16	Max V image size (“21.481cm”)	15	00010101
23	17	Display Gamma (Gamma = ”2.2”)	78	01111000
24	18	Feature support	02	00000010
25	19	Red/Green (Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0)	D1	11010001
26	1A	Blue/White (Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0)	F5	11110101
27	1B	Red-x (Rx = “0.577”)	93	10010011
28	1C	Red-y (Ry = “0.364”)	5D	01011101
29	1D	Green-x (Gx = ”0.348”)	59	01011001
30	1E	Green-y (Gy = ”0.563”)	90	10010000
31	1F	Blue-x (Bx = ”0.151”)	26	00100110
32	20	Blue-y (By = ”0.116”)	1D	00011101
33	21	White-x (Wx = ”0.313”)	50	01010000
34	22	White-y (Wy = ”0.329”)	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer’s reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock (“138.53MHz”, According to VESA CVT Rev1.4)	1D	00011101
55	37	# 1 Pixel clock (hex LSB first)	36	00110110
56	38	# 1 H active (“1920”)	80	10000000
57	39	# 1 H blank (“160”)	A0	10100000
58	3A	# 1 H active : H blank (“1920 :160”)	70	01110000
59	3B	# 1 V active (”1080”)	38	00111000
60	3C	# 1 V blank (”30”)	1E	00011110
61	3D	# 1 V active : V blank (”1080 :30”)	40	01000000
62	3E	# 1 H sync offset (”46”)	2E	00101110
63	3F	# 1 H sync pulse width ("30”)	1E	00011110
64	40	# 1 V sync offset : V sync pulse width (”2 : 4”)	24	00100100
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width (”46: 30 : 2 : 4”)	00	00000000
66	42	# 1 H image size (”382 mm”)	7E	01111110
67	43	# 1 V image size (”215 mm”)	D7	11010111
68	44	# 1 H image size : V image size (”382 : 215”)	10	00010000
69	45	# 1 H boarder (”0”)	00	00000000
70	46	# 1 V boarder (”0”)	00	00000000
71	47	# 1 Non-interlaced, Normal Display, Digital Separate Sync, H/V pol Negatives	18	00011000
72	48	Detailed timing description # 1 Pixel clock (“330.31MHz”, According to VESA CVT Rev1.4)	07	00000111
73	49	# 2 Pixel clock (hex LSB first)	81	10000001
74	4A	# 2 H active (“1920”)	80	10000000
75	4B	# 2 H blank (“160”)	A0	10100000
76	4C	# 2 H active : H blank (“1920 :160”)	70	01110000
77	4D	# 2 V active (”1080”)	38	00111000
78	4E	# 2 V blank (”508”)	FC	11111100
79	4F	# 2 V active : V blank (”1080 :508”)	41	01000001
80	50	# 2 H sync offset (”46”)	2E	00101110
81	51	# 2 H sync pulse width ("30”)	1E	00011110
82	52	# 2 V sync offset : V sync pulse width (”2 : 4”)	24	00100100
83	53	# 2 H sync offset : H sync pulse width : V sync offset : V sync width (”46: 30 : 2 : 4”)	00	00000000
84	54	# 2 H image size (”382 mm”)	7E	01111110
85	55	# 2 V image size (”215 mm”)	D7	11010111

86	56	# 2 H image size : V image size (”382 : 215”)	10	00010000
87	57	# 2 H boarder (”0”)	00	00000000
88	58	# 2 V boarder (”0”)	00	00000000
89	59	# 2 Non-interlaced, Field sequential stereo, left image when stereo sync signal = 1, Digital Separate Sync, H/V pol Negatives	58	01011000
90	5A	Detailed timing description # 1 Pixel clock (“363.34MHz”, According to VESA CVT Rev1.4)	EE	11101110
91	5B	# 3 Pixel clock (hex LSB first)	8D	10001101
92	5C	# 3 H active (“1920”)	80	10000000
93	5D	# 3 H blank (“160”)	A0	10100000
94	5E	# 3 H active : H blank (“1920 :160”)	70	01110000
95	5F	# 3 V active (”1080”)	38	00111000
96	60	# 3 V blank (”508”)	FC	11111100
97	61	# 3 V active : V blank (”1080 :508”)	41	01000001
98	62	# 3 H sync offset (”46”)	2E	00101110
99	63	# 3 H sync pulse width ("30”)	1E	00011110
100	64	# 3 V sync offset : V sync pulse width (”2 : 4”)	24	00100100
101	65	# 3 H sync offset : H sync pulse width : V sync offset : V sync width (”46: 30 : 2 : 4”)	00	00000000
102	66	# 3 H image size (”382 mm”)	7E	01111110
103	67	# 3 V image size (”215 mm”)	D7	11010111
104	68	# 3 H image size : V image size (”382 : 215”)	10	00010000
105	69	# 3 H boarder (”0”)	00	00000000
106	6A	# 3 V boarder (”0”)	00	00000000
107	6B	# 3 Non-interlaced, Field sequential stereo, left image when stereo sync signal = 1, Digital Separate Sync, H/V pol Negatives	58	01011000
108	6C	Detailed timing description # 1 Pixel clock (“396.37MHz”, According to VESA CVT Rev1.4)	D5	11010101
109	6D	# 4 Pixel clock (hex LSB first)	9A	10011010
110	6E	# 4 H active (“1920”)	80	10000000
111	6F	# 4 H blank (“160”)	A0	10100000
112	70	# 4 H active : H blank (“1920 :160”)	70	01110000
113	71	# 4 V active (”1080”)	38	00111000
114	72	# 4 V blank (”508”)	FC	11111100
115	73	# 4 V active : V blank (”1080 :508”)	41	01000001
116	74	# 4 H sync offset (”46”)	2E	00101110
117	75	# 4 H sync pulse width ("30”)	1E	00011110
118	76	# 4 V sync offset : V sync pulse width (”2 : 4”)	24	00100100
119	77	# 4 H sync offset : H sync pulse width : V sync offset : V sync width (”46: 30 : 2 : 4”)	00	00000000
120	78	# 4 H image size (”382 mm”)	7E	01111110
121	79	# 4 V image size (”215 mm”)	D7	11010111
122	7A	# 4 H image size : V image size (”382 : 215”)	10	00010000
123	7B	# 4 H boarder (”0”)	00	00000000
124	7C	# 4 V boarder (”0”)	00	00000000
125	7D	# 4 Non-interlaced, Field sequential stereo, left image when stereo sync signal = 1, Digital Separate Sync, H/V pol Negatives	58	01011000
126	7E	No extension	00	00000000
127	7F	Checksum	A6	10100110

Appendix. OUTLINE DRAWING



NOTES:
1. MAX. SCREW DEPTH: 2.5mm.
2. MAX SCREW TORQUE: 2 kgf-cm.
3. LCD MODULE INPUT CONNECTOR : STARCONN 111A40-0000RA-G3, TYCO# 5-2069716-3, OR EQUIVALENT.
4. GAP BETWEEN BEZEL AND PANEL: 0.5mm MAX.
5. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT,
   NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA,
   WLAN, WAN OR OTHER FOREIGN OBJECTS OVER TCON AND VR LOCATION.
6. MODULE FLATNESS 0.5mm MAX.
7. '( )' MARKS THE REFERENCE DIMENSIONS.