Doc. Number: DN0281715

☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: R213T3
SUFFIX: L01

Customer:

APPROVED BY **SIGNATURE**

Name / Title
Note

Please return 1 copy for your confirmation with your signature and comments.

核准時間	部門	審核	角色	投票
2011-12-07 17:40:07	APPL 產品管理處	yuhsiang.chang (張喻翔/514-10922)	Director	Accept

CONTENTS

REVISION HISTORY

Version	Date	Page	Description
2.1	Oct.13, 2010	All	Modify the format of spec.
		5	Sec.2, modify the module weight
		23	Sec. 4.6, modify the timing definition of power on-off sequence
2.2	Nov. 1, 2011	16	Sec 4.3.4 Modify the input current typ. 4.5A to 4.9A max. 5.0A to 5.5A Modify the power consumption Typ. 54W to 59W Max. 60W to 66W
		22	Sec 4.5 Modify the description of Note
		29	Sec 6 Vibration test required condition frequency range from 1~200Hz to 10~300Hz
		30	Change the packing bag and carton label
		31	Change the carton label

1. GENERAL DESCRIPTION

1.1 OVERVIEW

R213T3-L01 is a 21.3" TFT Liquid Crystal Display module with 12 CCFLs Backlight unit and two port 31 pins 2ch-LVDS interface. This module supports 2560 x 2048 QSXGA screen and can display monochrome driven by 8bit drivers. The LCD module includes built-in inverter for Backlight.

1.2 FEATURES

This specification applies to the Type 21.3" Mono TFT LCD Module, Model R213T3-L01- This module includes an inverter card for the backlight.

- The screen format is intended to support QSXGA 2560(H) x 2048(V) resolution.
- Screen with sensor area (176(H) x 16(V)) at the top of the screen
- All input signals are LVDS (Low Voltage Differential Signaling) interface.
- This module is designed for a module with neutral white (0.294, 0.309) and DICOM gamma curve.
- This module is especially designed for wide view performance
- This module is UL approved and RoHs compliant

1.3 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	21.3" real diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	2560(x3) x 2048	pixel	-
Pixel Pitch	0.165 (H) x 0.165 (V)	mm	-
Pixel Arrangement	Sub-pixel Vertical stripe	-	-
Display Colors	8-bit per1(one) sub-pixel, grayscale	-	-
Transmissive Mode	Dual domain IPS, Normally Black	-	-
Surface Treatment	AG type	-	-
Luminance, White	1100	Cd/m2	-
Power Consumption	Total 65.28W (typ.) @ cell 11.28 W (typ.), BL 54 W (typ.)		(1)

Note (1) The specified power consumption: Total= cell (reference 4.3.1)+ BL (reference 4.3.4)

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	459.3	459.8	460.3	mm	(1)
	Vertical (V)	374.8	375.3	375.8	mm	
	Thickness (T)	48	48.5	49	mm	
Bezel Area	Horizontal	426.1	426.4	426.9	mm	
	Vertical	344.0	344.5	345.0	mm	
Active Area	Horizontal	-	422.4	-	mm	
	Vertical	-	337.92	-	mm	
Weight		2840	2890	3010	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

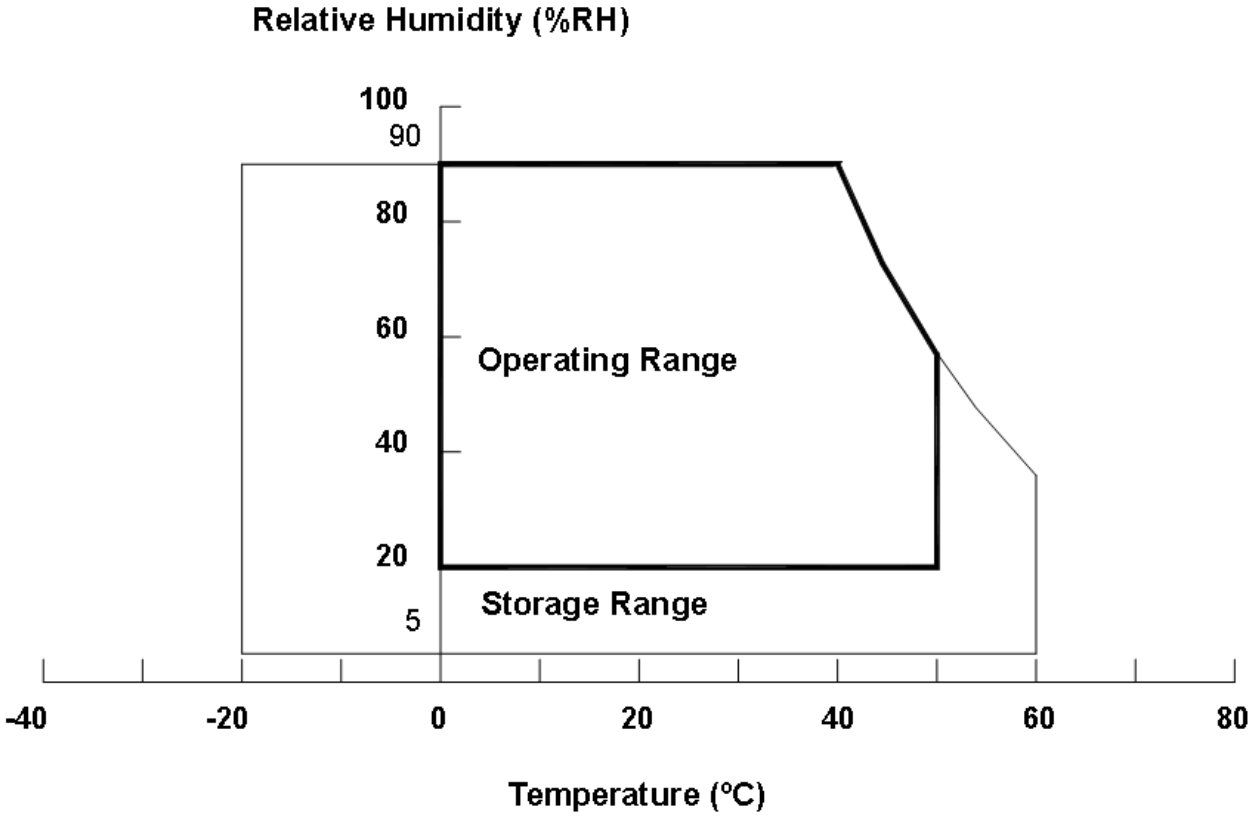
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	60	ºC	(1)
Operating Ambient Temperature	TOP	0	50	ºC	(1), (2)

Note (1)

(a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.



Note (2) The temperature of panel surface should be 0 ºC min. and 60 ºC max.

3.2 ELECTRICAL ABSOLUTE RATINGS

3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+13.2	V	(1)
Logic Input Voltage	V_{IN}	-0.3	+4.3	V	

3.2.2 BACKLIGHT UNIT

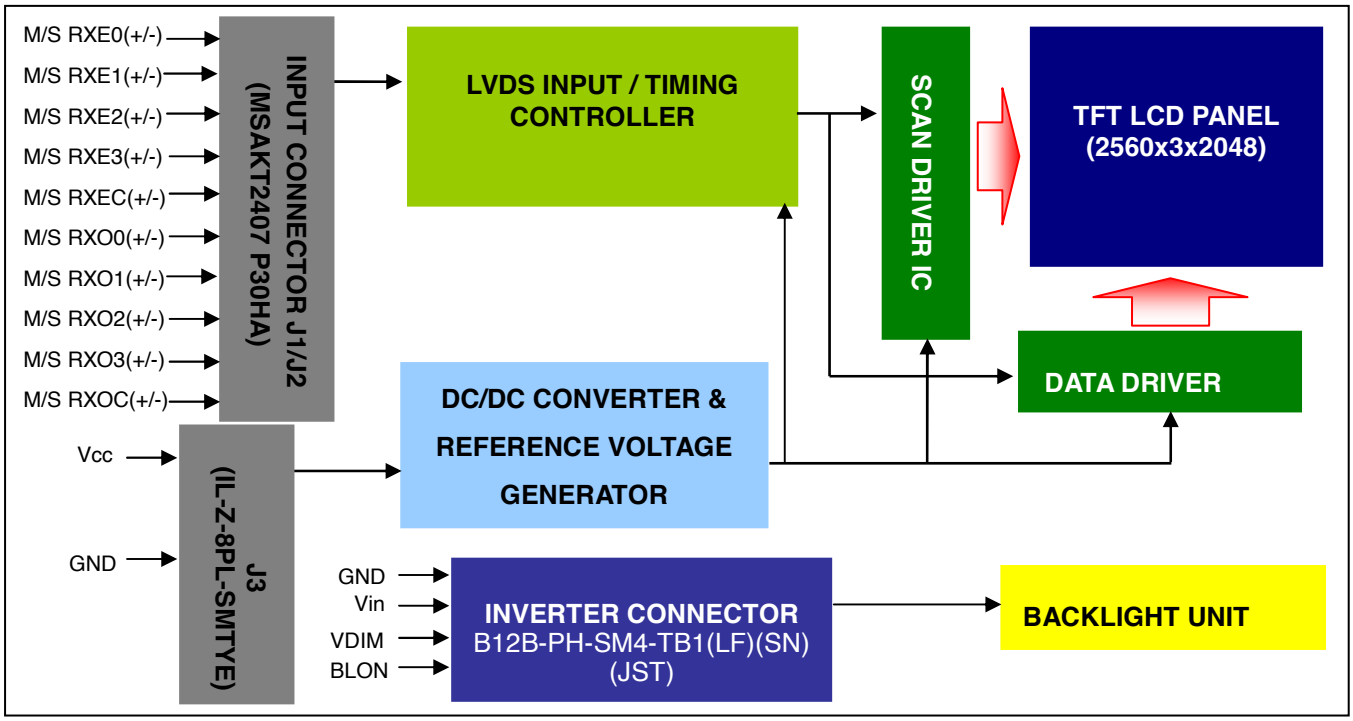
Item	Symbol	Value			Unit	Note
		Min.	Typ	Max.		
Lamp Voltage	V_L	666	740	814	V_{RMS}	(1), (2)
Lamp current	I_L	6.0	6.5	7.0	mA_{RMS}	
Lamp frequency	F_L	46	50	54	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 4.3.3 and 4.3.4 for further information).

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2. INPUT INTERFACE CONNECTIONS

4.2.1 J1 (MASTER) : LEFT SIDE(FRONT VIEW)

Pin	Name	Description
1	MRXE0-	Negative LVDS differential data input. Channel E0 (even)
2	MRXE0+	Positive LVDS differential data input. Channel E0 (even)
3	GND	LVDS Ground
4	MRXE1-	Negative LVDS differential data input. Channel E1 (even)
5	MRXE1+	Positive LVDS differential data input. Channel E1 (even)
6	GND	LVDS Ground
7	MRXE2-	Negative LVDS differential data input. Channel E2 (even)
8	MRXE2+	Positive LVDS differential data input. Channel E2 (even)
9	GND	LVDS Ground
10	MRXEC-	Negative LVDS differential clock input. (even)
11	MRXEC+	Positive LVDS differential clock input. (even)
12	GND	LVDS Ground
13	MRXE3-	Negative LVDS differential data input. Channel E3 (even)
14	MRXE3+	Positive LVDS differential data input. Channel E3 (even)
15	GND	LVDS Ground
16	GND	LVDS Ground
17	MRXO0-	Negative LVDS differential data input. Channel O0 (odd)
18	MRXO0+	Positive LVDS differential data input. Channel O0 (odd)

19	GND	LVDS Ground
20	MRXO1-	Negative LVDS differential data input. Channel O1 (odd)
21	MRXO1+	Positive LVDS differential data input. Channel O1 (odd)
22	GND	LVDS Ground
23	MRXO2-	Negative LVDS differential data input. Channel O2 (odd)
24	MRXO2+	Positive LVDS differential data input. Channel O2 (odd)
25	GND	LVDS Ground
26	MRXOC-	Negative LVDS differential clock input. (odd)
27	MRXOC+	Positive LVDS differential clock input. (odd)
28	GND	LVDS Ground
29	MRXO3-	Negative LVDS differential data input. Channel O3 (odd)
30	MRXO3+	Positive LVDS differential data input. Channel O3 (odd)

4.2.2 J2(SLAVE) : RIGHT SIDE(FRONT VIEW)

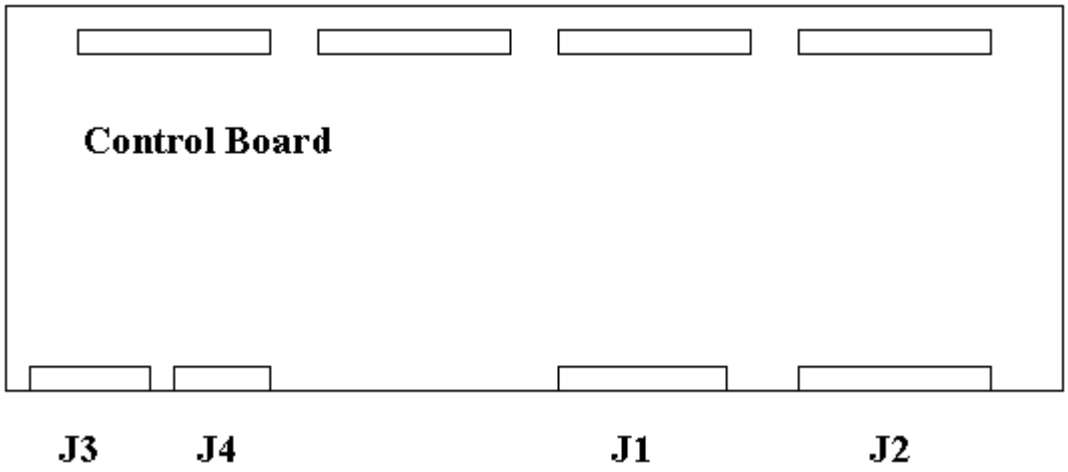
Pin	Name	Description
1	SRXE0-	Negative LVDS differential data input. Channel E0 (even)
2	SRXE0+	Positive LVDS differential data input. Channel E0 (even)
3	GND	LVDS Ground
4	SRXE1-	Negative LVDS differential data input. Channel E1 (even)
5	SRXE1+	Positive LVDS differential data input. Channel E1 (even)
6	GND	LVDS Ground
7	SRXE2-	Negative LVDS differential data input. Channel E2 (even)
8	SRXE2+	Positive LVDS differential data input. Channel E2 (even)
9	GND	LVDS Ground
10	SRXEC-	Negative LVDS differential clock input. (even)
11	SRXEC+	Positive LVDS differential clock input. (even)
12	GND	LVDS Ground
13	SRXE3-	Negative LVDS differential data input. Channel E3 (even)
14	SRXE3+	Positive LVDS differential data input. Channel E3 (even)
15	GND	LVDS Ground
16	GND	LVDS Ground
17	SRXO0-	Negative LVDS differential data input. Channel O0 (odd)
18	SRXO0+	Positive LVDS differential data input. Channel O0 (odd)
19	GND	LVDS Ground
20	SRXO1-	Negative LVDS differential data input. Channel O1 (odd)
21	SRXO1+	Positive LVDS differential data input. Channel O1 (odd)
22	GND	LVDS Ground
23	SRXO2-	Negative LVDS differential data input. Channel O2 (odd)
24	SRXO2+	Positive LVDS differential data input. Channel O2 (odd)
25	GND	LVDS Ground
26	SRXOC-	Negative LVDS differential clock input. (odd)
27	SRXOC+	Positive LVDS differential clock input. (odd)
28	GND	LVDS Ground
29	SRXO3-	Negative LVDS differential data input. Channel O3 (odd)
30	SRXO3+	Positive LVDS differential data input. Channel O3 (odd)

Note (1) The first pixel is even.

Note (2) Input signal of even and odd clock should be the same timing.

Note (3) The module uses a 100-ohm resistor between positive and negative data lines of each receiver input

Note (4) Control board front view

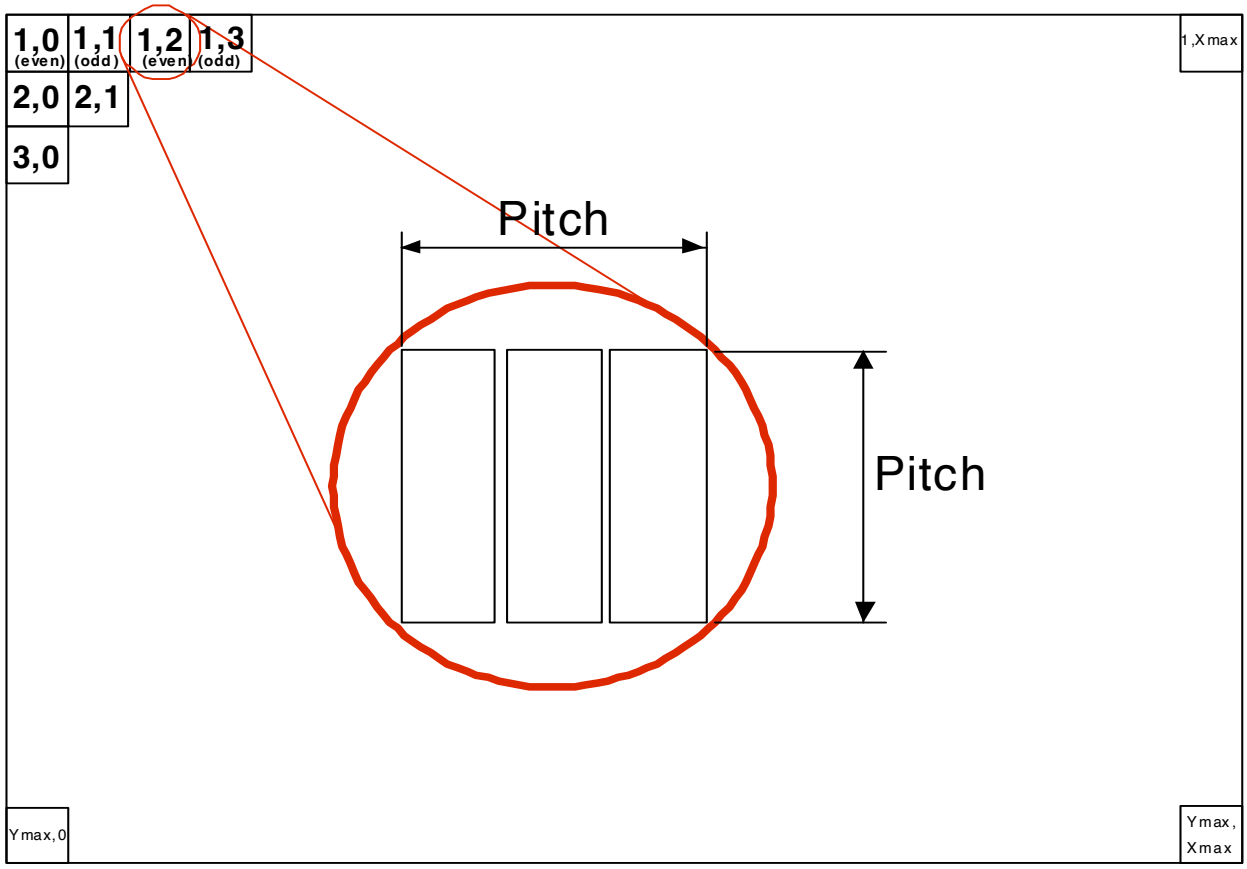


J1 : MSAKT2407P30HA (STM) or equivalent; LVDS input for LEFT half screen

J2 : MSAKT2407P30HA (STM) or equivalent; LVDS input for RIGHT half screen

J3 : IL-Z-8PL-SMTYE(JAE) : Power input (+12V) ; Mating Connector: IL-Z-8S-S125C3 (JAE)

J4 : IL-Z-5PL-SMTYE(JAE) : EDID interface ; Mating Connector: IL-Z-5S-S125C3 (JAE)



4.2.3 DC INPUT PIN ASSIGNMENT

Pin	Name	Description
1	GND	Ground for Vcc
2	GND	Ground for Vcc
3	GND	Ground for Vcc
4	GND	Ground for Vcc
5	Vcc	+12.0V Power Supply for Control board
6	Vcc	+12.0V Power Supply for Control board
7	Vcc	+12.0V Power Supply for Control board
8	Vcc	+12.0V Power Supply for Control board

4.2.4 EDID INTERFACE PIN ASSIGNMENT

Pin	Name	Description
1	Vcc-EDID	+3.3V Power Supply for EDID Chip
2	NC	Not Connection
3	SCL	EDID Clock
4	SDA	EDID Data
5	GND	Ground for Vcc-EDID

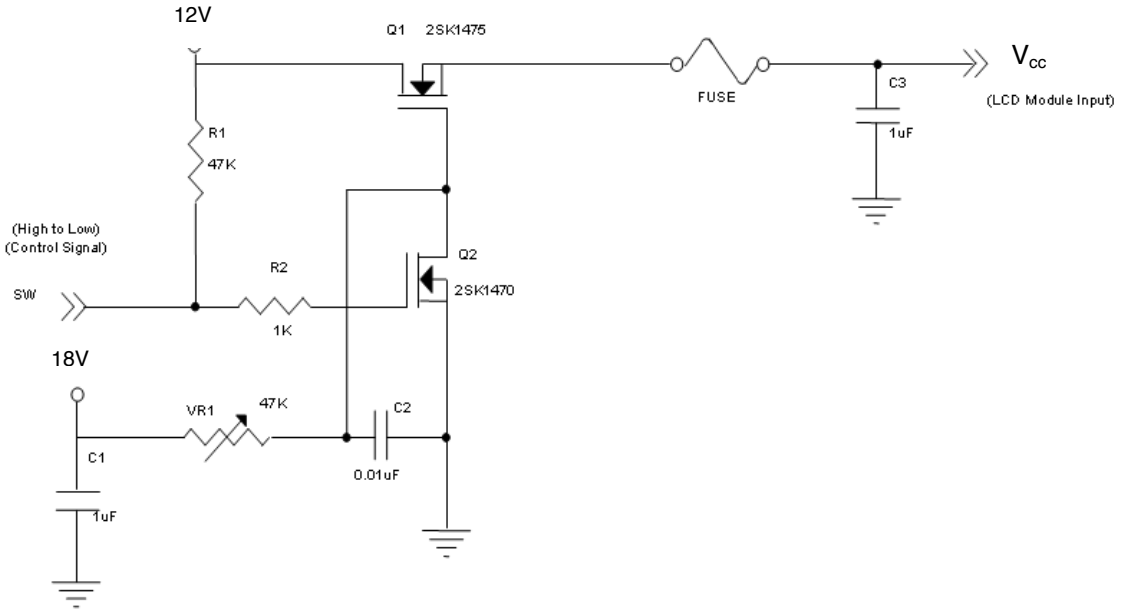
4.3 ELECTRICAL CHARACTERISTICS

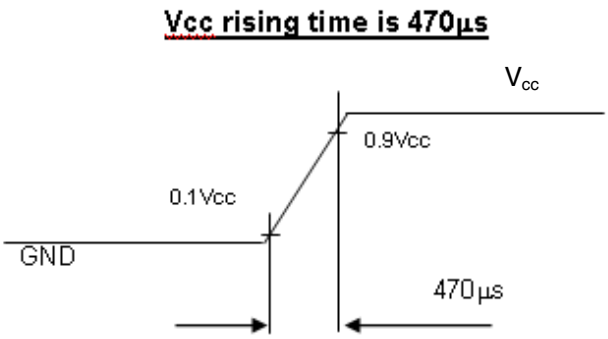
4.3.1 LCD ELETRONICS SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	11.4	12	12.6	V	-
Ripple Voltage		V_{RP}	-	-	300	mV	-
Rush Current		I_{RUSH}	-	-	3.8	A	(2)
Power Supply Current	White		-	0.940	1.220	A	(3)a
	Black		-	0.520	0.670	A	(3)b
	Vertical Stripe		-	0.810	1.050	A	(3)c
Power Consumption			-	11.28	14.64	W	(4)
LVDS differential input voltage		Vid	200	-	600	mV	
LVDS common input voltage		Vic	1.0	1.2	1.4	V	
Logic High Input Voltage		V_{IH}	2.64	-	-	V	
Logic Low Input Voltage		V_{IL}	-	-	0.66	V	

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) Measurement Conditions:





Note (3) The specified power supply current is under the conditions at Vcc =12.0 V, Ta = 25 ± 2 °C, Fr = 60Hz, whereas a power dissipation check pattern below is displayed.

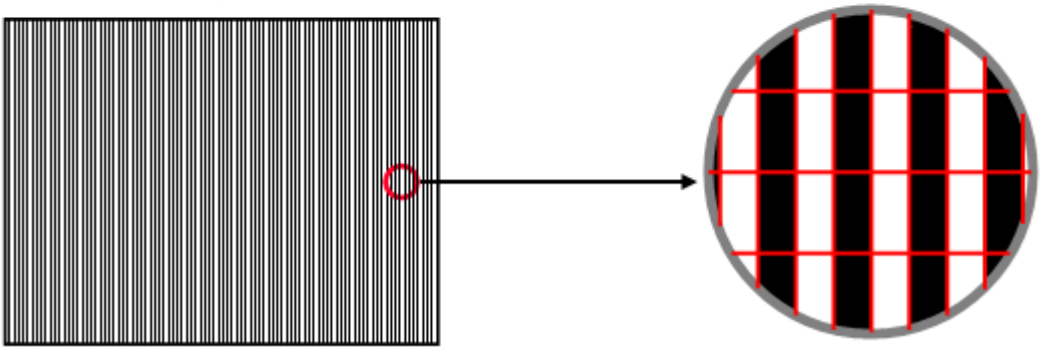
a. White Pattern

Active Area

b. Black Pattern

Active Area

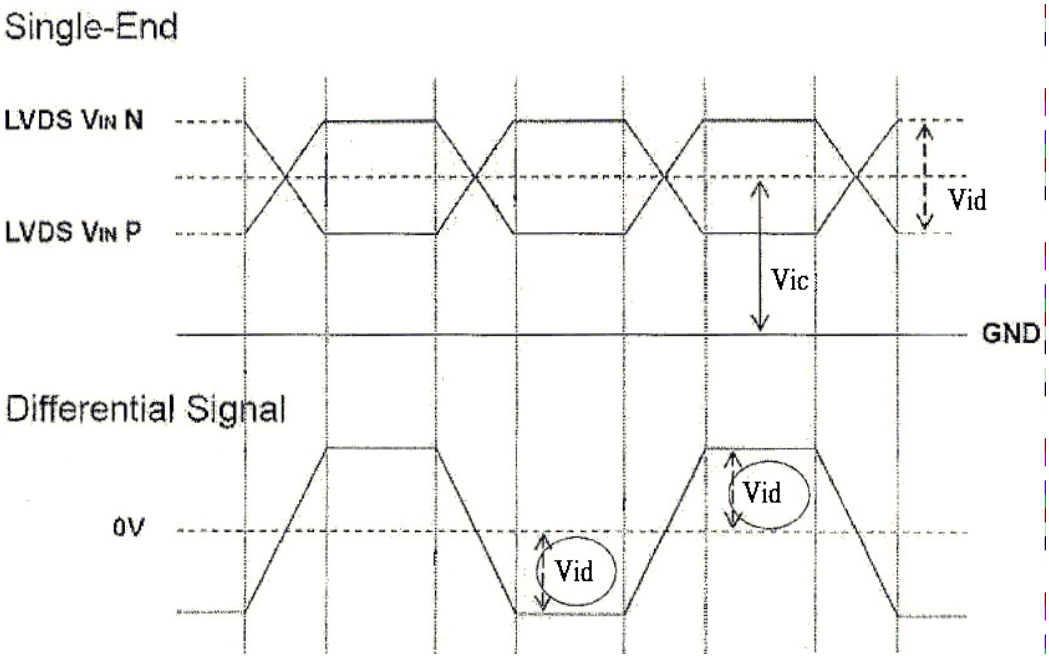
c. Vertical Stripe Pattern



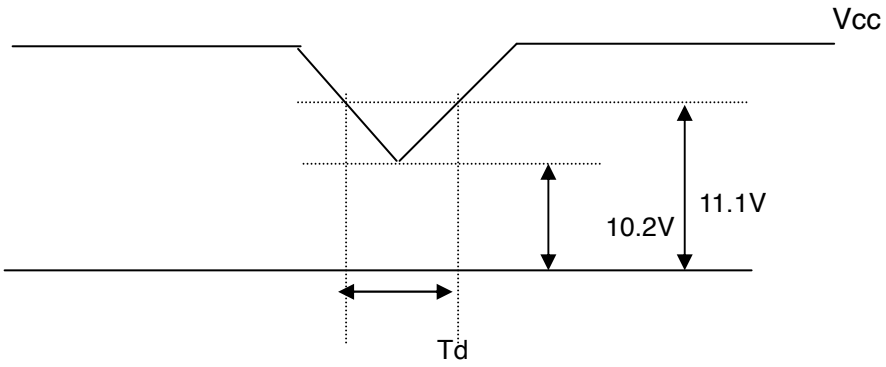
Active Area

Note (4) The power consumption is specified at the pattern with the maximum current.

Note (5) VID waveform condition



4.3.2 Vcc Power Dip Condition

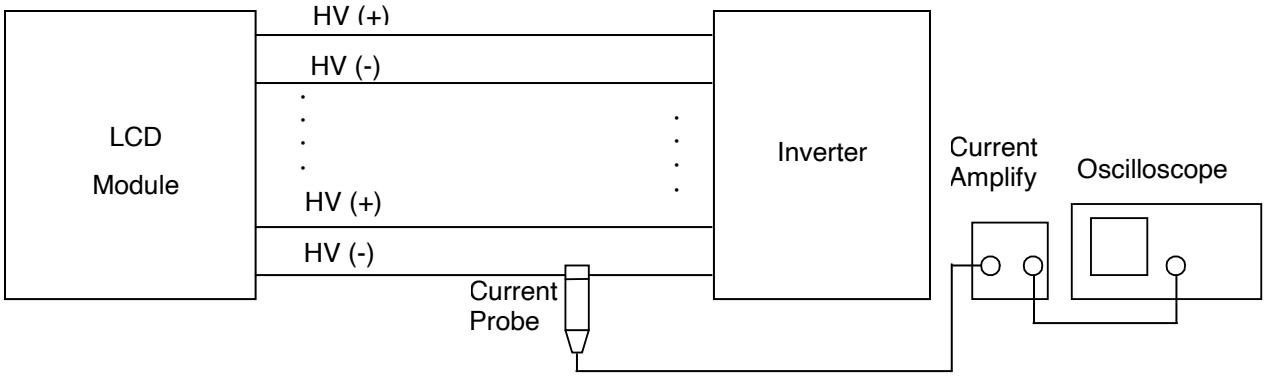


Dip condition: $10.2V \le Vcc \le 11.1V, Td \le 20ms$

4.3.3 BACKLIGHT UNIT

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	666	740	814	V_{RMS}	I_L = 6.5mA
Lamp Current	I_L	6.0	6.5	7.0	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	---	---	1080(25℃)	V_{RMS}	(2)
		---	---	1300(0℃)	V_{RMS}	(2)
Operating Frequency	F_L	46	50	54	KHz	(3)
Lamp Life Time	L_{BL}	50,000	---	---	Hrs	(4)

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:



Note (2) The voltage shown above should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The lifetime of lamp can be defined as the time in which it continues to operate under the condition Ta = 25 ±2 °C and I_L = 6.0~7.0 mA_{rms} until one of the following events occurs:

(a) When the brightness becomes or lower than 50% of its original value.

(b) When the effective ignition length becomes lower than 80% of its original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)

Note (5) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid producing too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

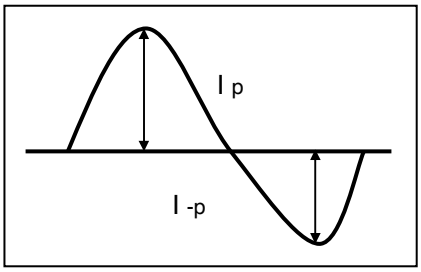
The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform.(Unsymmetrical ratio is less than 10%) Please do not use the inverter, which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

a. The asymmetry rate of the inverter waveform should be 10% below;

b. The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$;

c. The ideal sine wave form shall be symmetric in positive and negative polarities.



* Asymmetry rate:

$| I_p - I_{-p} | / I_{rms} * 100\%$

* Distortion rate

I_p (or I_{-p}) / I_{rms}

4.3.4 INVERTER ELECTRICAL CHARATERISTIC

Item	Symbol	Description	Min.	Typ.	Max.	Unit
1	V_{in}	Input voltage	11.4	12	12.6	V
2	I_{in}	Input current (@Vin=12V)	---	4.9	5.5	A
3	P_{in}	Input power	---	59	65	W
4	BLON	Inverter On/Off control: OFF	0	---	0.8	V
		Inverter On/Off control: ON	2.0	---	5.0	V
5	VDIM	Output current control VDIM: 0V, maximum brightness VDIM: 3V, minimum brightness	0	---	3	V
6	F_b	Burst Mode Frequency	150	160	170	Hz
7	$F_{req.}$	Operating frequency	46	50	54	KHz
8	I_{out}	Output current, VDIM=0V (high side)	6.0	6.5	7.0	mA
9	V_{lamp}	Lamp ignite voltage	---	---	1300	V_{rms}

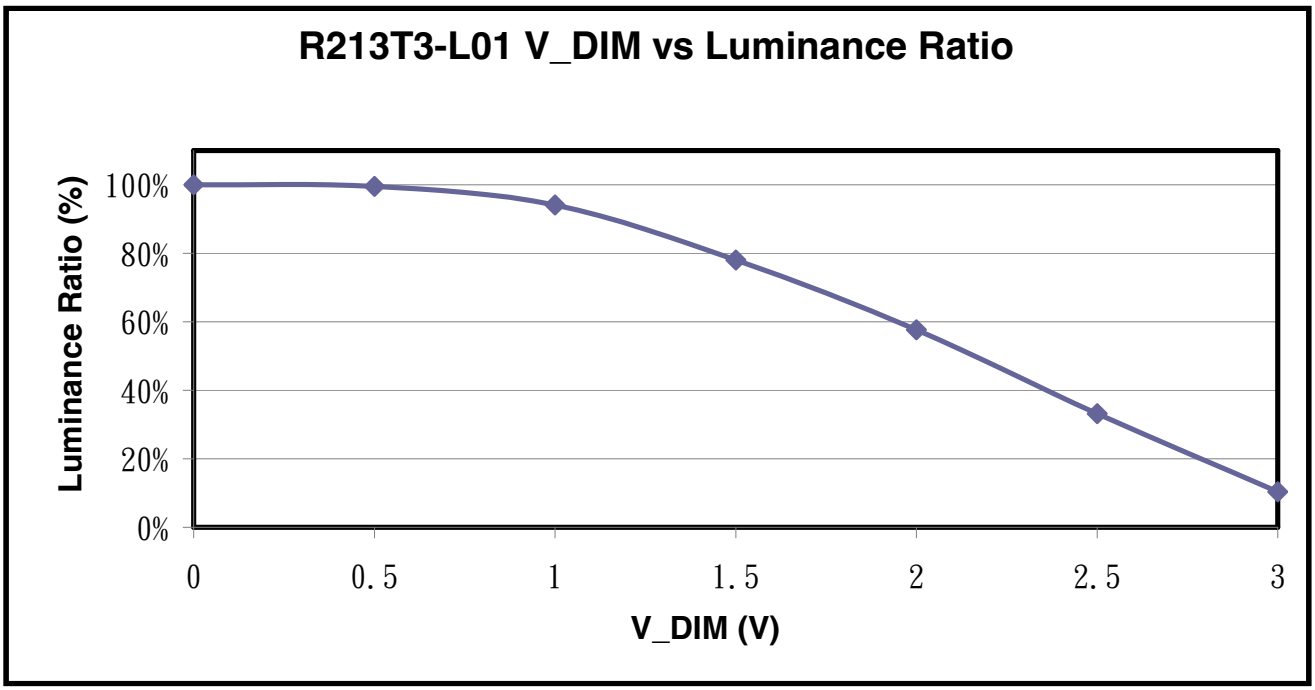
4.3.5 INVERTER INPUT SIGNAL

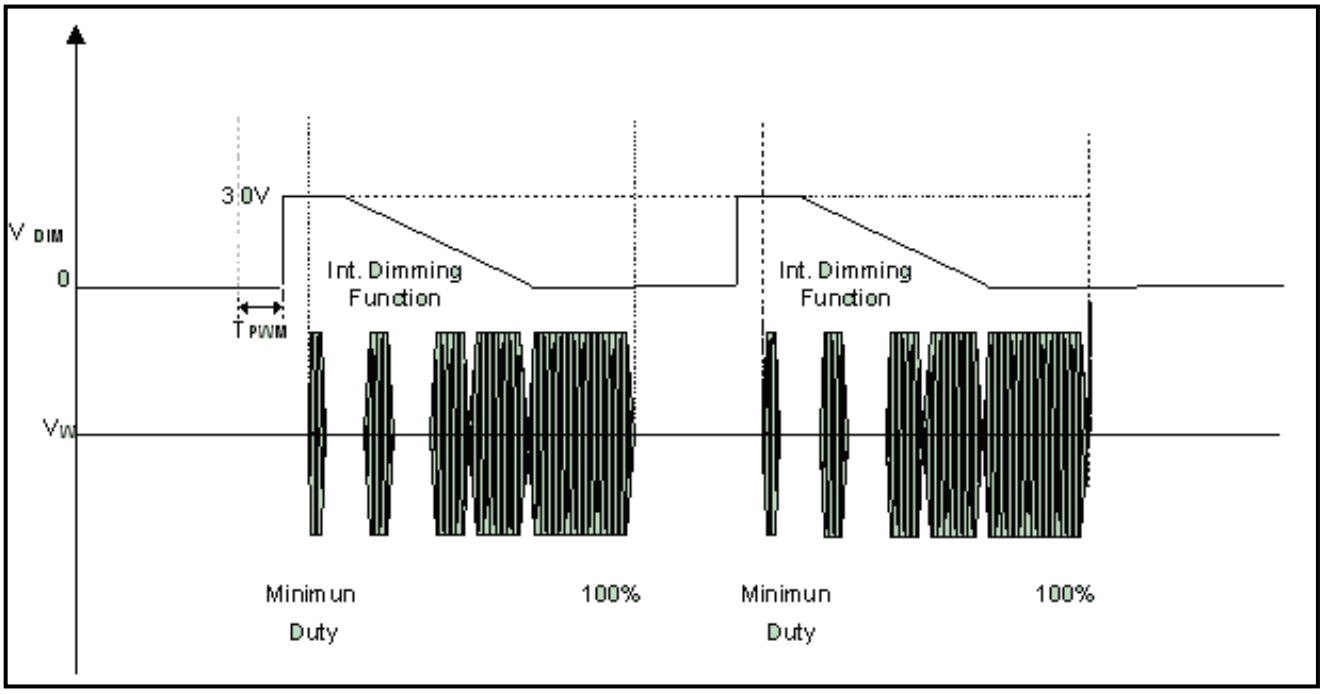
Pin No.	Symbol	Description
1	V_{in}	Input voltage
2	V_{in}	Input voltage
3	V_{in}	Input voltage
4	V_{in}	Input voltage
5	V_{in}	Input voltage
6	Gnd	Ground
7	Gnd	Ground
8	Gnd	Ground
9	Gnd	Ground
10	Gnd	Ground
11	VDIM	Brightness control (0~3V)
12	BLON	Inverter On/Off control (0~5V)

Note (1) Connector Part No.: B12B-PH-SM4-TB1(LF) (SN)(JST) or equivalent

Note (2) User's connector Part No.: PHR-12 (JST)

The following chart is the VDIM vs. Dimming Range for your reference.





4.4 LVDS INPUT SIGNAL SPECIFICATIONS

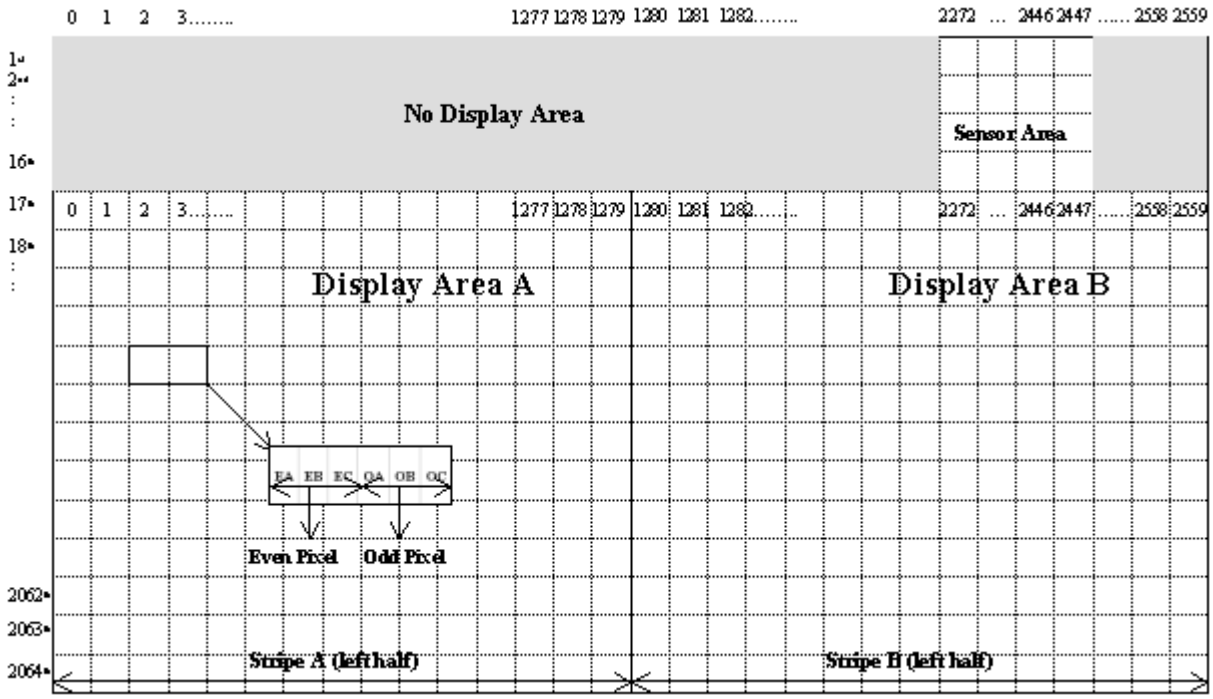
4.4.1 LVDS DATA INPUT DATA ORDER (MASTER)

LVDS interface receiver required input data mapping table								
LVDS Channel E0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	EB2	EA7	EA6	EA5	EA4	EA3	EA2
LVDS Channel E1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	EC3	EC2	EB7	EB6	EB5	EB4	EB3
LVDS Channel E2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	EC7	EC6	EC5	EC4
LVDS Channel E3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	EC1	EC0	EB1	EB0	EA1	EA0
LVDS Channel O0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	OB2	OA7	OA6	OA5	OA4	OA3	OA2
LVDS Channel O1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	OC3	OC2	OB7	OB6	OB5	OB4	OB3
LVDS Channel O2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	OC7	OC6	OC5	OC4
LVDS Channel O3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	OC1	OC0	OB1	OB0	OA1	OA0

4.4.2 LVDS DATA INPUT DAT ORDER (SLAVE)

LVDS interface receiver required input data mapping table								
LVDS Channel E0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	EB2	EA7	EA6	EA5	EA4	EA3	EA2
LVDS Channel E1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	EC3	EC2	EB7	EB6	EB5	EB4	EB3
LVDS Channel E2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	EC7	EC6	EC5	EC4
LVDS Channel E3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	EC1	EC0	EB1	EB0	EA1	EA0
LVDS Channel O0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	OB2	OA7	OA6	OA5	OA4	OA3	OA2
LVDS Channel O1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	OC3	OC2	OB7	OB6	OB5	OB4	OB3
LVDS Channel O2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	OC7	OC6	OC5	OC4
LVDS Channel O3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	OC1	OC0	OB1	OB0	OA1	OA0

4.4.3 PIXEL FORMAT IMAGE



4.4.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

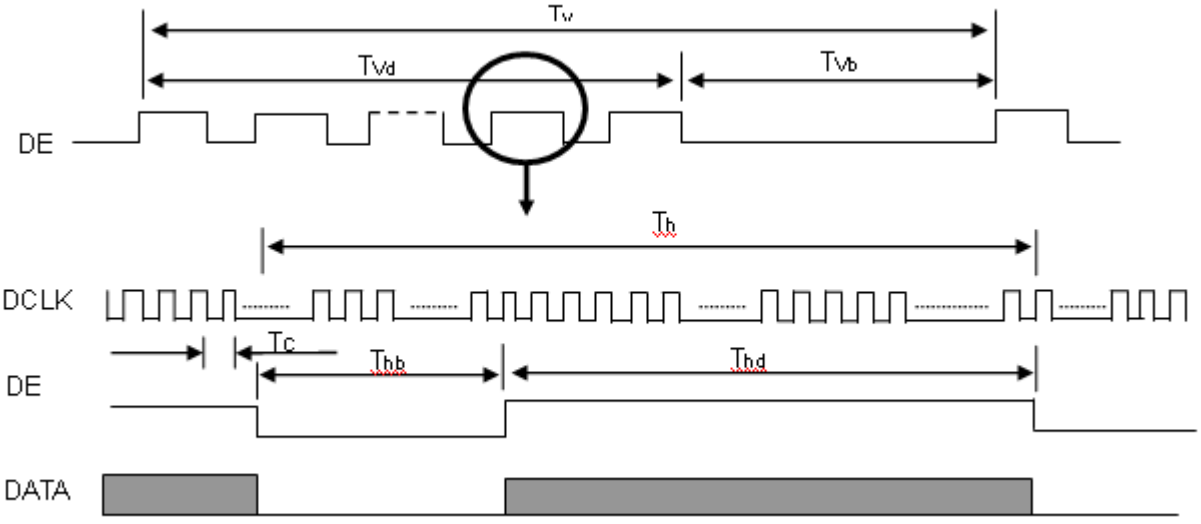
4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

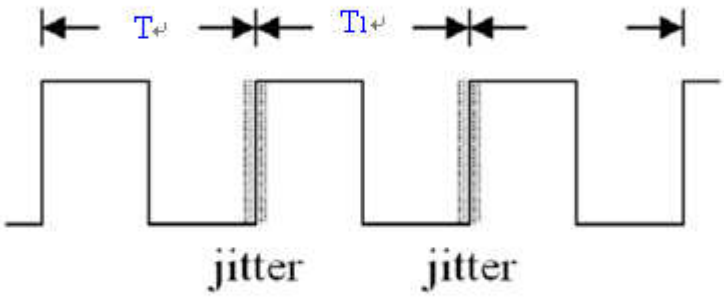
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	F_c	72.97	74	78.15	MHz	-
	Period	T_c	12.79	13.51	13.70	ns	
	Input cycle to cycle jitter	T_{rcl}	---	---	250	ns	(1)
	Spread spectrum modulation range	F_{clkin_mod}	---	---	1.02*Fc	MHz	
	Spread spectrum modulation frequency	F_{SSM}	---	---	200	KHz	(2)
	High Time	T_{ch}	---	4/7	---	Tc	
	Low Time	T_{cl}	---	3/7	---	Tc	
LVDS data	Setup Time	T_{lvs}	600	---	---	ps	(3)
	Hold Time	T_{lvh}	600	---	---	ps	
Vertical Display Term	Frame Rate	Fr	--	50	---	Hz	
	Total	T_v	2075	2076	2134	Th	$T_v=T_{vd}+T_{vb}$
	Active Display	T_{vd}	2064	2064	2064	Th	
	Sensor Line/frame	K	---	16	---	Th	
	Blank	T_{vb}	T_v-T_{vd}	12	T_v-T_{vd}	Th	
Horizontal Display Term	Total	T_h	703	712	732	Tc	$T_h=T_{hd}+T_{hb}$
	Active Display	T_{hd}	640	640	640	Tc	
	Blank	T_{hb}	T_h-T_{hd}	72	T_h-T_{hd}	Tc	

Note: This module is operated by DE only mode.

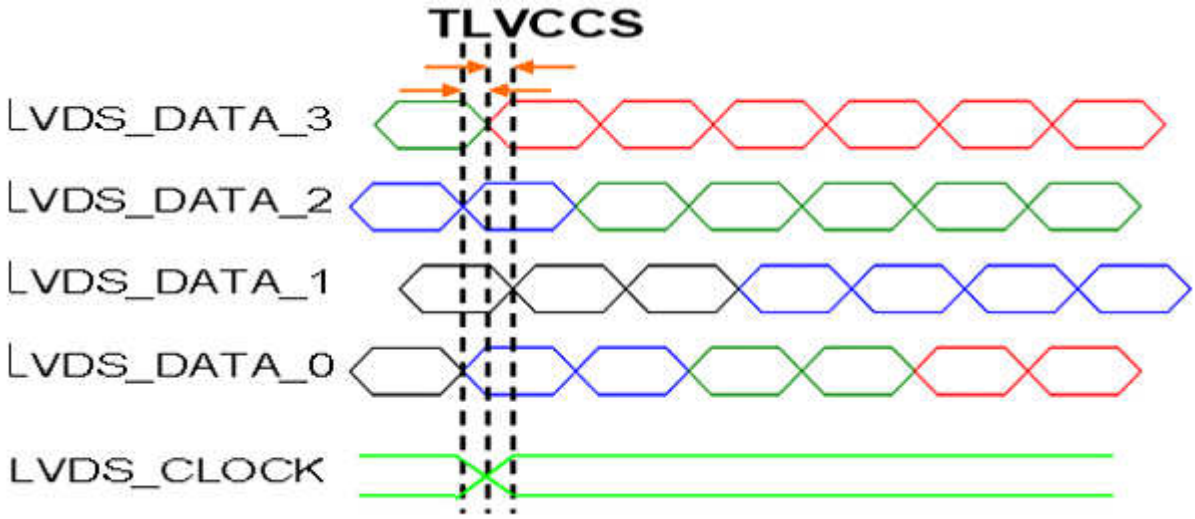
INPUT SIGNAL TIMING DIAGRAM



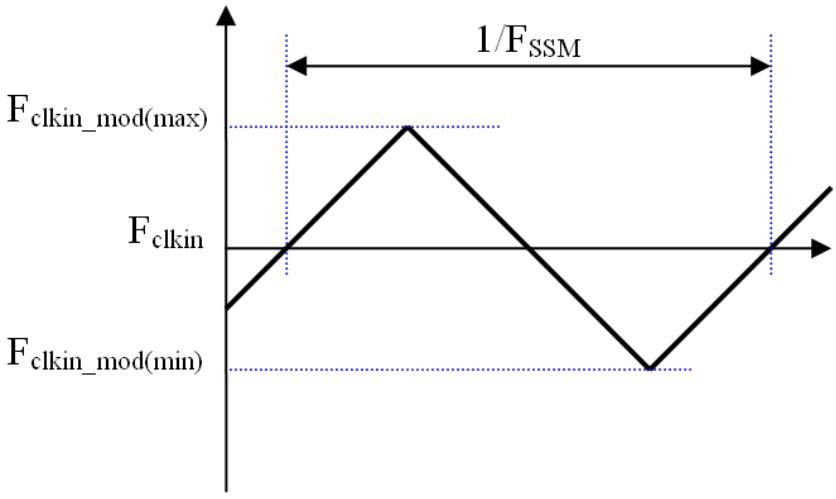
Note (1) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI



Note (2) Input Clock to data skew is defined as below figures.

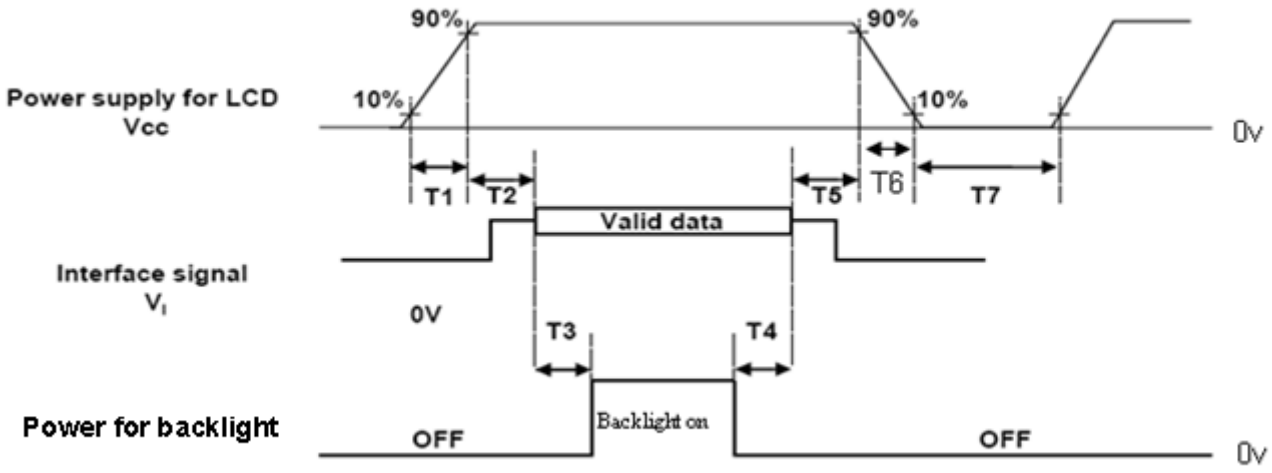


Note (3) The SSCG (Spread spectrum clock generator) is defined as below figures.



4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.



Timing Specifications:

Parameters	Values			Units
	Min	Typ.	Max	
T1	0.5	-	10	ms
T2	0	-	50	ms
T3	450	-	-	ms
T4	90	-	-	ms
T5	0	-	50	ms
T6	5	-	100	ms
T7	500	-	-	ms

Note.

(1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.

(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation of the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case of V_{CC} = off level, please keep the level of input signals on the low or keep a high impedance.

(4) T7 should be measured after the module has been fully discharged between power of and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

(6) It is not guaranteed that products are damaged which is caused by not following the Power Sequence.

(7) It is suggested that Vcc falling time follows T6 specification; else slight noise is likely to occur when LCD is turned off (even backlight is already off).

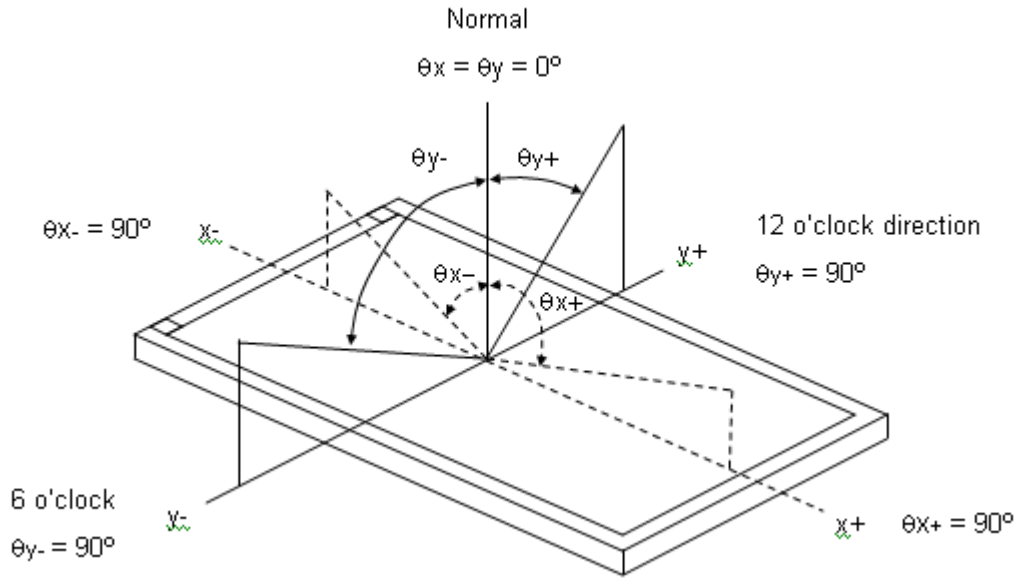
5. OPTICAL CHARACTERISTICS

5.1 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 5.1. The following items should be measured under the test conditions described in 5.1 and stable environment shown in Note (5).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
White Balance	White	W_x	θ_x=0°, θ_Y =0° CS-2000	Typ – 0.03	0.294	Typ+ 0.03		(1), (5)
		W_y			0.309			
Center Luminance of White		L_C		850	1100	---	cd/m^2	(4), (5)
Contrast Ratio		CR		670	850	---	-	(2), (5)
Response Time		T_R	θ_x=0°, θ_Y =0°	---	18	20	ms	(3)
		T_F		---	18	20	ms	
White Variation(adjacent)		δW_a	θ_x=0°, θ_Y =0° USB2000	80	---	---	-	(5), (6)
White Variation(total)		δW_t	θ_x=0°, θ_Y =0° USB2000	70	---	---	-	(5), (6)
Viewing Angle		In all azimuth	CR ≧ 20 USB2000	80	85	-	Deg.	(1), (5)

Note (1)Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

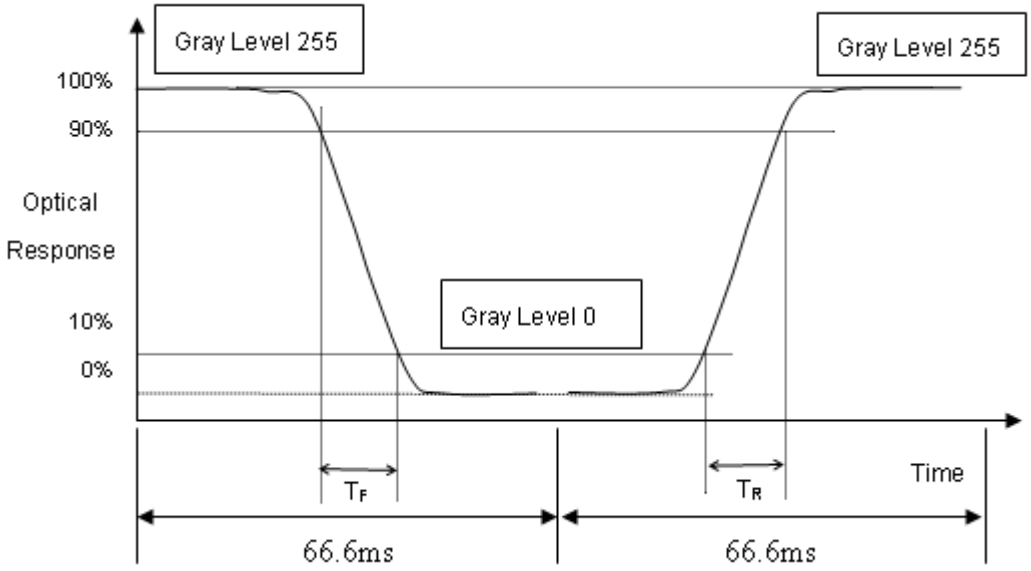
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (4).

Note (3) Definition of Response Time (T_R, T_F):

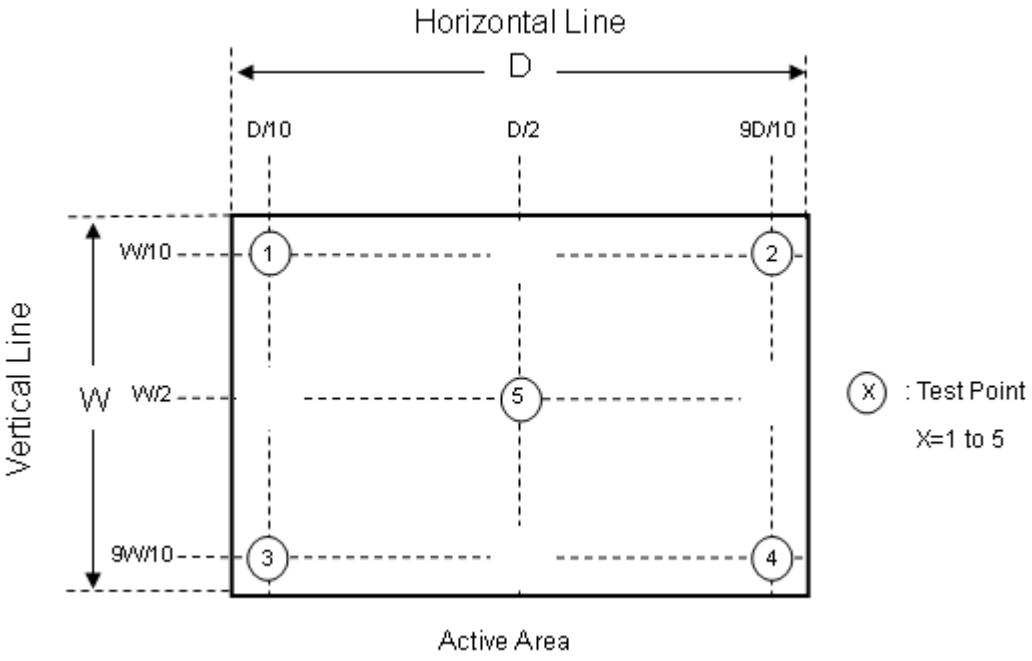


Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point

L_C = L (5)

L (x) is corresponding to the luminance of the point X at the following figure.



Note (5) Measurement Setup:

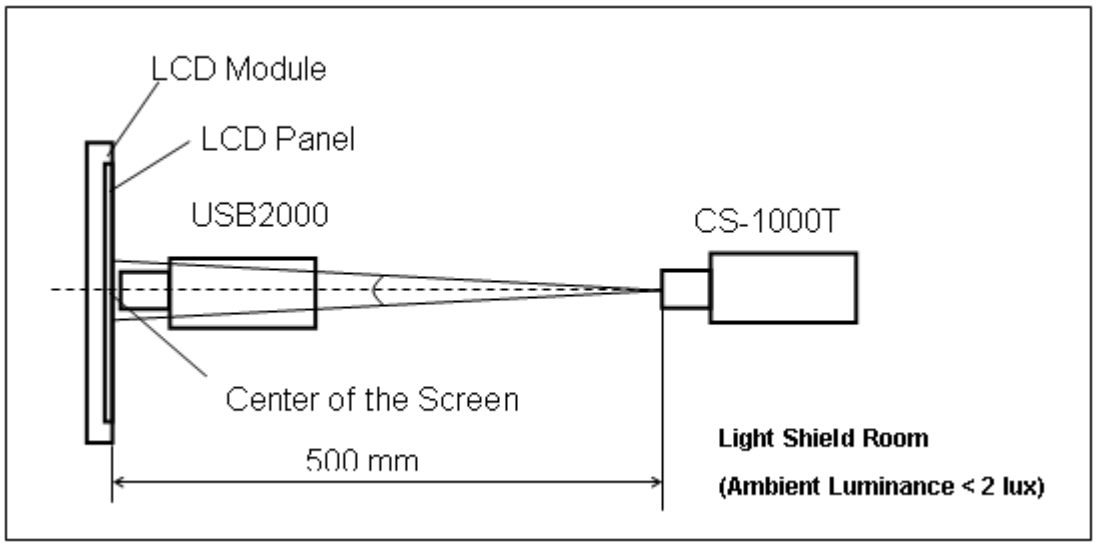
The LCD module should be stabilized at given temperature for 60 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 60 minutes in a windless room.

Unless otherwise specified, the ambient conditions are as following.

Ambient Temperature: 25 ± 2 (degreeC)

Ambient Humidity: 25 ~ 85 (%)

Atmospheric Pressure: 86.0 ~ 104.0 (kP_a)

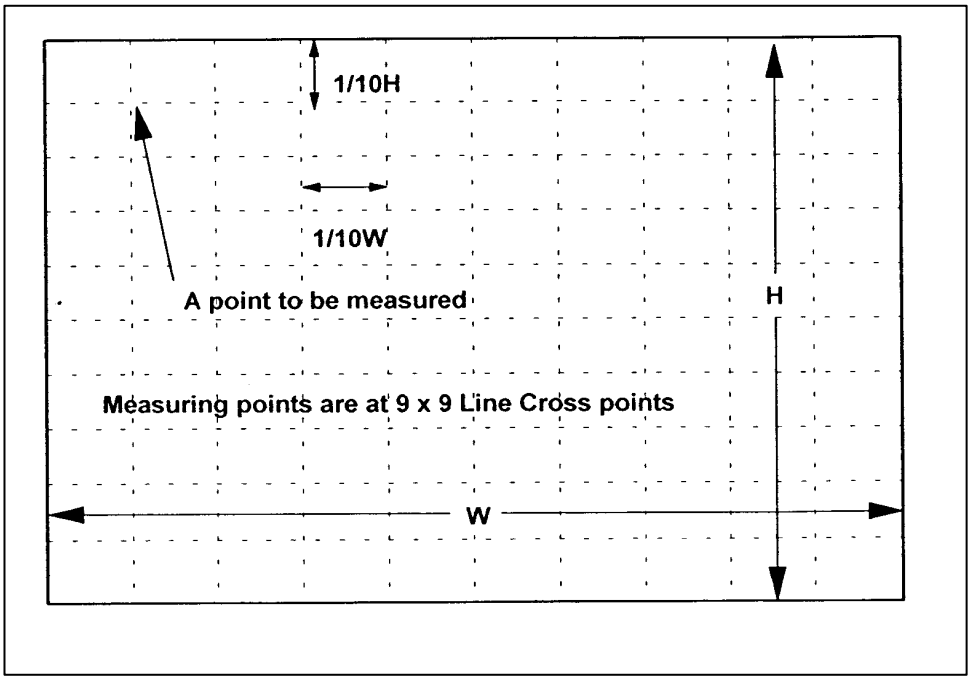


Note (6) There is the Uniformity Measurement below:

'L_{bright} ' represents the Luminance of the point that is brighter than the other point to be compared.

'L_{dark} ' represents the Luminance of the point that is darker than the other point to be compared.

Measuring points are shown in the following Fig.



When the backlight is on with all pixels in the white (maximum gray) level, the luminance uniformity is defined as follows;

Where:

L_{bright}: The luminance of the brightness part of the area

L_{dark}: The luminance of the darkest part of the area

1. Adjacent Area

$$\text{Luminance Uniformity} = \frac{L_{dark}}{L_{bright}} \geqq 0.80$$

over a circular area of 10mm diameter placed anywhere on the screen.

2. Screen Total

$$\text{Luminance Uniformity} = \frac{L_{dark}}{L_{bright}} \geqq 0.70$$

over the entire screen.

6. RELIABILITY TEST ITEM

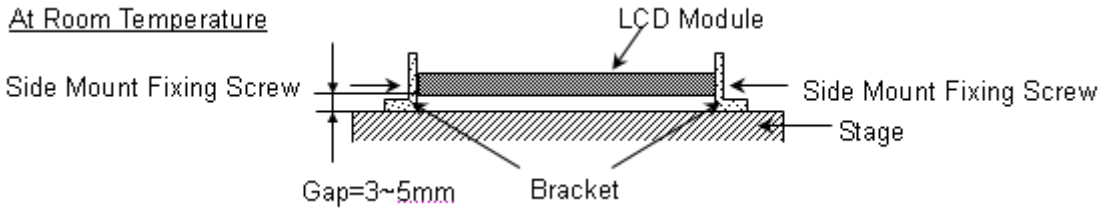
Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50℃ , 80%RH, 240hours	
High Temperature Operation (HTO)	Ta= 50℃ , 240hours	
Low Temperature Operation (LTO)	Ta= 0℃ , 240hours	
High Temperature Storage (HTS)	Ta= 60℃ , 240hours	
Low Temperature Storage (LTS)	Ta= -20℃ , 240hours	
Vibration Test (Non-operation)	Acceleration: 1.5 G_{rms} Wave: Half-sine Frequency: 10 - 300 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 11 ms Direction : ± X, ± Y, ± Z.(one time for each Axis)	
Thermal Shock Test (TST)	-20℃/30min , 60℃ / 30min , 100 cycles	
ESD (Electro Static Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω)	
	Air Discharge: ± 15KV, 150pF(330Ω)	

Note (1) criteria: Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:



7. PACKING

7.1 PACKING SPECIFICATIONS

(1) 4 LCD modules / 1 Box

(2) Box dimensions: 590(L) X 396(W) X 505(H) mm

(3) Weight: approximately: 14.08kg (4 modules per box)

7.2 PACKING METHOD

(1) Carton Packing should have no failure in the following reliability test items.

Test Item	Test Conditions	Note
Vibration	ISTA STANDARD Random, Frequency Range: 1 – 200 Hz Top & Bottom: 30 minutes (+Z), 10 min (-Z), Right & Left: 10 minutes (X) Back & Forth 10 minutes (Y)	Non Operation
Dropping Test	1 Corner , 3 Edge, 6 Face, 60cm	Non Operation

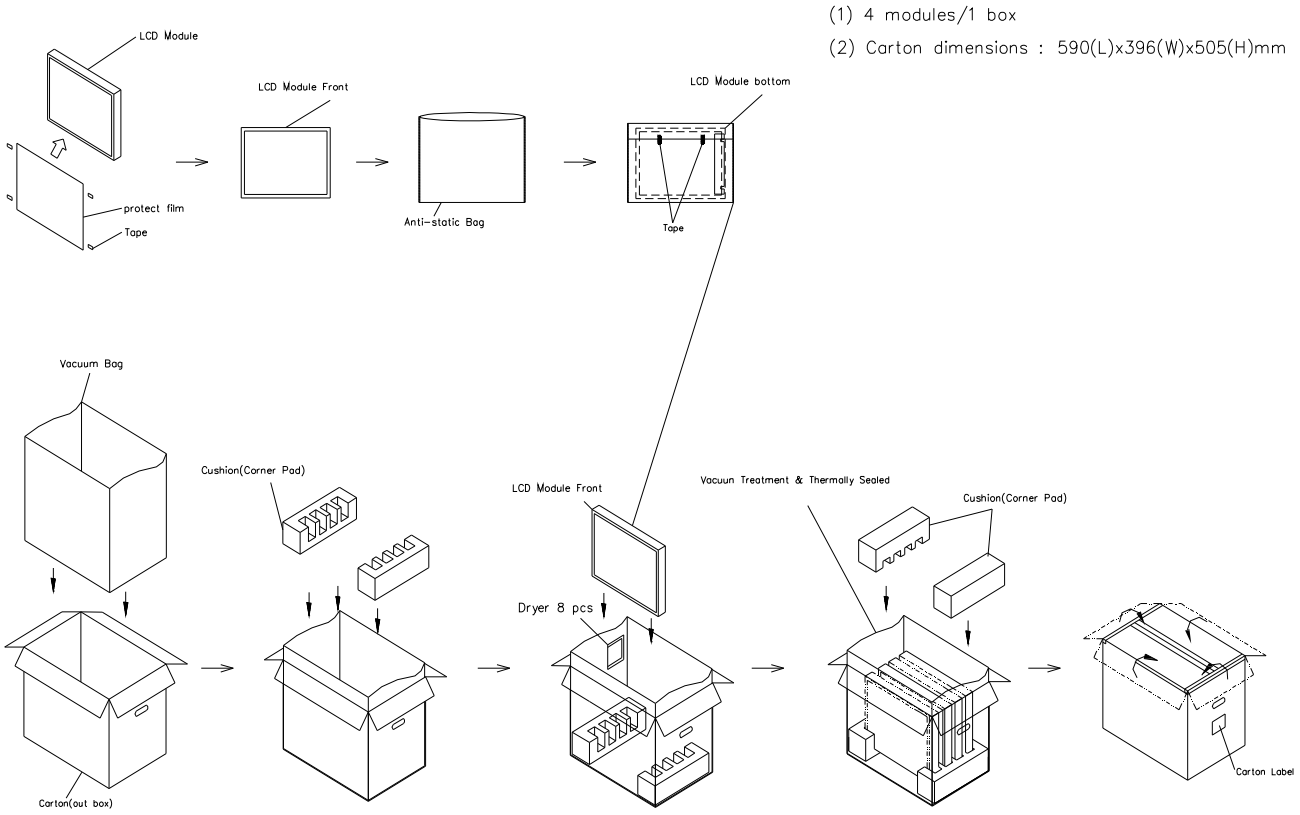


Figure. 7-1 Packing method

7.3 PALLET

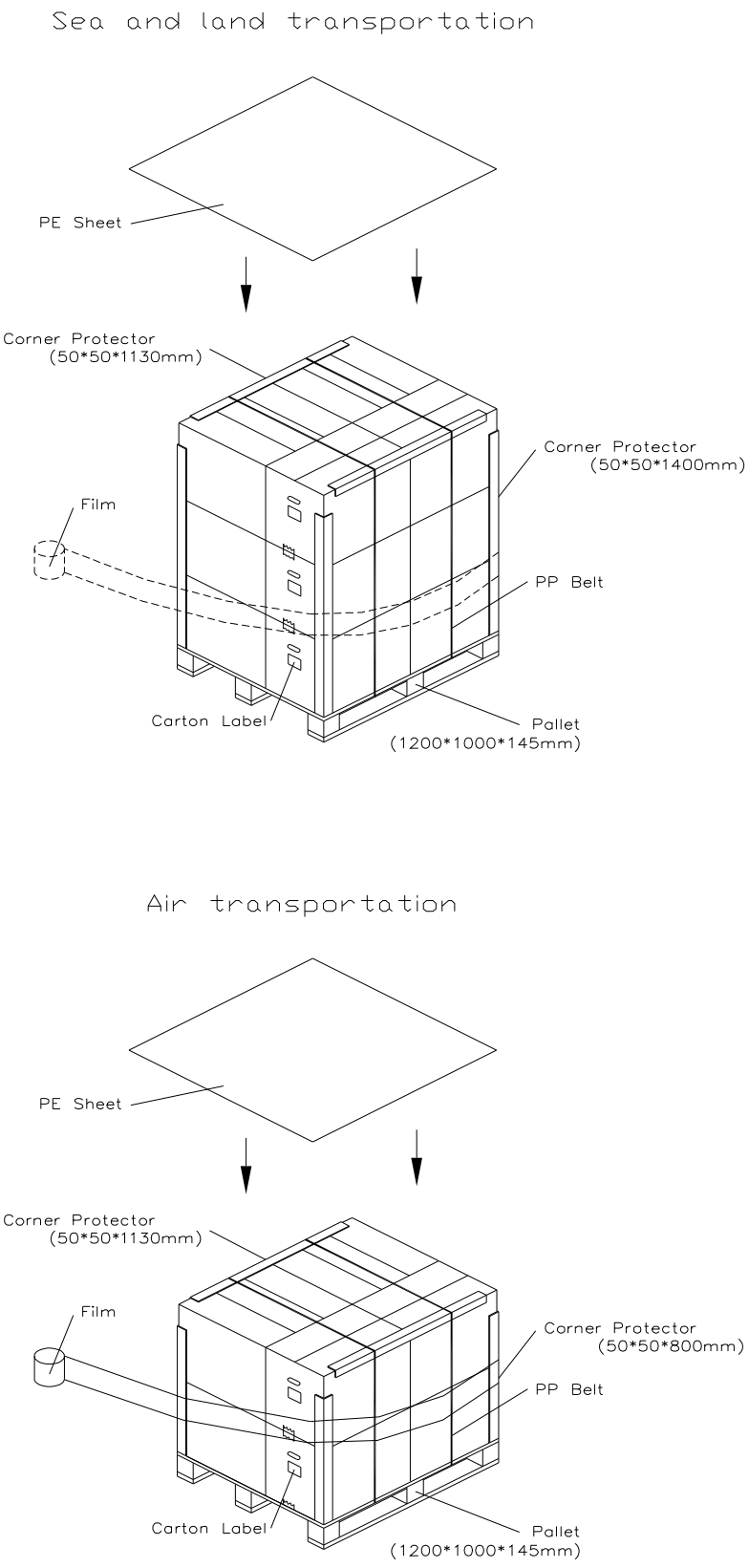
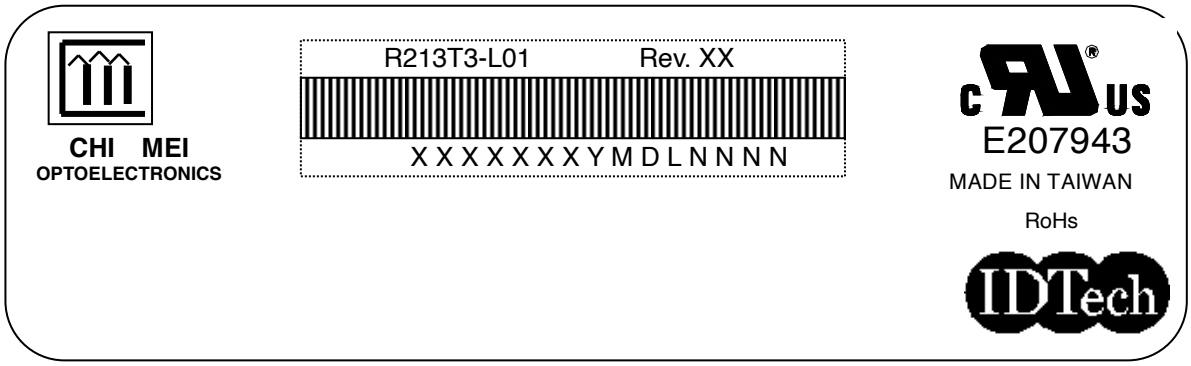


Figure. 7-2 Packing method

8. CMI MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: R213T3-L01

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) CMI barcode definition:

Serial ID: XX-XX-X-XX-YMD-L-NNNN

Code	Meaning	Description
XX	CMI internal use	-
XX	Revision	Cover all the change
X	CMI internal use	-
XX	CMI internal use	-
YMD	Year, month, day	Year: 0~9, 2001=1, 2002=2, 2003=3…2010=0, 2011=1, 2012=2… Month: 1~12=1, 2, 3, ~, 9, A, B, C Day: 1~31=1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U.
L	Product line #	Line 1=1, Line 2=2, Line 3=3, …
NNNN	Serial number	Manufacturing sequence of product

9. PRECAUTIONS

9.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.

(4) Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.

(5) Do not pull the I/F connector in or out while the module is operating.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.

(9) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(10)When ambient temperature is lower than 10ºC may reduce the display quality. For example, the response time will become slowly.

9.2 STORAGE PRECAUTIONS

(1) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0℃ to 35℃ and relative humidity of less than 70%

(2) Do not store the TFT – LCD module in direct sunlight

(3) The module should be stored in dark place. It is prohibited to apply sunlight or fluorescent light in storing

9.3 OPERATION PRECAUTIONS

(1) The LCD product should be operated under normal condition.

Normal condition is defined as below :

Temperature : 20±15℃

Humidity: 65±20%

Display pattern: continually changing pattern (Not stationary)

(2) If the product will be used in extreme conditions such as high temperature, high humidity, high altitude ,display pattern or operation time etc…It is strongly recommended to contact CMO for application engineering advice . Otherwise, Its reliability and function may not be guaranteed.

9.4 SAFETY PRECAUTIONS

(1) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(2) After the module's end of life, it is not harmful in case of normal operation and storage.

9.5 SAFETY STANDARDS

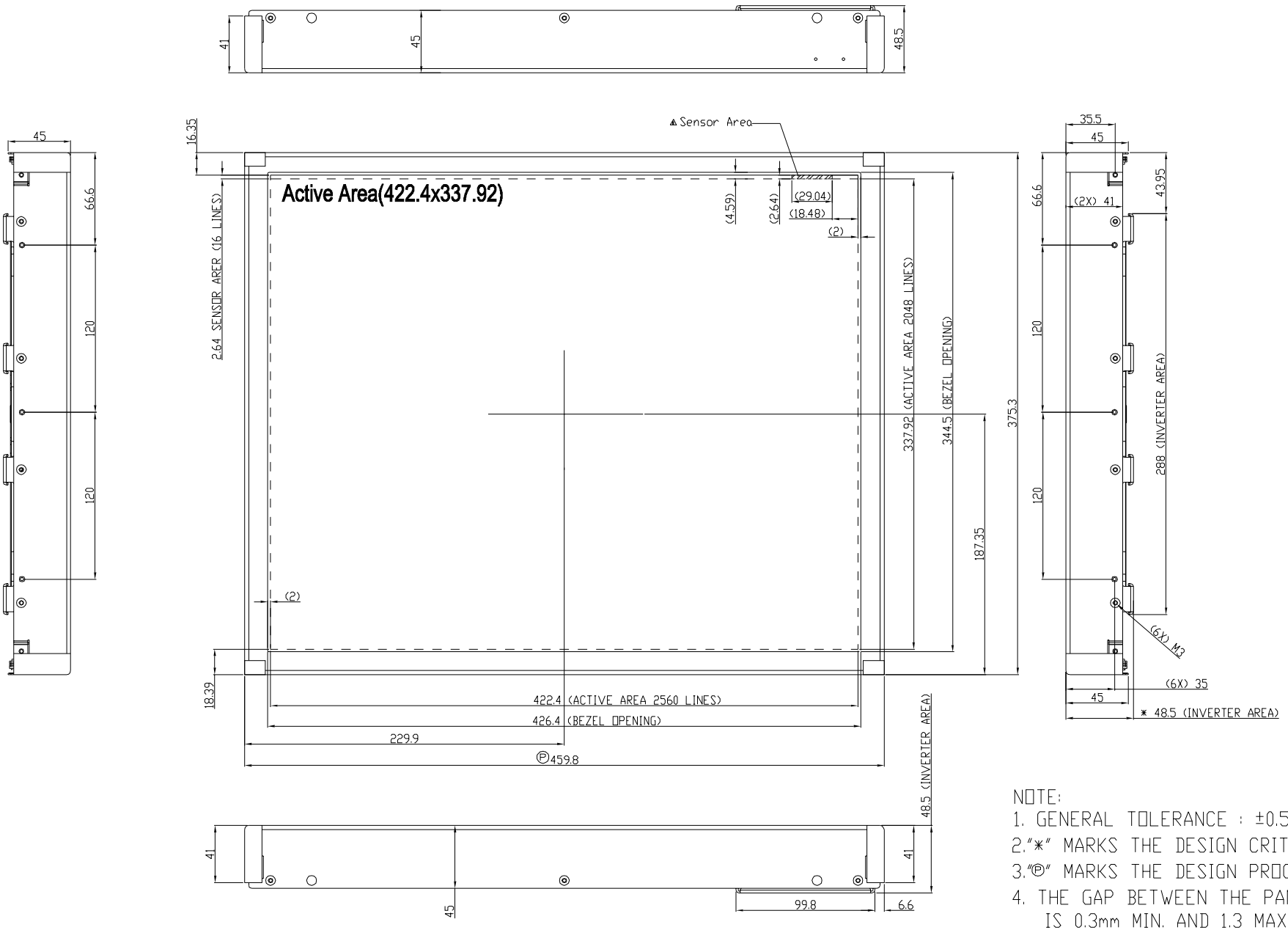
The LCD module should be certified with safety regulations as follows:

(1) UL60950-1 or updated standard.

(2) IEC60950-1 or updated standard.

9.6 OTHER

When fixed patterns are displayed for a long time, remnant image is likely to occur.



NOTE:

1. GENERAL TOLERANCE : ±0.5mm
2. "*" MARKS THE DESIGN CRITICAL DIMENSION.
3. "Ⓟ" MARKS THE DESIGN PROCESS DIMENSION.
4. THE GAP BETWEEN THE PANEL AND THE BEZEL IS 0.3mm MIN. AND 1.3 MAX.

Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark
A	Modify Title and Add Sensor Area Position	2011.03.22	ML.Hsieh	CK.Hung	--	

General Tolerance Unless Specified					
0~3	±0.05	30~120	±0.15	1000~2000	±0.5
3~6	±0.05	120~400	±0.2	2000~4000	--
6~30	±0.1	400~1000	±0.3	VERTICAL ANGLE	4°
				BEND ANGLE	2.5°

TITLE	ASSY_MODULE_R2137.1-L01/L02 A		00 REV:B1 01 REV:N/A
Approved	CK.Hung	Drawing No.	MD12410318
Checked	Fergit.Yang	Part No.	TBD
Drawn	ML.Hsieh	Material	TBD
Designer	CJW1813	Date	22-Mar-2011
		Scale	1:1
		Unit	mm
		Sheet	1 / 2

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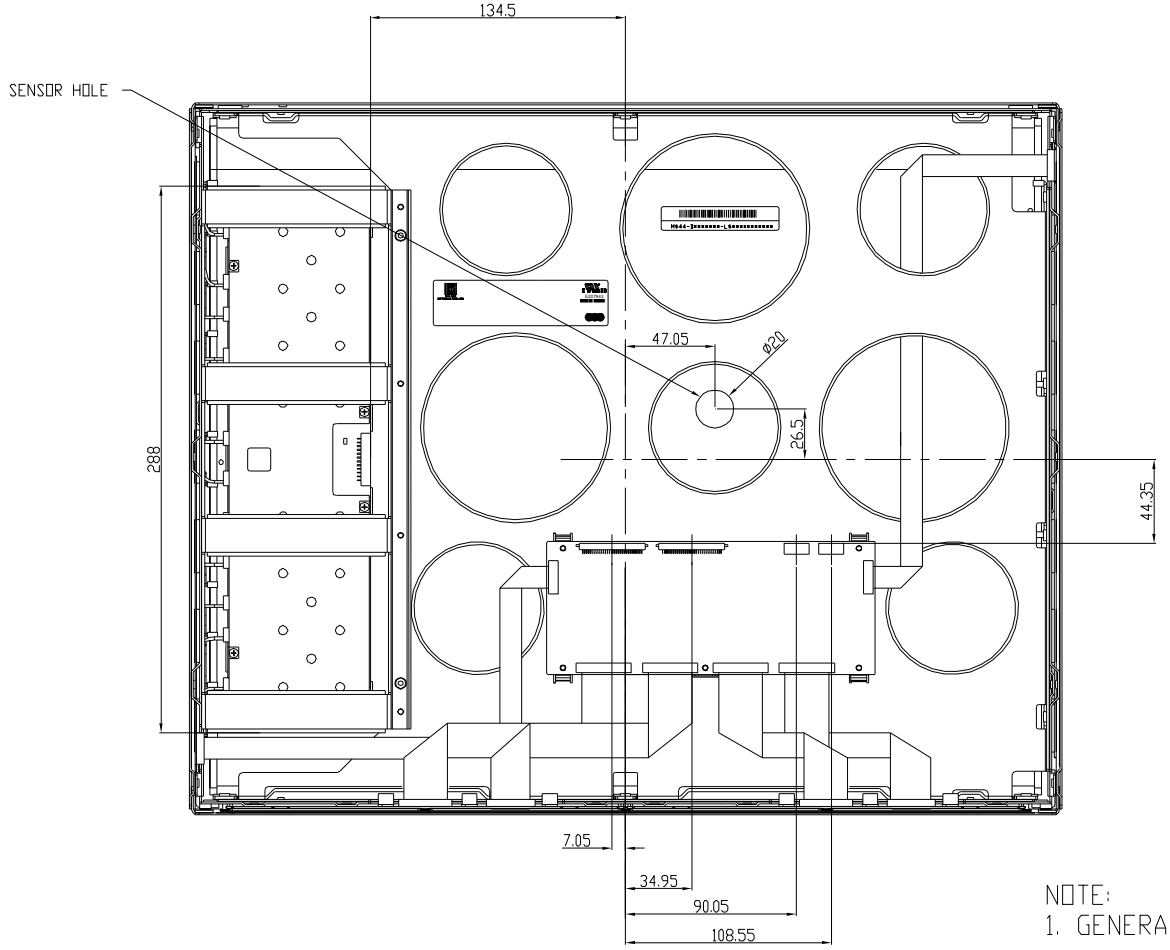

NOTE:
1. GENERAL TOLERANCE : ±0.5mm
2."*" MARKS THE DESIGN CRITICAL DIMENSION.
3."Ⓟ" MARKS THE DESIGN PROCESS DIMENSION.
4. THE GAP BETWEEN THE PANEL AND THE BEZEL IS 0.3mm MIN. AND 1.3 MAX.

Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark
⚠	Modify Title and Add Sensor Area Position	2011.03.22	ML.Hsieh	CK.Hung	--	

General Tolerance Unless Specified					
0~3	±0.05	30~120	±0.15	1000~2000	±0.5
3~6	±0.05	120~400	±0.2	2000~4000	--
6~30	±0.1	400~1000	±0.3	VERTICAL ANGLE	45°
				BEND ANGLE	22.5°

TITLE	ASSY_MODULE_R21373-LB1/LB2 ⚠		00 REV:B1 01 REV:N/A
Approved	CK.Hung	Drawing No.	MD1341038
Checked	Fergit.tang	Part No.	TBD
Drawer	ML.Hsieh	Material	TBD
Designer	CJW1813	Date	22-Mar-2011
		Scale	1:1
		Sheet	2 / 2
		Version	

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