

TFT LCD Tentative Specification

MODEL NO.: N133I5 - L01

Customer: Dell

Approved by:

Note:

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
0.0	Jan, 22,'07	All	All	Tentative specification was first issued.

1 GENERAL DESCRIPTION

1.1 OVERVIEW

N133I5 - L01 is a 13.3" TFT Liquid Crystal Display module with LED Backlight unit and 40 pins LVDS interface. This module supports 1280 x 800 WXGA mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction. The converter module for Backlight is built in.

1.2 FEATURES

- Thin and Light Weight
- WXGA (1280 x 800 pixels) resolution
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 1 pixel/clock
- RoHS compliance

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	286.08 (H) x 178.8 (V)	mm	(1)
Bezel Opening Area	289.48 (H) x 182.2 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1280 x R.G.B. x 800	pixel	-
Pixel Pitch	0.2235 (H) x 0.2235 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Glare, 3H	-	-

1.5 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note	
Module Size	Horizontal(H)	303.50	304.00	304.50	mm	(1)
	Vertical(V)	202.00	202.50	203.00	mm	
	Depth(D)	---	---	2.97	mm	
Weight	---	235	245	g	(2)	
Weight				g	(3)	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions

(2) Weight without inverter

(3) Weight with inverter.

2 ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)
Shock (Non-Operating)	S _{NOP}	-	200/2	G	(3), (5)
Vibration (Non-Operating)	V _{NOP}	-	1.5	G	(4), (5)

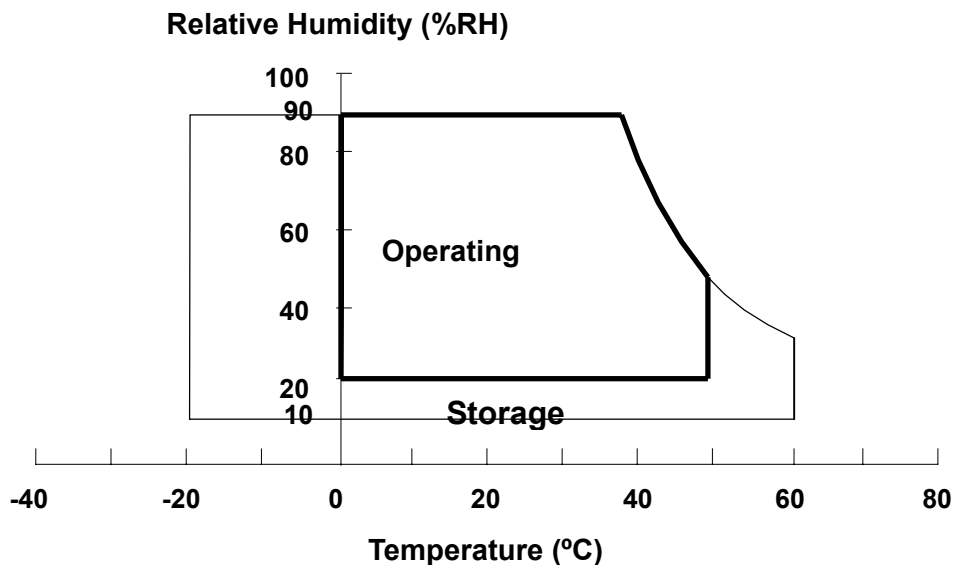
Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. ($T_a \leq 40$ °C).

(b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40$ °C).

(c) No condensation.

Note (2) The ambient temperature means the temperature of panel surface.

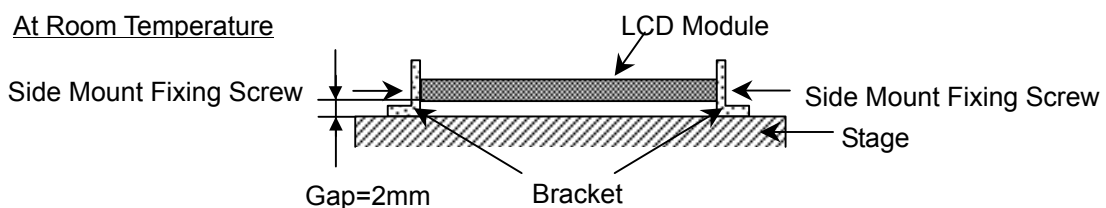


Note (3) 1 time for $\pm X$, $\pm Y$, $\pm Z$. for Condition (200G / 2ms) is half Sine Wave,

Note (4) 10 ~ 500 Hz, 30 min / Cycle, 1 cycles for each X, Y, Z axis.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V _{CC}	-0.3	+4.0	V	(1)
Logic Input Voltage	V _{IN}	-0.3	V _{CC} +0.3	V	

2.2.2 BACKLIGHT UNIT

Item	Value		Unit	Note
	Min	Max.		
LED Light Bar Input Current	(22.4)	(29.6)	V _{RMS}	(1), (2)
LED Light Bar Input Current	(115.5)	(150)	mA _{RMS}	
LED Peak Pulse Current	-	(100)	mA _{RMS}	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to Section 3.2 for further information).

3 ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Ta = 25 ± 2 °C

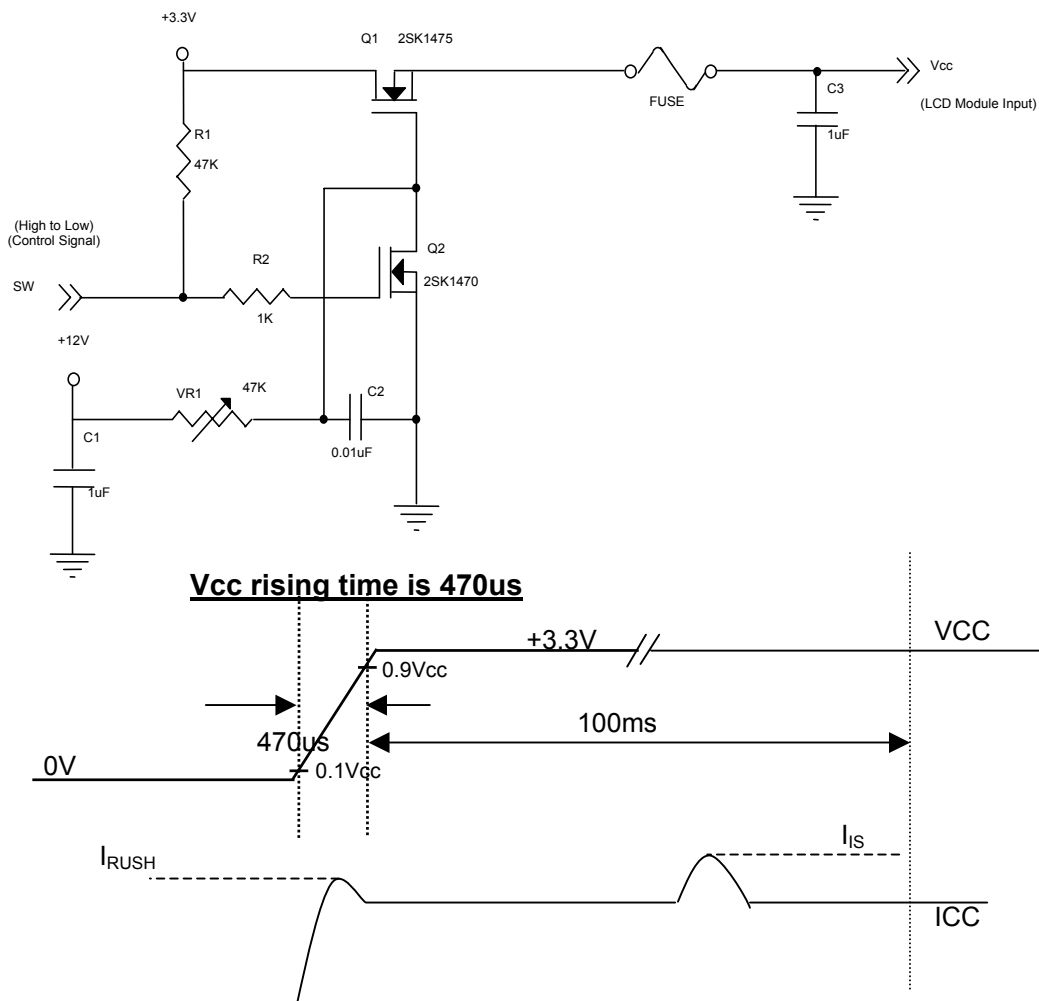
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage	V _{CC}	3.0	3.3	3.6	V	-
Permissible Ripple Voltage	V _{RP}		50		mV	-
Rush Current	I _{RUSH}			1.5	A	(2)
Initial Stage Current	I _{IS}			1.0	A	(2)
Power Supply Current	White	I _{CC}	(364)	(400)	mA	(3)a
	Black		(424)	(460)		
LVDS Differential Input High Threshold	V _{TH(LVDS)}			+100	mV	(5), V _{CM} =1.2V
LVDS Differential Input Low Threshold	V _{TL(LVDS)}	-100			mV	(5) V _{CM} =1.2V
LVDS Common Mode Voltage	V _{CM}	1.125		1.375	V	(5)
LVDS Differential Input Voltage	V _{ID}	100		600	mV	(5)
Terminating Resistor	R _T		100		Ohm	
Power per EBL WG	P _{EBL}	-	TBD	-	W	(4)

Note (1) The ambient temperature is Ta = 25 ± 2 °C.

Note (2) I_{RUSH}: the maximum current when VCC is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black



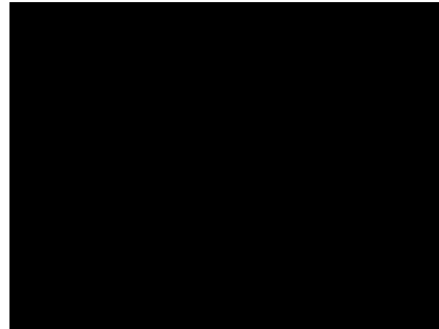
Note (3) The specified power supply current is under the conditions at $V_{CC} = 3.3 \text{ V}$, $T_a = 25 \pm 2 \text{ }^\circ\text{C}$, DC Current and $f_v = 60 \text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



Active Area

b. Black Pattern

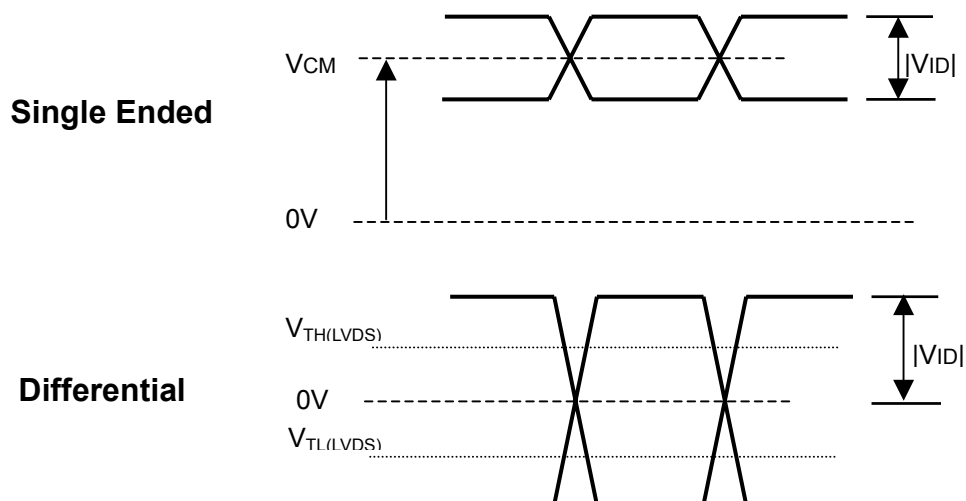


Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.

- $V_{CC} = 3.3 \text{ V}$, $T_a = 25 \pm 2 \text{ }^\circ\text{C}$, $f_v = 60 \text{ Hz}$,
- The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.
- Luminance: 60 nits.
- The inverter used is provided from Sumida. Please contact them for detail information. CMO doesn't provide the inverter in this product.

Note (5) The parameters of LVDS signals are defined as the following figures.

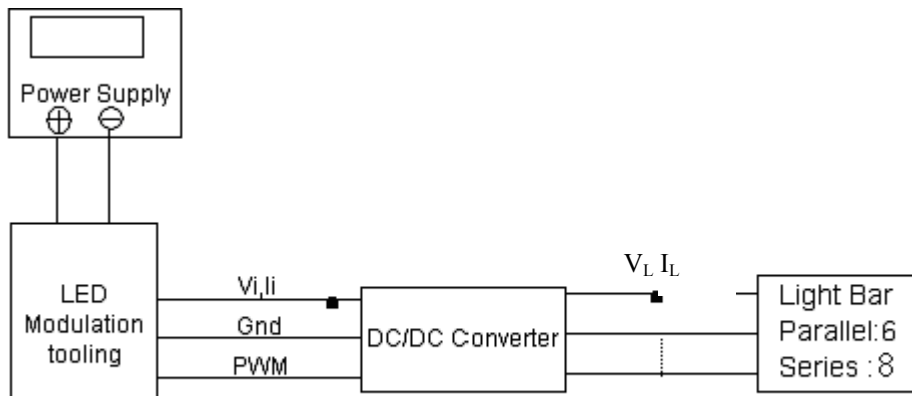


3.2 BACKLIGHT UNIT

Ta = 25 ± 2 °C

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED light bar input voltage	V _L	(22.4)	(26.4)	(29.6)	V _{RMS}	(1), (Duty 100%)
LED light bar input current	I _L	(115.5)	(120)	(150)	mA _{RMS}	(1), (Duty 100%)
LED Current Peak	I _f	-	-	(100)	mA _{RMS}	Per EA
Power Consumption	P _L	(2.59)	(3.17)	(4.44)	W	(2), I _L = 120 mA
LED Life Time	L _{BL}	(10000)	-	-	Hrs	(3)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below:

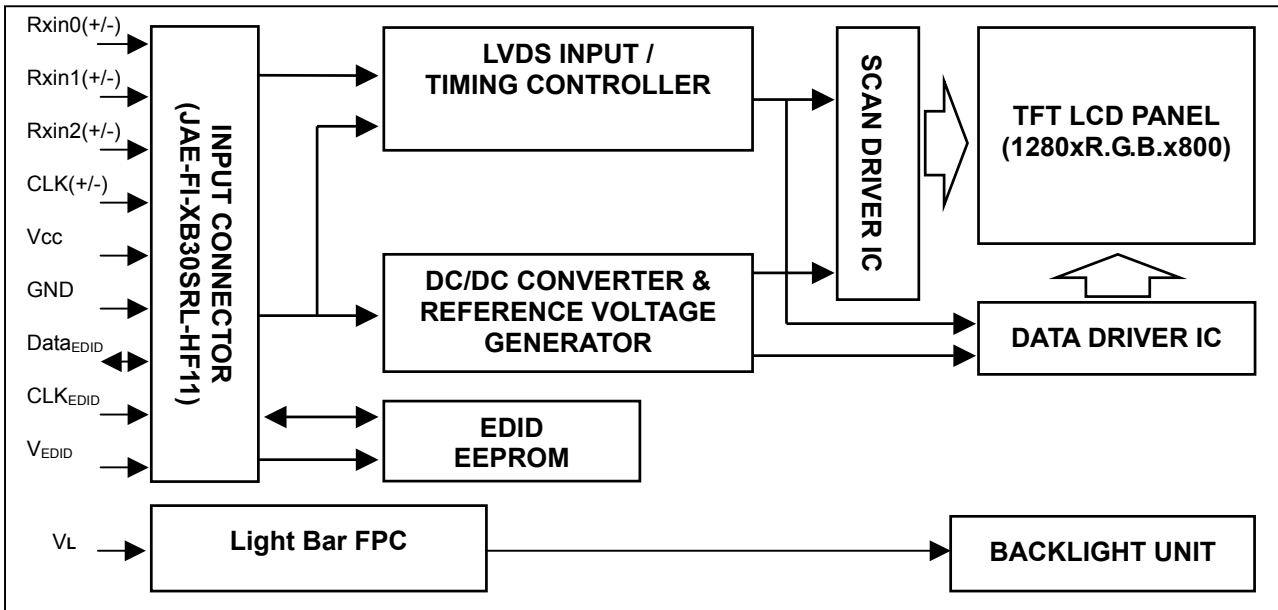


Note (2) $P_L = I_L \times V_L$

Note (3) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ± 2 °C and I = 20 mA(Per EA) until one of the following events occurs:

- (a) When the brightness becomes $\leq 50\%$ of its original value.

4 BLOCK DIAGRAM
4.1 TFT LCD MODULE



5 INPUT TERMINAL PIN ASSIGNMENT

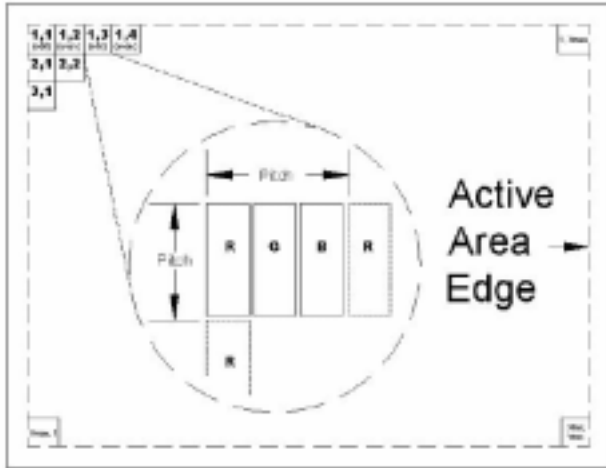
5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	VSS	Ground		
2	CONNTST	Connector test		
3	VDD	Logic power 3.3V (Panel logic, BL logic)		
4	VDD	Logic power 3.3V (Panel logic, BL logic)		
5	VDD	Logic power 3.3V (Panel logic, BL logic)		
6	VEDID	EDID 3.3V power		DDC 3.3V Power
7	TEST	Panel Self Test		
8	CLK	EDID clock		DDC Clock
9	DATA	EDID data		DDC Data
10	VSS	Ground (Panel logic, BL logic)		
11	VSS	Ground (Panel logic, BL logic)		
12	NC	no connect		
13	RIN0-	- LVDS differential data input (R0-R5, G0)	Negative	R0~R5, G0
14	RIN0+	+ LVDS differential data input (R0-R5, G0)	Positive	
15	VSS0	Ground-LVDS0		
16	RIN1-	- LVDS differential data input (G1-G5, B0-B1)	Negative	G1~G5, B0, B1
17	RIN1+	+ LVDS differential data input (G1-G5, B0-B1)	Positive	
18	VSS1	Ground-LVDS1		
19	RIN2-	- LVDS differential data input (B2-B5, HS, VS, DE)	Negative	B2~B5, DE, Hsync, Vsync
20	RIN2+	+ LVDS differential data input (B2-B5, HS, VS, DE)	Positive	
21	VSS2	Ground-LVDS2		
22	CLK-	- LVDS differential clock input		LVDS Level Clock
23	CLK+	+ LVDS differential clock input		
24	VSS3	Ground-LVDS3		
25	INV_PWM / R_PWM	PWM brightness control / Red PWM		
26	VSS	LED Ground		
27	VSS	LED Ground		
28	VSS	LED Ground		
29	VSS	LED Ground		
30	VSS	LED Ground		
31	NC	no connect		
32	VBL+	7V - 20V LED power		
33	VBL+	7V - 20V LED power		
34	VBL+	7V - 20V LED power		
35	VBL+	7V - 20V LED power		
36	VBL+	7V - 20V LED power		
37	CONNTST	Connector test		
38	Reserved	Green PWM / etc. (SMBus Clk for Dell)		
39	Reserved	Blue PWM / etc. (SMBus Data for Dell)		
40	VSS	Ground		

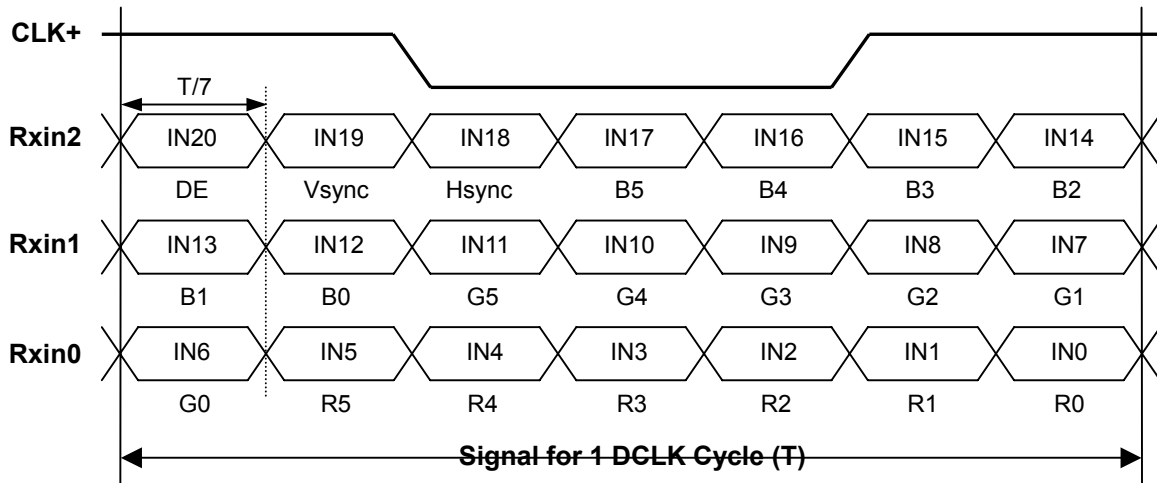
Note (1) Connector Part No.: 20347-040E-20 or equivalent

Note (2) User's connector Part No: 20345-*40T or equivalent

Note (3) The first pixel is odd as shown in the following figure.



5.2 TIMING DIAGRAM OF LVDS INPUT SIGNAL



5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.4 EDID DATA STRUCTURE(EDID 未完成確認)

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPD/ standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name ("CMO")	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AF	10101111
10	0A	ID product code (N141I3-L05)	26	00100110
11	0B	ID product code (hex LSB first; N141I3-L05)	14	00010100
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed week code)	0C	00001100
17	11	Year of manufacture (fixed year code)	11	00010001
18	12	EDID structure version # ("1")	01	00000001
19	13	EDID revision # ("3")	03	00000011
20	14	Video I/P definition ("digital")	80	10000000
21	15	Active area horizontal 30.336cm	1E	00011110
22	16	Active area vertical 18.96cm	13	00010011
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("Active off, RGB Color")	0A	00001010
25	19	Rx1 Rx0 Ry1 Ry0 Gx1 Gx0 Gy1 Gy0	9F	10011111
26	1A	Bx1 Bx0 By1 By0 Wx1 Wx0 Wy1 Wy0	05	00000101
27	1B	Red-x (Rx = "0.588")	96	10010110
28	1C	Red-y (Ry = "0.337")	56	01010110
29	1D	Green-x (Gx = "0.315")	50	01010000
30	1E	Green-y (Gy = "0.534")	88	10001000
31	1F	Blue-x (Bx = "0.152")	27	00100111
32	20	Blue-y (By = "0.125")	20	00100000
33	21	White-x (Wx = "0.313")	50	01010000
34	22	White-y (Wy = "0.329")	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

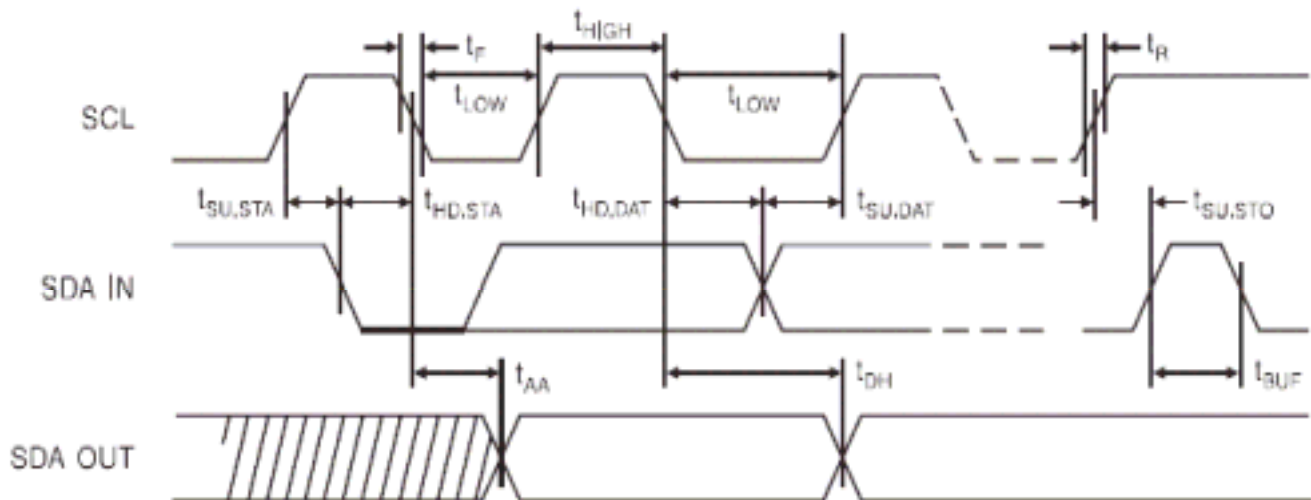
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("71MHz", According to VESA CVT Rev1.1)	BC	10111100
55	37	# 1 Pixel clock (hex LSB first)	1B	00011011
56	38	# 1 H active ("1280")	00	00000000
57	39	# 1 H blank ("160")	A0	10100000
58	3A	# 1 H active : H blank ("1280 : 160")	50	01010000
59	3B	# 1 V active ("800")	20	00100000
60	3C	# 1 V blank ("23")	17	00010111
61	3D	# 1 V active : V blank ("800 : 23")	30	00110000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("3 : 6")	36	00110110
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 3 : 6")	00	00000000
66	42	# 1 H image size ("303 mm")	2F	00101111
67	43	# 1 V image size ("190 mm")	BE	10111110
68	44	# 1 H image size : V image size ("303 : 190")	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
72	48	Detailed timing description # 2 Pixel clock ("58.75 MHz", According to VESA CVT Rev1.1)	F3	11110011
73	49	# 2 Pixel clock (hex LSB first)	16	00010110
74	4A	# 2 H active ("1280")	00	00000000
75	4B	# 2 H blank ("160")	A0	10100000
76	4C	# 2 H active : H blank ("1280 : 160")	50	01010000
77	4D	# 2 V active ("800")	20	00100000
78	4E	# 2 V blank ("19")	13	00010011
79	4F	# 2 V active : V blank ("800 : 19")	30	00110000
80	50	# 2 H sync offset ("48")	30	00110000
81	51	# 2 H sync pulse width ("32")	20	00100000
82	52	# 2 V sync offset : V sync pulse width ("3 : 6")	36	00110110
83	53	# 2 H sync offset : H sync pulse width : V sync offset : V sync width ("48 : 32 : 3 : 6")	00	00000000
84	54	# 2 H image size ("303 mm")	2F	00101111
85	55	# 2 V image size ("190 mm")	BE	10111110

86	56	# 2 H image size : V image size ("303 : 190")	10	00010000
87	57	# 2 H boarder ("0")	00	00000000
88	58	# 2 V boarder ("0")	00	00000000
89	59	Module "A" Revision = Example: 00, 01, 02, 03, etc.	00	00000000
90	5A	Detailed timing description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 FE (hex) defines ASCII string (Model Name "N141I3-L05", ASCII)	FE	11111110
94	5E	# 3 Flag	00	00000000
95	5F	# Dell P/N "GR551" 1st character ("G")	47	01000111
96	60	# Dell P/N " GR551" 1st character ("R")	52	01010010
97	61	# Dell P/N " GR551" 1st character ("5")	35	00110101
98	62	# Dell P/N " GR551" 1st character ("5")	35	00110101
99	63	# Dell P/N " GR551" 1st character ("1")	31	00110001
100	64	LCD Supplier EEDID Revision #: "1"	31	00110001
101	65	Manufacturer P/N ("N")	4E	01001110
102	66	Manufacturer P/N ("1")	31	00110001
103	67	Manufacturer P/N ("4")	34	00110100
104	68	Manufacturer P/N ("1")	31	00110001
105	69	Manufacturer P/N ("I")	49	01001001
106	6A	Manufacturer P/N ("3")	33	00110011
107	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000
110	6E	Flag	00	00000000
111	6F	Data Type Tag:	FE	11111110
112	70	Flag	00	00000000
113	71	SMBUS value @ 10nits = 31d	1F	00011111
114	72	SMBUS value @ 17nits = 43d	2B	00101011
115	73	SMBUS value @ 24nits = 52d	34	00110100
116	74	SMBUS value @ 30nits = 58d	3A	00111010
117	75	SMBUS value @ 60nits = 85d	55	01010101
118	76	SMBUS value @ 100nits = 111d	6F	01101111
119	77	SMBUS value @ 140nits = 139d	8B	10001011
120	78	SMBUS value @ 250 nits = 244d	F4	11110100
121	79	Numbers of LVDS Recevier chip = 1	01	00000001
122	7A	BIST Enable: Yes = '01' No = '00' ("Yes")	01	00000001
123	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
124	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
125	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	9F	10011111

5.5 EDID SIGNAL SPECIFICATION

(1) EDID Power

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc	—	1.8	—	5.5	V



(2) DC characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current Vcc=5.0V	Icc	READ at 100kHz	—	0.4	1.0	mA
Supply current Vcc=5.0V	Icc	WRITE at 100kHz	—	2.0	3.0	mA
Standby Current	ISB	Vin=Vcc or Vss	—	1.6	4.0	μ A
Input Leakage Current	ILI	Vin=Vcc or Vss	—	0.1	3.0	μ A
Output Leakage Current	ILO	Vout=Vcc or Vss	—	0.05	3.0	μ A
Input Low Level	VIL	—	-0.6	—	Vcc x 0.3	V
Input High Level	VIH	—	Vcc x 0.7	—	Vcc+0.5	V
Output Low Level Vcc=3.0V	VOL2	IOL=2.1mA	—	—	0.4	V
Output Low Level Vcc=1.8V	VOL1	IOL=0.15mA	—	—	0.2	V

(3) AC characteristics (VCC=1.8~5.5V standard operation mode)

Parameter	Symbol	Min	Max	Unit
Clock Frequency, SCL	F _{SCL}	—	400	kHz
Clock Pulse Width Low	T _{LOW}	1.2	—	μs
Clock Pulse Width High	T _{HIGH}	0.6	—	μs
Noise Suppression Time	T _I	—	50	ns
Clock Low to Data Out Valid	T _{AA}	0.1	0.9	μs
Time the bus must be free before a new transmission can start	T _{BUF}	1.2	—	μs
Start Hold Time	T _{HD.STA}	0.6	—	μs
Start Set-up Time	T _{SU.STA}	0.6	—	μs
Data in Hold Time	T _{HD.DAT}	0	—	μs
Data in Set-up Time	T _{SU.DAT}	100	—	ns
Inputs Rise Time	T _R	—	0.3	μs
Inputs Fall Time	T _F	—	300	ns
Stop Set-up Time	T _{SU.STO}	0.6	—	μs
Data Out Hold Time	T _{DH}	50	—	ns
Write Cycle Time	T _{WR}	—	5	ms

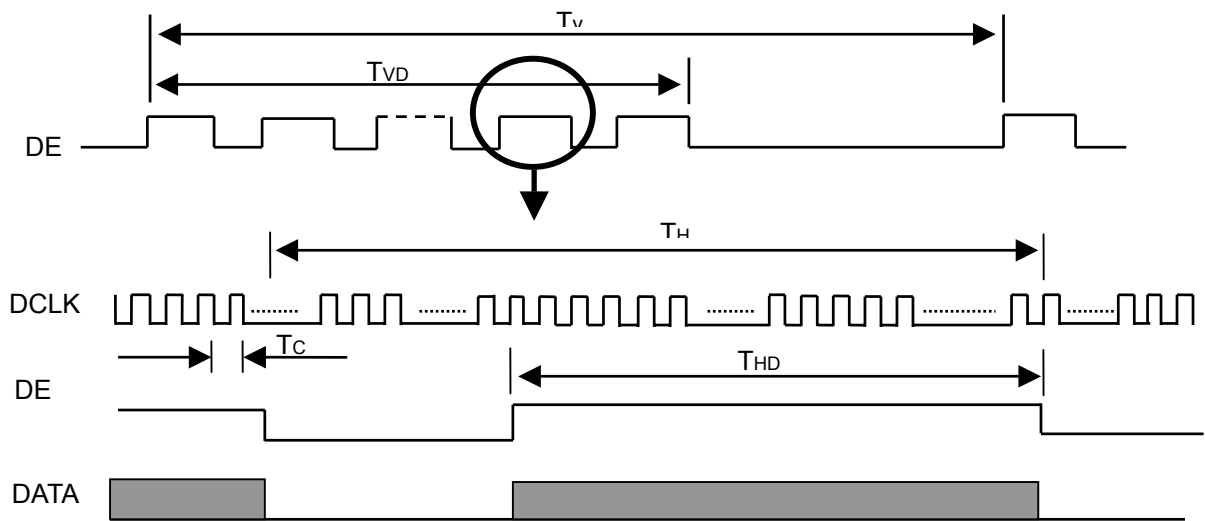
6 INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

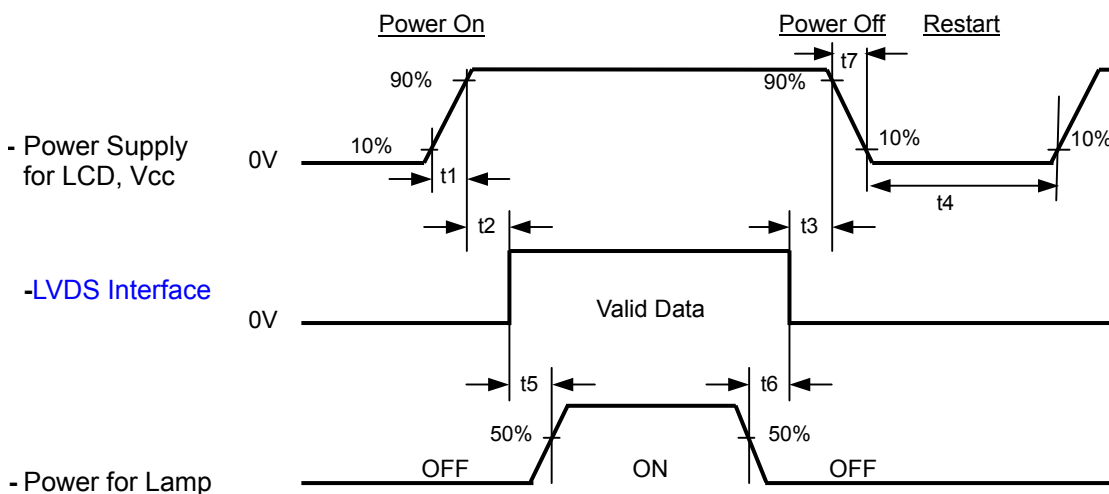
The specifications of input signal timing are as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	50	71.1	80	MHz	-
DE	Vertical Total Time	TV	810	823	2000	TH	-
	Vertical Addressing Time	TVD	800	800	800	TH	-
	Horizontal Total Time	TH	1360	1440	1900	Tc	-
	Horizontal Addressing Time	THD	1280	1280	1280	Tc	-

INPUT SIGNAL TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE



Timing Specifications:

$$0.5 < t_1 \cong 10 \text{ msec}$$

$$0 < t_2 \cong 50 \text{ msec}$$

$$0 < t_3 \cong 50 \text{ msec}$$

$$t_4 \cong 500 \text{ msec}$$

$$t_5 \cong 200 \text{ msec}$$

$$t_6 \cong 200 \text{ msec}$$

Note (1) Please avoid floating state of interface signal at invalid period.

Note (2) When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time had better to follow

$$t_7 \cong 5 \text{ msec}$$

7 OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

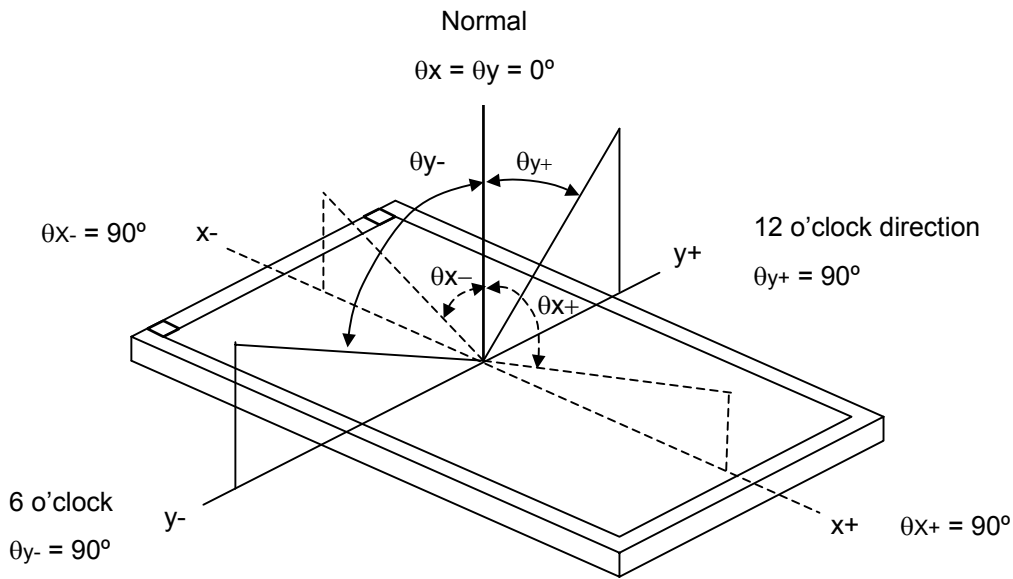
Item	Symbol	Value	Unit
Ambient Temperature	T _a	25±2	°C
Ambient Humidity	H _a	50±10	%RH
Supply Voltage	V _{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I _L	120	mA

The measurement methods of optical characteristics are shown in Section 7.2. The following items should be measured under the test conditions described in Section 7.1 and stable environment shown in Note (6).

7.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Contrast Ratio		CR	θ _x =0°, θ _y =0° Viewing Normal Angle	(350)	(500)		-	(2), (5)	
Response Time		T _R		-	(9)	(14)	ms	(3)	
		T _F		-	(16)	(21)	ms		
Average Luminance of White		L _{AVE}			(250)	(300)		cd/m ²	(4), (5)
White Variation		δW				(1.5)	-	-	(5), (6)
Color Chromaticity	Red	R _x		θ _x =0°, θ _y =0° Viewing Normal Angle	TYP (-0.05)	(0.613)	TYP (+0.05)	-	(1)
		R _y				(0.358)		-	
	Green	G _x				(0.363)		-	
		G _y				(0.544)		-	
	Blue	B _x				(0.156)		-	
		B _y	(0.144)			-			
	White	W _x	0.313			-			
		W _y	0.329			-			
Viewing Angle	Horizontal	θ _{x+}	CR≥10	(50)	(60)		Deg.		
		θ _{x-}		(50)	(60)				
	Vertical	θ _{y+}		(40)	(50)				
		θ _{y-}		(50)	(60)				

Note (1) Definition of Viewing Angle (θ_x, θ_y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

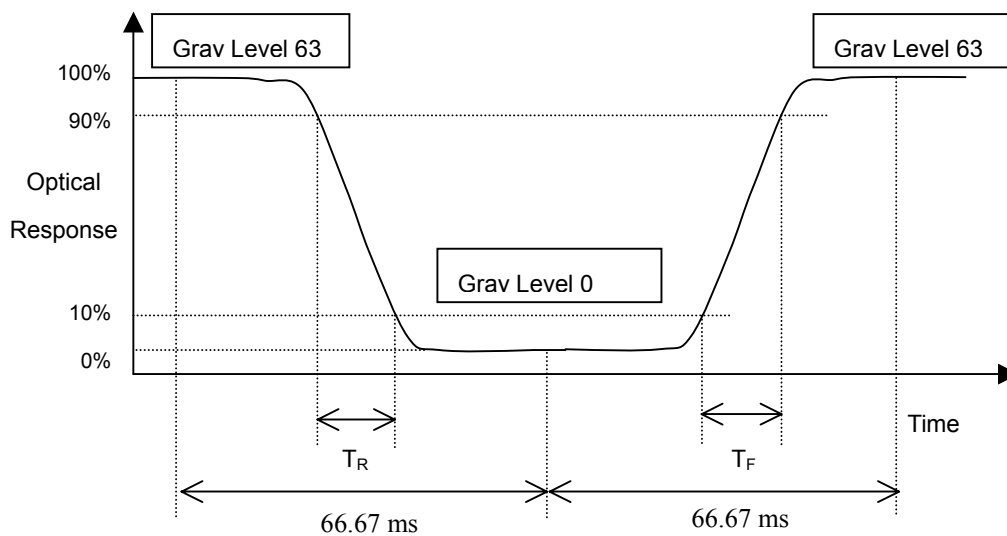
L_{63} : Luminance of gray level 63

L_0 : Luminance of gray level 0

$$\text{CR} = \text{CR} (5)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{5p}):

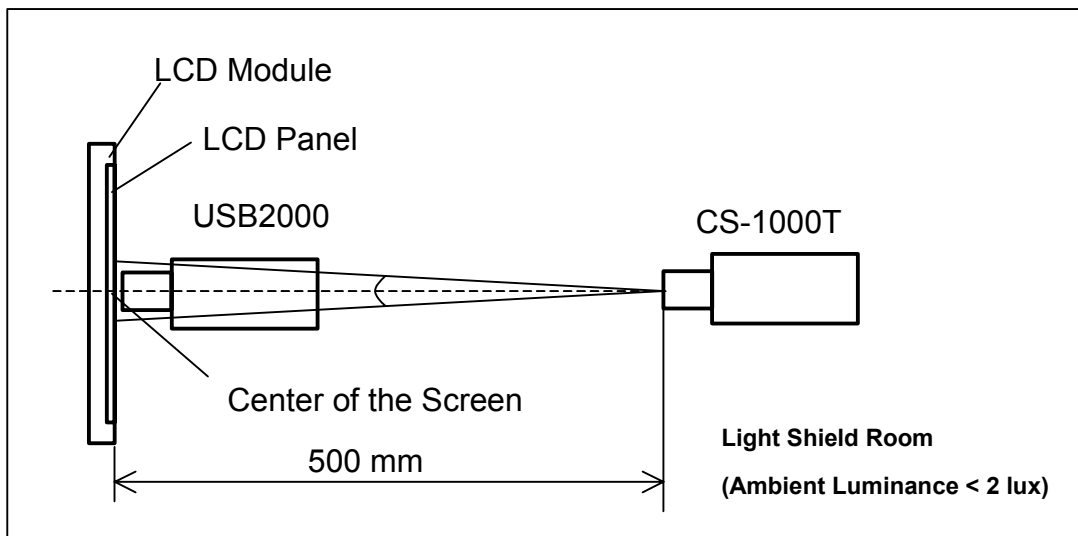
Measure the luminance of gray level 63 at 5 points

$$L_{5p} = [L(5) + L(10) + L(11) + L(12) + L(13)] / 5$$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

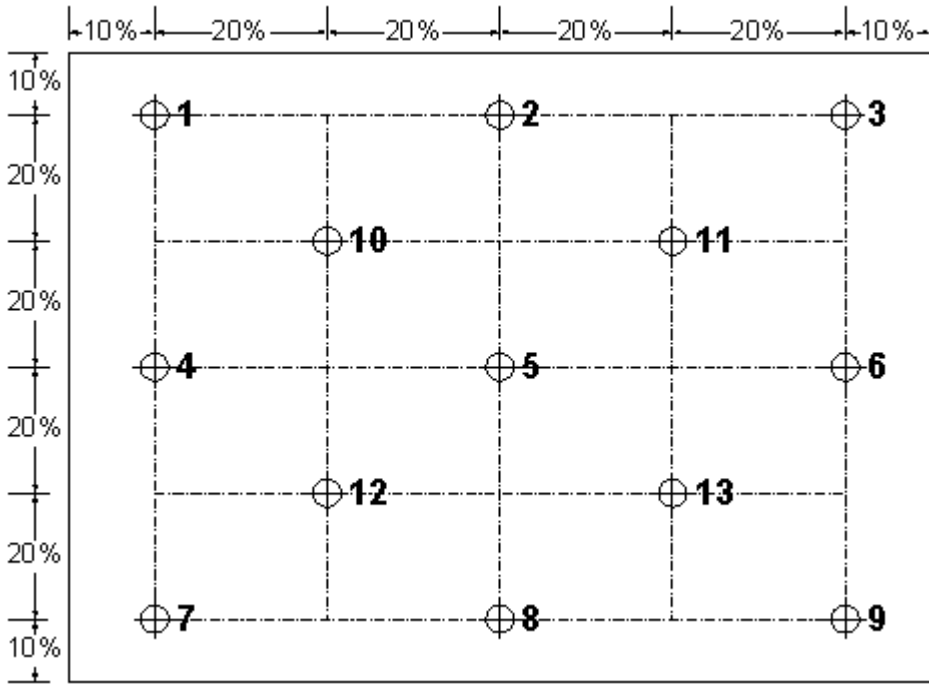


Note (6) Definition of White Variation (δW_{5p} , δW_{13p}):

Measure the luminance of gray level 63 at 5, 13 points

$$\delta W_{5p} = \{1 - \frac{\text{Minimum} [L(5) + L(10) + L(11) + L(12) + L(13)]}{\text{Maximum} [L(5) + L(10) + L(11) + L(12) + L(13)]}\} * 100\%$$

$$\delta W_{13p} = \{1 - \frac{\text{Minimum} [L(1) \sim L(13)]}{\text{Maximum} [L(1) \sim L(13)]}\} * 100\%$$



Note (7) Definition of color gamut (C.G):

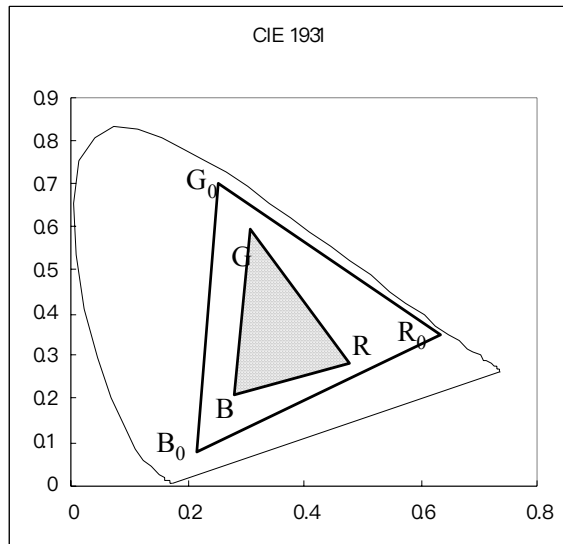
$$C.G = \frac{\Delta R G B}{\Delta R_0 G_0 B_0} * 100\%$$

R_0, G_0, B_0 : color coordinates of red, green, and blue defined by NTSC, respectively.

R, G, B : color coordinates of module on 63 gray levels of red, green, and blue, respectively.

$\Delta R_0 G_0 B_0$: area of triangle defined by R_0, G_0, B_0

$\Delta R G B$: area of triangle defined by R, G, B



8 PRECAUTIONS

8.1 HANDLING PRECAUTIONS

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the lamp wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

- (1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (3) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

- (1) Do not pull the I/F connector in or out while the module is operating.
- (2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.
- (3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

9 PACKAGING
 9.1 CARTON

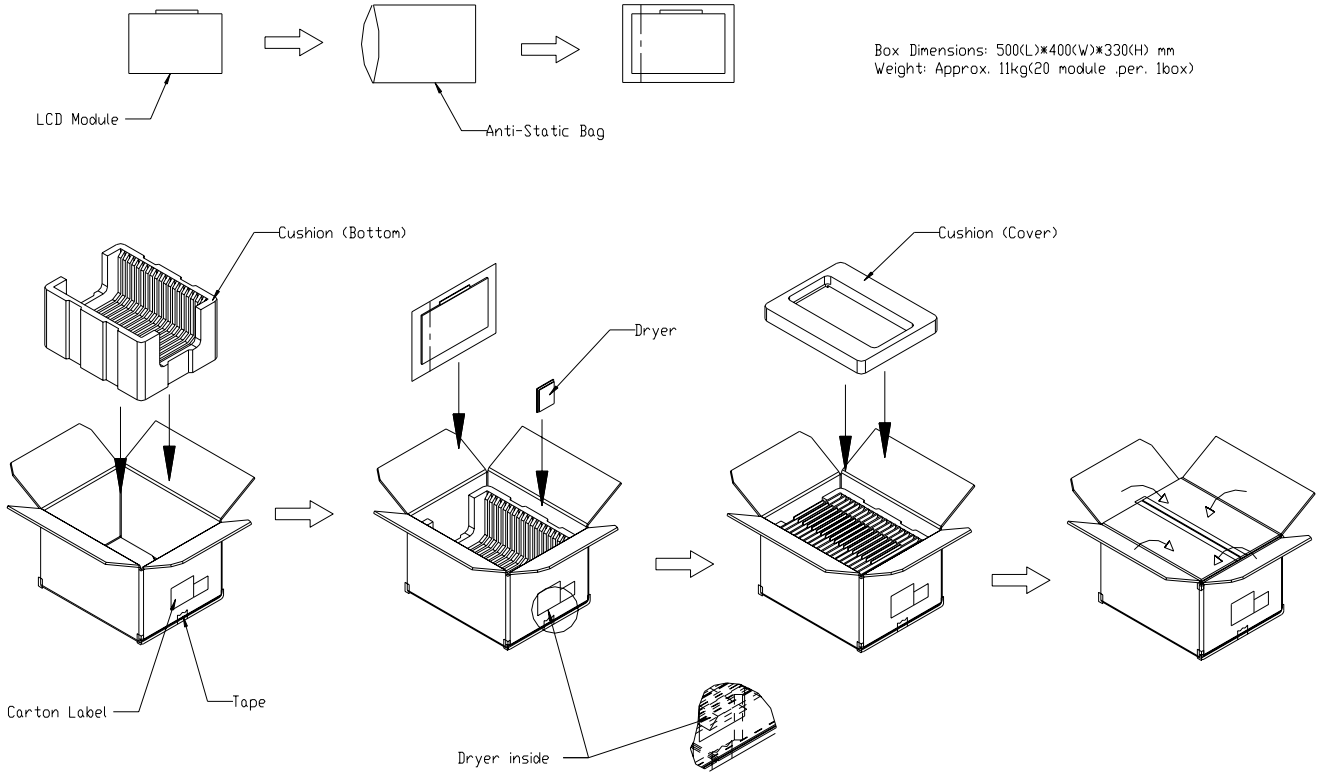


Figure. 10-1 Packing method

9.2 PALLET

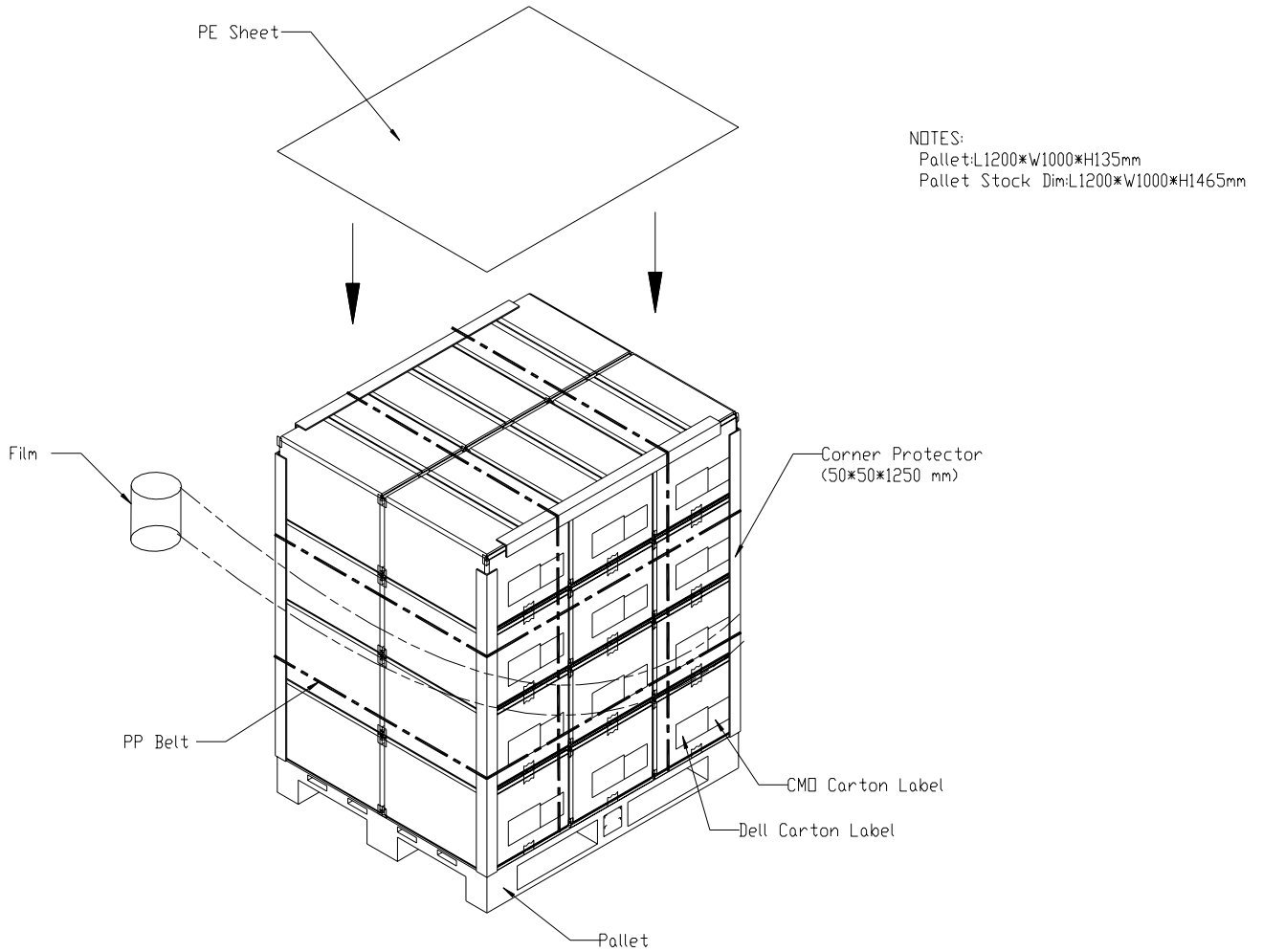
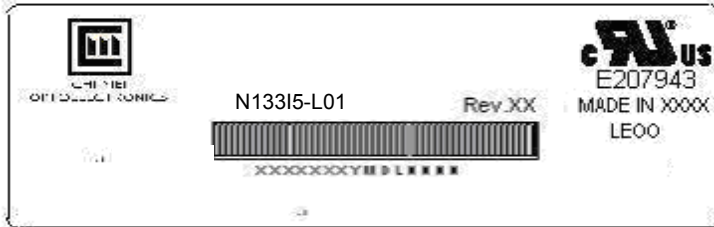


Figure. 10-2 Packing method

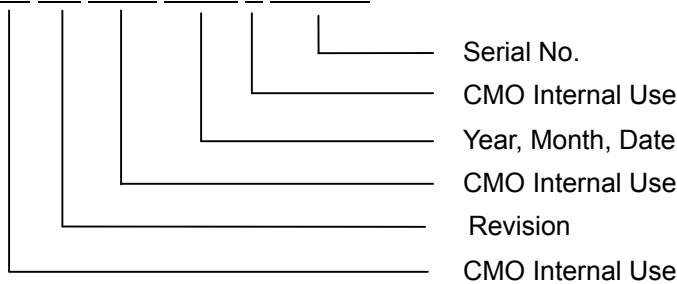
10 DEFINITION OF LABELS

10.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: N133I5 - L01
- (b) Revision: Rev. XX, for example: A1, ..., C1, C2 ...etc.
- (c) Serial ID: XXXXXXXXYMDXNNNN



- (d) Production Location: MADE IN XXXX. XXXX stands for production location.
- (e) UL/CB logo: "LEOO" especially stands for panel manufactured by CMO Ningbo satisfying UL/CB requirement. "LEOO" is the CMO's UL factory code for Ningbo factory.

Serial ID includes the information as below:








- (a) Manufactured Date: Year: 1~9, for 2001~2009
Month: 1~9, A~C, for Jan. ~ Dec.
Day: 1~9, A~Y, for 1st to 31st, exclude I, O and U
- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product

10.2 CMO CARTON LABEL



- (a) Production location: Made In XXXX. XXXX stands for production location.









10.3 CARTON LABEL

PKG ID (3S)124161241729112345609886C20 	 REV.A06
DP/N 03J849 	 Vendor ID Loc Id 12416 12416
BOX Qty 20 	Made in Taiwan 
	 Mfg Id 70896

Type J Label

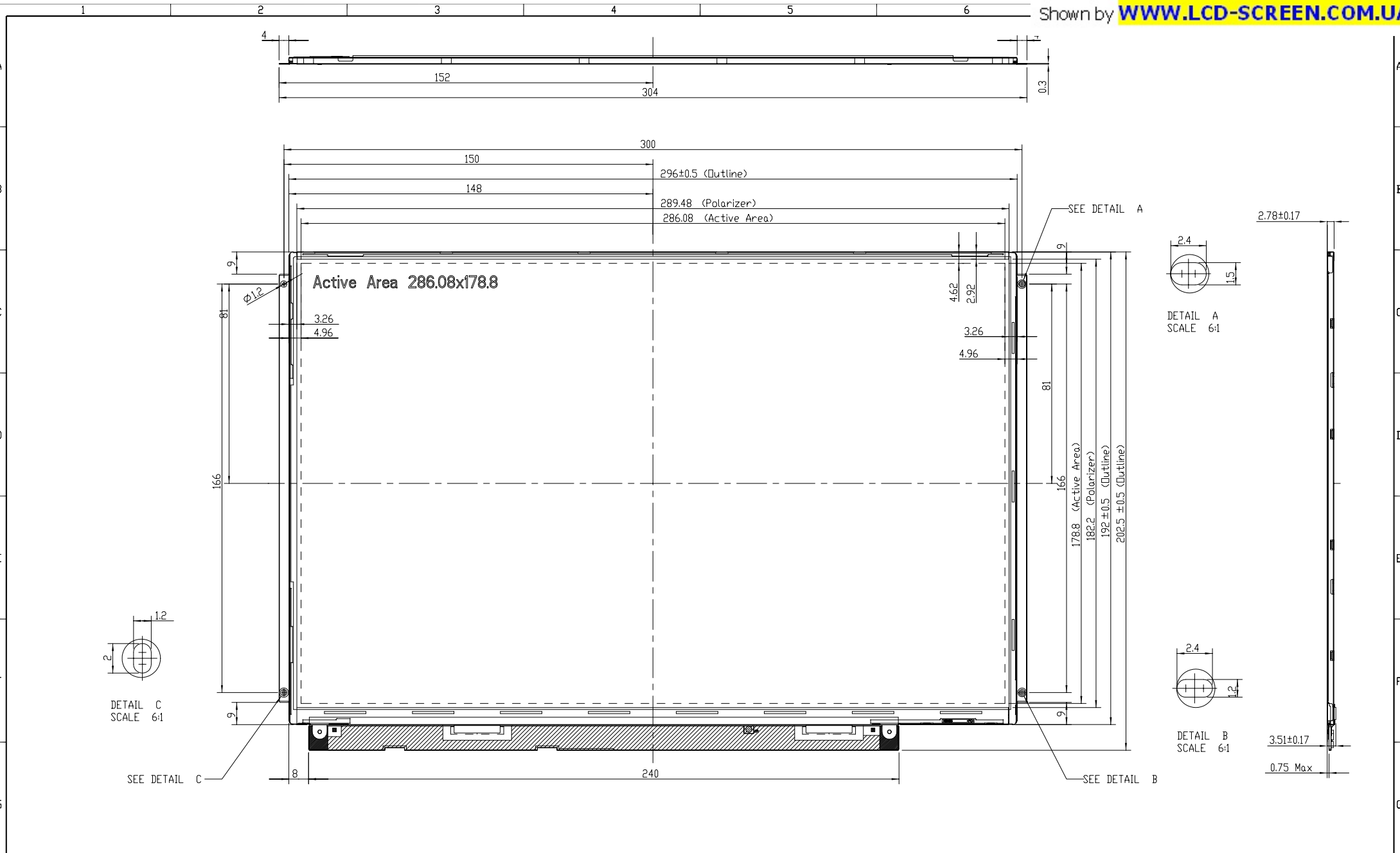
- Verdana font or equivalent,bold
- 20pt.-all fields
- 203 DPI printer minimum
- Code 128B
- 10-15 mil minimum narrow bar
- .75"minimum barcode height
- .10" or greater quiet zone
- 4.0" x 6.0" label size
- Brady THT -25-402-1 or equivalent
- Brady R6107 series ribbon or equivalent

10.4 PALLET LABEL

FROM :CMO Corporation Tainan, Taiwan 744 R.O.C	TO:DELL COMPUTER 2128 West Braker Austin TX
P.O.NUMBER 12345678	
	DELL P/N 12345
COUNTRY OF ORIGIN TW	
	PACKING LIST# 1234567890123
PACKING LIST QTY 654321	
	DESTINATION MAS LOC 60
DESTINATION LOCATION B4	
AIRBILL NUMBER 12345678901234567890	
	
PKG CNT 999 OF 999	BOX CNT 12345
REVISION A00-00	SHIP DATE Apr 29,2003
PART DESCRIPTION XXXXXXXXXXXXXXXXXXXXXXXX 12345678901234567890123456789012345678901	

Type K Label

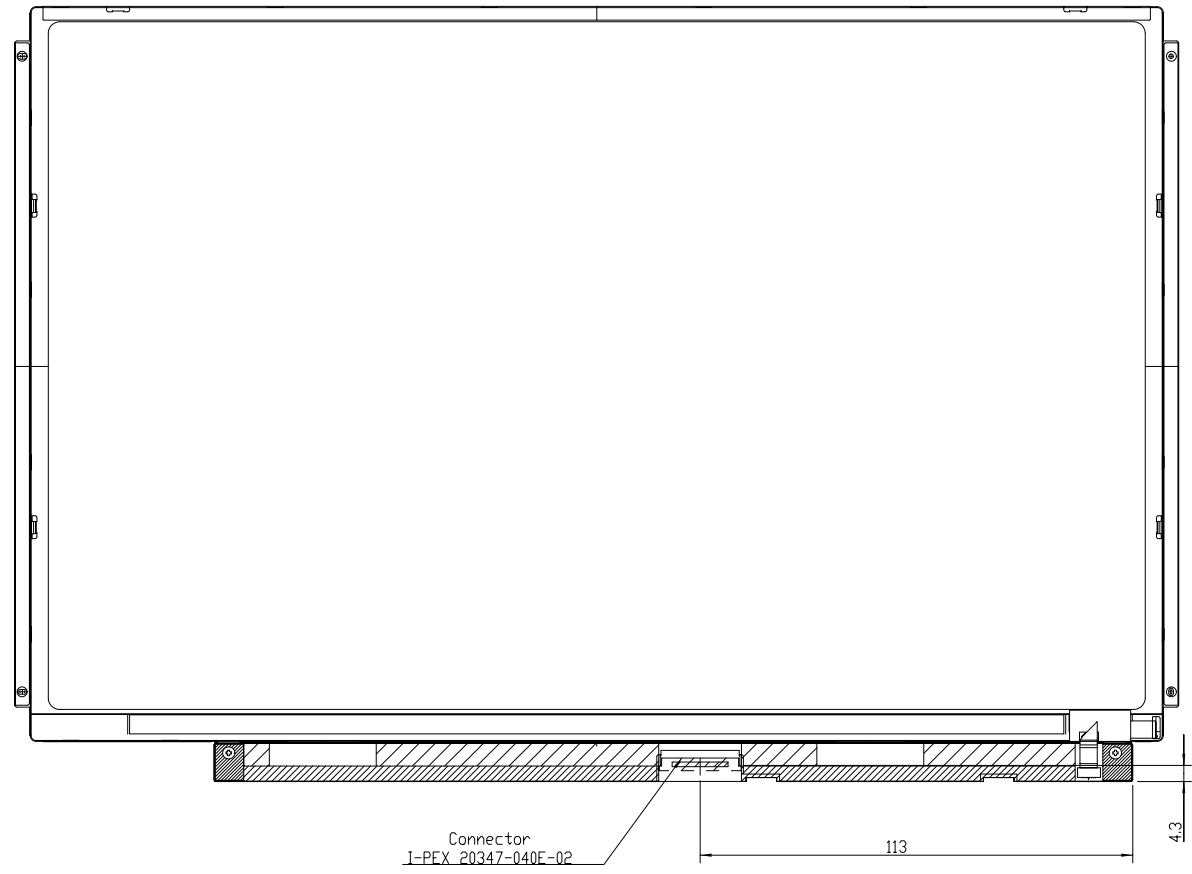
- Verdana font or equivalent,bold
- 12pt.-all descript fields
- 10pt.-all data fields
- 203 DPI printer minimum
- Code 128B
- 10 mil minimum narrow bar
- .30-.50"minimum barcode height
- .10" or greater quiet zone
- 4.0" x 6.5" label size
- Brady THT -78-402-.9 or equivalent
- Brady R6107 series ribbon or equivalent



NOTES:
 1. OUTLINE TOLERANCE: ±0.5mm.
 2. * MARKS THE DESIGN CRITICAL DIMENSION.
 3. ⊕ MARKS THE PROCESS CRITICAL DIMENSION.

TITLE		ASSY_MODULE_N13315-L01		2D REV: 1	
				3D REV: 1.11	
Approved	BILL_SHEU	Drawing No.	N133541021		
Checked	SHUNNAN	Part No.	N/A		
Drawer	HSINHUNG_CHEN	Material	N/A	Sheet	1 / 2 A2
Designer	HSINHUNG_CHEN	Date	17-Dec-2006	Scale	1:1
		Unit	mm		
CHI MEI OPTOELECTRONICS CORP.		ALL RIGHTS RESERVED, COPYING FORBIDDEN.			

Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark




Connector
I-PEX 20347-040E-02

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Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark

TITLE	ASSY_MODULE_N13315-LXX			2D REV: 1
				3D REV: 1.11
Approved	BILL_SHEU	Drawing No.	N133541021	
Checked	SHUNNAN	Part No.	N/A	
Drawer	YAOCHIEH	Material	N/A	Sheet 2 / 2 A2
Designer	YAOCHIEH	Date	11-Jan-2007	Scale 1:1 Unitmm
 CHI MEI OPTOELECTRONICS CORP.		ALL RIGHTS RESERVED, COPYING FORBIDDEN.		