TFT LCD Approval Specification

MODEL NO.: V236H1-P01

Customer : _____

Approved by : _____

Note :

核准時間	部門	審核	角色	投票
2009-10-29 08:48:56	MTR 產品管理處	吳 2009.10.29 柏勳	Director	Accept

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REVISION HISTORY

Version	Date	Section	Description
Ver. 2.0	Sep, 16, '09	-	V236H1-P01 Approval Specification was first issued.
Ver. 2.1	Oct, 19, '09	1.5	Modified weight（Column "Typ." and "Max."）
		3.1	Modified the value of【Minimum Logic Low Input Voltage】from "-0.3" to "0".

1. GENERAL DESCRIPTION

1.1 OVERVIEW

The V236H1-P01 is a 23.6-inch wide TFT LCD open cell with driver ICs and a 30-pins-2ch-LVDS circuit board. The product supports 1920 x 1080 Full HD mode and can display up to 16.7M colors. The backlight unit is not built in.

1.2 FEATURES

- Super wide viewing angle
- High contrast ratio
- Fast response time
- High color saturation
- Full HDTV (1920 x 1080 pixels) resolution
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- RoHS Compliance

1.3 APPLICATION

- TFT LCD Monitor/TV

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Diagonal Size	23.547	inch	
Active Area	521.28 (H) x 293.22 (V)	mm	(1)
Driver Element	a-Si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch	0.2715 (H) x 0.2715 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Transmissive Mode	Normally White	-	-
Surface Treatment	Hard coating (3H), Anti-glare (Haze 25%)	-	-
Power Consumption	7.5	Watt	(3)

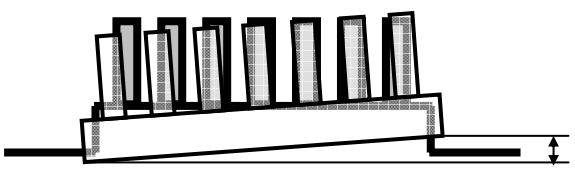
1.5 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight	-	720	-	g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within ±0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

(2) Connector mounting position

(3) Please refer to sec.3.1 for more information of power consumption.



2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT (BASED ON CMO MODULE V236H1-L01)

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)

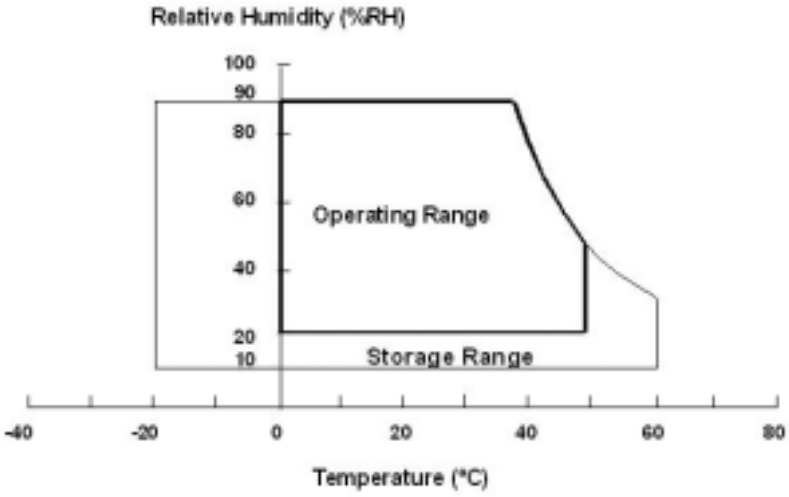
Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC)

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC)

(c) No condensation.

Note (2) The temperature of panel display surface area should be 0 ºC Min. and 60 ºC Max.



2.2 ABSOLUTE RATINGS OF ENVIRONMENT (OPEN CELL)

High temperature or humidity may reduce the performance of panel. Please store LCD panel within the specified storage conditions.

Storage Condition: With packing

Storage temperature range: 25±5 ºC

Storage humidity range: 50±10%RH

Shelf life: 30days

2.3 ELECTRICAL ABSOLUTE RATINGS (OPEN CELL)

Item	Symbol	Value		Unit	Note
		Min	Max		
Power Supply Voltage	V_{CC}	-0.3	+6.0	V	(1)
Logic Input Voltage	Vlogic	-0.3	+3.6	V	

Note (1) Permanent damage might occur if the module is operated at conditions exceeding the maximum values.

3. ELECTRICAL CHARACTERISTICS

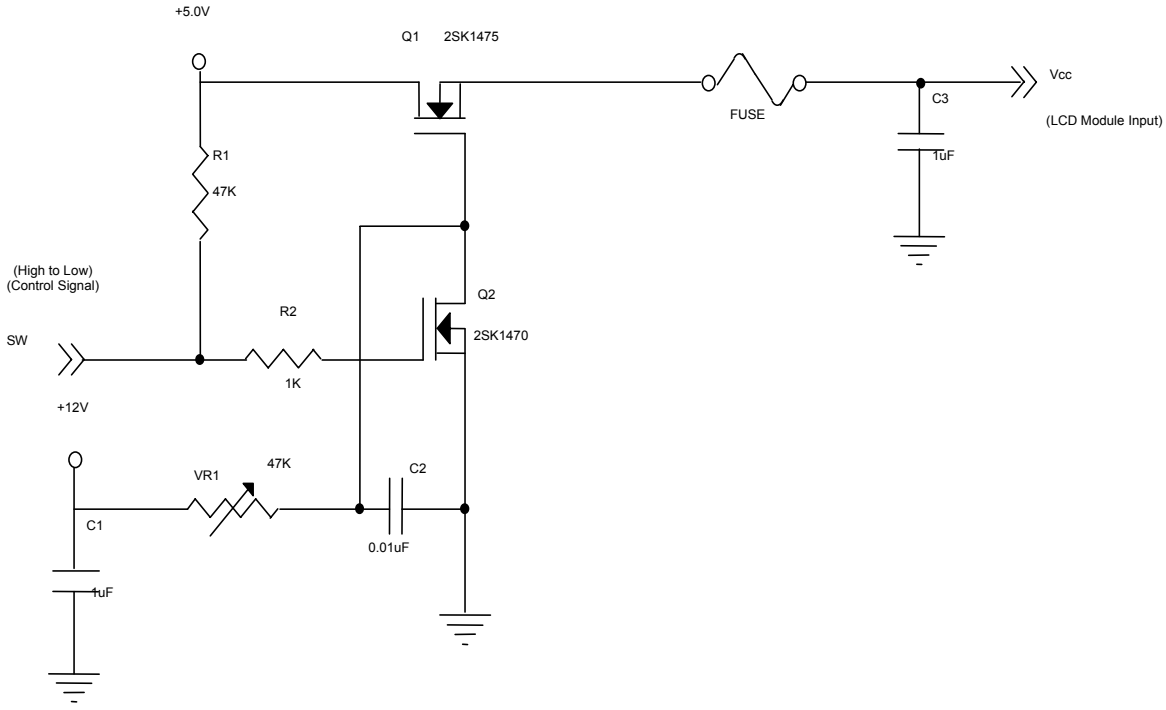
3.1 TFT LCD OPEN CELL

Ta = 25 ± 2 ºC

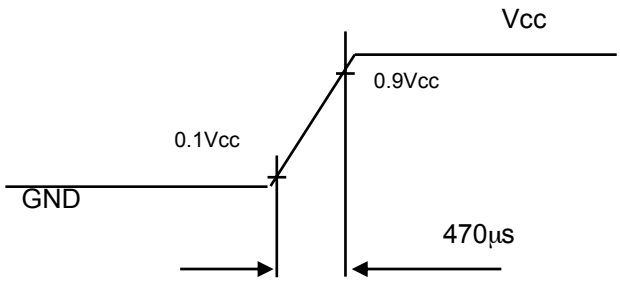
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	4.5	5.0	5.5	V	-
Ripple Voltage		V_{RP}	-	--	300	mV	-
Rush Current		I_{RUSH}	-	-	3.5	A	(2)
Power Supply Current	White	Icc	-	0.55	0.67	A	(3)a
	Black		-	1.5	1.9	A	(3)b
	Vertical Stripe		-	1.18	1.43	A	(3)c
Power Consumption		P_{LCD}		7.5	9.5	Watt	(4)
LVDS differential input voltage		Vid	100	-	600	mV	
LVDS common input voltage		Vic	-	1.2	-	V	
Logic High Input Voltage		VIH	2.64	-	3.6	V	
Logic Low Input Voltage		VIL	0	-	0.66	V	

Note (1) The product should be always operated within above ranges.

Note (2) Power On Rush Current Measurement Conditions: (must follow power sequence)



Vcc rising time is 470μs



Note (3) The specified power supply current is under the conditions at Vcc = 5.0 V, Ta = 25 ± 2 ºC, Fv = 60 Hz, whereas a power dissipation check pattern below is displayed.

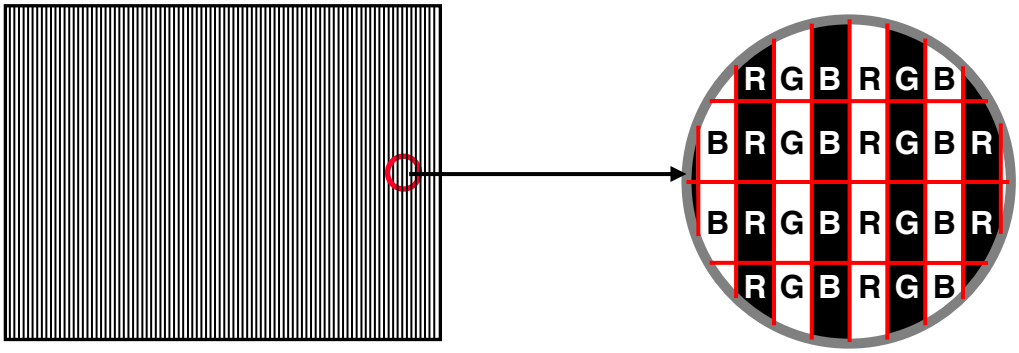
a. White Pattern

Active Area

b. Black Pattern

Active Area

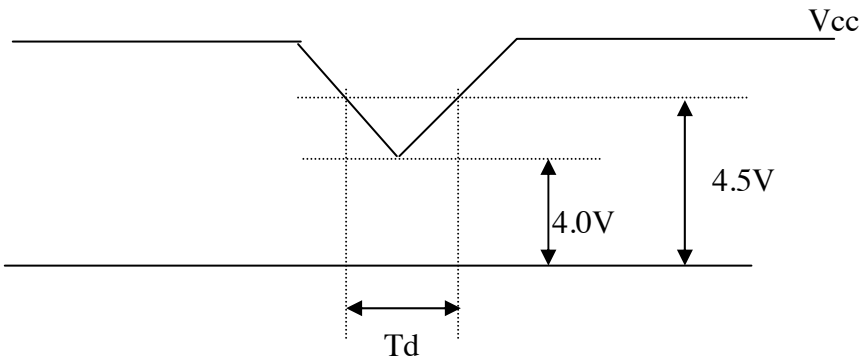
c. Vertical Stripe Pattern



Active Area

Note (4) The power consumption is specified at the pattern with the maximum current.

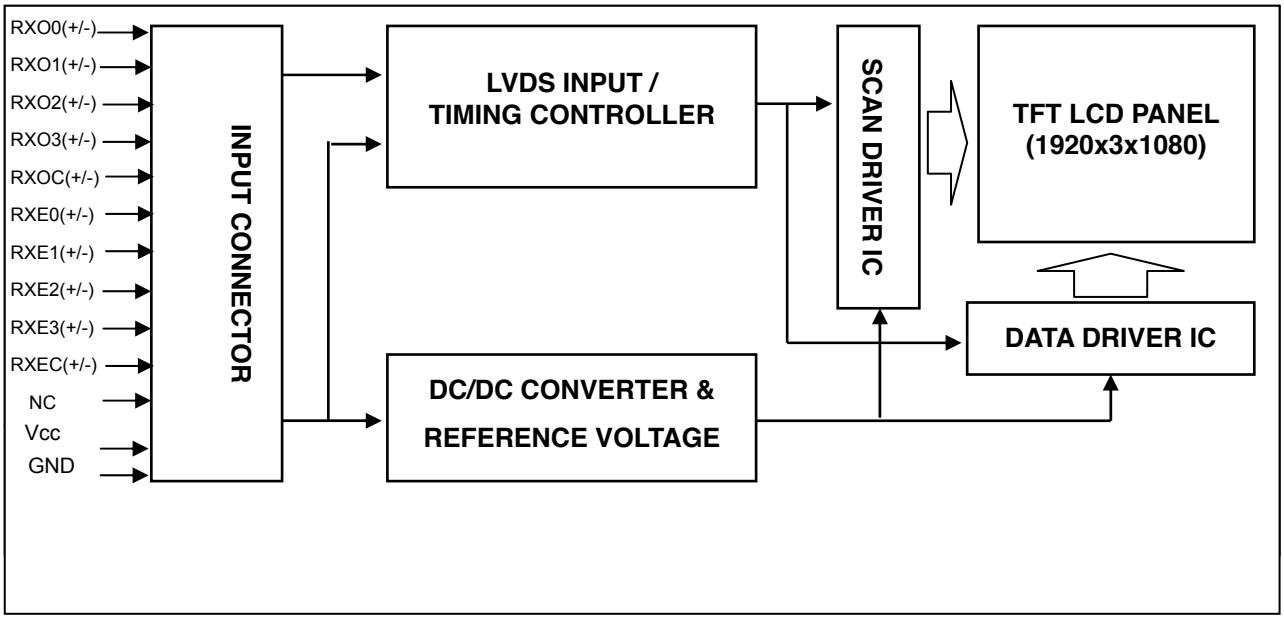
3.2 Vcc Power Dip Condition:



Dip condition: $4.0V \leq Vcc \leq 4.5V, Td \leq 20ms$

4. BLOCK DIAGRAM

4.1 TFT LCD OPEN CELL



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

Pin	Name	Description
1	RXO0-	Negative LVDS differential data input. Channel O0 (odd)
2	RXO0+	Positive LVDS differential data input. Channel O0 (odd)
3	RXO1-	Negative LVDS differential data input. Channel O1 (odd)
4	RXO1+	Positive LVDS differential data input. Channel O1 (odd)
5	RXO2-	Negative LVDS differential data input. Channel O2 (odd)
6	RXO2+	Positive LVDS differential data input. Channel O2 (odd)
7	GND	Ground
8	RXOC-	Negative LVDS differential clock input. (odd)
9	RXOC+	Positive LVDS differential clock input. (odd)
10	RXO3-	Negative LVDS differential data input. Channel O3(odd)
11	RXO3+	Positive LVDS differential data input. Channel O3 (odd)
12	RXE0-	Negative LVDS differential data input. Channel E0 (even)
13	RXE0+	Positive LVDS differential data input. Channel E0 (even)
14	GND	Ground
15	RXE1-	Negative LVDS differential data input. Channel E1 (even)
16	RXE1+	Positive LVDS differential data input. Channel E1 (even)
17	GND	Ground
18	RXE2-	Negative LVDS differential data input. Channel E2 (even)
19	RXE2+	Positive LVDS differential data input. Channel E2 (even)
20	RXEC-	Negative LVDS differential clock input. (even)
21	RXEC+	Positive LVDS differential clock input. (even)
22	RXE3-	Negative LVDS differential data input. Channel E3 (even)
23	RXE3+	Positive LVDS differential data input. Channel E3 (even)
24	GND	Ground
25	NC	Not connection, this pin should be open.
26	NC	Not connection, this pin should be open.
27	NC	Not connection, this pin should be open.
28	Vcc	+5.0V power supply
29	Vcc	+5.0V power supply
30	Vcc	+5.0V power supply

Note (1) Connector Part No.: STM MSAKT2407P30HA or Starconn 093G30-B0001A or Equivalent
Note (2) The first pixel is odd.
Note (3) Input signal of even and odd clock should be the same timing.

5.2 LVDS DATA MAPPING TABLE

LVDS Channel O0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	OG0	OR5	OR4	OR3	OR2	OR1	OR0
LVDS Channel O1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	OB1	OB0	OG5	OG4	OG3	OG2	OG1
LVDS Channel O2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	OB5	OB4	OB3	OB2
LVDS Channel O3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	OB7	OB6	OG7	OG6	OR7	OR6
LVDS Channel E0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	EG0	ER5	ER4	ER3	ER2	ER1	ER0
LVDS Channel E1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	EB1	EB0	EG5	EG4	EG3	EG2	EG1
LVDS Channel E2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	EB5	EB4	EB3	EB2
LVDS Channel E3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	EB7	EB6	EG7	EG6	ER7	ER6

5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

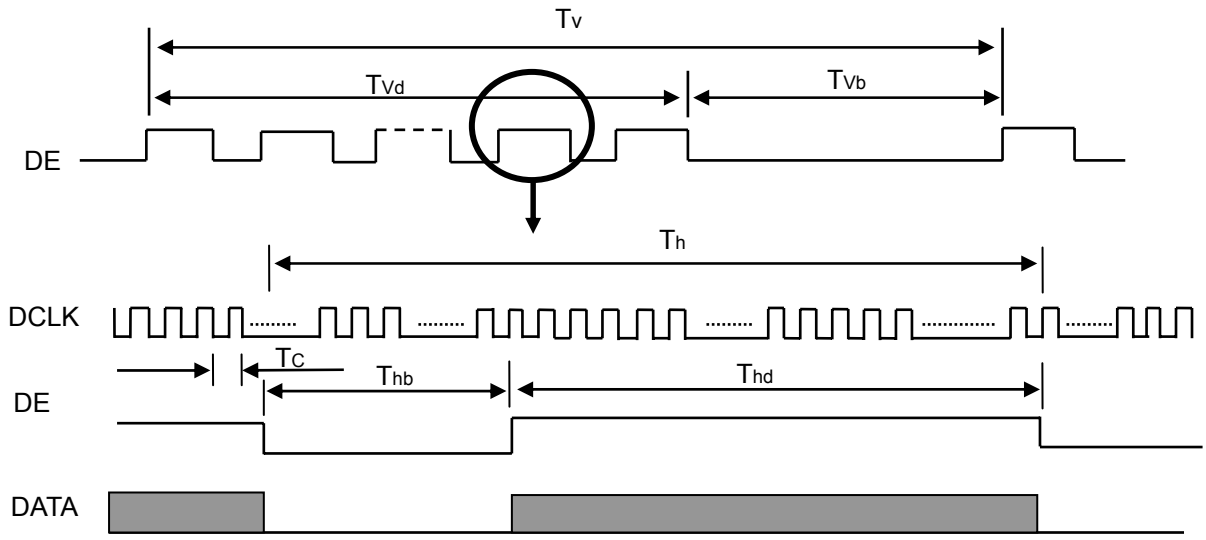
6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

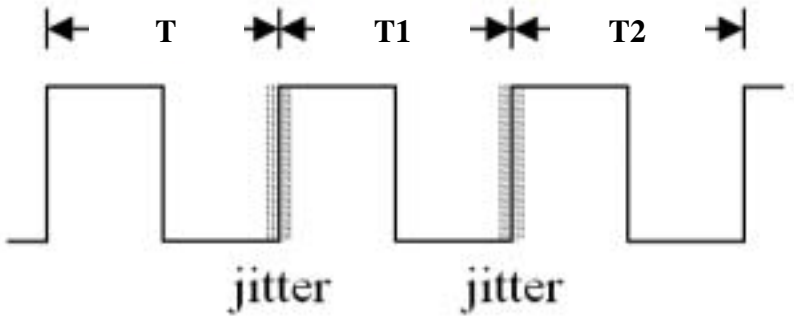
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	Fc	58.54	74.25	98	MHz	-
	Period	Tc	-	13.47	-	ns	
	Input cycle to cycle jitter	T_{rcl}	-0.02*Tc	-	0.02*Tc	ns	(1)
	Spread spectrum modulation range	F_{clkin_mod}	0.98*Fc	-	1.02*Fc	MHz	(2)
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
	High Time	Tch	-	4/7	-	Tc	-
	Low Time	Tcl	-	3/7	-	Tc	-
LVDS Data	Setup Time	Tlvs	600	-	-	ps	(3)
	Hold Time	Tlvh	600	-	-	ps	
Vertical Active Display Term	Frame Rate	Fr	50	60	75	Hz	Tv=Tvd+Tvb
	Total	Tv	1115	1125	1136	Th	-
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	35	45	56	Th	-
Horizontal Active Display Term	Total	Th	1050	1100	1150	Tc	Th=Thd+Thb
	Display	Thd	960	960	960	Tc	-
	Blank	Thb	90	140	190	Tc	-

Note: (1) Because this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

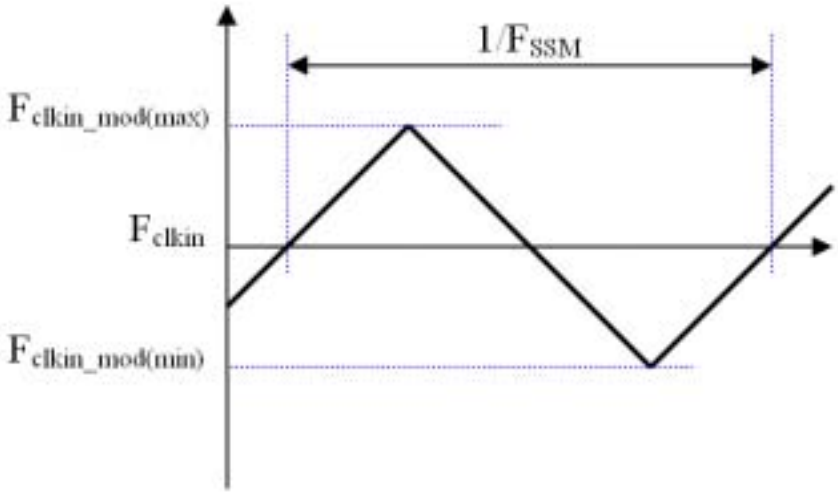
INPUT SIGNAL TIMING DIAGRAM



Note (1) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI

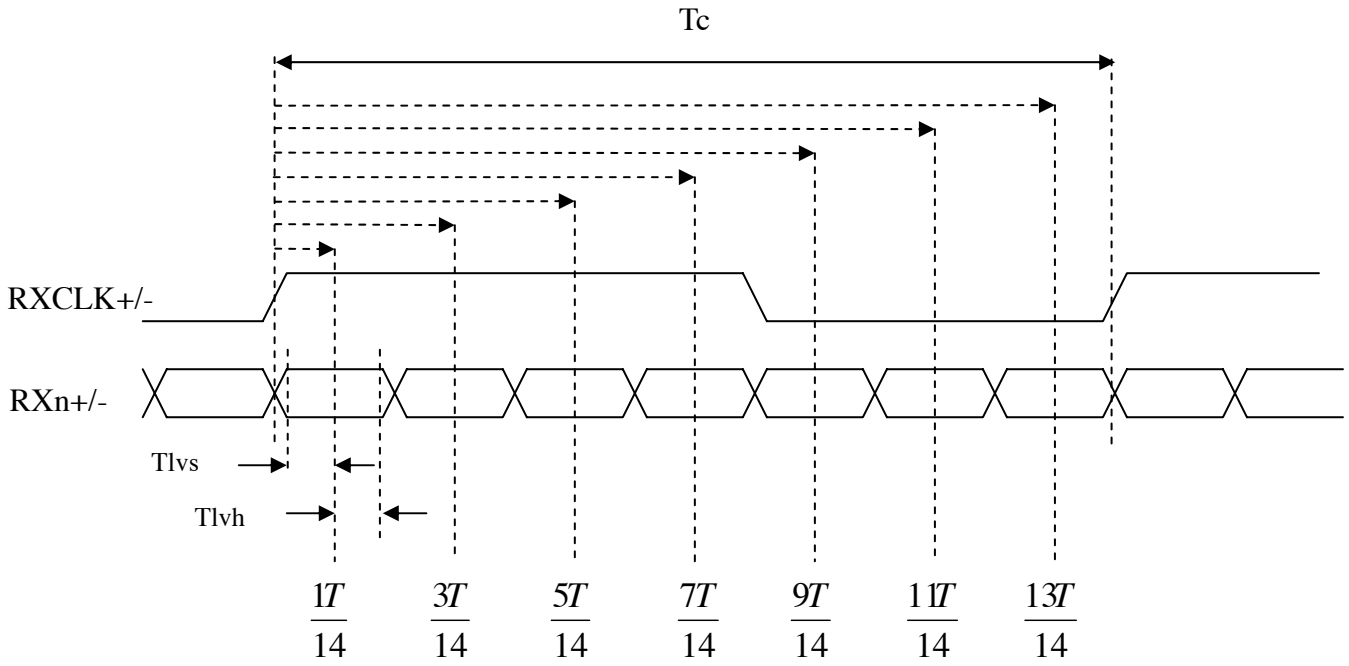


Note (2) The SSCG (Spread spectrum clock generator) is defined as below figures.



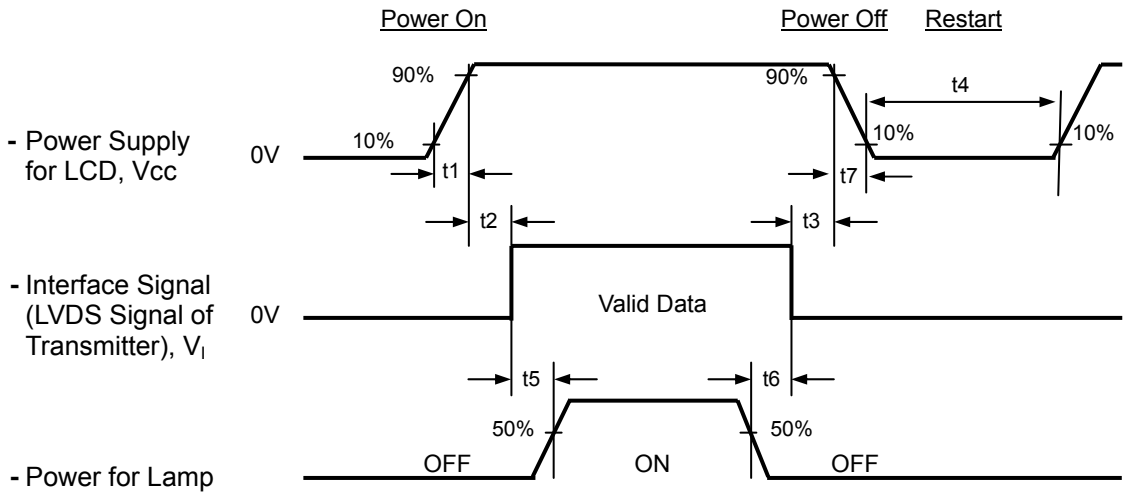
Note (3) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the conditions shown in the following diagram.



Timing Specifications:

0.5< t1 ≦ 10 msec

0 < t2 ≦ 50 msec

0 < t3 ≦ 50 msec

t4 ≧ 500 msec

t5 ≧ 450 msec

t6 ≧ 90 msec

5 ≦ t7 ≦ 100 msec

Note:

(1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.

(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation of the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case of VCC = off level, please keep the level of input signals on the low or keep a high impedance.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

(6) CMO won't take any responsibility for the products which are damaged by the customers not following the Power Sequence.

(7) There might be slight electronic noise when LCD is turned off (even backlight unit is also off). To avoid this symptom, we suggest "Vcc falling timing" to follow "t7 spec".

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25 ±2	°C
Ambient Humidity	Ha	50 ±10	%RH
Supply Voltage	V_{CC}	7.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I_L	7.0 ±0.5	mA
Inverter Driving Frequency	F_L	55 ±5	KHz

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity (CIE 1931)	Red	Rcx	θ_x=0° , θ_Y =0° Viewing Angle at Normal Direction Standard light source "C"	-	0.654	-	-	(0),(6)
		Rcy			0.327		-	
	Green	Gcx			0.268		-	
		Gcy			0.603		-	
	Blue	Bcx			0.147		-	
		Bcy			0.106		-	
	White	Wcx			0.322		-	
		Wcy			0.358		-	
Center Transmittance		T%	θ_x=0° , θ_Y =0° with CMO module	-	6	-	%	(1), (5)
Contrast Ratio		CR		-	800	-	-	(1), (3)
Response Time		T_R	θ_x=0° , θ_Y =0° with CMO Module@60Hz	-	1.5	-	ms	(4)
		T_F		-	3.5	-	ms	
White Variation		δW	θ_x=0° , θ_Y =0° with CMO module	-	-	1.3	-	(1),(7)
Viewing Angle	Horizontal	θ_x+	CR≥10 With CMO module	-	80	-	Deg.	(1), (2)
		θ_x-		-	80	-		
	Vertical	θ_Y+		-	80	-		
		θ_Y-		-	70	-		

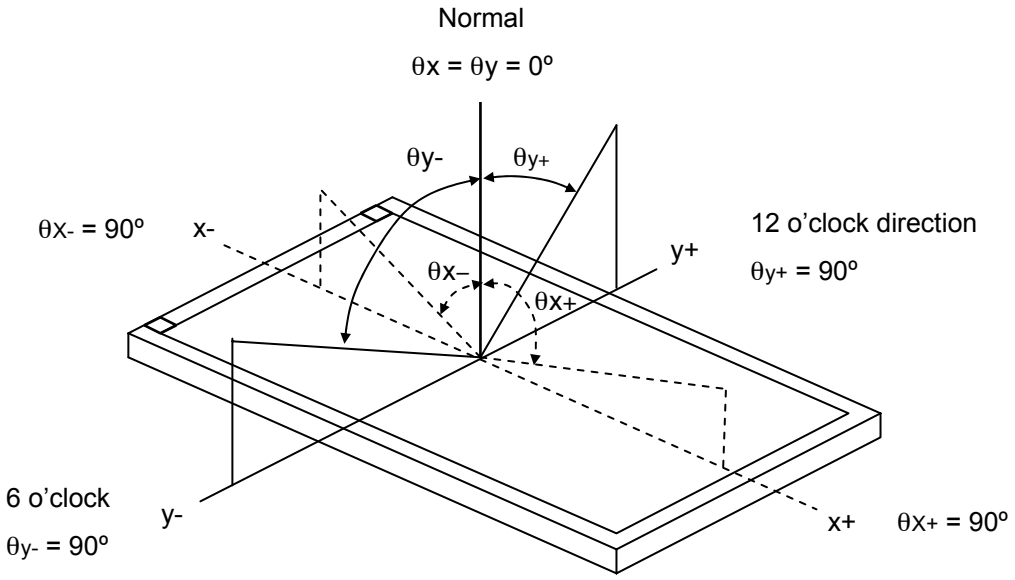
Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltage are based on suitable gamma voltages. The calculating method is as following:

1. Measure Module's and BLU's spectrum. White is without signal input and R, G, B are with signal input. CMO V236H1-L01 BLU is adopted in the measurement.
2. Calculate cell's spectrum.
3. Calculate cell's chromaticity by using the spectrum of standard light source "C".

Note (1) Light source is the BLU, which is supplied by CMO, and driving voltage is based on suitable gamma voltages.

Note (2) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Conoscope Cono-80.



Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

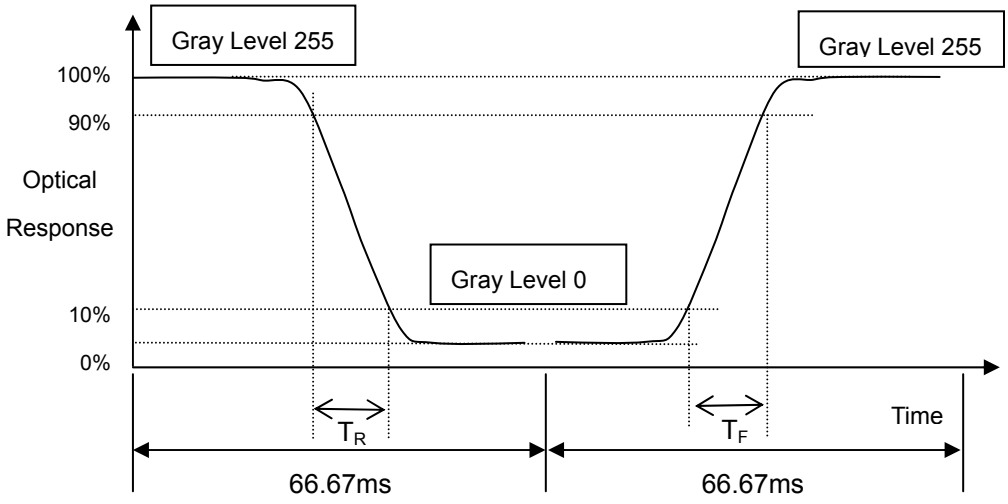
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (7).

Note (4) Definition of Response Time (T_R, T_F):



Note (5) Definition of Transmittance (T%):

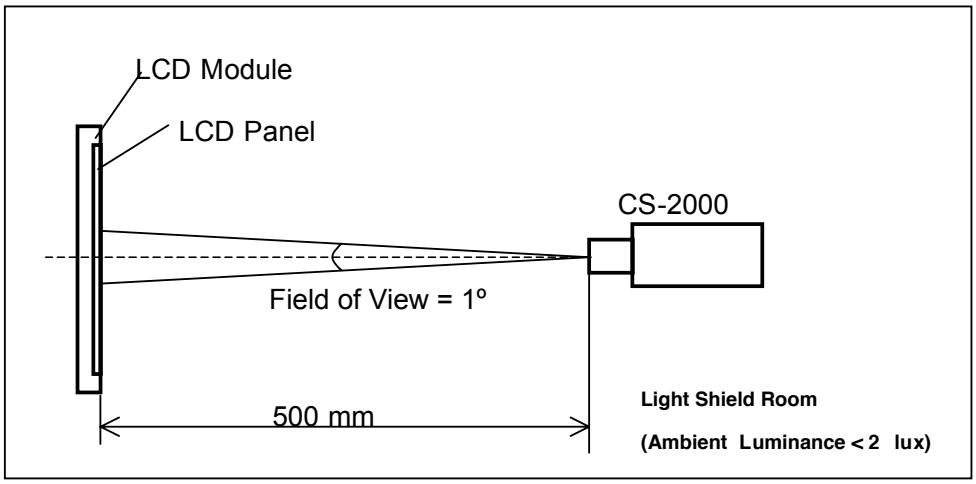
Module is without signal input.

$$\text{Transmittance} = \frac{\text{Luminance of LCD module L(5)}}{\text{Luminance of backlight } L_{BLU}(5)} * 100\%$$

L (x) and $L_{BLU}(X)$ are corresponding to the luminance of the point X at Figure in Note (7).

Note (6) Measurement Setup:

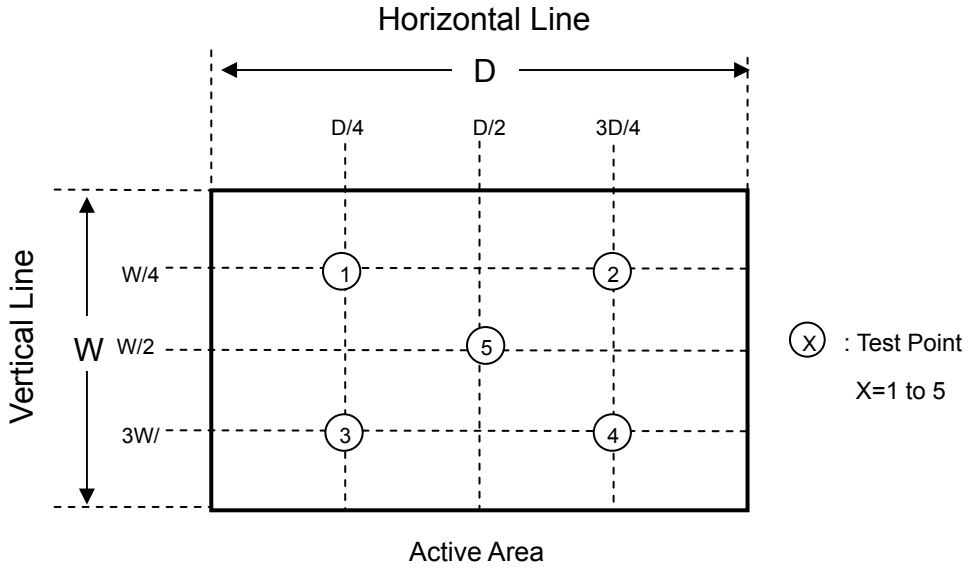
The LCD module should be stabilized at given temperature for 60 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 60 minutes in a windless room.



Note (7) Definition of White Variation (δW):

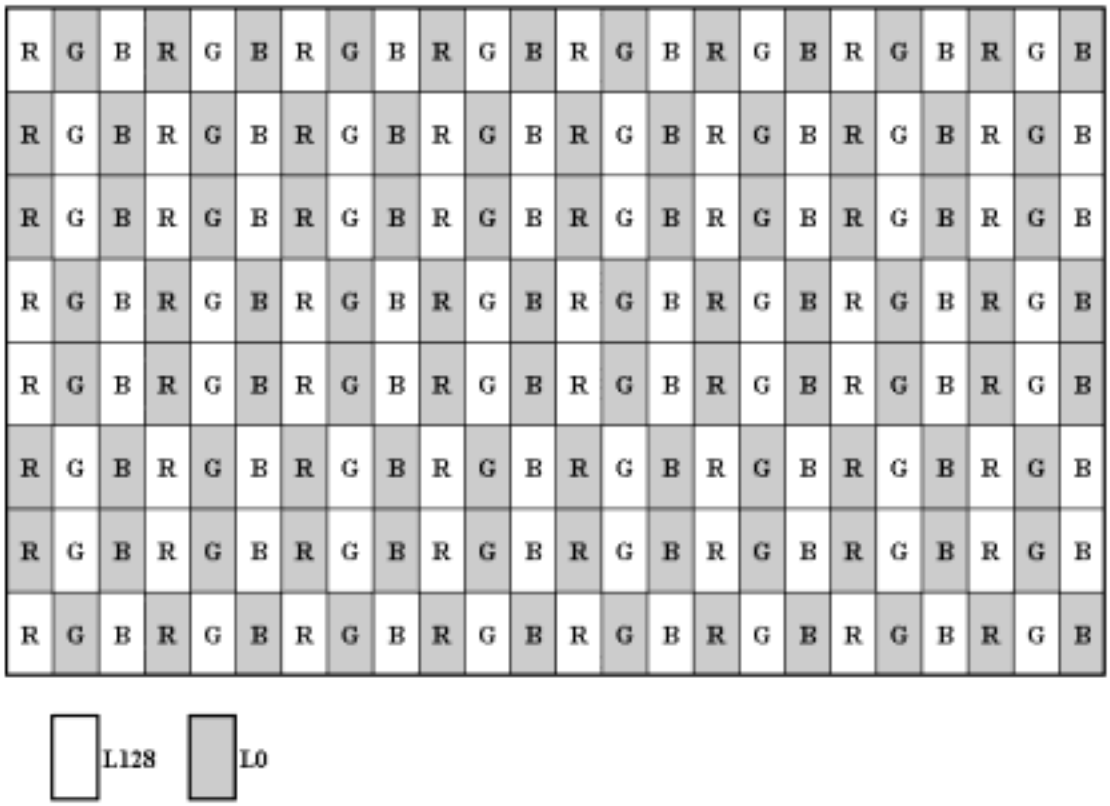
Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



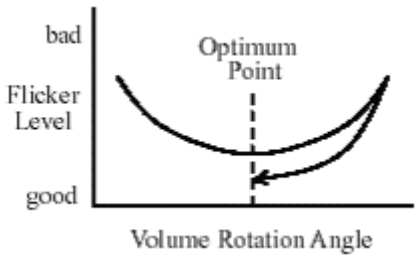
7.3 Flicker Adjustment

(1) Adjustment Pattern: 2H1V checker pattern as follows.



(2) Adjustment Method:

Flicker should be adjusted by turning the volume for flicker adjustment by the ceramic driver. It is adjusted to the point with least flickering of the whole screen. After making it surely overrun at once, it should be adjusted to the optimum point.



8. PACKAGING

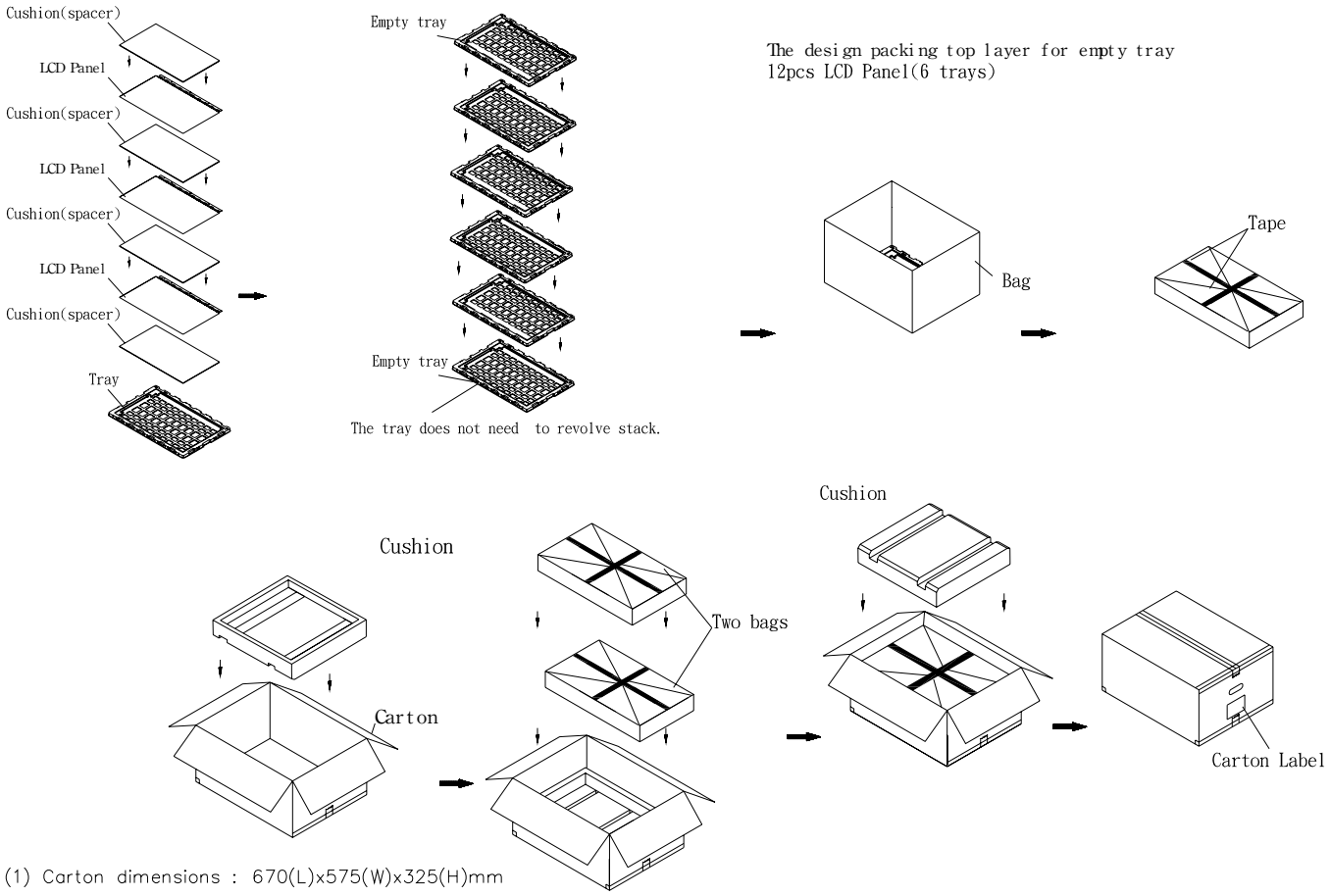
8.1 PACKING SPECIFICATIONS

(1) 24 open cells / 1 Box

(2) Box dimensions: 670 (L) X 575 (W) X 325 (H) mm

(3) Weight: approximately 23.8Kg (24 open cells per box)

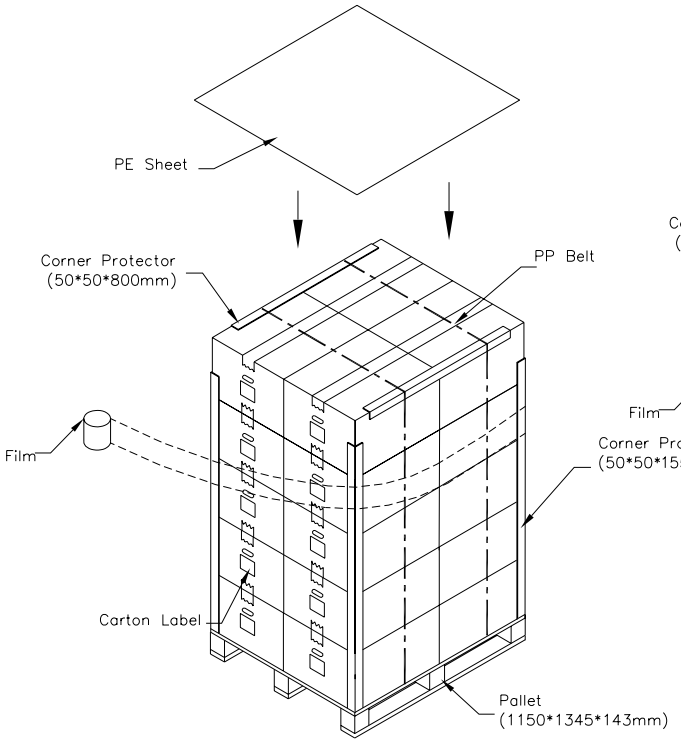
8.2 PACKING METHOD



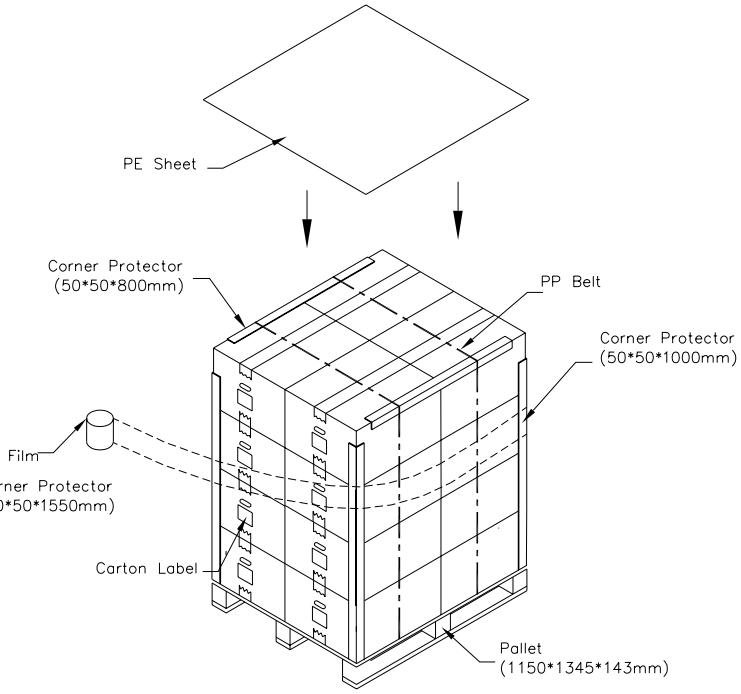
(1) Carton dimensions : 670(L)x575(W)x325(H)mm

(2) Weight :Appro 23.8Kg(24 panels/12 trays)

Sea and Land Transportation



Air Transportation



9. DEFINITION OF LABELS

9.1 CMO OPEN CELL LABEL

The barcode nameplate is pasted on each OPEN CELL as illustration for CMO internal control.

9.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation.

(a) Model Name: V236H1–P01

(b) Carton ID: CMO internal control

(c) Quantities: 24 pcs

10. RELIABILITY TEST

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50℃, 80%RH, 240hours	(1)
High Temperature Operation (HTO)	Ta= 50℃, 50%RH , 240hours	
Low Temperature Operation (LTO)	Ta= 0℃, 240hours	
High Temperature Storage (HTS)	Ta= 60℃, 240hours	
Low Temperature Storage (LTS)	Ta= -20℃, 240hours	
Package Vibration Test	ISTA STANDARD 1.14Grms Random, Frequency Range: 1 ~ 200 Hz Top & Bottom: 30 minutes (+Z), 10 min (-Z), Right & Left: 10 minutes (X) Back & Forth 10 minutes (Y)	(2)
Thermal Shock Test (TST)	-20℃/30min, 60℃ / 30min, 100 cycles	(1)
On/Off Test	25℃, On/10sec, Off /10sec, 30000 cycles	
Altitude Test	Operation: 10000 ft / 24hours Non-Operation: 30000 ft / 24hours	

Note (1) The tests are done with LCD modules.

Note (2) The test is done with a package (24 open cells / 1 Box) shown in Section 8.

11. PRECAUTIONS

11.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the product during assembly.

(2) To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) It is not permitted to have pressure or impulse on the product because the LCD panel will be damaged.

(4) Always follow the correct power sequence when the product is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.

(5) Do not pull the I/F connector in or out while the module is operating.

(6) Use a soft dry cloth without chemicals for cleaning because the surface of polarizer is very soft and easily scratched.

(7) It is dangerous that moisture come into or contacted the product because moisture may damage the product when it is operating.

(8) High temperature or humidity may reduce the performance of module. Please store this product within the specified storage conditions.

(9) When ambient temperature is lower than 10ºC may reduce the display quality. For example, the response time will become slowly.

11.2 SAFETY PRECAUTIONS

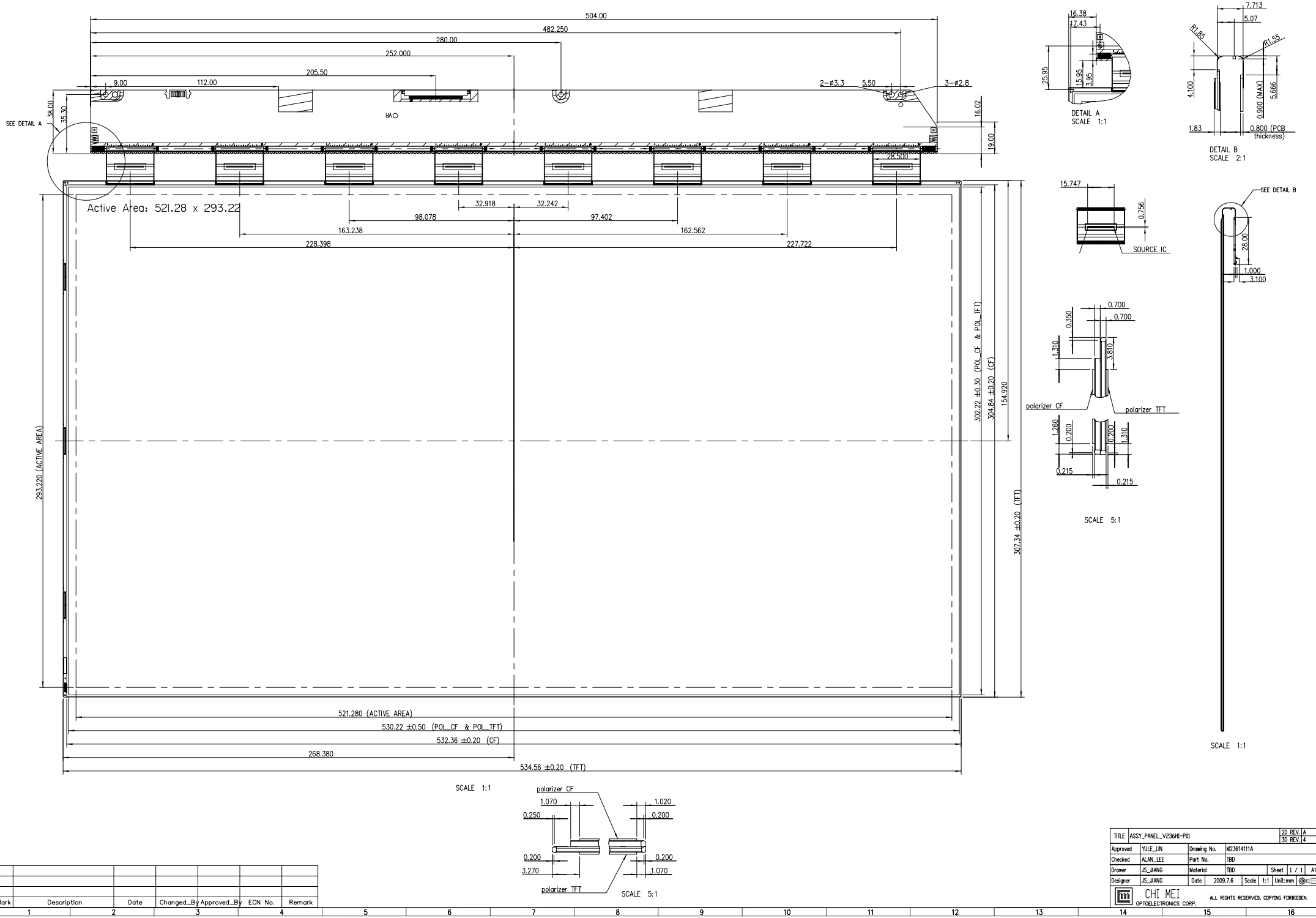
(1) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(2) After the product's end of life, it is not harmful in case of normal operation and storage.

11.3 OTHER

(1) When fixed patterns are displayed for a long time, remnant image is likely to occur.

12. MECHANICAL DRAWING



Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark

TITLE	ASSY_PANEL_V236H1-P01			2D REV.	A
				3D REV.	4
Approved	YULE_LIN	Drawing No.	M23614111A		
Checked	ALAN_LEE	Part No.	TBD		
Drawer	JS_JIANG	Material	TBD	Sheet	1 / 1 A1
Designer	JS_JIANG	Date	2009.7.6	Scale 1:1	Unit:mm

CHI MEI OPTOELECTRONICS CORP.