TFT LCD Approval Specification

MODEL NO.: V420H1 – L15

Customer: _____

Approved by:_____

Note:

Approved By	TV Head Division
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REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 0.0	Nov. 06, 2008	All	All	The tentative specification was first issued.
Ver. 1.0	Dec. 19, 2008	9 11 11-12 13 18 22-23 26 28 33	3.1 3.2.1 3.2.2 3.2.3 5.3 5.5 6.2 7.2 10.2	Updated TFT LCD Module Parameter Updated Lamp Specification Updated BL Electrical Specification Updated Internal PWN Control Voltage Updated Pin 12 define Updated LVDS Interface Updated Power ON/OFF Sequence Updated Optical Specifications Updated Figure.10-1 packing method
Ver. 1.0	Dec. 23, 2008	18	5.3	Updated inverter pin 12 define
Ver. 1.1	Dec. 31, 2008	13	3.2.3	add note(4)
		14	3.2.3	Updated power sequence and control signal timing fig.
Ver. 2.0	Feb. 16. 2009	9 11 15 16~17 21 24 26 27 28~30 33~34 35~37	3.1 3.2.1 4.1 5.5.1 5.4 6.6.1 6.2 7.1 7.2 10.1 11	Update Power Supply Current Update Lamp Specification & Electrical specification UpdateBLOCK DIAGRAM OF INTERFACE Update Input Terminal Pin Assignment Update Block Diagram of Interface note 3 Input Signal Timing Specifications update Update POWER ON/OFF SEQUENCE Updated optical measurement condition Optical Specifications update Update Mechanical Characteristics Update Packaging specifications
Ver. 2.1		33~34 35~37	10.1 11	Update Mechanical Characteristics Update Packaging specifications

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V420H1-L15 is a 42" TFT Liquid Crystal Display module with 12-CCFL Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display 16.7M colors (8-bit/color). The inverter module for backlight is built-in.

1.2 FEATURES

- High brightness (500 nits)
- High contrast ratio (4000:1)
- Fast response time (Gray to gray average 6.5 ms)
- High color saturation (NTSC 72%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 60 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- RoHS compliance

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	930.24(H) x 523.26 (V) (42.02" diagonal)	mm	(1)
Bezel Opening Area	937.24 (H) x 530.26 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.1615 (H) x 0.4845 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating (Haze 11%)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec. of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	-	983.0	-	mm	(1), (2)
	Vertical (V)	-	576.0	-	mm	
	Depth (D)	-	50.8	-	mm	
Weight		-	10400	-	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth is between bezel to T-CON cover.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	ºC	(1)
Operating Ambient Temperature	TOP	0	50	ºC	(1), (2)
Shock (Non-Operating)	SNOP	-	50	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

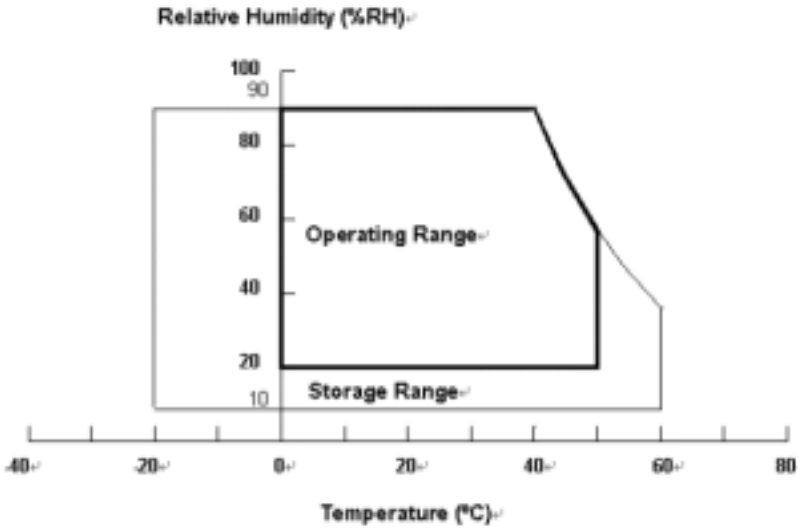
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 ℃ at normal humidity without condensation.

(b) The module shall be stroed in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

2.3.2 BACKLIGHT INVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	VW	–	3000	VRMS	
Power Supply Voltage	VBL	0	30	V	(1)
Control Signal Level	–	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and Internal PWM Control.

3. ELECTRICAL CHARACTERISTICS

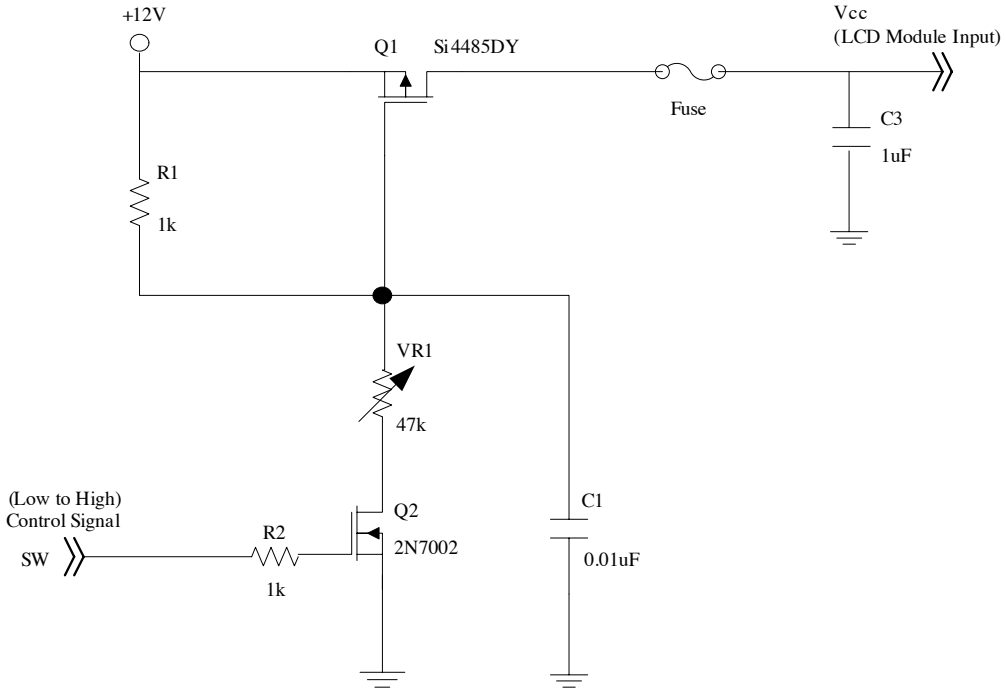
3.1 TFT LCD MODULE

(Ta = 25 ± 2 °C)

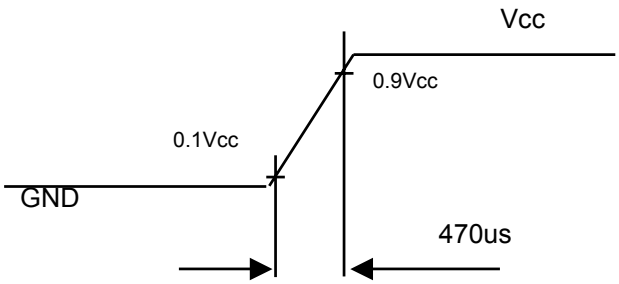
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	-	-	4.3	A	(2)
Power Supply Current	White Pattern	-	-	0.84	1.1	A	(3)
	Vertical Stripe	-	-	0.83	-	A	
	Black Pattern	-	-	0.48	-	A	
LVDS interface	Common Input Voltage	V_{LVC}	1.125	1.25	1.375	V	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

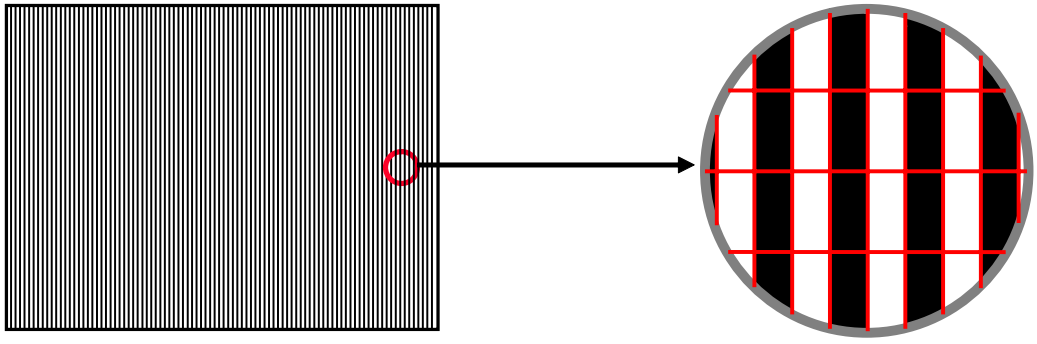
a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



Active Area

3.2 BACKLIGHT CONNECTOR PIN CONFIGURATION

3.2.1 LAMP SPECIFICATION

(Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	VL	-	1090	-	Lamp Input Voltage	VL
Lamp Current	IL	9.7	10.2	10.7	Lamp Current	IL
Lamp Turn On Voltage	VS	-	-	1910	Lamp Turn On Voltage	VS
		-	-	1560		
Operating Frequency	FL	35	-	70	Operating Frequency	FL
Lamp Life Time	LBL	50,000	-	-	Lamp Life Time	LBL

3.2.2 ELECTRICAL SPECIFICATION

(Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P_{BL}	-	130	-	W	(5), IL = 10.2 mA
		-	110	-		(5), IL = 8.7 mA
Power Supply Voltage	V_{BL}	22.8	24.0	25.2	VDC	
Power Supply Current	I_{BL}	-	5.4	-	A	Non Dimming
			4.6			
Input Ripple Noise	-	-	-	912	mVP-P	VBL=22.8V
Oscillating Frequency	F_W	39	42	45	kHz	
Dimming Frequency	F_B	150	160	170	Hz	
Minimum Duty Ratio	D_{MIN}	10	20	-	%	(6)

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board. VIPWM : 3V is 100%,V_{ADIM} = HI : Lamp current is 10.2mA; V_{ADIM} = LO : Lamp current is 8.7mA.

Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

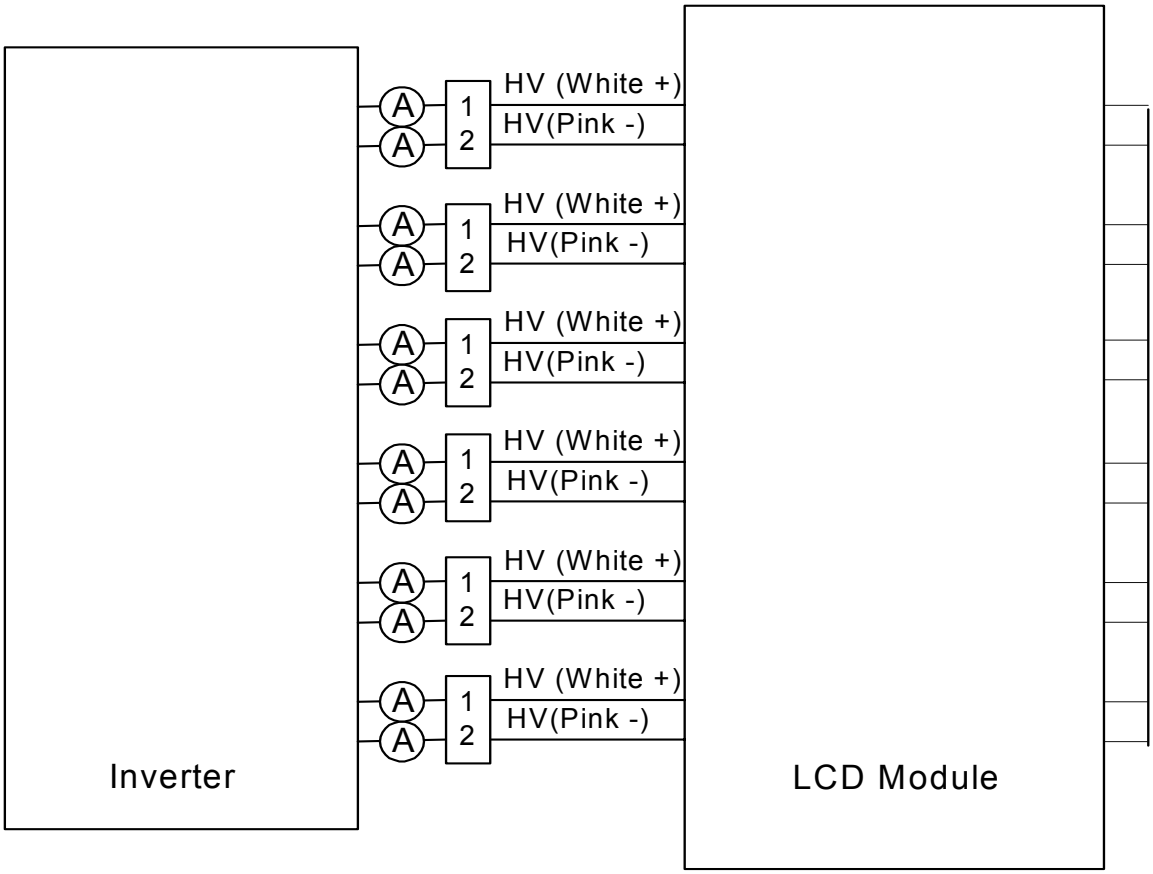
Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency

should be detached from the horizontal synchronous frequency and itó harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2℃ and IL =9.7~10.7 mArms..

Note (5) The measurement condition of Max. value is based on 42” backlight unit under input voltage 24V, average lamp current 10.2 mA and 8.7 mA ,lighting 30 minutes later.

Note (6) 10% minimum duty ratio is only valid for electrical operation.



3.2.3 INVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	V_{BLON}	–	2.0	–	5.0	V	
	OFF		–	0	–	0.8	V	
Internal PWM Control Voltage	MAX	V_{IPWM}	–	3.15	–	5.0	V	Max. Duty Ratio
	MIN		–	–	0	–	V	Min. Duty Ratio
Status Signal	HI	Status	–	3.0	3.3	3.6	V	Normal
	LO		–	0	–	0.8	V	Abnormal
VBL Rising Time		Tr1	–	30	–	–	ms	See as below
VBL Falling Time		Tf1	–	30	–	–	ms	
Control Signal Rising Time		Tr	–	–	–	100	ms	
Control Signal Falling Time		Tf	–	–	–	100	ms	
PWM Signal Rising Time		T_{PWMR}	–	–	–	50	us	
PWM Signal Falling Time		T_{PWMF}	–	–	–	50	us	
Input Impedance		R_{IN}	–	1	–	–	MΩ	
PWM Delay Time		T_{PWM}	–	100	–	–	ms	
BLON Delay Time		T_{on}	–	300	–	–	ms	
BLON Off Time		$\mathbf{T_{on1}}$	–	300	–	–	ms	

Note (1) The dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight turn on period.

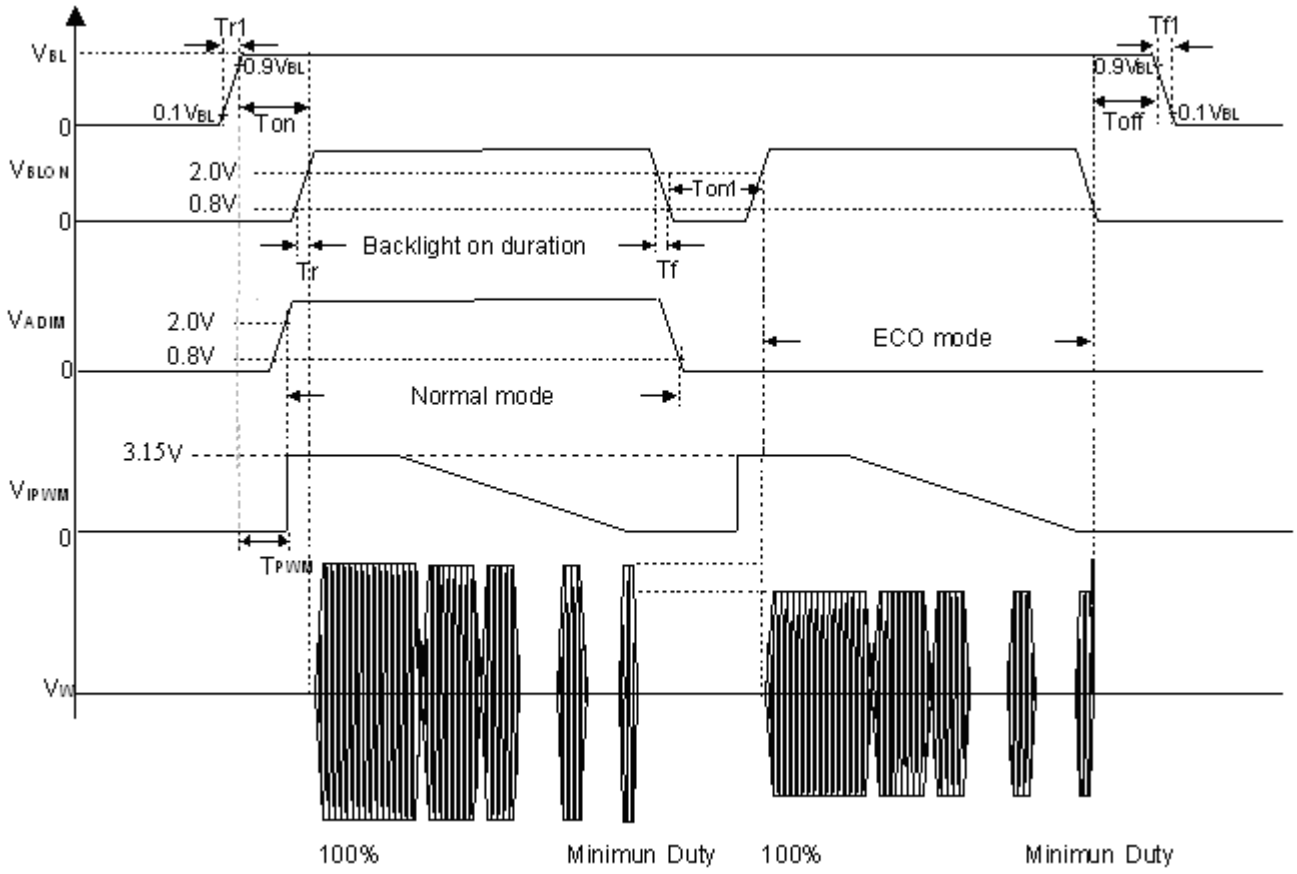
Note (2) The power sequence and control signal timing are shown in the following figure. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

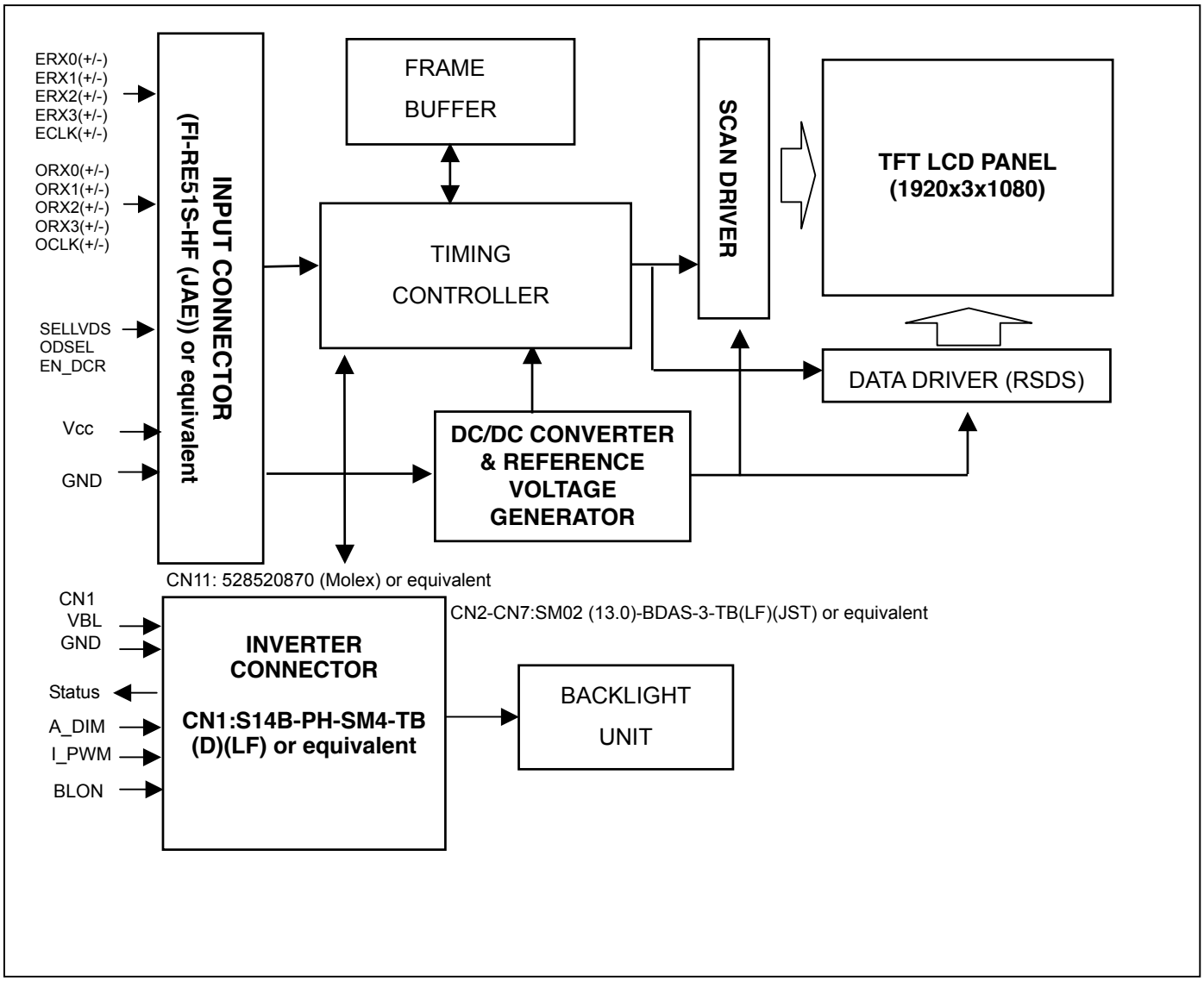
Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) When the Dynamic CR has been turned on, the skipped range of VIPWM, 2.85V ~ 3.15V, is suggested to avoid the abnormal phenomenon.


Tr1
Tf1
VBL
0.9VBL
0.1VBL
Ton
Toff
VBLON
2.0V
0.8V
Ton1
Backlight on duration
Tr
Tf
VADIM
ECO mode
Normal mode
3.15V
VIPWM
TPWM
VW
100%
Minimun Duty
100%
Minimun Duty

4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	SELLVDS	LVDS data format Selection	(2)
8	N.C.	No Connection	(1)
9	ODSEL	Overdrive Lookup Table Selection	(3)
10	N.C.	No Connection	(1)
11	N.C.	No Connection	
12	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	
13	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
14	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
15	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
16	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
17	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	ECLK-	Even pixel Negative LVDS differential clock input	
20	ECLK+	Even pixel Positive LVDS differential clock input	
21	GND	Ground	
22	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	
23	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
24	N.C.	No Connection	
25	N.C.	No Connection	
26	N.C.	No Connection	(1)
27	N.C.	No Connection	(1)
28	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	
29	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
30	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
31	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
32	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
33	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	OCLK-	Odd pixel Negative LVDS differential clock input.	
36	OCLK+	Odd pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	
39	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
40	N.C.	No Connection	
41	N.C.	No Connection	
42	N.C.	No Connection	(1)
43	N.C.	No Connection	(1)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	GND	Ground	

48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

Note (1) Reserved for internal use. Please leave it open.

Note (2) Low : VESA LVDS Format (default), High : JEIDA Format.

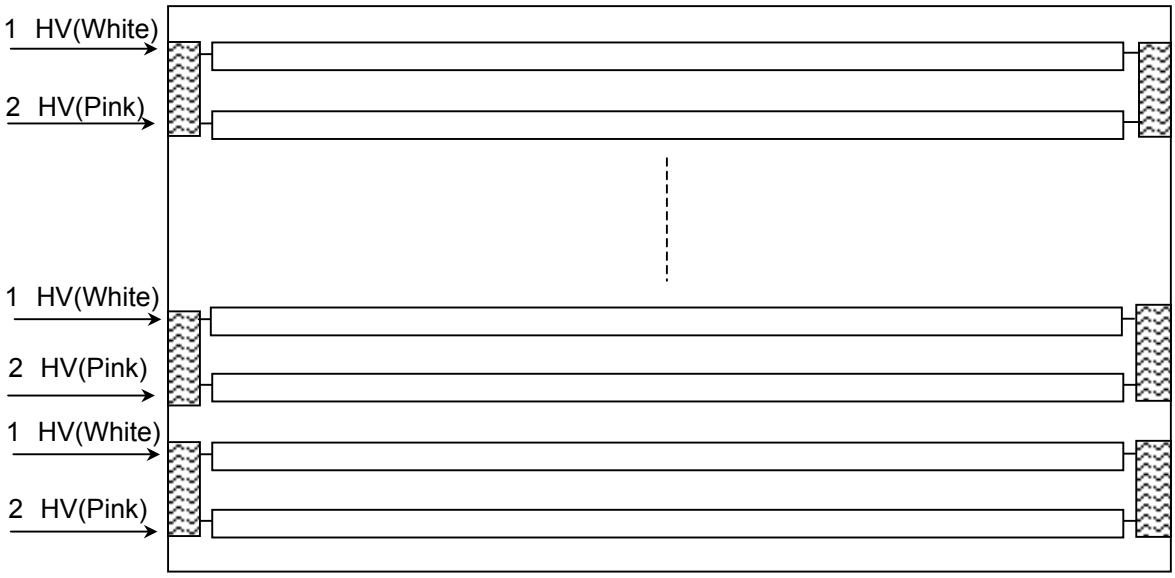
Note (3) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance with the frame rate to optimize image quality.

ODSEL	Note
L	Lookup table was optimized for 60 Hz frame rate.
H	Lookup table was optimized for 50 Hz frame rate.

5.2 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

Pin	Name	Description	Wire Color
1	HV	High Voltage	White
2	HV	High Voltage	Pink



5.3 INVERTER UNIT

CN1: S14B-PH-SM4-TB(D)(LF)(JST) or equivalent

Pin №	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	STATUS	Normal (3.3V) Abnormal(GND)
12	A_DIM	Amplitude Dimming Control HI (2.0V ~ 5.0V) LO(0V~0.8V)
13	I_PWM	Internal PWM Control Signal
14	BLON	BL ON/OFF

CN2-CN7: SM02 -BDAS-3-TB(JST) or equivalent

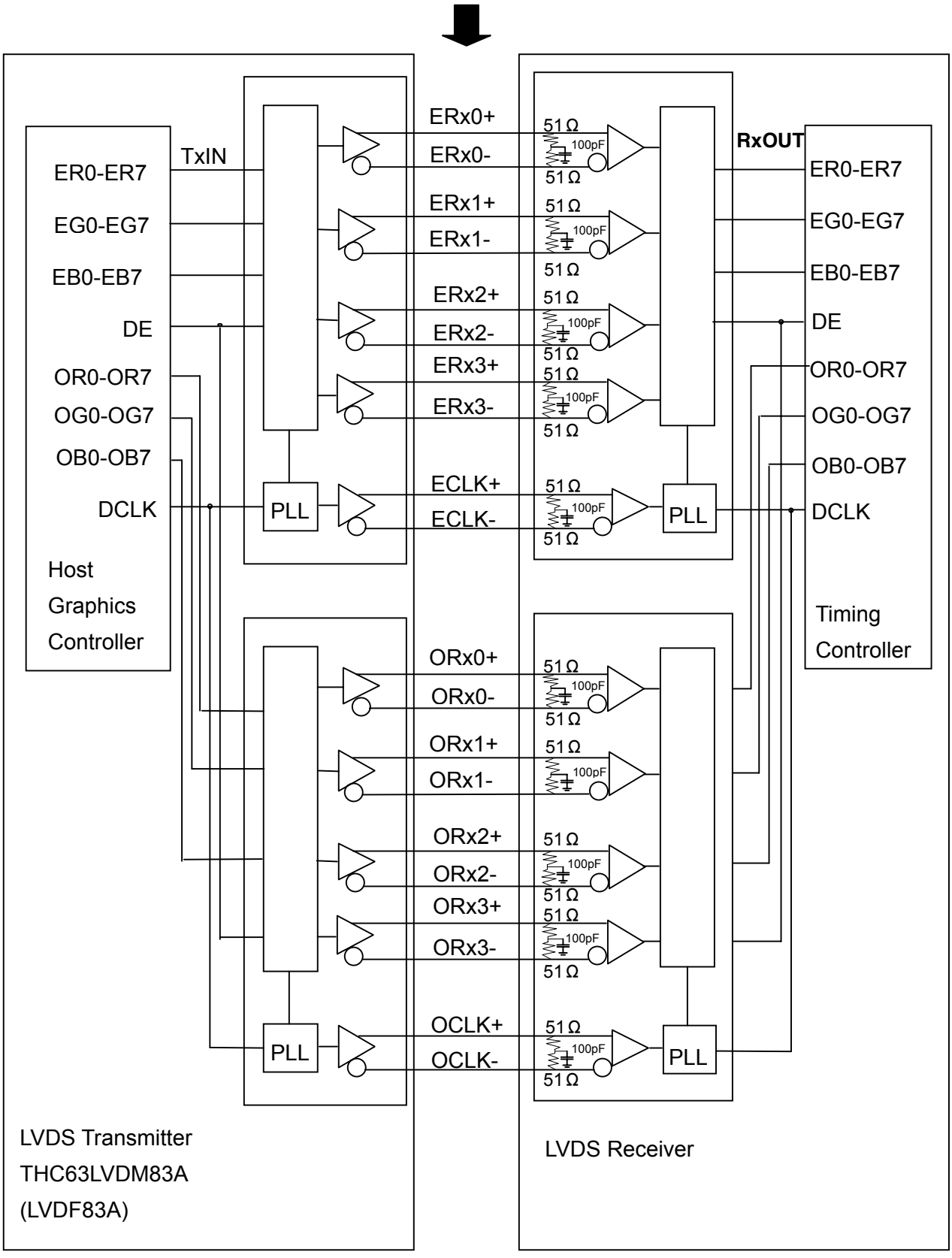
Pin No.	Symbol	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage

CN8: 528520870 (Molex) or equivalent

Pin No.	Symbol	Description
1	Control Signal	Board to Board
2		Board to Board
3		Board to Board
4		Board to Board
5		Board to Board
6		Board to Board
7		Board to Board
8		Board to Board

Note (1) Floating of any control signal is not allowed.

5.4 BLOCK DIAGRAM OF INTERFACE



ER0~ER7: Even pixel R data

EG0~EG7: Even pixel G data

EB0~EB7: Even pixel B data

OR0~OR7: Odd pixel R data

OG0~OG7: Odd pixel G data

OB0~OB7: Odd pixel B data

DE: Data enable signal

DCLK: Data clock signal

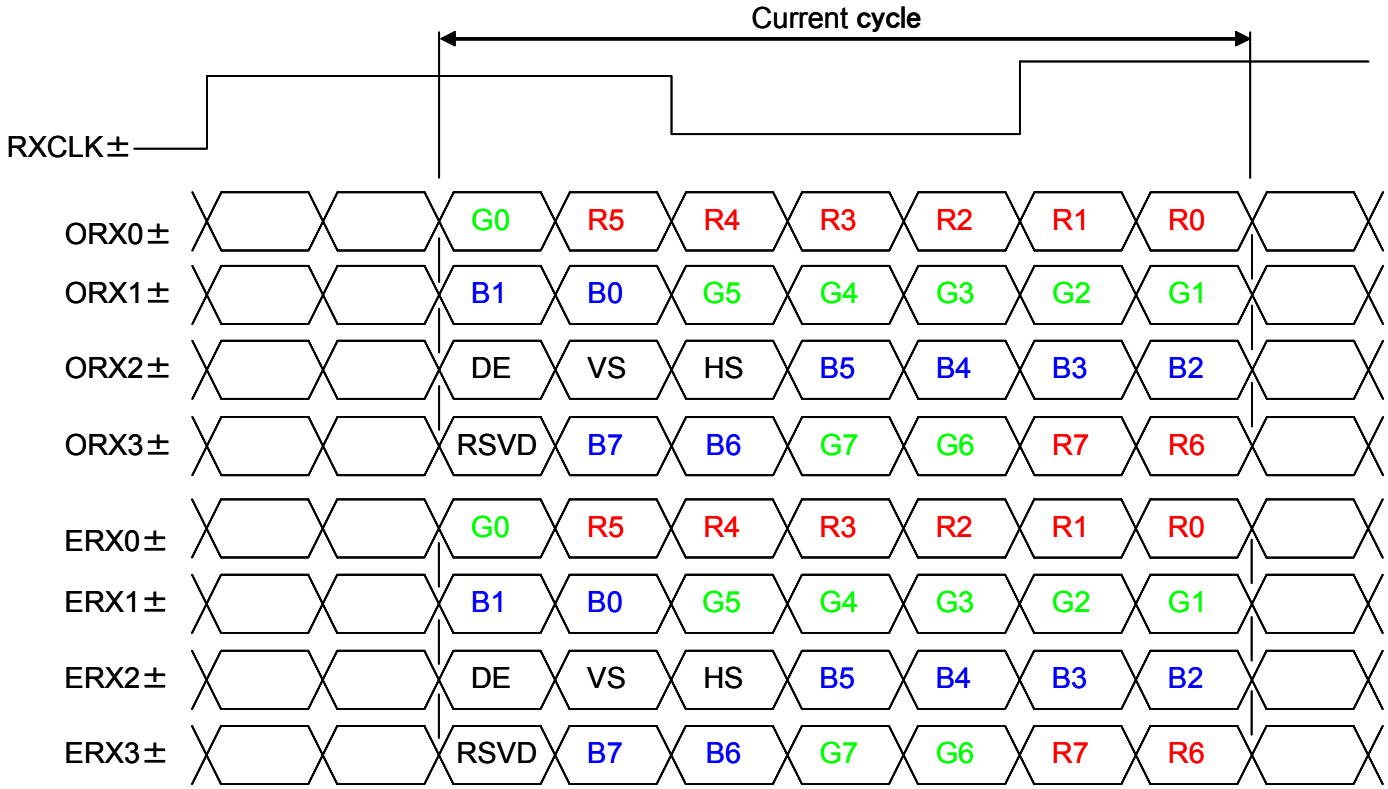
Notes (1) The system must have the transmitter to drive the module.

Notes (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

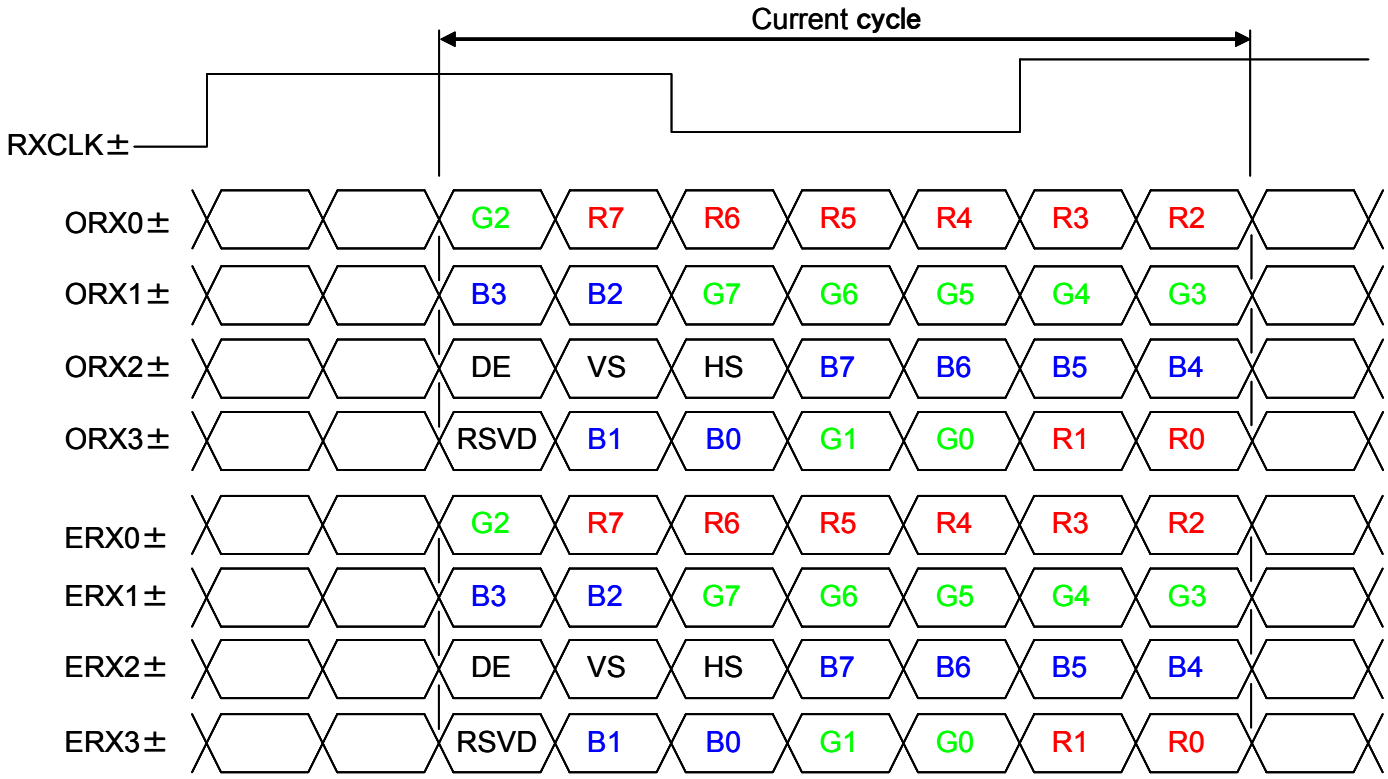
Notes (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

5.5 LVDS INTERFACE

VESA LVDS format：(SELLVDS pin=L)



JEDIA LVDS format：(SELLVDS pin=H)



R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be “H” or “L”.

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 ºC)

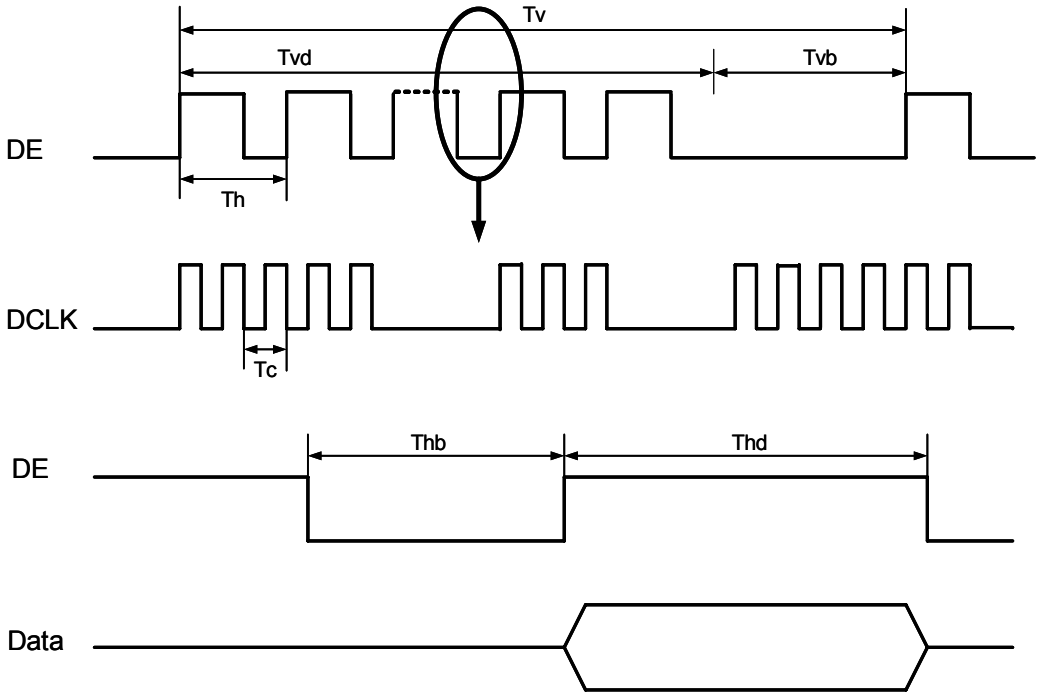
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74.25	80	MHz	-
	Input cycle to cycle jitter	Trcl	-	-	200	ps	-
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	-
	Hold Time	Tlvhd	600	-	-	ps	-
Vertical Active Display Term	Frame Rate	Fr5	47	50	53	Hz	(1)
		Fr6	57	60	63	Hz	(1)
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	35	45	55	Th	-
Horizontal Active Display Term	Total	Th	1050	1100	1150	Tc	Th=Thd+Thb
	Display	Thd	960	960	960	Tc	-
	Blank	Thb	90	140	190	Tc	-

Note (1) : (ODSEL) = (H) , (L). Please refer to 5.1 for detail information

Note (2) : Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

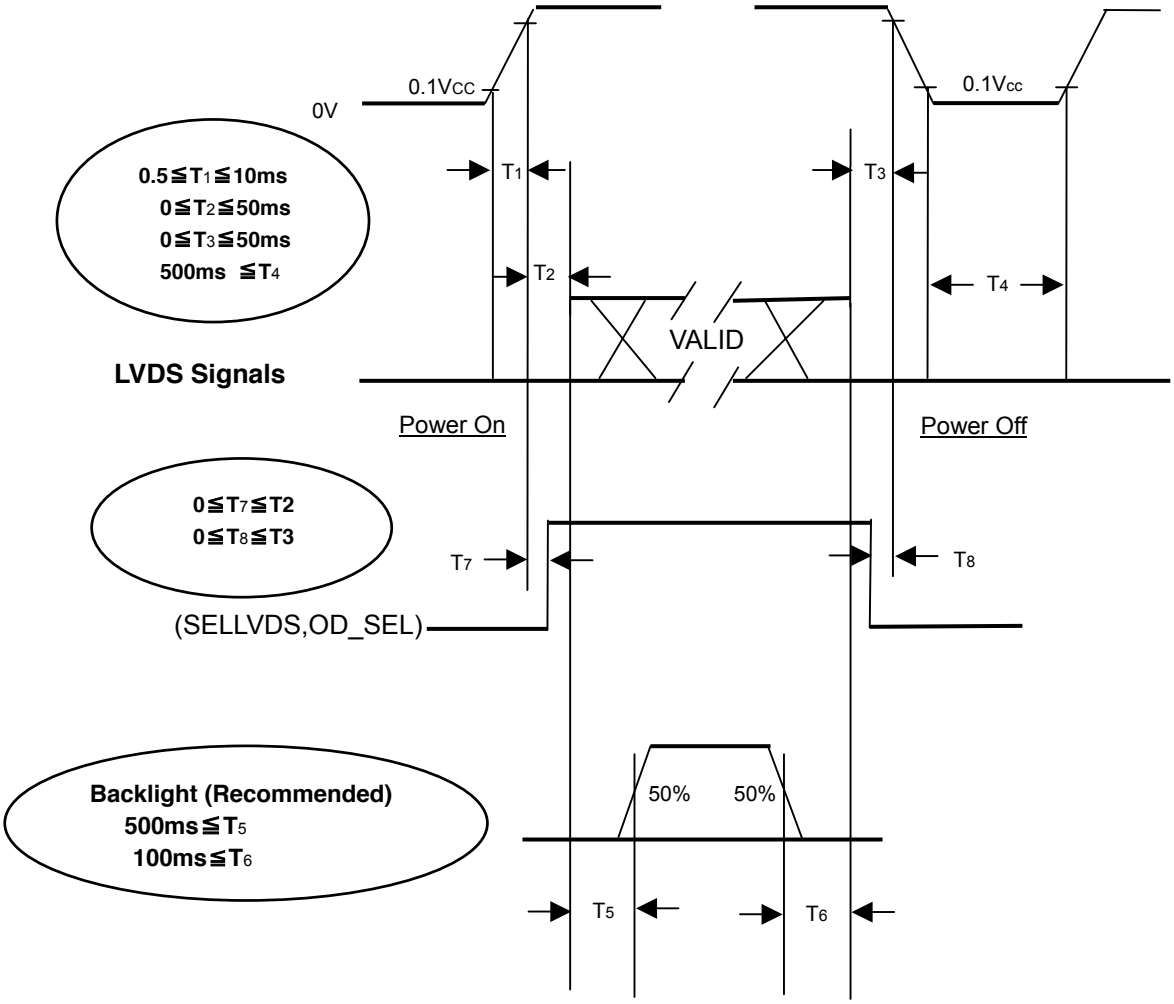
INPUT SIGNAL TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0,that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

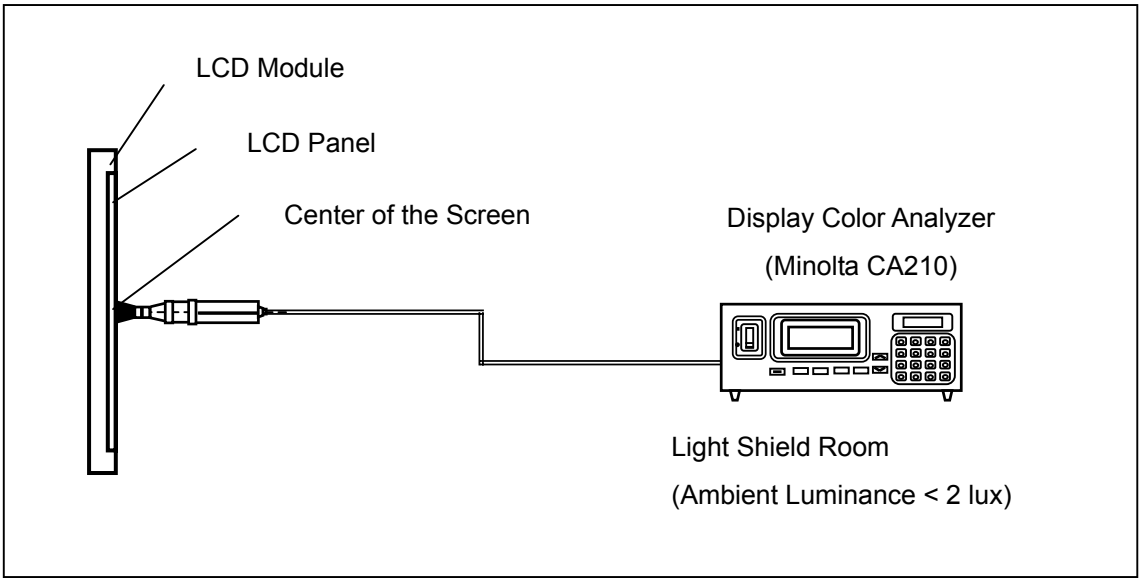
Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	IL	8.7/10.2	mA
Oscillating Frequency (Inverter)	FW	42	KHz
Vertical Frame Rate	Fr	120	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement (CS-1000 or CA-210 calibrated by CS-1000) should be executed after lighting backlight for 1 hour in a windless room.



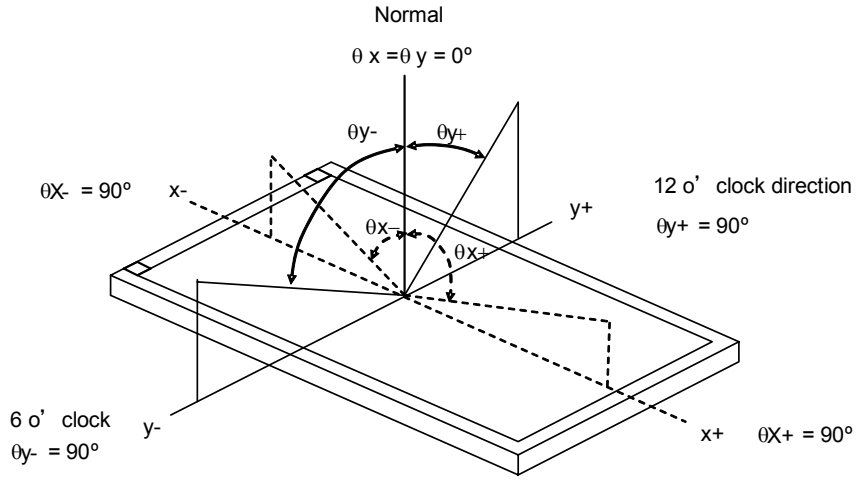
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θx=0°, θy =0° Viewing angle at normal direction	3000	4000	-	-	Note 2
Response Time		Gray to gray		-	6.5	12	ms	Note 3
Center Luminance of White	Noraml mode	LC		400	500	-	cd/m^2	Note 4
	ECO mode	LC		350	450	-	cd/m^2	Note 4, 7
White Variation		δW		-	-	1.3	-	Note 6
Cross Talk		CT		-	-	4	%	Note 5
Color Chromaticity	Red	Rx		Typ. -0.03	0.651	Typ. +0.03	-	-
		Ry			0.330		-	
	Green	Gx			0.270		-	
		Gy			0.608		-	
	Blue	Bx			0.148		-	
		By			0.060		-	
	White	Wx			0.280		-	
		Wy			0.285		-	
	Color Gamut	C.G		-	72	-	%	NTSC
Viewing Angle	Horizontal	θx+	CR≥20	80	88	-	Deg.	Note (1)
		θx-		80	88	-		
	Vertical	θY+		80	88	-		
		θY-		80	88	-		

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Eldim EZ-Contrast 160R



Note (2) Definition of Contrast Ratio (CR):

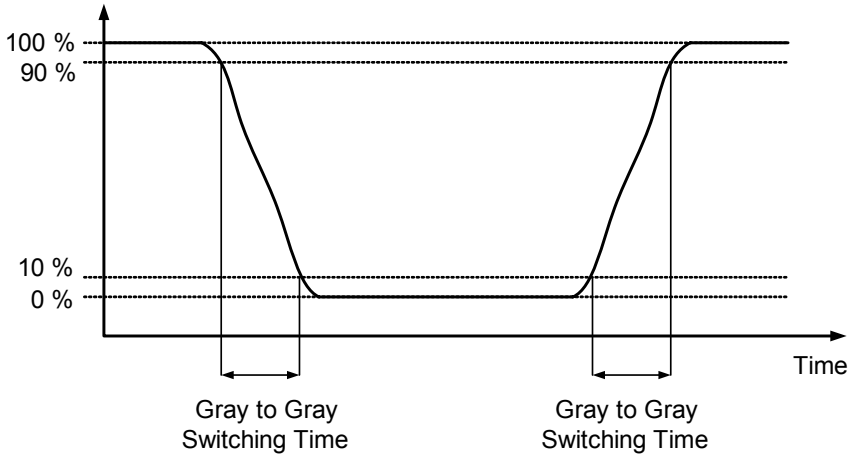
The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time:

Optical Response



The driving signal means the signal of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255.

Gray to gray average time means the average switching time of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255 to each other.

Note (4) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

L_C = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (6).

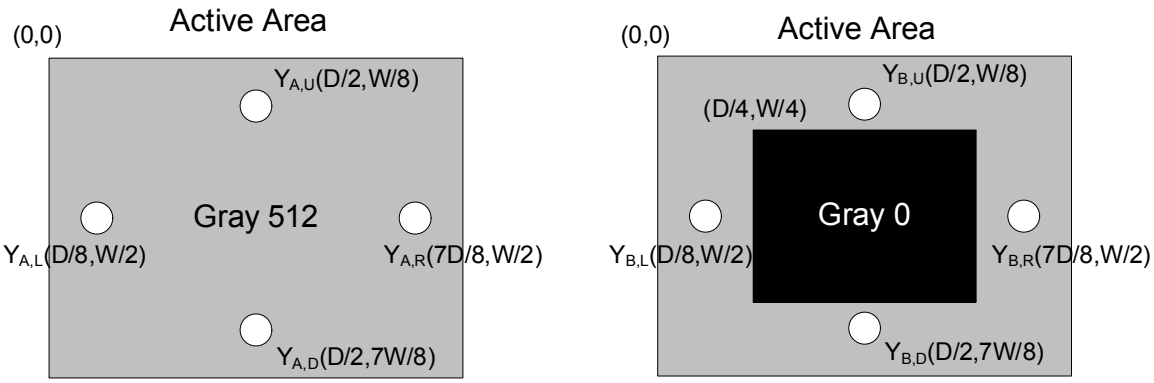
Note (5) Definition of Cross Talk (CT):

CT = | YB – YA | / YA × 100 (%)

Where:

YA = Luminance of measured location without gray level 0 pattern (cd/m2)

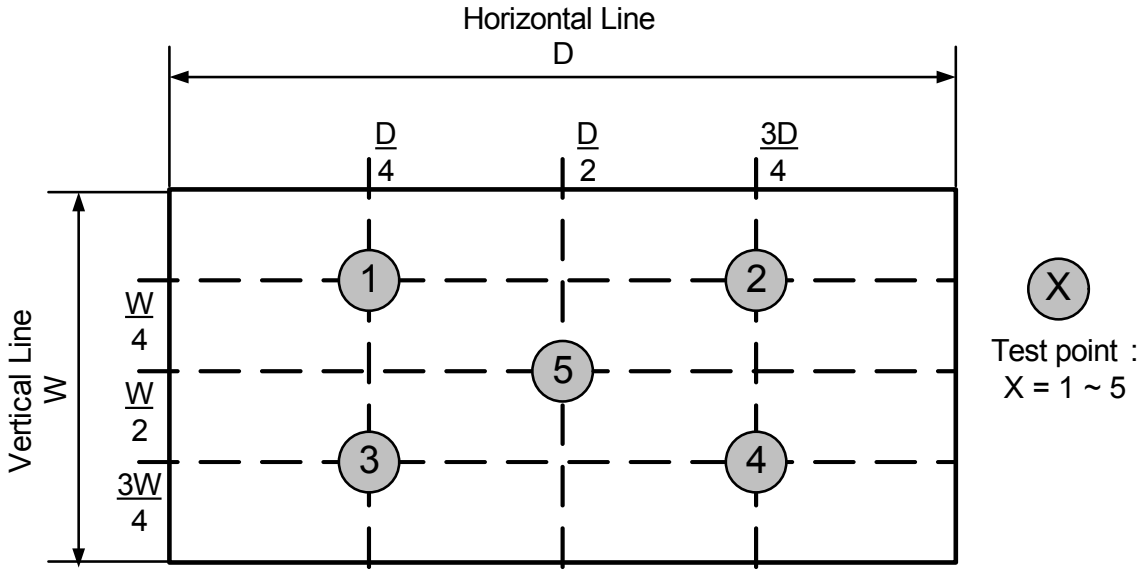
YB = Luminance of measured location with gray level 0 pattern (cd/m2)



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



Note (7) ECO mode:

ECO mode was selected by inverter pin: A_DIM.

8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[5] Do not plug in or pull out the I/F connector while the module is in operation.

[6] Do not disassemble the module.

[7] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[8] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[9] When storing modules as spares for a long time, the following precaution is necessary.

[9.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

[9.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[10] When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

[1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

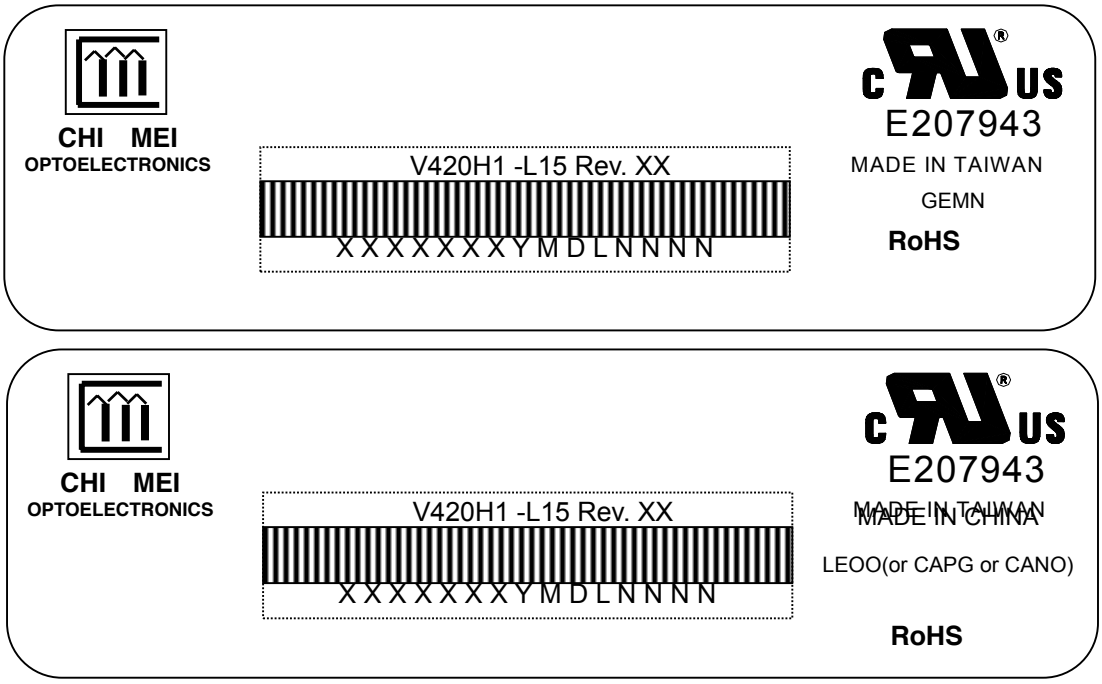
[2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[3] After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 CMO MODULE LABEL

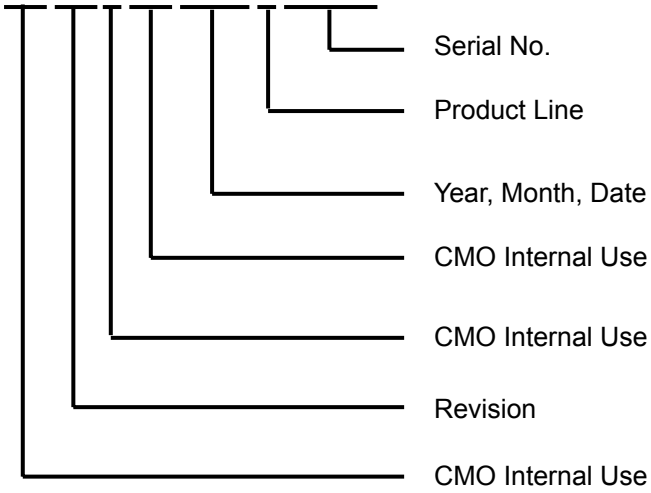
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V420H1-L15

Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year: 0~9, for 2000~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

Serial No.: Manufacturing sequence of product

Product Line: 1 -> Line1, 2 -> Line 2, …etc.

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

(1) 4 LCD TV modules / 1 Box

(2) Box dimensions : 1100(L)x317(W)x670(H)mm

(3) Weight : Approx. 53.17Kg(4 modules per carton)

10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method

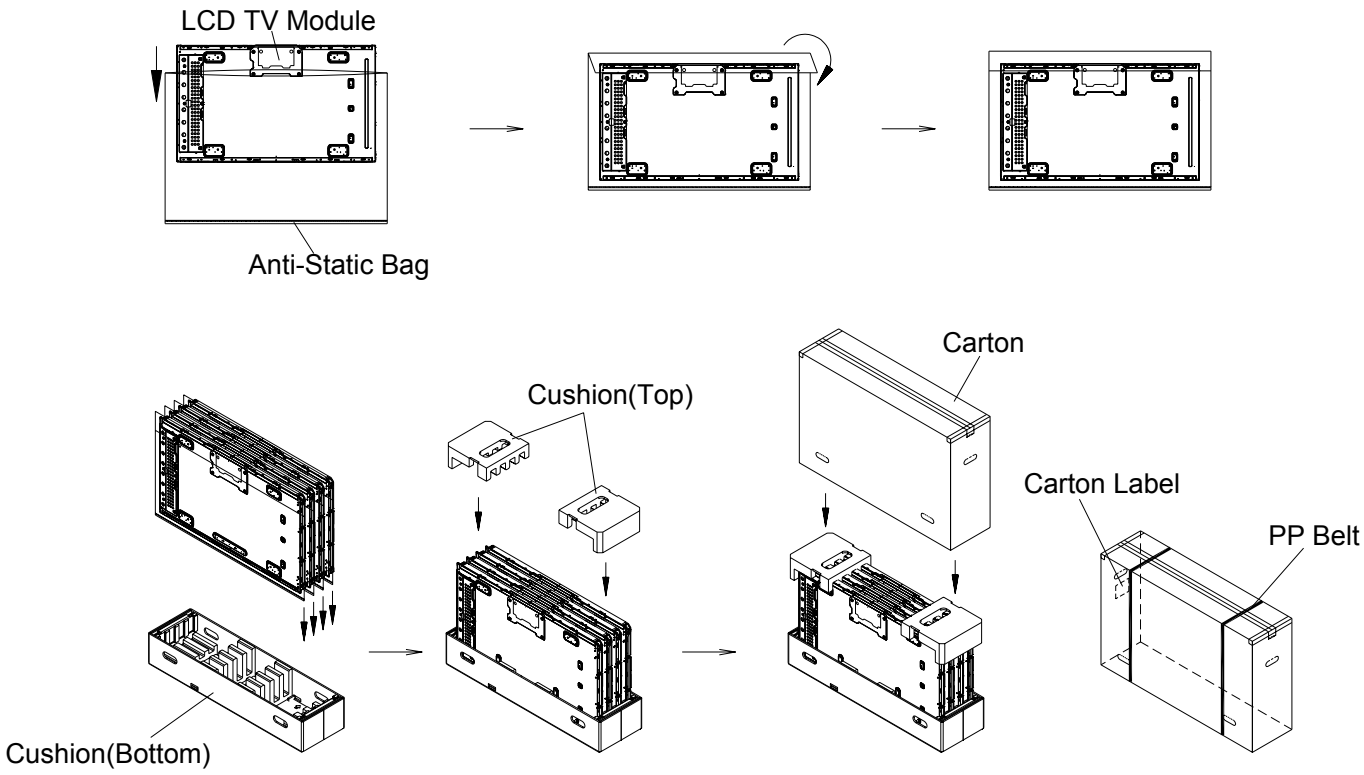
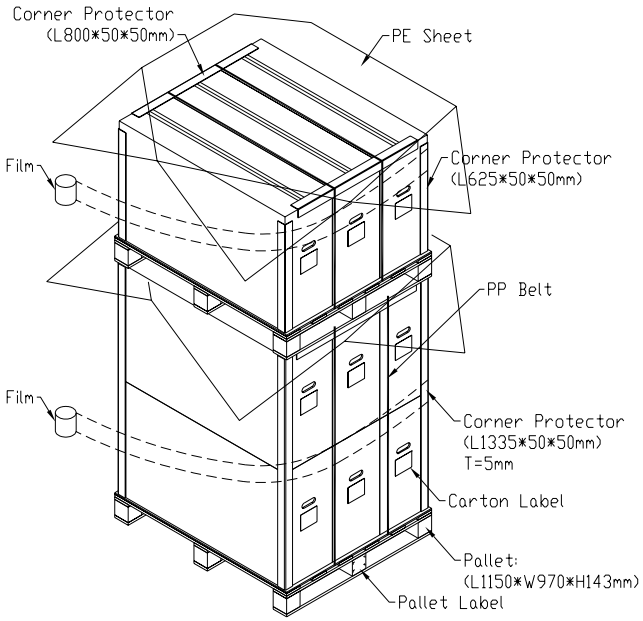


Figure.10-1 packing method

Sea / Land Transportation
(40ft Container)

Air Transportation



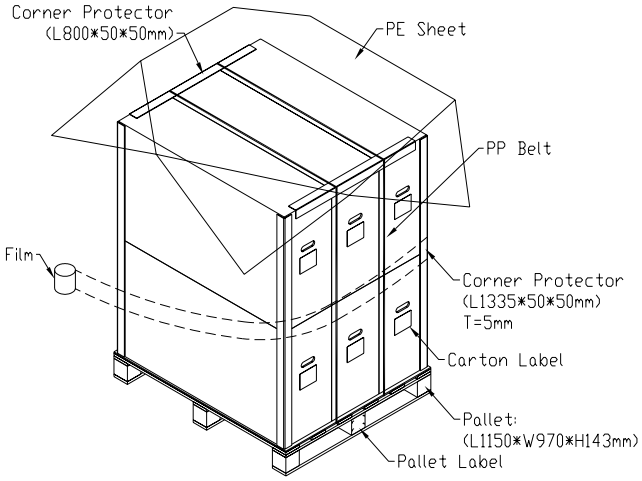
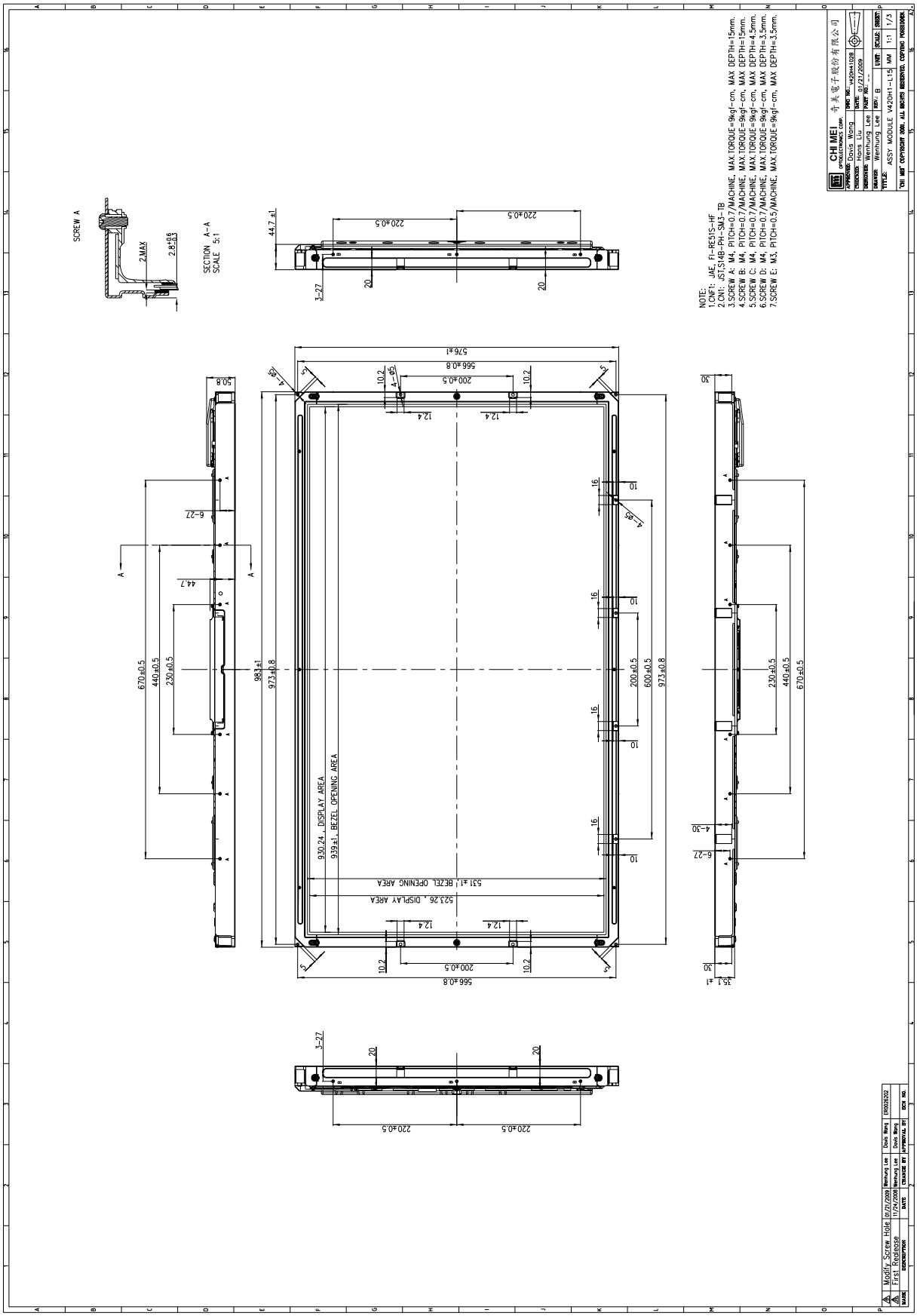
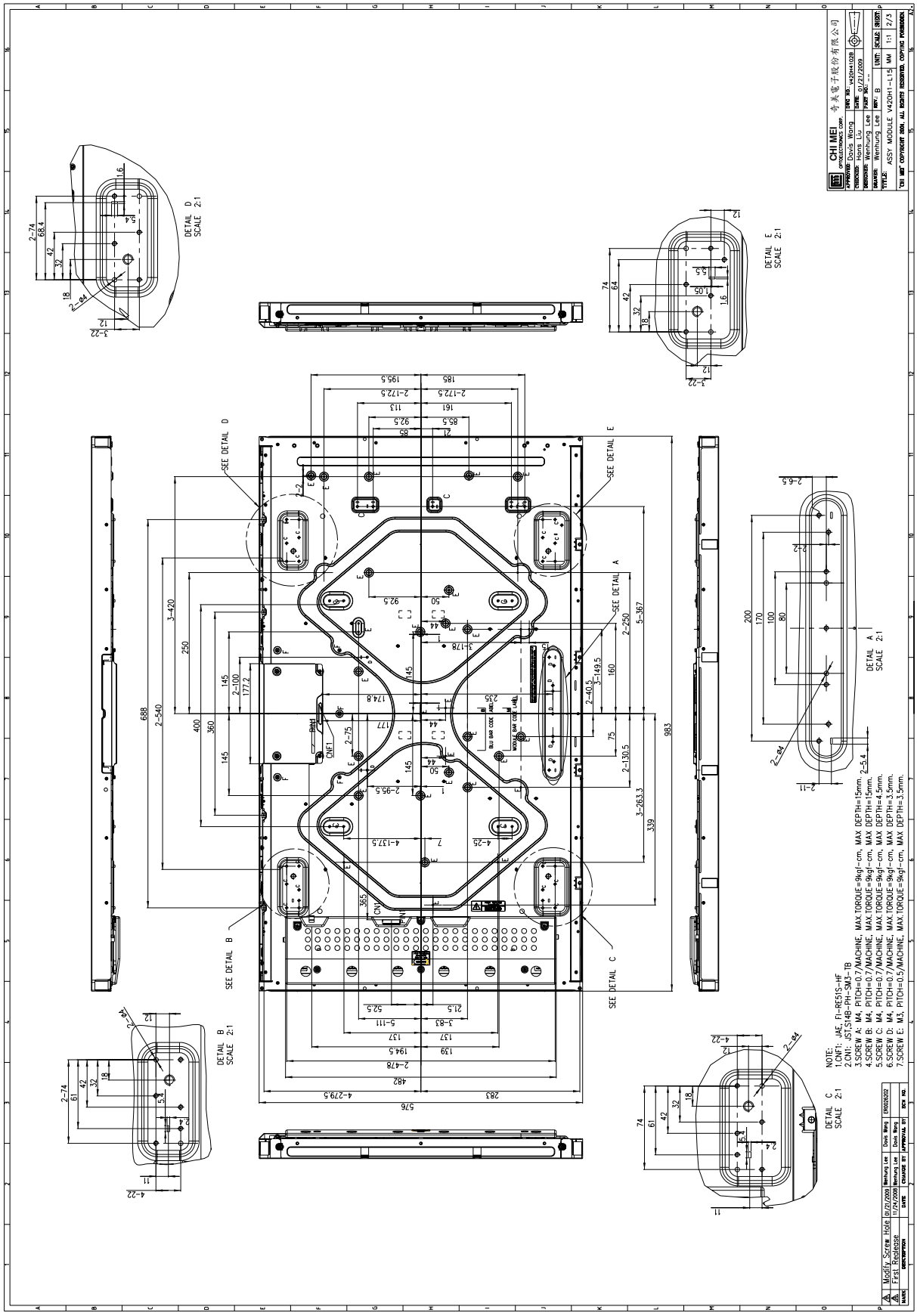
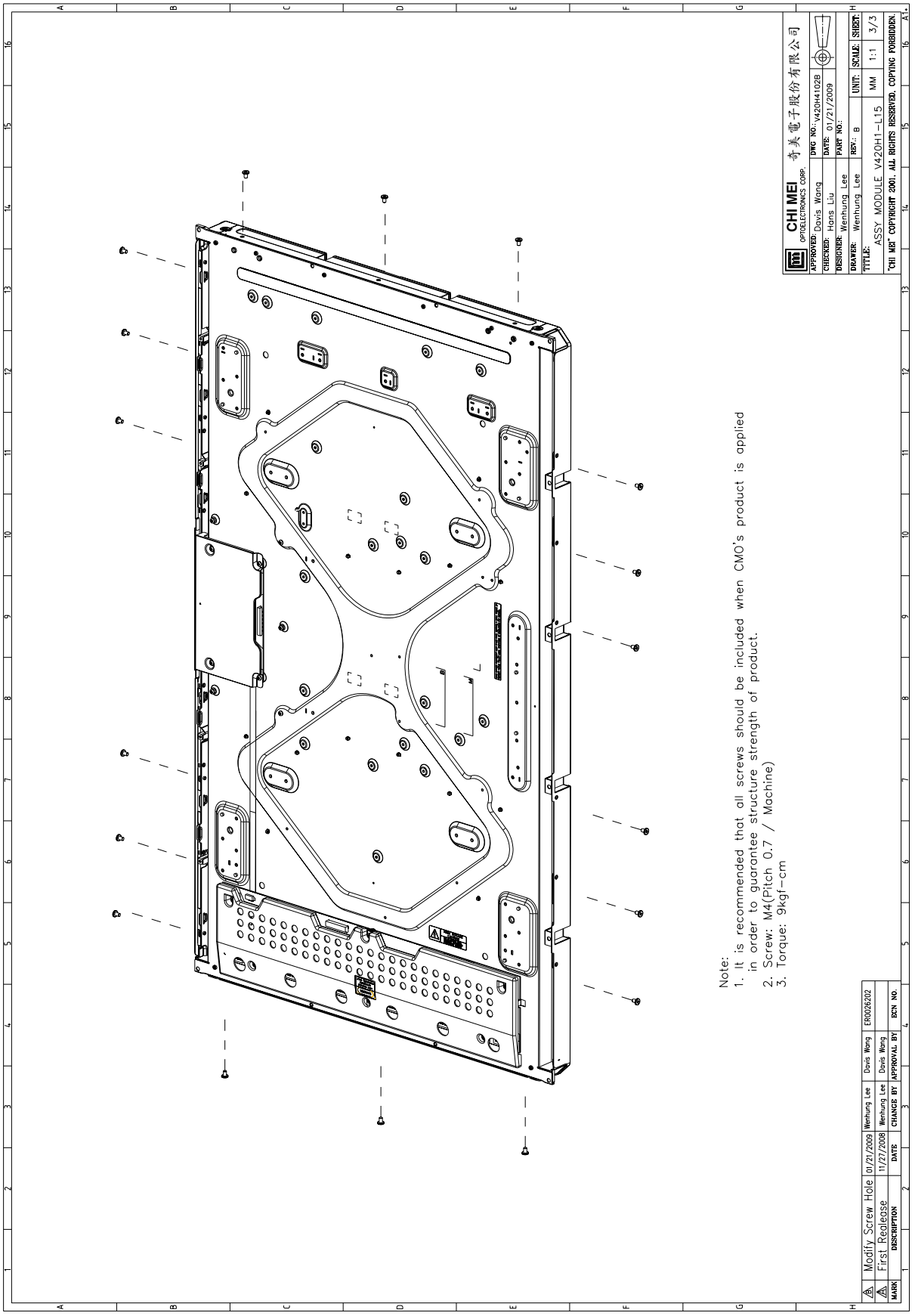


Figure.10-2 packing method

11. MECHANICAL CHARACTERISTICS




DETAIL D
SCALE 2:1
DETAIL E
SCALE 2:1
SEE DETAIL D
SEE DETAIL E
SEE DETAIL A
SEE DETAIL B
SEE DETAIL C
DETAIL A
SCALE 2:1
DETAIL B
SCALE 2:1
DETAIL C
SCALE 2:1
CHI MEI
ASSY MODULE V420H1-L15
NOTE:
1.CNF1: JAE FI-RE51S-HF
2.CN1: JST S14B-PH-SM3-TB
3.SCREW A: M4, PITCH=0.7/MACHINE, MAX.TORQUE=9kgf-cm, MAX DEPTH=15mm
4.SCREW B: M4, PITCH=0.7/MACHINE, MAX.TORQUE=9kgf-cm, MAX DEPTH=15mm
5.SCREW C: M4, PITCH=0.7/MACHINE, MAX.TORQUE=9kgf-cm, MAX DEPTH=4.5mm
6.SCREW D: M4, PITCH=0.7/MACHINE, MAX.TORQUE=9kgf-cm, MAX DEPTH=3.5mm
7.SCREW E: M3, PITCH=0.5/MACHINE, MAX.TORQUE=9kgf-cm, MAX DEPTH=3.5mm
Modify Screw Hole
First Release


Note:
1. It is recommended that all screws should be included when CMO's product is applied in order to guarantee structure strength of product.
2. Screw: M4(Pitch 0.7 / Machine)
3. Torque: 9kgf-cm
CHI MEI OPTOELECTRONICS CORP.
奇美電子股份有限公司
APPROVED: Davis Wang
CHECKED: Hans Liu
DESIGNED: Wenhung Lee
DRAWER: Wenhung Lee
DWG NO: V420H4102B
DATE: 01/21/2009
PART NO.:
REV: B
UNIT: MM
SCALE: 1:1
SHEET: 3/3
TITLE: ASSY MODULE V420H1-L15
"CHI MEI COPYRIGHT 2001. ALL RIGHTS RESERVED. COPYING FORBIDDEN."
MARK DESCRIPTION DATE CHANGE BY APPROVAL BY ECN NO.
Modify Screw Hole 01/21/2009 Wenhung Lee Davis Wang ER0026202
First Release 11/27/2008 Wenhung Lee Davis Wang