

# Chunghwa Picture Tubes, Ltd. Technical Specification

To:

Date: 2008/04/30

CPT TFT-LCD

CLAA154WB05A

**ACCEPTED BY:** 

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#### **RECORD OF REVISIONS**

Revision No.		Page	Description
1	2006/6/02		Tentative specification for 154WB05A was the NEW edition issued.
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#### 1. OVERVIEW

**CLAA154WB05A** Nis 15.4" color (39.116cm) TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, LVDS driver ICs, control circuit and backlight. By applying 6 bit digital data, 1280×RGB(3)×800, 262K-color images are displayed on the 15.4" diagonal screen. General specifications are summarized in the following table:

ITEM	SPECIFICATION
Display Area (mm)	331.2 (H)x207.0 (V) (15.4-inch diagonal)
Number of Pixels	1280 x3(H)x800(V)
Pixel Pitch (mm)	0.25875(H)×0.25875(V)
Color Pixel Arrangement	RGB vertical stripe
Display Mode	Normally white
Number of Colors	262,144(6bits)(RSDS)
Gamut	50%(typ); 45%(min)
Optimum Viewing Angle	6 o'clock
Response Time (ms)	16ms
Viewing Angle	40° \ 40° /10° \ 30° (Min.)
Brightness (cd/m^2)	200 cd/m <sup>2</sup> (5point)/6 mA ( <b>Typ</b> .)
Brightness (Cd/IIF 2)	170 cd/m <sup>2</sup> (5point)/6 mA ( <b>Min.</b> )
Uniformity	5point: <b>80</b> %
Chiloritaty	13point: <b>75</b> %
Consumption of Power (W)	7W (Max)
Module Size (mm)	344.5(W)x222.5(H)x6.2(D) ( Max )
Module Weight (g)	585 (max)

The LCD Products listed on this document are not suitable for use of aerospace equipment, submarine cable, and nuclear reactor control system and life support systems. If customers intend to use these LCD products for applications listed above or those not included in the "Standard" list as follows, please contact our sales in advance.

Standard: Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tool, Industrial robot, Audio and Visual equipment, Other consumer products.

#### 2. ABSOLUTE MAXIMUM RATINGS

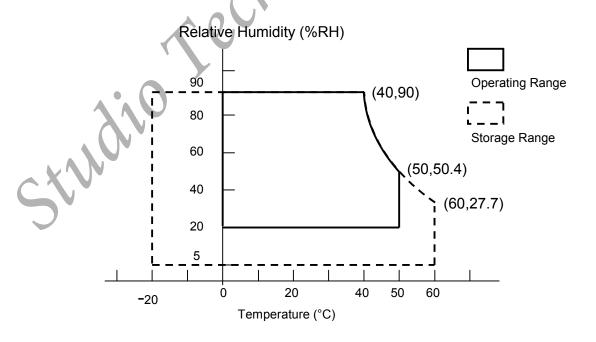
FD1 C 11 ' '	1	1 1 1 1 1 1 1		C 1.	. •	11
The following are maximum v	zalne v	which it exceeded	may	v cause faulty	operation or	damage to the limit
The following are maximum v	aruc,	Willell II CACCCGCG	, ma	y cause raurty	operation of	damage to the unit.

ITEM	SYMBOL	MIN.	MAX.	UNIT	REMARK
Power Supply Voltage for LCD	VCC	0	4.0	V	
Lamp voltage	VL	700	945	Vrms	
Lamp current	IL	3	6.5	mArms	*1). 2)
Lamp frequency	FL	50	80	kHz	
Operation Temperature	Тор	0	50	$^{\circ}\!\mathbb{C}$	*3). 4). 5). 6)
Storage Temperature	Tstg	-25	65	$^{\circ}\!\mathbb{C}$	*3). 4). 5)
Delayed Discharge Time	TD		1	sec	*7)

#### [Note]

- \*1) Product life-time relate to lamp current, please operate production follow statement at page 9 "(b)back light".
- \*2) When lamp current over the definition of absolute max. ,product life-time will decay rapidly or operate unusual.
- \*3) The relative temperature and humidity range are as below sketch, 90%RH Max. (Ta  $\leq$  40°C)
- \*4) The maximum wet bulb temperature  $\leq 39^{\circ}$  (Ta>40°C) and without dewing.
- \*5) If product in environment which over the definition of the relative temperature and humidity out of range too long, it will affect visual of LCD.
- \*6) If you operate LCD in normal temperature range, the center surface of panel should be under  $60\,^{\circ}\mathrm{C}$ .
- \*7) Delay discharge time test condition : starting lamp voltage=1650Vrms.(please follow statement at page 9 "(b)back light"

Before test TD,lamp should operate at least 1min,and lamp current should follow trpical lamp current specification. To place panel at room temp.( $25\pm2^{\circ}$ C)below for 24hrs.,and then to measue TD with the same starting lamp voltage in dark room.



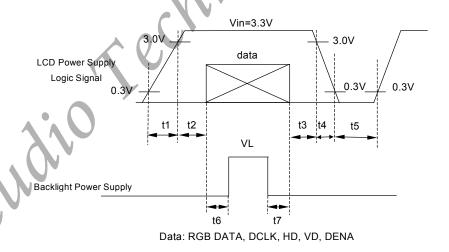
# 3. ELECTRICAL CHARACTERISTICS (A) TFT LCD

TEM		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
LCD POWER VOLTAGE		VCC	3.0	3.3	3.6	V	[Note 1]
LCD PO	WER CURRENT	ICC	-	400	600	mA	[Note 2]
Rusl	n CURRENT	Irush	-	-	2	A	[Note 3]
	INPUT VOLTAGE	VIN	0	-	VCC	V	
LOGIC INPUT	COMMON VOLTAGE	VCM	1.125	1.25	1.375	V	1
VOLTAGE (LVDS:	DIFFRENTIAL INPUT VOLTAGE	VID	250	350	450	mV	x O
IN+,IN-) [Note 3]	THRESHOLD VOLTAGE (HIGH)	VTH	-	-	100	mV	When $VCM = +1.2V$
THRESHOLD VOLTAGE (LOW)		VTL	-100	-	-	mV	
DIFFRENTIAL INPUT VOLTAGE TOLERANCE		△VID	-	-	35	mV	
	ION VOLTAGE DLERANCE	△VCM	-	-	35	mV	

# [Note 1] Power Sequence:

 $\begin{array}{lll} t1 \! \leq \! 10 ms & 1 \; sec \! \leq \! t5 \\ 0.01 \; ms \! < \! t2 \! \leq \! 50 \; ms & 200 \; ms \! \leq \! t6 \\ 0.01 \; ms \! < \! t3 \! \leq \! 50 \; ms & 200 \; ms \! \leq \! t7 \end{array}$ 

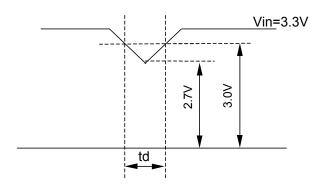
 $0.01 \text{ ms} < t4 \le 10 \text{ ms}$ 



VCC-dip state

(1)when 3.0 > VCC $\geq$  2.7V , td $\leq$  10 ms

(2)when VCC < 2.7V  $\,^{\circ}$  VCC-dip condition should as the VCC-turn-off condition.



[Note 2]

Typical value is  $0 \sim 63$  gray level.(horizontal line Pattern)

800 line mode , VCC = +3.3V

Circuit condition(Typ.)

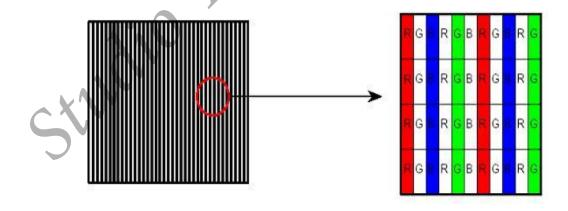
VCC=3.3 V  $^{,}$   $f_{v}\!\!=\!\!60$  Hz  $f_{\scriptscriptstyle H}\!\!=\!\!48.9$  kHz  $^{,}$   $f_{\scriptscriptstyle CLR}\!\!=\!\!68.9$  MHz



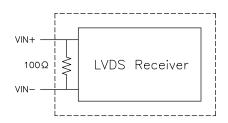
64-Gray : 0 ~ 63 Gray

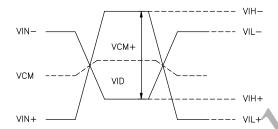
Circuit condition(MAX.)

VCC=3.3 V , fv=60 Hz f=48.9 kHz , fclk=68.9 MHz



[Note 3] LVDS Signal Definite:





VIN+ : Positive differential DATA & CLK Input

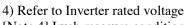
VIN- : Negative differential DATA & CLK Input

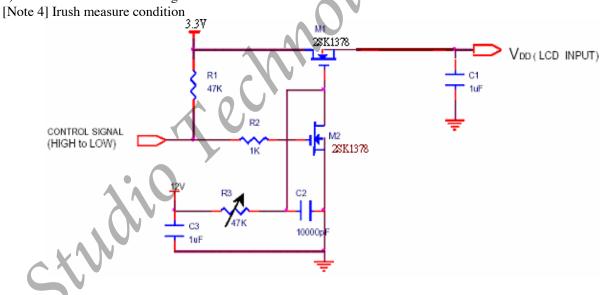
$$\begin{split} VID &= VIN_{+} - VIN_{-}, \\ \triangle VCM &= \mid VCM_{+} - VCM_{-} \mid , \\ \triangle VID &= \mid VID_{+} - VID_{-} \mid , \\ VID_{+} &= \mid VIH_{+} - VIH_{-} \mid , \\ VID_{-} &= \mid VIL_{+} - VIL_{-} \mid , \end{split}$$

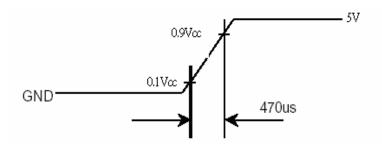
 $VCM = (VIN_+ + VIN_-)/2,$ 

 $VCM+=(VIH_{+}+VIH_{-})/2,$ 

 $VCM = (VIL_+ + VIL_-)/2$ 







#### (B) BACK LIGHT

#### (a.) ELECTRICAL CHARACTERISTICS

Ta=25°C

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	REMARK
Lamp Voltage(IL=6.0mA)	VL	657	700	803	Vrms	IL=6.0mA
Lamp Current	IL	3	6.0	6.5	mArms	*1)
Inverter Frequency	FI	50		60	kHz	*2)
Lamp Initial Voltage	VS	1460			Vrms	Ta=25°C
Lamp initial voltage	V S	1730			Vrms	Ta=0°C

#### (b) LAMP LIFE – TIME

ITEM	IL at 2.0 mA	IL at 6.0 mA	IL at 6.5 mA	單位	備註
LAMP LIFE-TIME (LT)	Min. 15,000	Min. 15,000	Min.10,000	hr	Continuous Operation*3)
Turn-on and turn-off Operation		Min.100,000		times	Continuous Operation *4)

<sup>\*1)</sup>Measure method: galvanometer connect to low voltage



\*2)Frequency in this range can make the characterisitics of electric and optics maintain in +/- 10% except hue.

Lamp frequency of inverter may produce interference with horizontal synchronous frequency, and this may cause horizontal beat on the display. Therefore, please adjust lamp frequency, and keep inverter as far from module as possible or use electronic shielding between inverter and module to avoid the interference.

Under optimum operate frequency range (50~80 KHz), will not effect panel life-time and relability.

- \*3) Definition of the lamp life time:
  - a. Luminance (L) under 50% of specification starting lamp voltage
  - b. Starting Lamp Voltage: over130% of the initial value. Ta=25℃
- \*4) For keeping good lighting situation ,when design the inverter,it must be considered that the voltage large than starting lamp voltage.
- \*5) WL=IL x VL  $\circ$  (IL=6mA  $\cdot$  Ta=25 $^{\circ}$ C)

#### 4. Connector Interface PIN & Function

(a) CN1(Interface signal)

Outlet connector: FI-XB30SL-HF10 (JAE) , AL2304-A0G1D-P(P-TWO)

Link connector: FI-X30H (JAE, Link Type )
(Note) DDC: Display Data Requirements

(Note)Refer to page6、7、8、9之 Data Mapping

Pin No. SYMBOL FUNCTION  1 Vss Ground 2 Vin +3.3V Power 3 Vin +3.3V Power 4 V_EDID DDC 3.3V Power 5 NC No Connect 6 CLK_EDID DDC Clock 7 DATA_EDID DDC Data 8 RON minus signal of channel 0(LVDS) 9 ROP plus signal of channel 0(LVDS) 10 Vss Ground 11 R1N minus signal of channel 1(LVDS) 12 R1P plus signal of channel 1(LVDS) 13 Vss Ground 14 R2N minus signal of channel 2(LVDS) 15 R2P plus signal of channel 2(LVDS) 16 Vss Ground 17 RCLKN minus signal of clock channel (LVDS)	
2 Vin +3.3V Power 3 Vin +3.3V Power 4 V_EDID DDC 3.3V Power 5 NC No Connect 6 CLK_EDID DDC Clock 7 DATA_EDID DDC Data 8 R0N minus signal of channel 0(LVDS) 9 R0P plus signal of channel 0(LVDS) 10 Vss Ground 11 R1N minus signal of channel 1(LVDS) 12 R1P plus signal of channel 1(LVDS) 13 Vss Ground 14 R2N minus signal of channel 2(LVDS) 15 R2P plus signal of channel 2(LVDS) 16 Vss Ground 17 RCLKN minus signal of clock channel (LVDS)	
3 Vin +3.3V Power 4 V_EDID DDC 3.3V Power 5 NC No Connect 6 CLK_EDID DDC Clock 7 DATA_EDID DDC Data 8 R0N minus signal of channel 0(LVDS) 9 R0P plus signal of channel 0(LVDS) 10 Vss Ground 11 R1N minus signal of channel 1(LVDS) 12 R1P plus signal of channel 1(LVDS) 13 Vss Ground 14 R2N minus signal of channel 2(LVDS) 15 R2P plus signal of channel 2(LVDS) 16 Vss Ground 17 RCLKN minus signal of clock channel (LVDS)	
4 V_EDID DDC 3.3V Power  5 NC No Connect  6 CLK_EDID DDC Clock  7 DATA_EDID DDC Data  8 R0N minus signal of channel 0(LVDS)  9 R0P plus signal of channel 0(LVDS)  10 Vss Ground  11 R1N minus signal of channel 1(LVDS)  12 R1P plus signal of channel 1(LVDS)  13 Vss Ground  14 R2N minus signal of channel 2(LVDS)  15 R2P plus signal of channel 2(LVDS)  16 Vss Ground  17 RCLKN minus signal of clock channel (LVDS)	
5 NC No Connect 6 CLK_EDID DDC Clock 7 DATA_EDID DDC Data 8 R0N minus signal of channel 0(LVDS) 9 R0P plus signal of channel 0(LVDS) 10 Vss Ground 11 R1N minus signal of channel 1(LVDS) 12 R1P plus signal of channel 1(LVDS) 13 Vss Ground 14 R2N minus signal of channel 2(LVDS) 15 R2P plus signal of channel 2(LVDS) 16 Vss Ground 17 RCLKN minus signal of clock channel (LVDS)	
6 CLK_EDID DDC Clock 7 DATA_EDID DDC Data 8 R0N minus signal of channel 0(LVDS) 9 R0P plus signal of channel 0(LVDS) 10 Vss Ground 11 R1N minus signal of channel 1(LVDS) 12 R1P plus signal of channel 1(LVDS) 13 Vss Ground 14 R2N minus signal of channel 2(LVDS) 15 R2P plus signal of channel 2(LVDS) 16 Vss Ground 17 RCLKN minus signal of clock channel (LVDS)	
7 DATA_EDID DDC Data  8 R0N minus signal of channel 0(LVDS)  9 R0P plus signal of channel 0(LVDS)  10 Vss Ground  11 R1N minus signal of channel 1(LVDS)  12 R1P plus signal of channel 1(LVDS)  13 Vss Ground  14 R2N minus signal of channel 2(LVDS)  15 R2P plus signal of channel 2(LVDS)  16 Vss Ground  17 RCLKN minus signal of clock channel (LVDS)	
8 RON minus signal of channel O(LVDS) 9 ROP plus signal of channel O(LVDS) 10 Vss Ground 11 R1N minus signal of channel 1(LVDS) 12 R1P plus signal of channel 1(LVDS) 13 Vss Ground 14 R2N minus signal of channel 2(LVDS) 15 R2P plus signal of channel 2(LVDS) 16 Vss Ground 17 RCLKN minus signal of clock channel (LVDS)	
9 ROP plus signal of channel O(LVDS) 10 Vss Ground 11 R1N minus signal of channel 1(LVDS) 12 R1P plus signal of channel 1(LVDS) 13 Vss Ground 14 R2N minus signal of channel 2(LVDS) 15 R2P plus signal of channel 2(LVDS) 16 Vss Ground 17 RCLKN minus signal of clock channel (LVDS)	<b>A</b> '
10         Vss         Ground           11         R1N         minus signal of channel 1(LVDS)           12         R1P         plus signal of channel 1(LVDS)           13         Vss         Ground           14         R2N         minus signal of channel 2(LVDS)           15         R2P         plus signal of channel 2(LVDS)           16         Vss         Ground           17         RCLKN         minus signal of clock channel (LVDS)	
11 R1N minus signal of channel 1(LVDS) 12 R1P plus signal of channel 1(LVDS) 13 Vss Ground 14 R2N minus signal of channel 2(LVDS) 15 R2P plus signal of channel 2(LVDS) 16 Vss Ground 17 RCLKN minus signal of clock channel (LVDS)	
12     R1P     plus signal of channel 1(LVDS)       13     Vss     Ground       14     R2N     minus signal of channel 2(LVDS)       15     R2P     plus signal of channel 2(LVDS)       16     Vss     Ground       17     RCLKN     minus signal of clock channel (LVDS)	
13 Vss Ground 14 R2N minus signal of channel 2(LVDS) 15 R2P plus signal of channel 2(LVDS) 16 Vss Ground 17 RCLKN minus signal of clock channel (LVDS)	)
14 R2N minus signal of channel 2(LVDS) 15 R2P plus signal of channel 2(LVDS) 16 Vss Ground 17 RCLKN minus signal of clock channel (LVDS)	
15 R2P plus signal of channel 2(LVDS) 16 Vss Ground 17 RCLKN minus signal of clock channel (LVDS)	
16 Vss Ground 17 RCLKN minus signal of clock channel (LVDS)	
17 RCLKN minus signal of clock channel (LVDS)	
8	
18 RCLKP plus signal of clock channel (LVDS)	
19 Vss Ground	
20 NC No connect	
NC VCOM test provided , but customer-end unused (	open)
22 NC No connect	
23 NC No connect	
24 NC No connect	
25 NC No connect	
26 NC No connect	
27 NC No connect	
28 NC No connect	
29 NC No connect	
30 NC No connect	

# (b) CN2 (BACKLIGHT)

Backlight-side connector: BHSR-02VS-1 (JST) Inverter-side connector: SM02B-BHSS-1 (JST)

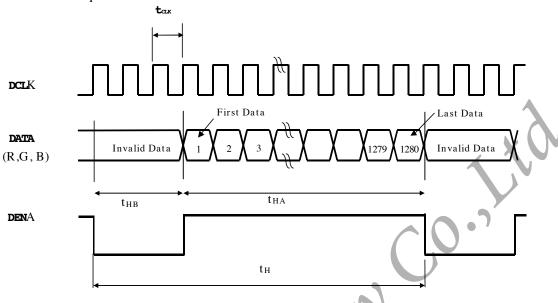
Pin No.	Symbol	Function
Y	СТН	VBLH (High)
2	CTL	VBLL (Low)

[Note]: VBLH-VBLL=VL

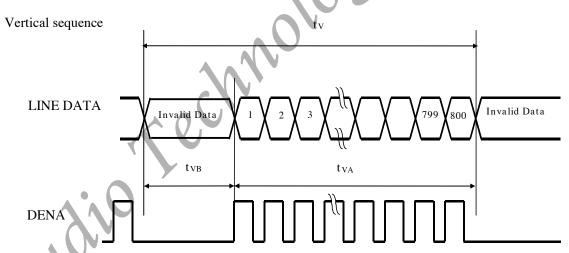
# **5. INTERFACE TIMING CHART**

# (a). LVDS input time sequence

Horizontal sequence



# (b) LCD input time sequence



# (1) Timing Chart

		項目			MIN	TYP	MAX	UNIT
	D	CLK	Frequency	$f_{CLK}$	65.3	68.9	74.7	MHz
	D	CLK	Period	$t_{CLK}$	15.3	14.5	13.3	ns
			Horizontal total time	t <sub>H</sub>	1344	1408	1500	$t_{CLK}$
LCD		Horizontal	Horizontal Active time	t <sub>HA</sub>	1280	1280	1280	$t_{CLK}$
Timing	DENA		Horizontal Blank time	t <sub>HB</sub>	64	128	220	$t_{\mathrm{CLK}}$
	DENA		Vertical total time	$t_{V}$	810	816	830	$t_{\mathrm{H}}$
		Vertical	Vertical Active time	$t_{VA}$	800	800	800	$t_{\mathrm{H}}$
			Vertical Blank time	$t_{ m VB}$	10	16	30	$t_{\mathrm{H}}$

#### [Note]

- \*1) Data is latched during DCLK falling period.
- \*2) HD · VD is negative.
- \*3) DENA (DATA ENABLE) usually is positive.
- \*4) During the whole blank period, DCLK should keep input. During the vertical blank period, HD should keep input.

# (2) DATA mapping

	R DATA		G DATA				B DATA												
Color	Input Data	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	В3	B2	B1	B0
Coloi	піриі Даіа	MS		!	!	!	LS	MS		!	!	!	LS	MS					LS
		В		i			В	В				i	В	В					В
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Basic	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Color	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	. 1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	Ι	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1			1	1	1	1	1	1	1	1
	RED(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	RED(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
RED																			
	RED(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	. 1	0	0	0	0	0	0	0
Green				U			]			!		]	I						
	,			!							:	!						;	
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
<b>•</b>	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Blue				! 	<u>.</u>	<u>.</u>	<u> </u>	L		<u>.</u>	<u>.</u>	! 	<u>.</u>					! !	
1 7 . 1	/																		
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	, 0	0	1	1	1	1	1	1

#### [Note]

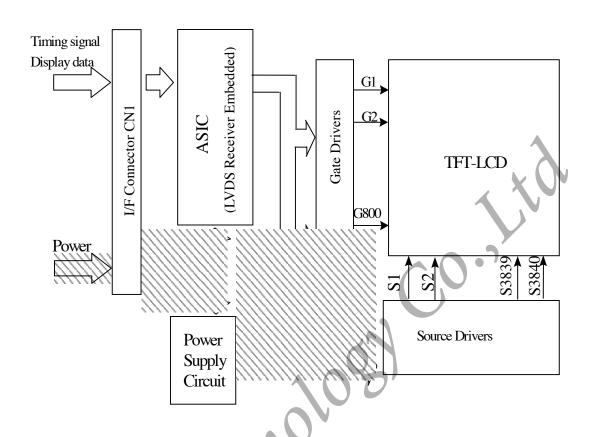
1) Gray level:

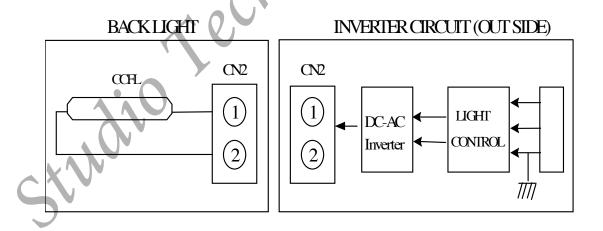
Color(n): n is level order; higher n means brighter level.

2) DATA:

1: high , 0: low

# 6. BLOCK DIAGRAM

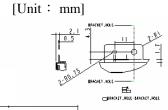


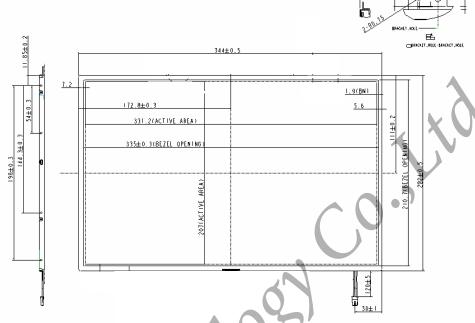


# 7. MECHANICAL SPECIFICATION

#### (1) Front side

The tolerance, not show in the figure, is  $\pm 0.5$ mm.

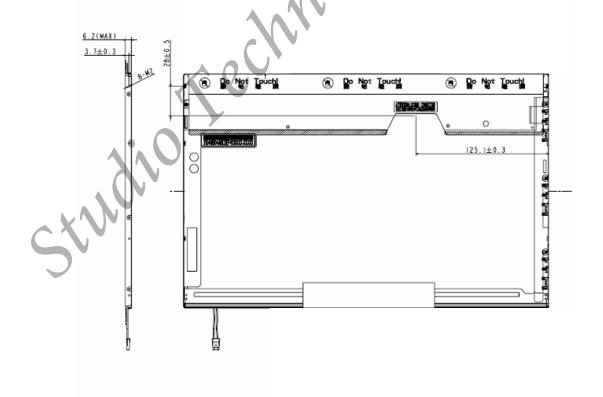




## (2) Rear side

The tolerance, not show in the figure, is  $\pm 0.5$ mm.





#### 8. OPTICAL CHARACTERISTICS

ITEN	И	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
Contrast Ratio		CR	$\theta = \psi = 0^{\circ}$	300	500			*1)
Luminance (5P)		L	$\theta = \psi = 0^{\circ}$	170	200		cd/m <sup>2</sup>	*2)
Uniformity(5	(P)	ΔL	$\theta = \psi = 0^{\circ}$		80		%	*2)
D Ti.		Tr	$\theta = \psi = 0^{\circ}$		6	9	ms	*4)
Response Tir	ne	Tf	$\theta = \psi = 0^{\circ}$		10	16	ms	*4)
Cross talk		CT	$\theta = \phi = 0^{\circ *3}$			1	%	*5)
Miany and a	Horizont	Ψ	CD > 10	40/-40	45/-45		0	*3)
View angle	Vertical	θ	$CR \ge 10$	10/-30	15/-35		0	*3)
	W	X		0.283	0.313	0.343	X	
	VV	Y		0.299	0.329	0.359		7
Color	R	X		0.584	0.614	0.644		
_		Y	$\theta = \psi = 0^{\circ}$	0.306	0.336	0.366		*2)
Temperature Coordinate	G	X		0.281	0.311	0.341		. 2)
		Y		0.534	0.564	0.594	• /	
	D	X		0.123	0.153	0.183		
	В	Y		0.100	0.130	0.160		

These items are measured using BM-5A (TOPCON) under the dark room condition (no ambient light).

Measurement Condition: IL=6.0×6mA

Inverter: SUMIDA / IV12139/T

Definition of these measurement items is as follows:

#### \*1) Definition of Contrast Ratio

CR=ON (White) Luminance/OFF (Black) Luminance

#### \*2) Definition of Luminance and Luminance uniformity

Central luminance: The white luminance is measured at the center position "5" on the screen, see Fig.1 below.

5P Luminance (AVG): The white luminance is measured at measuring points  $5 \cdot 10 \cdot 11 \cdot 12 \cdot 13$ , see Fig.1 below.

5P Uniformity:  $\Delta L = (Lmin / Lmax) \times 100\%$ 

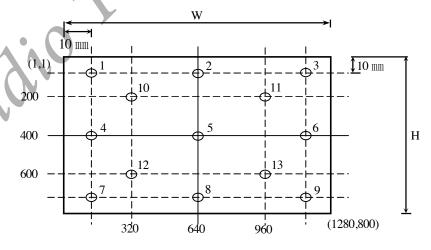
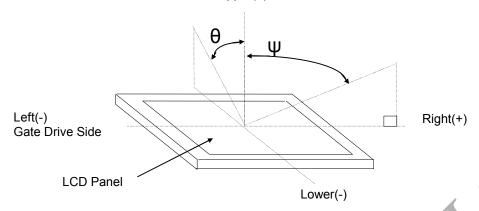


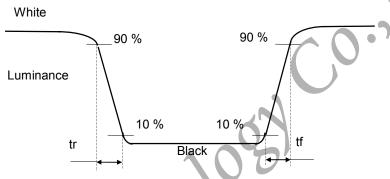
Fig.1 Measure

# \*3) Definition of view angle( $\theta$ , $\psi$ )





#### \*4) Definition of response time



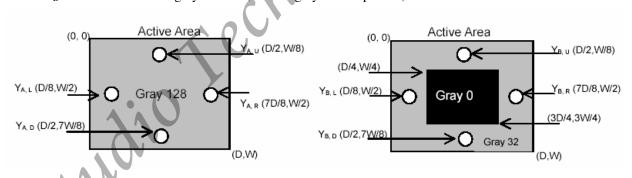
## \*5) Crosstalk Modulation Ratio:

 $CT = | Y_{B}-Y_{A} | / Y_{A\times} \times 100\%$ 

 $Y_A \cdot Y_B$  measure position and definition

Y<sub>A</sub> means luminance at gray level 32(exclude gray level 0 pattern)

Y<sub>B</sub> means luminance at gray level 32(include gray level 0 pattern)



# 9.RELIABILITY TEST CONDITIONS

# (1) Temperature and Humidity

TEST ITEMS	CONDITIONS		
High Temperature Operation	50° C ; 240HR Follow page 5 diagram		
High Temperature Storage	60° C ; 240HR Follow page 5 diagram		
High Temperature	240HR(No condensation)		
High Humidity Operation	Follow page5 diagram		
II'-1 T II'-1 II I'-C	48HR(No condensation)		
High Temperature High Humidity Storage	Follow page5 diagram		
Low Temperature Operation	0° C ; 240HR Follow page5 diagram		
Low Temperature Storage	-20° C ; 240HR Follow page5 diagram		
The arrest Cheeds	$-20^{\circ} \text{C} (0.5 \text{ hr}) \sim 60^{\circ} \text{C} (0.5 \text{ hr})$		
Thermal Shock	Ramp<20°C → 100 CYCLE		
Temperature & Pressure Storage	25° C ; 260hPa(about 10000m), 24 Hrs		

# (2) Shock & Vibration

TEST ITEMS	CONDITIONS
Shock	Shock level: 1960m/s <sup>2</sup> (200G), Waveform: half
(Non-Operation)	sinusoidal wave, 2ms, 6 axis ( $\pm X, \pm Y, \pm Z$ ) per cycle
	Vibration level: 9.8m/s <sup>2</sup> (1.0G), sinusoidal wave (each
Vibration	x,y,z axis : 1hr, total 3hrs)
(Non-Operation)	Frequency range: 5~500 Hz
	Sweep speed: 0.5 Octave/min.

# (3) ESD

	Surface discharge(P Frame • PWB •	Electrics capacity of Connector	
	Contact Air		Contact
Capacity	150 pF	150 pF	200 pF
Resistance	330 Ω	330 Ω	0 Ω
Voltage	±8kV	±8kV/±15kV	±250 V
Interval	1 sec	1 sec	1 sec
Times(single point)	25	25	1

Acceptance Criteria	Air Discharge	Air Discharge		
, 1100 p	+/-8 kV	+/-15 kV		
A	Permitted	Permitted		
В	Permitted	Permitted		
С	Not Permitted	Permitted		
D	Not Permitted	Not Permitted		

	Acceptance Definitions
A	Normal operation. No degradation. No failures.
В	Some performance degradation allowed. No data lost. Self-recoverable.
С	Temporary performance degradation. Recovery by operator is acceptable.
D	Degradation or loss of function, which is not recoverable due to damage of equipment (components)

#### (4) Judgment standard

The judgment of the above test should be made as follow:

Pass: Normal display image with no obvious non-uniformity and no line defect.

Partial transformation of the module parts should be ignored.

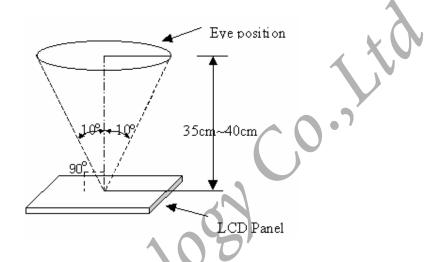
Fail: No display image, obvious non-uniformity, or line defects.



#### 10. VISUAL INSPECTION SPECIFICATION

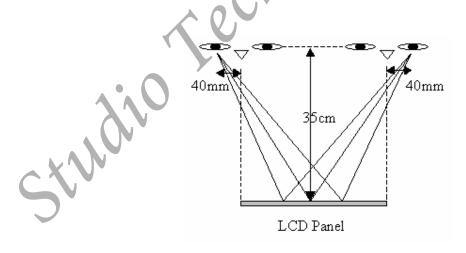
#### 10.1 Inspection condition

- (1) Viewing distance is approximately  $35 \sim 40$  cm.
- (2) Viewing angle is normal to the LCD panel as figure below(10°).
- (3) Ambient temperature is approximately  $25 \pm 5^{\circ}$ C.
- (4) Ambient humidity is  $60 \pm 5\%$  RH.
- (5) Ambient illumination is from  $300 \sim 500 \text{ lux}$ .
- (6) Input signal timing should be typical value.



#### 10.2 Special condition

- (1) Viewing distance is close for inspection of adjacent dots and distance between defect dots.
- (2) Viewing condition of "Shot block non-uniformity from oblique angle" is as figure below.
- (3) Exceptional case: View angle  $\pm 40^{\circ}$  while inspected image-sticking.

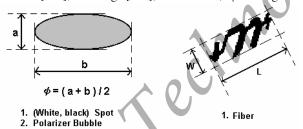


10.3 Inspection Criteria

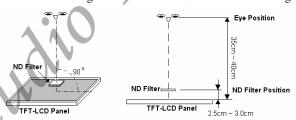
	DEFECT TYP	E	LIMIT	Note	
	SC	CRATCH	$\begin{array}{c c} 0.01\text{mm} \leq W \leq 0.05\text{mm} \\ L \leq 10\text{mm} \end{array} \qquad N \leq 4$		
VICTIAL DEDECE		SPOT	$0.15$ mm $\leq \varphi \leq 0.5$ mm $N \leq 4$		*1)
VISUAL DEFECT		FIBER	W≦0.1mm, L≦3.0mm	N≦4	*1)
	INTERNAL	POLARIZER BUBBLE	$0.15$ mm $\leq \varphi \leq 0.5$ mm	N≦4	*1)
		TOTAL	N≦4		
	BRI	GHT DOT	N≦4	*2)	
	DARK DOT		N≦5	7-	
	TOTAL DOT		N≦6	*2)	
	TWO ADJACENT DOT		≦1 PAIRS	*3)	
ELECTRICAL DEFECT	THREE OR MORE ADJACENT DOT		NOT ALLOWED		
	DISTANCE BETWEEN DEFECT DOT		Bright dot and dark dot ≥ 15mm		*4)
		_	Two dark dots	≥15mm	*4)
	LIN	E DEFECT	NOT ALLOWED		
	MURA		≤ 5% ND		

One pixel consists of 3 sub-pixels, including R,G, and B dot.(Sub-pixel = Dot)

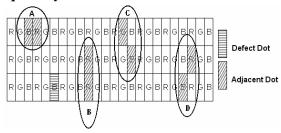
[Note1] W: Width[mm], L: Length[mm], N: Number,  $\phi$ : Average Diameter



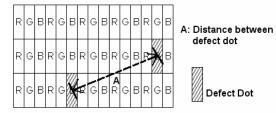
[Note2] Bright dot is defined through 5% transmission ND Filter as following.



[Note3] Judge defect dot and adjacent dot as following. Allow below (as A, B, C and D status) adjacent defect dots, including bright and dart adjacent dot. And they will be counted 2 defect dots in total quantity.



[Note4] Definition of distance between defect dot as following.



#### 10.4 Handling precaution

- (1) Don't disassemble and reassemble the module by self. (禁止自行拆解。)
- (2) Acid, alkali, alcohol or touched directly by hand will damage the display. (酸性、鹼性、酒精或手的直接接觸將會損傷顯示面。)
- (3) Static electricity will damage the module. Please configure grounding device. (靜電會損傷模組。請裝配接地設備。)
- (4) The strong vibration, shock, twist or bend will cause material damage, even module broken. (強烈的衝擊、震動、扭轉或彎曲將會造成原材損傷,甚至面板破裂)
- (5) It is easy to cause image sticking while displaying the same pattern for very long time. (長期顯示同一畫面亦造成影像殘留。)
- (6) The response time, brightness and performance will vary from different temperature.



#### 11. HANDLING PRECAUTIONS FOR TFT-LCD MODULE

Please pay attention to the followings in handling- TFT-LCD products;

#### 11.1 ASSEMBLY PRECAUTION

- (1) Please use the mounting hole on the module side in installing and do not beading or wrenching LCD in assembling. And please do not drop, bend or twist LCD module in handling.
- (2) Please design display housing in accordance with the following guidelines.
  - Housing case must be destined carefully so as not to put stresses on LCD all sides and not to wrench module. The stresses may cause non-uniformity even if there is no non-uniformity statically.
  - Keep sufficient clearance between LCD module back surface and housing when the LCD module is mounted. Approximately 1.0 mm of the clearance in the design is recommended taking into account the tolerance of LCD module thickness and mounting structure height on the housing.
  - When some parts, such as, FPC cable and ferrite plate, are installed underneath the LCD module, still sufficient clearance is required, such as 0.5mm. This clearance is, especially, to be reconsidered when the additional parts are implemented for EMI countermeasure.
  - Design the inverter location and connector position carefully so as not to give stress to lamp cable, or not to interface the LCD module by the lamp cable.
  - Keep sufficient clearance between LCD module and the others parts, such as inverter and speaker so as not to interface the LCD module. Approximately 1.0mm of the clearance in the design is recommended.
- (3) Please do not push or scratch LCD panel surface with any-thing hard. And do not soil LCD panel surface by touching with bare hands. (Polarizer film, surface of LCD panel is easy to be flawed.)
- (4) Please do not press any parts on the rear side such as source TCP, gate TCP, control circuit board and FPCs during handling LCD module. If pressing rear part is unavoidable, handle the LCD module with care not to damage them.
- (5) Please wipe out LCD panel surface with absorbent cotton or soft clothe in case of it being soiled.
- (6) Please wipe out drops of adhesives like saliva and water on LCD panel surface immediately. They might damage to cause panel surface variation and color change.
- (7) Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.
- (8) Please do not touch metal frames with bare hands and soiled gloves. A color change of the metal frames can happen during a long preservation of soiled LCD modules.
- (9) Please pay attention to handling lead wire of backlight so that it is not tugged in connecting with inverter.

#### 11.2 OPERATING PRECAUTIONS

- (1) Please be sure to turn off the power supply before connecting and disconnecting signal input cable.
- (2) Please do not change variable resistance settings in LCD module. They are adjusted to the most suitable value. If they are changed, it might happen LCD does not satisfy the characteristics specification.
- (3) Please consider that LCD backlight takes longer time to become stable of radiation characteristics in low temperature than in room temperature.
- (4) A condensation might happen on the surface and inside of LCD module in case of sudden change of ambient temperature.
- (5) Please pay attention to displaying the same pattern for very long time. Image might stick on LCD. If then, time going on can make LCD work well.
- (6) Please obey the same caution descriptions as ones that need to pay attention to ordinary electronic parts.

#### 11.3 PRECAUTIONS WITH ELECTROSTATICS

- (1) This LCD module use CMOS-IC on circuit board and TFT-LCD panel, and so it is easy to be affected by electrostatics. Please be careful with electrostatics by the way of your body connecting to the ground and so on
- (2) Please remove protection film very slowly on the surface of LCD module to prevent from electrostatics occurrence.

#### 11.4 STORAGE PRECAUTIONS

- (1) When you store LCDs for a long time, it is recommended to keep the temperature between  $0^{\circ}$ C ~ $40^{\circ}$ C without the exposure of sunlight and to keep the humidity less than 90%RH.
- (2) Please do not leave the LCDs in the environment of high humidity and high temperature such as 60 ℃ 90%RH.
- (3) Please do not leave the LCDs in the environment of low temperature; below -20  $^{\circ}$ C.

#### 11.5 SAFETY PRECAUTIONS

- (1) When you waste LCDs, it is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.
- (2) If any liquid leaks out of a damaged-glass cell and comes in contact with the hands, wash off throughly with soap and water.

#### 11.6 OTHERS

- (1) A strong incident light into LCD panel might cause display characteristics' changing inferior because of polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight Land strong UV rays.
- (2) Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.
- (3) For the packaging box, please pay attention to the followings:
  - Packaging box and inner case for LCD are designed to protect the LCDs from the damage or scratching during transportation. Please do not open except picking LCDs up from the box.
  - Please do not pile them up more than 3 boxes. (They are not designed so.) And please do not turn over
  - Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.
- Packing box and inner case for LCDs are made of cardboard. So please pay attention not to get them wet. (Such like keeping them in high humidity or wet place can occur getting them wet.)

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