



Chunghwa Picture Tubes, Ltd.

Product Specification

To : GO CHUN

Date : 2010/7/27

TFT LCD

CLAP070LF01CW

ACCEPTED BY : (V0.2)

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CONTENTS

1. OVERVIEW	4
2. ABSOLUTE MAXIMUM RATINGS	5
3. ELECTRICAL CHARACTERISTICS.....	6
3.1 Typical operation conditions	6
3.2 Current consumption.....	6
3.3 Power 、 Signal sequence	7
3.4 Timing characteristics of input signals	8
4. INTERFACE CONNECTION:	11
4.1 CN1(Signal of interface)	11
5. MECHANICAL DIMENSION	13
5.1 Front Side	13
5.2 Rear Side	14
6. OPTICAL CHARACTERISTICS.....	15
7. RELIABILITY TEST	16

1. OVERVIEW

CLAP070LF01CW is 7.0" color TFT-LCD (Thin Film Transistor Liquid Crystal Display) OLB module (finish outer lead bonding) composed of LCD panel and driver ICs (the backlight is not included in this OLB module).

The 7.0" screen produces 800(*3)X480 resolution image. By applying R.G.B. input signal, full color images are displayed.

General specifications are summarized in the following table:

ITEM	SPECIFICATION
Display Area (mm)	154.08(H) × 85.92(V)
Number of Pixels	800(H) × 3(RGB) × 480(V)
Pixel Pitch (mm)	0.1926(H) × 0.1790(V)
Color Pixel Arrangement	RGB vertical stripe
Display Mode	Normally white
Number of color	16.2M
Response Time (Tr+Tf)	25ms (typ.)
Panel Transmittance (%)	5.1(typ)
Power Consumption(W)	327mW(typ.)
Surface Treatment	Anti-Glare, Hardness:3H

2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	DVDD	-0.3	+5.0	V	
Analog Supply Voltage	AVDD	-0.5	+13.5	V	
Gate On Voltage	VDDG	-0.3	+42	V	
Gate Off Voltage	VEEG	-20	+0.3	V	
Gate On-Gate Off Voltage	VDDG-VEEG	12	40	V	
Operation Temperature	T _{op}	-20	70	°C	Note 1
Storage Temperature	T _{stg}	-30	80	°C	Note 1

Note1 : If users use the product out off the environmental operation range (temperature and humidity) , it will have visual quality concerns.

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3. ELECTRICAL CHARACTERISTICS

3.1 Typical operation conditions

Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit.	Note.
Digital Supply Voltage	DVDD	3	3.3	3.6	V	
Analog Supply Voltage	AVDD	9.4	9.6	9.8	V	
Gate On Voltage	VDDG	17	18	19	V	
Gate Off Voltage	VEEG	-6.6	-6	-5.4	V	
Common Voltage	VCOM	3.8	4	4.2	V	Note1
Logic Input Voltage	VIH	0.7DVDD	-	DVDD	V	
	VIL	GND	-	0.3DVDD	V	

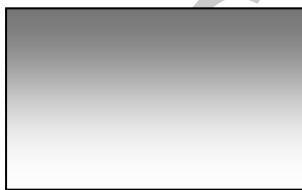
Note1 : Please adjust VCOM to make the flicker level be minimum.

3.2 Current consumption

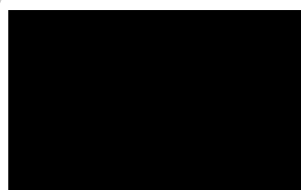
Item	Symbol	Condition	Min.	Typ.	Max.	Unit.	Note.
Gate on Current	IVDDG	VDDG = 18 V	-	0.5	1	mA	Note1
Gate off Current	IVEEG	VEEG = -6 V	-	0.5	1	mA	Note1
Digital Current	IDVDD	DVDD = 3.3V	-	8	15	mA	Note1
Analog Current	IAVDD	AVDD = 9.6 V	-	30	40	mA	Note1
Total Power Consumption	PC		-	327	458	mW	Note1

Note1: Typ. specification : Gray-level test Pattern

Max. specification : Black test Pattern



(a) Gray-level Pattern

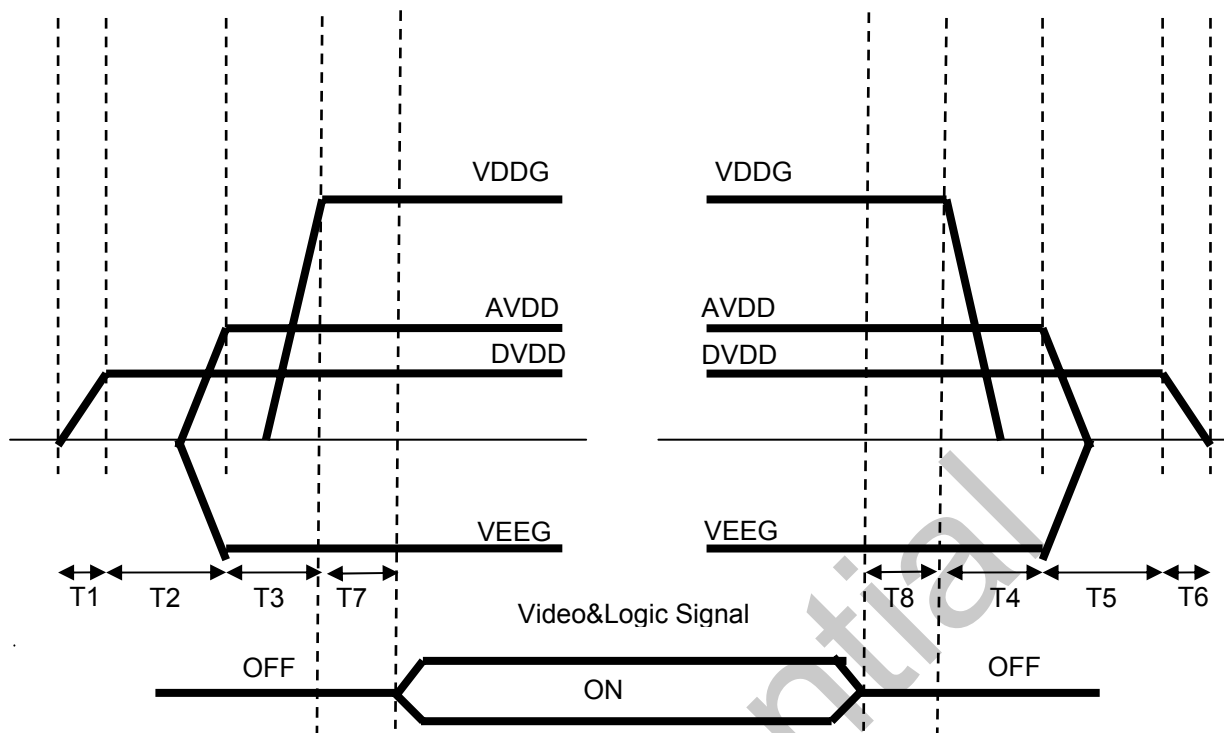


(b) Black Pattern

3.3 Power 、Signal sequence

Power On : DVDD→AVDD/VEEG→VDDG→Video & Logic Signal

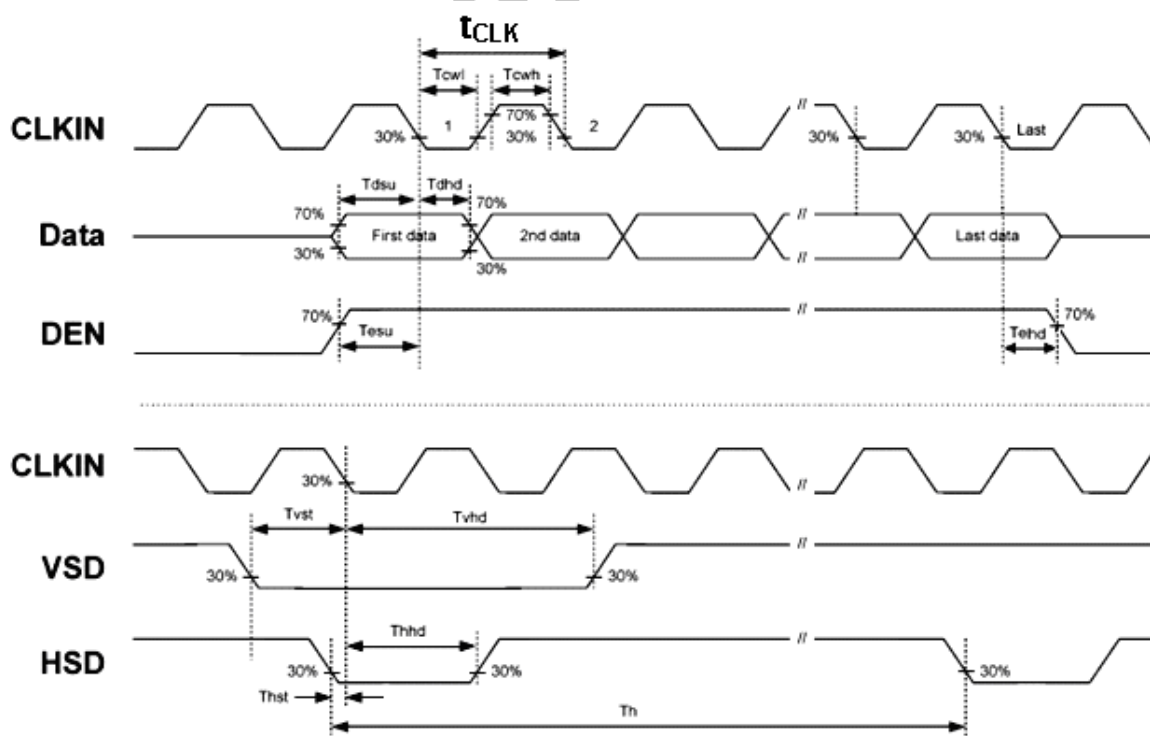
Power Off : Video & Logic Signal→VDDG→AVDD/VEEG→DVDD



- $0 < T1 \leq 10\text{ms}$
- $T2 > 20\text{ms}$
- $T3 > 10\text{ms}$
- $T4 > 0\text{ms}$
- $T5 > 0\text{ms}$
- $T6 > 0\text{ms}$
- $0 < T7 \leq 10\text{ms}$
- $0 < T8 \leq 10\text{ms}$

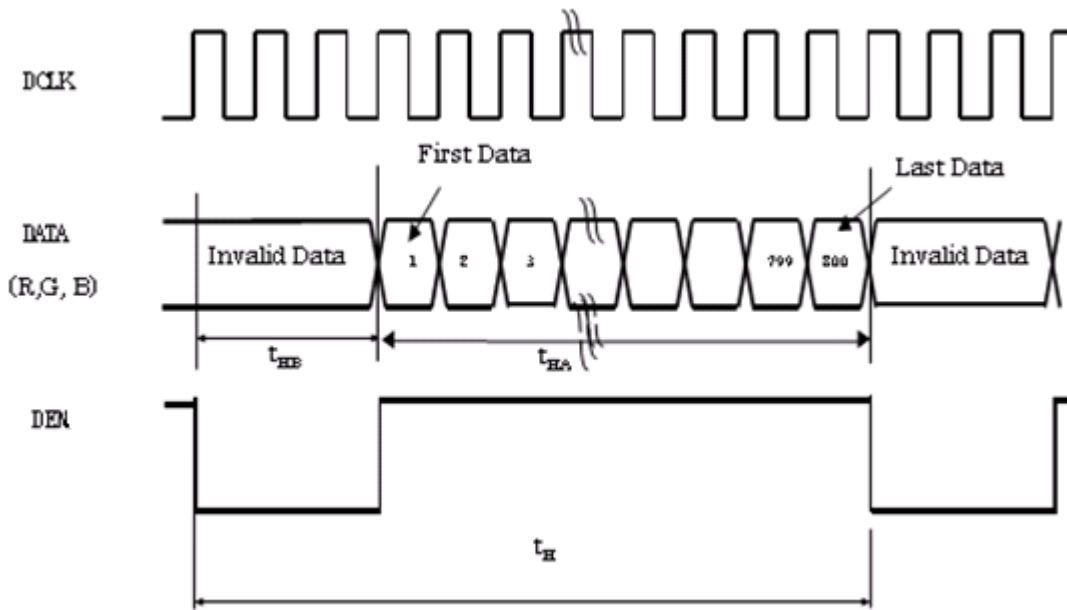
3.4 Timing characteristics of input signals

	ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	Note
DCLK	Dot Clock	$1/t_{CLK}$	29	33	38	MHz	
	DCLK pulse duty	T_{cwh}	40	50	60	%	
DE	Setup Time	T_{esu}	8	-	-	ns	
	Hold time	T_{ehd}	8	-	-	ns	
	Horizontal Period	t_H	1026	1056	1086	t_{CLK}	
	Horizontal Valid	t_{HA}	800			t_{CLK}	
	Horizontal Blank	t_{HB}	226	256	286	t_{CLK}	
	Vertical Period	t_V	515	525	535	t_H	
	Vertical Valid	t_{VA}	480			t_H	
	Vertical Blank	t_{VB}	35	45	55	t_H	
SYNC	HSYNC Setup Time	T_{hst}	8	-	-	ns	
	HSYNC Hold Time	T_{hhd}	8	-	-	ns	
	VSYNC Setup Time	T_{vst}	8	-	-	ns	
	VSYNC Hold Time	T_{vhhd}	8	-	-	ns	
	Horizontal Period	t_h	1026	1056	1086	t_{CLK}	
	Horizontal Pulse Width	t_{hpw}	-	30	-	t_{CLK}	$t_{hb} + t_{hpw} = 46DCLK$ is fixed
	Horizontal Back Porch	t_{hb}	-	16	-	t_{CLK}	
	Horizontal Front Porch	t_{hfp}	180	210	240	t_{CLK}	
	Horizontal Valid	t_{hd}	800			t_{CLK}	
	Vertical Period	t_v	515	525	535	t_h	
	Vertical Pulse Width	t_{vpw}	-	13	-	t_h	$t_{vpw} + t_{vb} = 23t_h$ is fixed
	Vertical Back Porch	t_{vb}	-	10	-	t_h	
	Vertical Front Porch	t_{vfp}	12	22	32	t_h	
	Vertical Valid	t_{vd}	480			t_h	
DATA	Setup Time	T_{dsu}	8	-	-	ns	
	Hold Time	T_{dhhd}	8	-	-	ns	

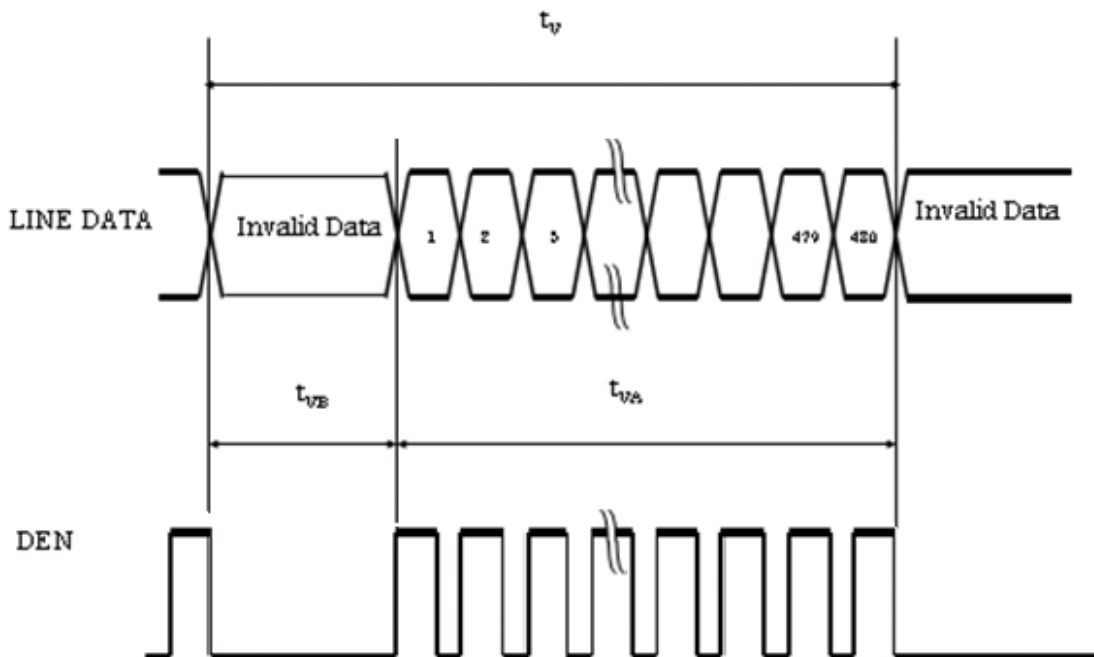


DE mode

Horizontal timing :

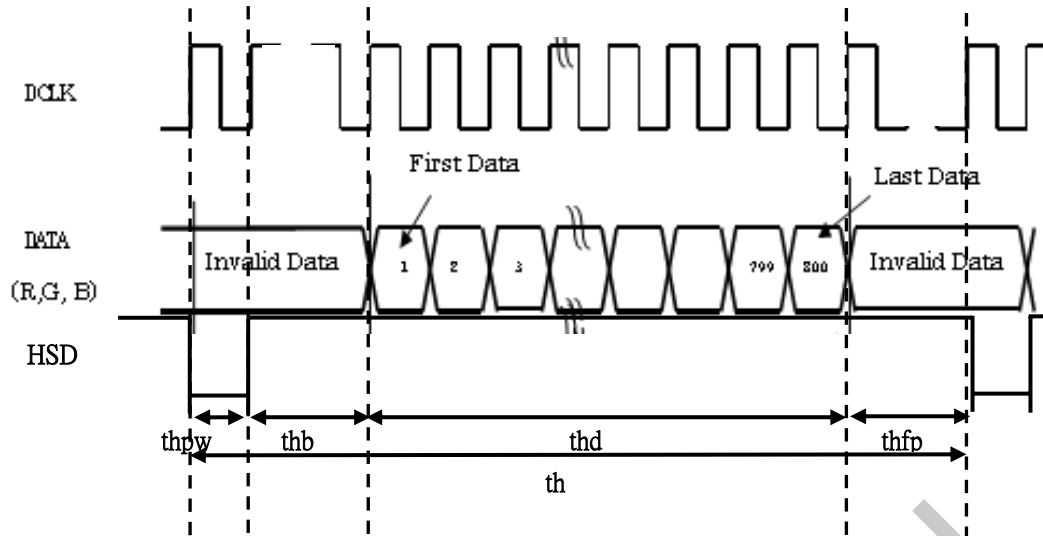


Vertical timing :

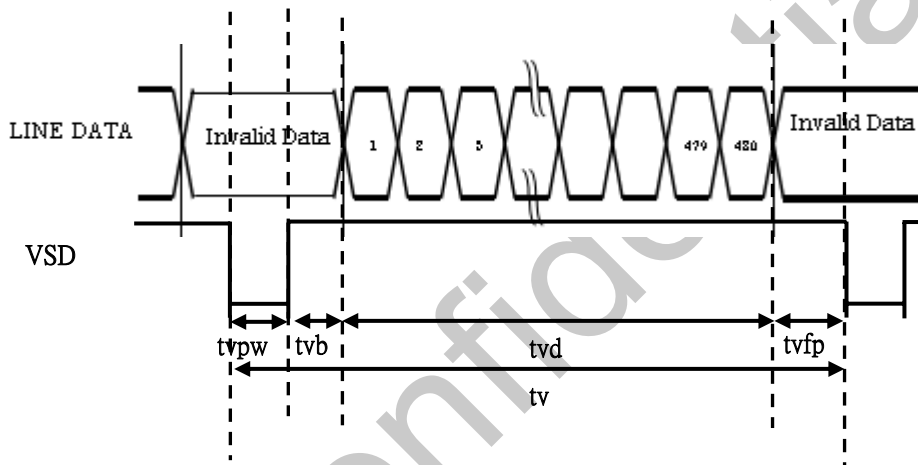


SYNC mode

Horizontal timing :



Vertical timing :



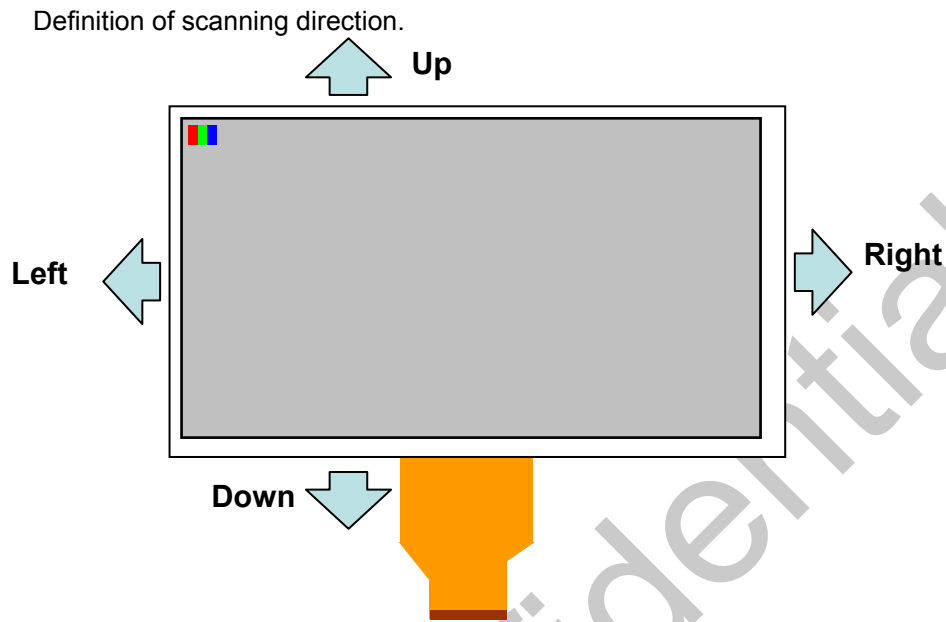
4. INTERFACE CONNECTION:

4.1 CN1(Signal of interface)

Pin NO.	SYMBOL	DESCRIPTION
1	V _{LED+}	Power for LED backlight (Anode)
2	V _{LED+}	Power for LED backlight (Anode)
3	V _{LED-}	Power for LED backlight (Cathode)
4	V _{LED-}	Power for LED backlight (Cathode)
5	GND	Power ground
6	VCOM	Common Voltage
7	DVDD	Digital Power
8	MODE	DE/SYNC mode select. Normally pull high H: DE mode. L: HSD/VSD mode
9	DE	Data Enable signal
10	VSD	Vertical sync input. Negative polarity
11	HSD	Horizontal sync input. Negative polarity
12	B7	Blue Data Input(MSB)
13	B6	Blue Data Input
14	B5	Blue Data Input
15	B4	Blue Data Input
16	B3	Blue Data Input
17	B2	Blue Data Input
18	B1	Blue Data Input
19	B0	Blue Data Input(LSB)
20	G7	Green Data Input(MSB)
21	G6	Green Data Input
22	G5	Green Data Input
23	G4	Green Data Input
24	G3	Green Data Input
25	G2	Green Data Input
26	G1	Green Data Input
27	G0	Green Data Input(LSB)
28	R7	Red Data Input(MSB)
29	R6	Red Data Input
30	R5	Red Data Input
31	R4	Red Data Input
32	R3	Red Data Input
33	R2	Red Data Input
34	R1	Red Data Input
35	R0	Red Data Input(LSB)
36	GND	Power ground
37	DCLK	Clock input
38	GND	Power ground
39	SHLR	Left or Right Display Control
40	UPDN	Up / Down Display Control
41	VDDG	Positive Power for TFT
42	VEEG	Negative Power for TFT
43	AVDD	Analog Power
44	RSTB	Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high. (R=10K Ω , C=1 μ F)
45	NC	Not connect
46	VCOM	Common Voltage
47	DITH	Dithering setting DITH="H" 6bit resolution(last 2 bit of input data truncated) DITH="L" 8bit resolution(default setting)
48	GND	Power ground
49	NC	Not connect
50	NC	Not connect

【Note1】 SHLR : left or right setting
 UPDN : up or down setting

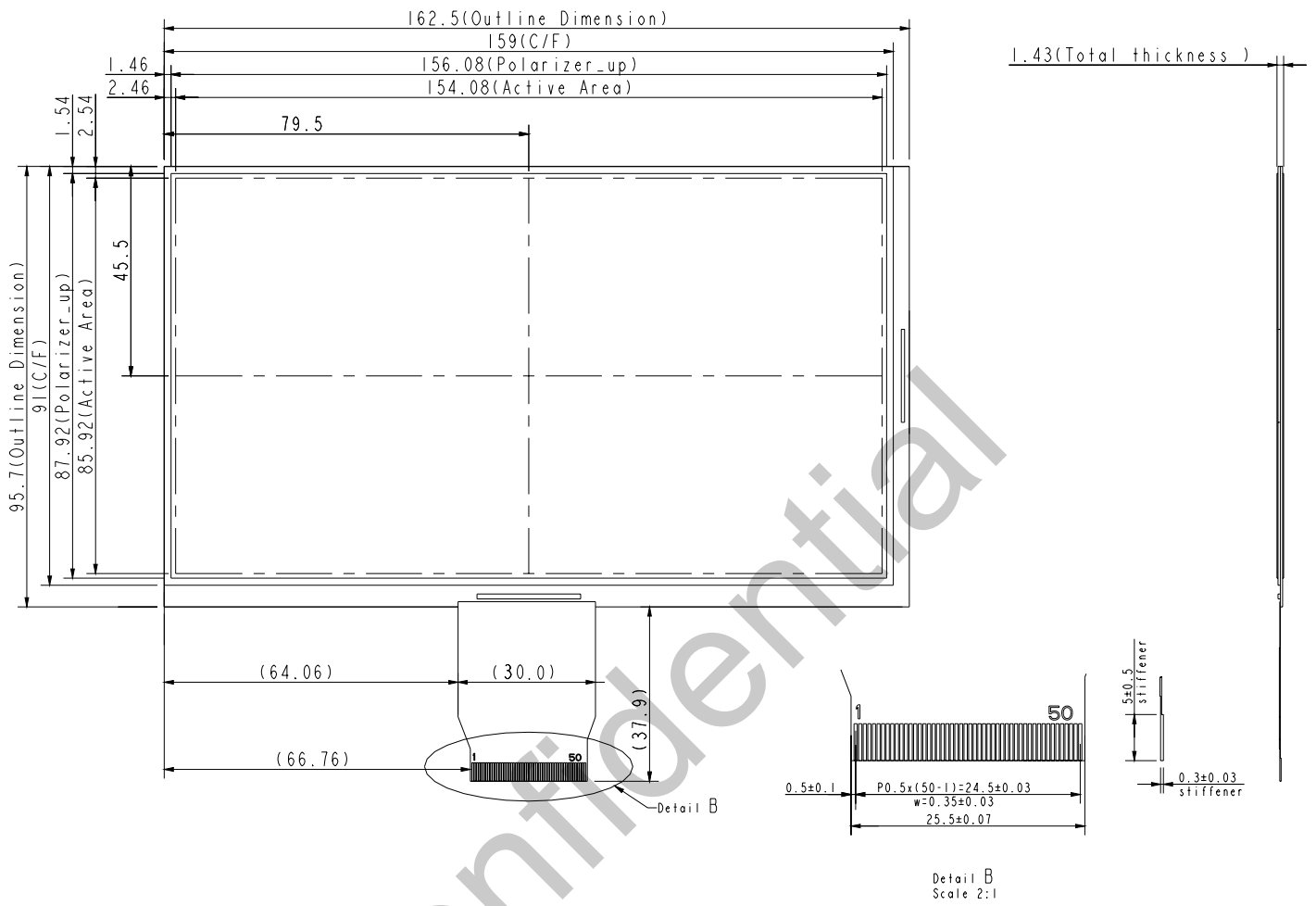
SHLR	UPDN	Data shifting
DVDD	GND	Left→Right , Up→Down(default)
GND	GND	Right→Left , Up→Down
DVDD	DVDD	Left→Right , Down→Up
GND	DVDD	Right→Left , Down→Up



5. MECHANICAL DIMENSION

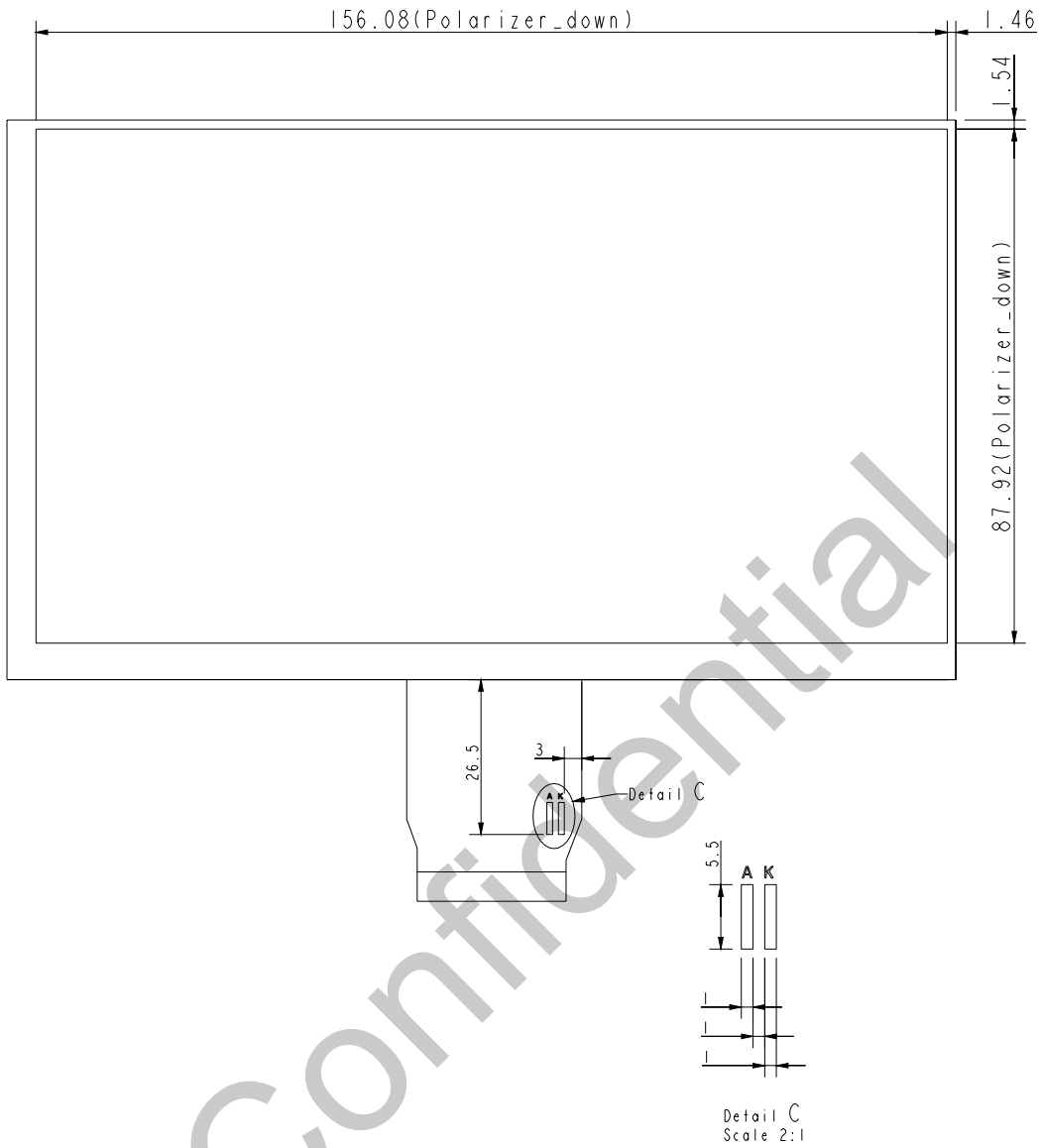
5.1 Front Side

(Unit : mm)



5.2 Rear Side

(Unit : mm)



NOTE: General tolerance=±0.3mm

6. OPTICAL CHARACTERISTICS

(Use CPT LED backlight)

Ta=25°C

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE	
Panel Transmittance	T	---	4.8	5.1	--	%		
Response Time	Tr +Tf	Point-5	--	25	35	ms	1	
Viewing Angle	Horizontal	Point-5 CR≥10	120	140	--	°	2	
	Vertical		100	120	--	°	2	
Color Filter Chromacity	White	$\theta = \phi = 0^\circ$	x	0.273	0.313	0.353		3
			y	0.289	0.329	0.369		3
	Red	$\theta = \phi = 0^\circ$	x	(0.562)	(0.602)	(0.642)		3
			y	(0.297)	(0.337)	(0.377)		3
	Green	$\theta = \phi = 0^\circ$	x	(0.309)	(0.349)	(0.389)		3
			y	(0.547)	(0.587)	(0.627)		3
	Blue	$\theta = \phi = 0^\circ$	x	(0.123)	(0.163)	(0.203)		3
			y	(0.074)	(0.114)	(0.154)		3

Note 1: Definition of Response Time.(White-Black)

The response time is defined as the time interval between the 10% and 90% amplitudes.

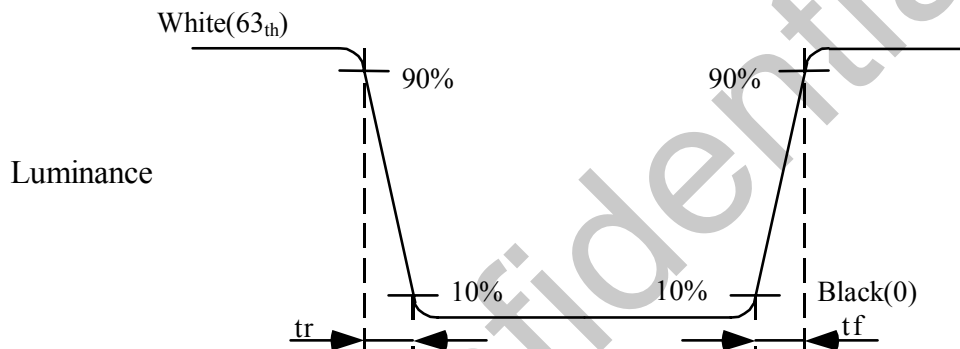


Fig. 6-1 Measuring point

Note 2: Definition of Viewing Angle(θ, ψ)

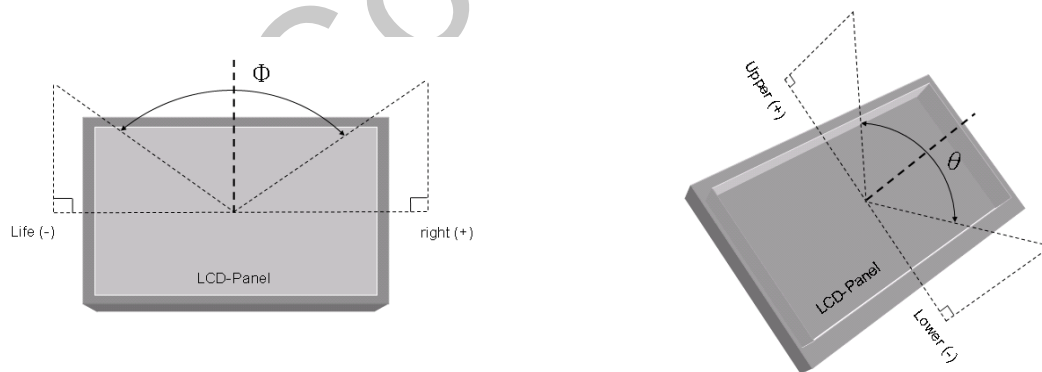


Fig.6-2 Definition of Viewing Angle

Note 3: Under C light

7. RELIABILITY TEST

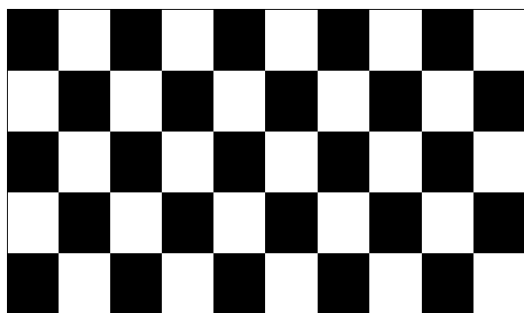
(These tests are conducted with CPT backlight.)

7.1 Temperature and Humidity

TEST ITEMS	CONDITIONS	NOTE
High Temperature Operation	70°C ; 240hrs	
High Temperature Storage	80°C ; 240hrs	
High Temperature High Humidity Operation	60°C ; 90%RH ; 240hrs (No condensation)	
Low Temperature Operation	-20°C ; 240hrs	
Low Temperature Storage	-30°C ; 240hrs	
Thermal Shock	-30°C (0.5hr) ~ 80°C (0.5hr) ; 200 Cycles	Non-Operating
Image Sticking	25°C ; 4hrs	1

Note 1: Condition of Image Sticking test : 25 °C ± 2 °C

Operation with test pattern sustained for 4 hrs, then change to gray pattern immediately.
After 5 mins, the mura must be disappeared completely .



(a) Test Pattern (chess board Pattern)



(b) Gray Pattern

7.2 Shock and Vibration

ITEMS	CONDITIONS
Shock (Non-Operation)	<ul style="list-style-type: none"> ● Shock level : 980m/s²(equal to 100G). ● Waveform : 1/2 Sine wave,6msec ● ±X , ±Y , ±Z , each axis 1 times
Vibration (Non-Operation)	<ul style="list-style-type: none"> ● Frequency range : 8~33.3Hz ● Stoke : 1.3 mm ● Vibration : sinusoidal wave, perpendicular axis (both x, z axis:2Hrs, y axis 4Hrs). ● Sweep : 2.9G, 33.3 Hz -400 Hz ● Cycle : 15 min

7.3 Electrostatic Discharge

TEST ITEM	CONDITIONS	NOTE
ESD	150pF , 330Ω , ±8kV&±15kV air& contact test	1
	200pF , 0Ω , ±200V contact test	2

Note: Measure point :

1. LCD glass and metal bezel
2. IF connector pins

7.4 Judgment Standard

The judgment of the above test should be made as follow:

Pass: Normal display image with no obvious non-uniformity and no line defect.

Partial transformation of the module parts should be ignored.

Fail: No display image, obvious non-uniformity, or line defects.

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