HITACHI

FOR MESSRS: DATE: Nov. 30th 2009

TECHNICAL DATA

10.4“ VGA UHB TFT with LED BACKLIGHT

Contents

2. RECORD OF REVISION

DATE	SHEET No.	SUMMARY

3. GENERAL DATA

3.1 DISPLAY FEATURES

This module is a 10.4” VGA of 4:3 format amorphous silicon TFT. The pixel format is vertical stripe and sub pixels are arranged as R (red), G (green), B (blue) sequentially. This display is RoHS compliant, COG (chip on glass) technology and LED backlight are applied on this display.

Part Name	TX26D**VM****
Module Dimensions	243.0(W) mm x 185.1(V) mm x (12.0) (D) mm
LCD Active Area	211.2(H) mm x 158.4(V) mm
Pixel Pitch	0.33(W) mm x 0.33 (H) mm
Resolution	640 x 3(RGB)(W) x 480(H) dots
Color Pixel Arrangement	R, G, B Vertical stripe
LCD Type	Transmissive Color TFT; Normally White; Anti-Reflection Polarizer
Display Type	Active Matrix
Number of Colors	262k Colors
Backlight	24 LEDs (6 series x 4)
Weight	TBD
Interface	1ch - LVDS / Receiver; 20 pins
Power Supply Voltage	3.3V for LCD; 12V for Backlight
Power Consumption	(0.66W) for LCD; (8.16W) for Backlight
Viewing Direction	12 O’clock (without image inversion and least brightness change)

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	VDD	-0.3	4	V	-
Input Voltage of Logic	VI	-0.2	VDD+0.3	V	Note 1
Operating Temperature	Top	(-20)	(70)	°C	Note 2
Storage Temperature	Tst	(-30)	(80)	°C	Note 2
Backlight Input Voltage	VLED	10.0	17.0	V	-

Note 1: The rating is defined for the signal voltages of the interface such as DTMG, DCLK, DIM, FRC, MSL and pixel data signal.

Note 2: The maximum rating is defined as above based on the temperature on the panel surface, which might be different from ambient temperature after assembling the panel into the application. Moreover, some temperature-related phenomenon as below needed to be noticed:

- Background color, contrast and response time would be different in temperatures other than 25°C.
- Operating under high temperature will shorten LED lifetime.
- Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

5. ELECTRICAL CHARACTERISTICS

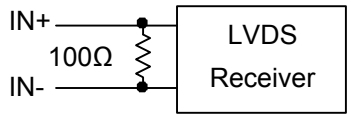
5.1 LCD CHARACTERISTICS

$T_a = 25\ ^\circ C,\ \mathrm{VSS} = 0\mathrm{V}$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	VDD	-	3.0	3.3	3.6	V	-
Differential Input Voltage for LVDS Receiver Threshold	VI	VIH	-	-	+100	mV	Note 1
		VIL	-100	-	-		
Power Supply Current	IDD	VDD-VSS =3.3V	-	TBD	-	mA	Note 2,3,4
Vsync Frequency	f_v	-	-	60	70	Hz	Note 5
Hsync Frequency	f_H	-	-	31.6	38	KHz	-
DCLK Frequency	f_{CLK}	-	-	25	29	MHz	-

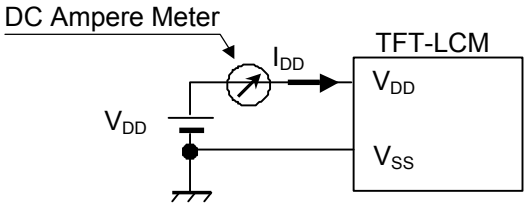
Note 1: VCM=+1.2V

VCM between vin+ and vin- is common mode voltage of LVDS transmitter/receiver. The input terminal of LVDS transmitter is terminated with 100Ω.



Note 2: fv=60Hz, fCLK=25.0MHz, and VDD=3.3V, are the test conditions.

Typical value is measured when displaying vertical 64 gray scale. Maximum is measured when displaying Vertical-stripe.



Note 3: For LVDS Transmitter Input

Note 4: 1A fuse is built in the LCM. Current capacity for VDD power supply should be larger than 2A, so that the fuse built in the LCM (maximum) could appropriately work under the abnormal conditions.

Note 5: Vertical Frequency 60Hz is recommended for best optical performance in terms of flicker.

5.2 BACKLIGHT CHARACTERISTICS

$T_a = 25\ ^\circ C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
LED Input Voltage	VLED	Backlight Unit	10.8	12.0	13.2	V	Note 1
LED Driving Current (DIM Control)	ILED	DIM=0V;0%Duty	-	(680)	-	mA	Note 2
		DIM=3.3V;100%Duty	-	(11)	-		
LED Lifetime	-	96mA x 4	-	(70k)	-	hrs	Note 3

Note 1: As Fig 5.1 shown, all LEDs are controlled by the LED Driver when applying 12V VLED.

Note 2: Dimming function can be obtained by applying DC voltage or PWM signal from the display interface CN1. The recommend PWM signal is 1KHz ~ 10KHz with 3.3V amplitude. The brightness is increased when applied DC voltage or PWM duty of DIM Pin is decreased.

Note 3: The estimated lifetime is specified as the time to reduce 50% brightness by applying 96mA x 4 at 25°C.

Note 4: 1A fuse is built in the LCM, current capacity for VDD power supply should be larger than 2A, so that the fuse built in the LCM (maximum) could appropriately work under the abnormal conditions.

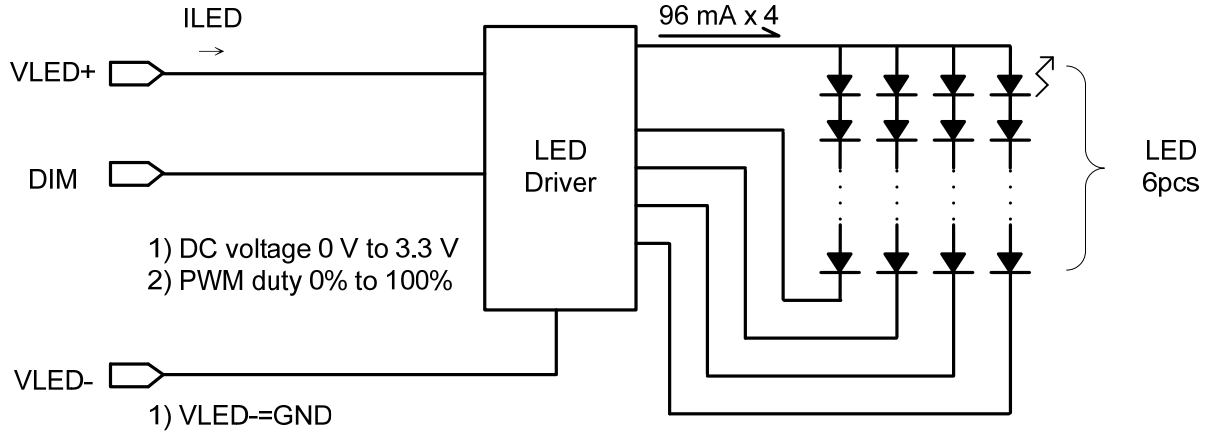


Fig 5.1

6. OPTICAL CHARACTERISTICS

The optical characteristics are measured based on the conditions as below:

- Supplying the signals and voltages defined in the section of electrical characteristics.
- The backlight unit needs to be turned on for 30 minutes.
- The ambient temperature is 25°C.
- In the dark room around 500~1000 lx, the equipment has been set for the measurements as shown in Fig 6.1.

$T_a = 25\ ^{\circ}C$, $f_v = 60$ Hz, VDD = 3.3V

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Brightness of White		-	$\phi = 0^{\circ}, \theta = 0^{\circ}$, ILED= (384mA)	TBD	(1000)	-	cd/m^2	Note 1
Brightness Uniformity		-		TBD	-	-	%	Note 2
Contrast Ratio		CR		-	(800)	-	-	Note 3
Response Time (Rising + Falling)		$T_r + T_f$	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	30	-	ms	Note 4
NTSC Ratio		-	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	TBD	-	%	-
Viewing Angle		θ x	$\phi = 0^{\circ}$, CR ≥ 10	-	(60)	-	Degree	Note 5
		θ x′	$\phi = 180^{\circ}$, CR ≥ 10	-	(60)	-		
		θ y	$\phi = 90^{\circ}$, CR ≥ 10	-	(55)	-		
		θ y′	$\phi = 270^{\circ}$, CR ≥ 10	-	(60)	-		
Color Chromaticity	Red	X	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	(0.62)	-	-	Note 6
		Y		-	(0.34)	-		
	Green	X		-	(0.31)	-		
		Y		-	(0.59)	-		
	Blue	X		-	(0.14)	-		
		Y		-	(0.09)	-		
	White	X		-	(0.31)	-		
		Y		-	(0.32)	-		

Note 1: The brightness is measured from the panel center point, P5 in Fig. 6.2, for the typical value.

Note 2: The brightness uniformity is calculated by the equation as below:

$$\text{Brightness uniformity} = \frac{\text{Min. Brightness}}{\text{Max. Brightness}} \times 100\%$$

, which is based on the brightness values of the 9 points measured by BM-5 as shown in Fig. 6.2.

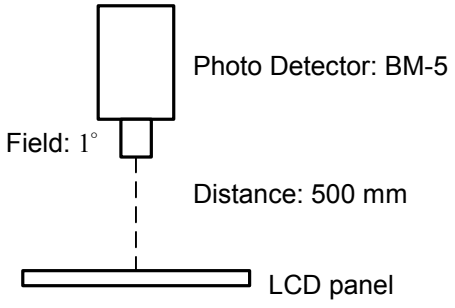


Fig. 6.1

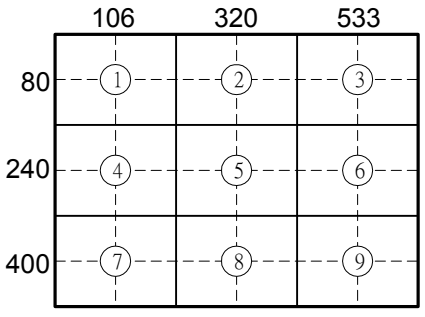


Fig. 6.2

Note 3: The Contrast Ratio is measured from the center point of the panel, P5, and defined as the following equation:

$$CR = \frac{\text{Brightness of White}}{\text{Brightness of Black}}$$

Note 4: The definition of response time is shown in Fig. 6.3. The rising time is the period from 90% brightness to 10% brightness when the data is from white to black. Oppositely, Falling time is the period from 10% brightness rising to 90% brightness.

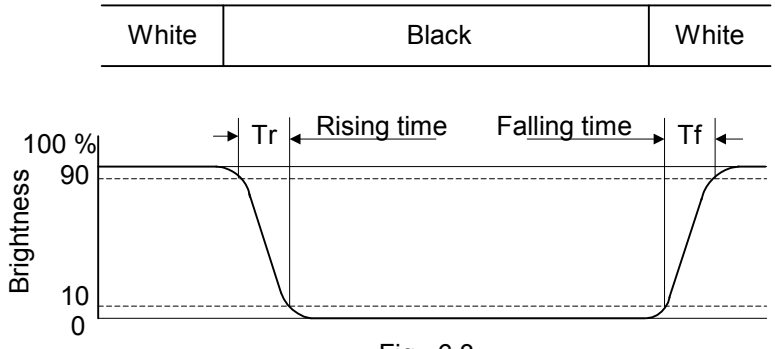


Fig . 6.3

Note 5: The definition of viewing angle is shown in Fig. 6.4. Angle ϕ is used to represent viewing directions, for instance, $\phi = 270^\circ$ means 6 o'clock, and $\phi = 0^\circ$ means 3 o'clock. Moreover, angle θ is used to represent viewing angles from axis Z toward plane XY.

The viewing direction of this display is 12 o'clock, which means that a photograph with gray scale would not be reversed in color and the brightness change would be less from this direction. However, the best contrast peak would be located at 6 o'clock.

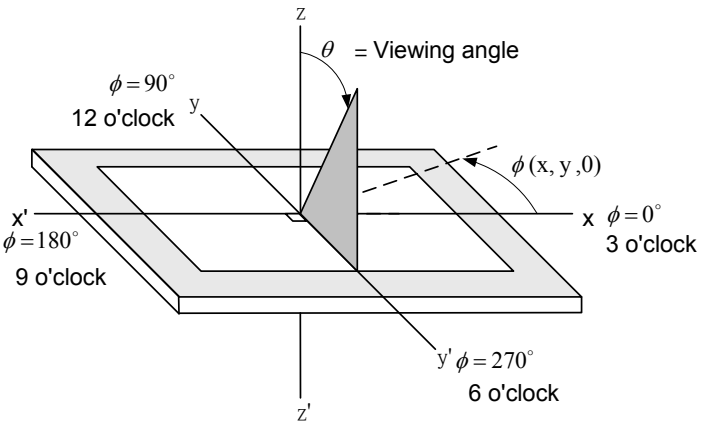
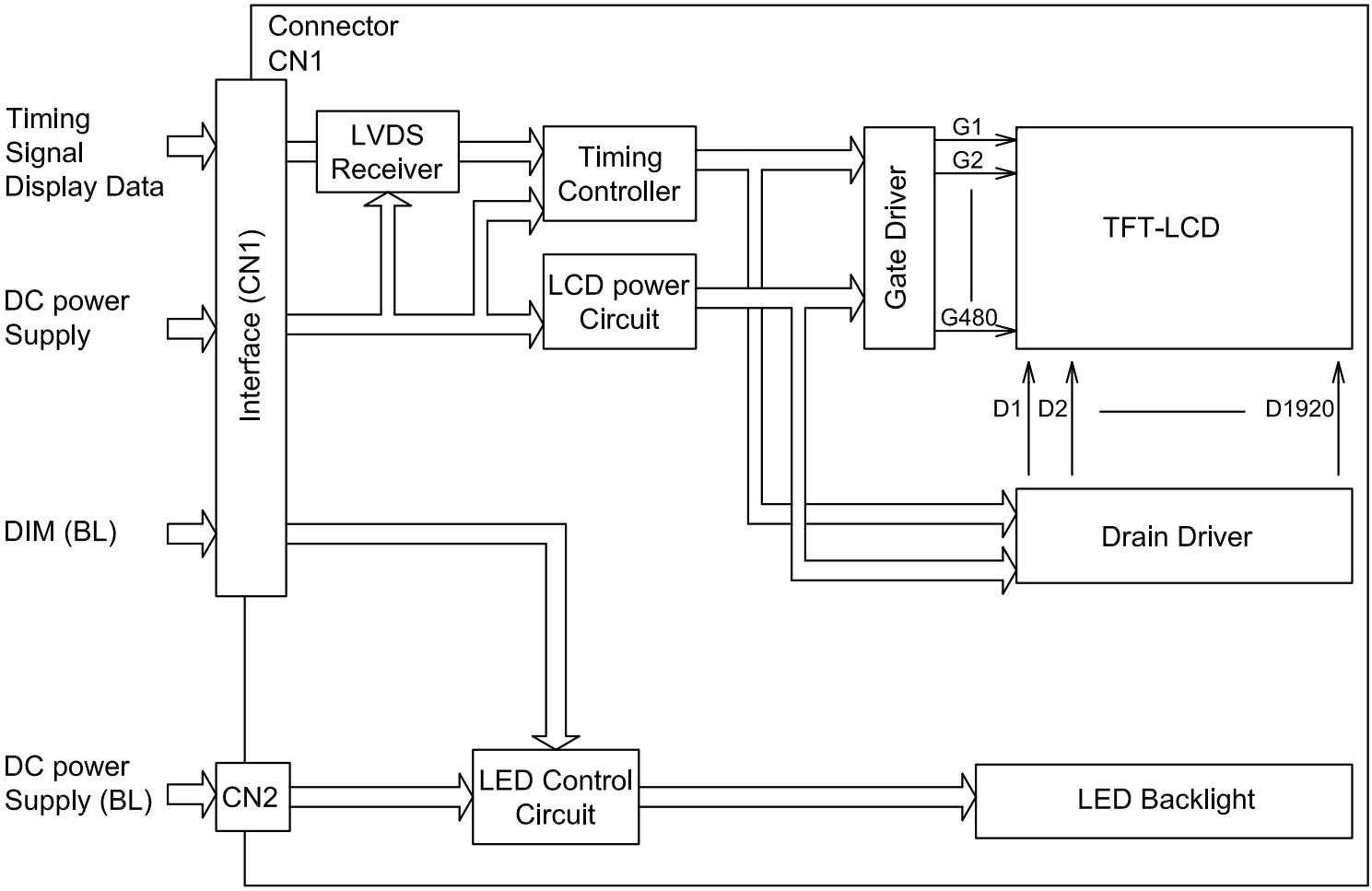


Fig 6.4

Note 6: The color chromaticity is measured from the center point of the panel, P5, as shown in Fig. 6.2.

7 BLOCK DIAGRAM



8. LCD INTERFACE

8.1 INTERFACE PIN CONNECTIONS

The display interface connector is FI-SEB20P-HF13E-E1500 made by JAE and more details of the connector are shown in the section of outline dimension.

Pin assignment of LCD interface is as below:

Pin No.	Signal	Function	Pin No.	Signal	Function
1	VDD	Power Supply for Logic	11	IN2-	Pixel Data
2	VDD		12	IN2+	
3	VSS	GND	13	VSS	GND
4	VSS		14	CLK IN-	Clock
5	IN0-	Pixel Data	15	CLK IN+	
6	IN0+		16	FRC	L:6 bit Mode H:8 bit Mode
7	VSS	GND	17	IN3-	Pixel Data
8	IN1-	Pixel Data	18	IN3+	
9	IN1+		19	MSL	LVDS Format Setting (Refer to P8-5/12)
10	VSS	GND	20	DIM	Dimming function

Note 1: IN n- and IN n+ (n=0,1,2,3),CLK IN- and CLK IN+ are recommended to be twisted or side-by-side FPC patterns, respectively.

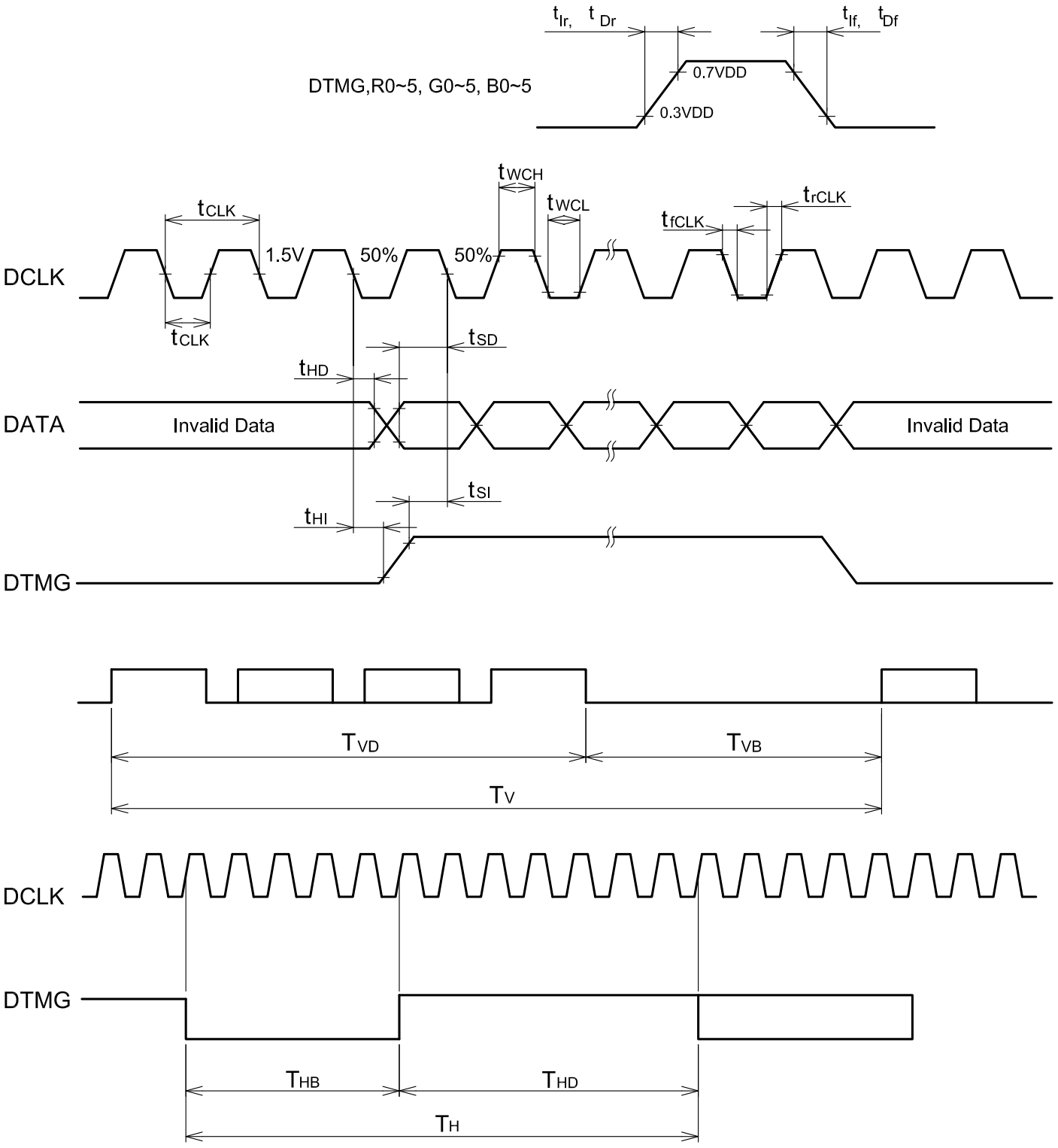
Note 2: When using 6 bit RGB, the connection circuit of IN3-, IN3+ and MSL refers to P8-8/12.

The backlight interface connector is SM08B-SRSS-TB made by JST, and pin assignment of backlight is as below:

Pin No.	Signal	Level	Function
1,2,3	V_{LED}+	-	Power Supply for LED
4,5	NC	-	No Connection
6,7,8	V_{LED}-	-	GND

8.2 TIMING CHART

DTMG (Data Enable) is the signal to determine valid data, and the timing of DTMG can be determined from Hsync and Vsync as below. For this display, only DTMG and DCLK are the essential signals. Hsync and Vsync are not necessary to connect to display interface after DTMG has been generated and input.



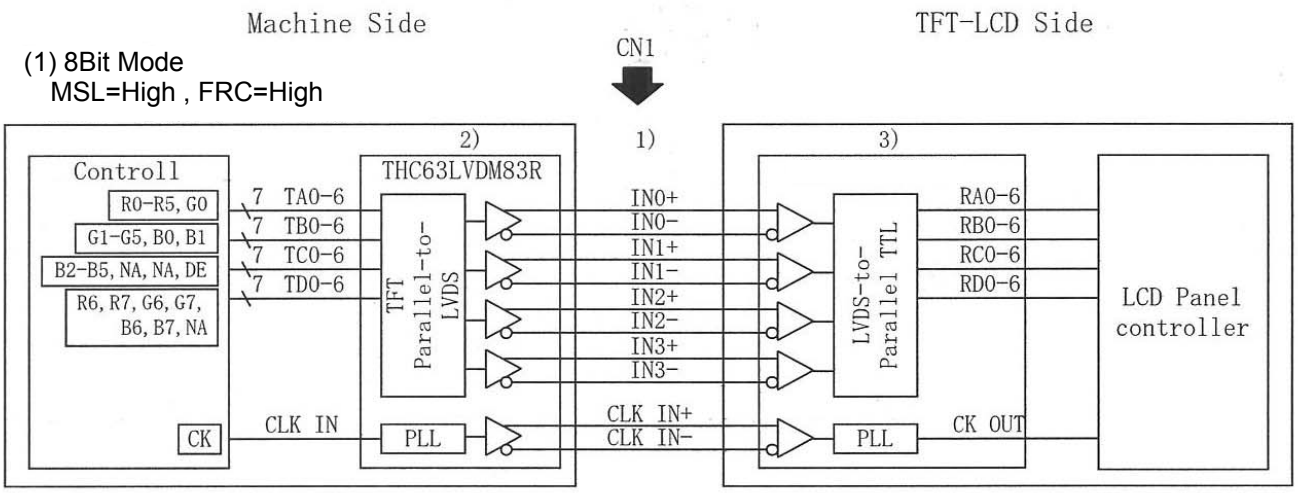
Data is latched by falling edge triggered DCLK

8.3 INTERFACE TIMING SPECIFICATIONS

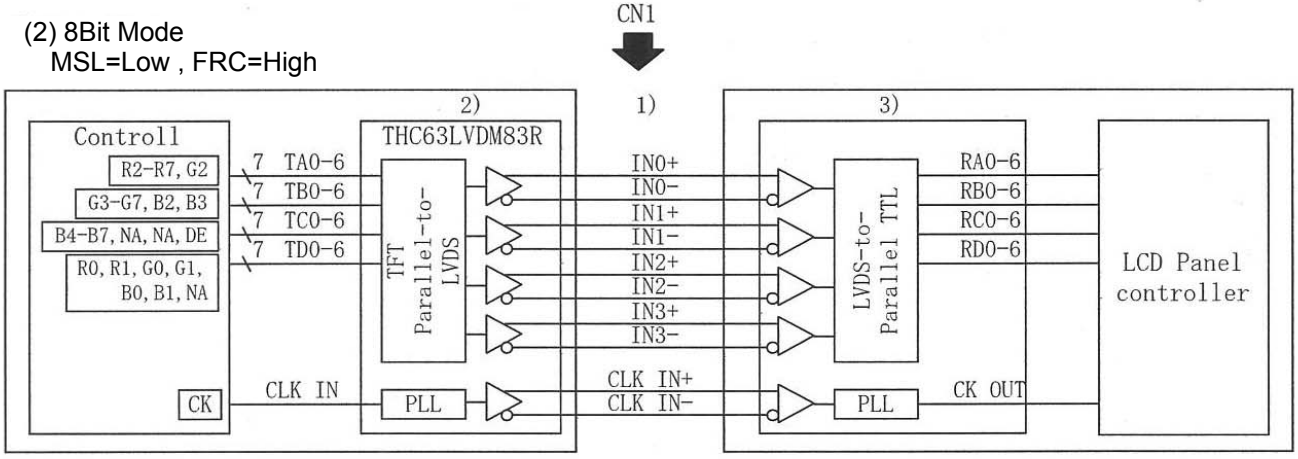
Item		Symbol	Min.	Typ.	Max.	Unit
DCLK	Cycle time	t_{CLK}	34.5	40	43	ns
	Low level Width	t_{WCL}	12	-	-	
	High level Width	t_{WCH}	12	-	-	
	Rise time	t_{rCLK}	-	-	5	
	Fall time	t_{fCLK}	-	-	5	
	Duty	D	0.45	0.5	0.55	-
DTMG	Set up time	t_{SI}	5	-	-	ns
	Hold time	t_{HI}	10	-	-	
	Rise/Fall time	t_{Ir},t_{If}	-	-	5	ns
	Horizontal Cycle	T_H	(760)	(800)	(870)	TH
	Horizontal Valid Data width	T_{HD}	-	640	-	
	Horizontal porch width	T_{HB}	-	(160)	-	
	Vertical Cycle	Tv	(515)	(525)	(609)	Tv
	Vertical Valid Data width	T_{VD}	-	480	-	
	Vertical porch width	T_{VB}	-	(45)	-	
Data	Set up time	t_{SD}	5	-	-	ns
	Hold time	t_{HD}	10	-	-	
	Rise/Fall time	t_{Dr},t_{Df}	-	-	5	ns

8.4 LVDS INTERFALE

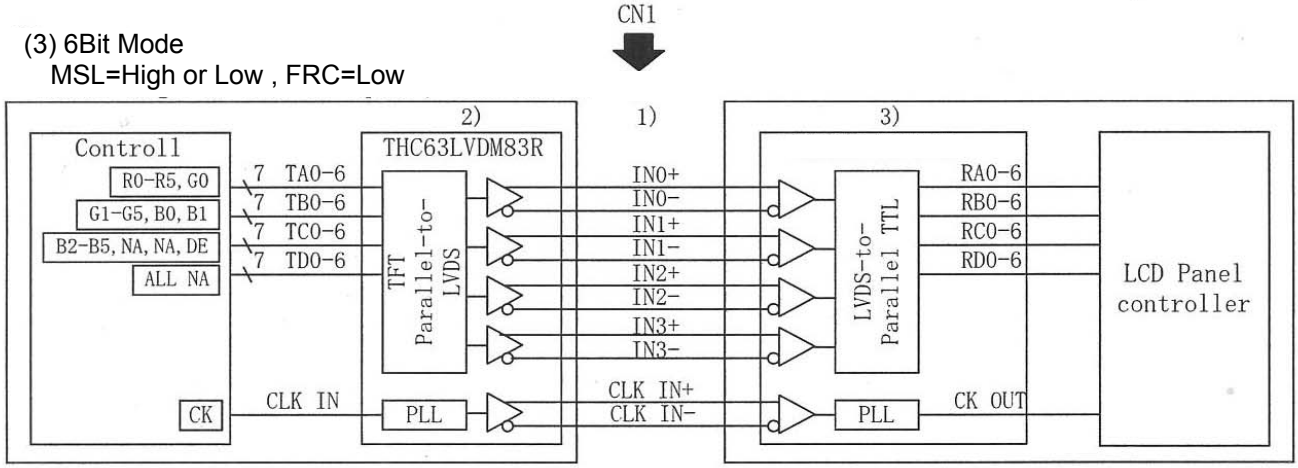
(1) 8Bit Mode
MSL=High , FRC=High



(2) 8Bit Mode
MSL=Low , FRC=High



(3) 6Bit Mode
MSL=High or Low , FRC=Low



Note 1) LVDS cable impedance should be 100 ohms per signal line when each
2-lines(+,-) is used in differential mode.

Note 2) Transmitter Made by Thine : THC63LVDM83R equivalent.
Transmitter is not contained in Module.

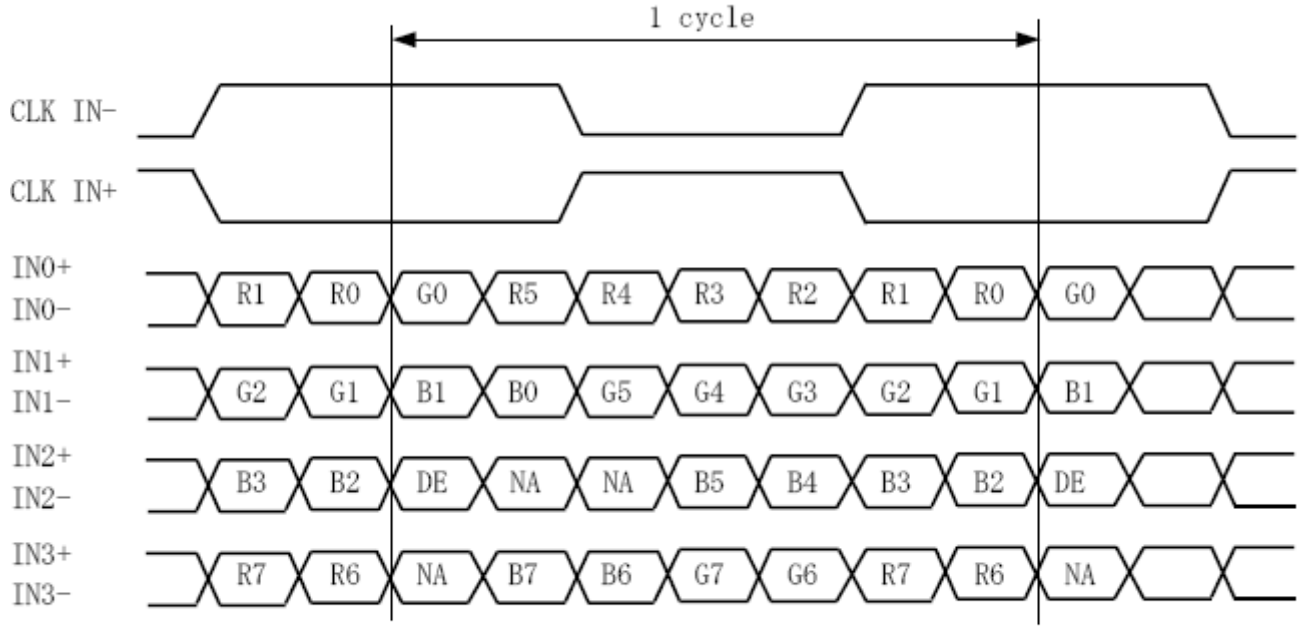
8.5 LVDS DATA MAPPING

1) 8 Bit Mode

Note : Assignment in the Mode A(THC63LVDM83R)

Transmitter		MSL	
Pin No.	Date	=High	=Low
51	TA0	R0 (LSB)	R2
52	TA1	R1	R3
54	TA2	R2	R4
55	TA3	R3	R5
56	TA4	R4	R6
3	TA5	R5	R7 (MSB)
4	TA6	G0 (LSB)	G2
6	TB0	G1	G3
7	TB1	G2	G4
11	TB2	G3	G5
12	TB3	G4	G6
14	TB4	G5	G7 (MSB)
15	TB5	B0 (LSB)	B2
19	TB6	B1	B3
20	TC0	B2	B4
22	TC1	B3	B5
23	TC2	B4	B6
24	TC3	B5	B7 (MSB)
27	TC4	(NA)	(NA)
28	TC5	(NA)	(NA)
30	TC6	DE	DE
50	TD0	R6	R0 (LSB)
2	TD1	R7 (MSB)	R1
8	TD2	G6	G0 (LSB)
10	TD3	G7 (MSB)	G1
16	TD4	B6	B0 (LSB)
18	TD5	B7 (MSB)	B1
25	TD6	(NA)	(NA)

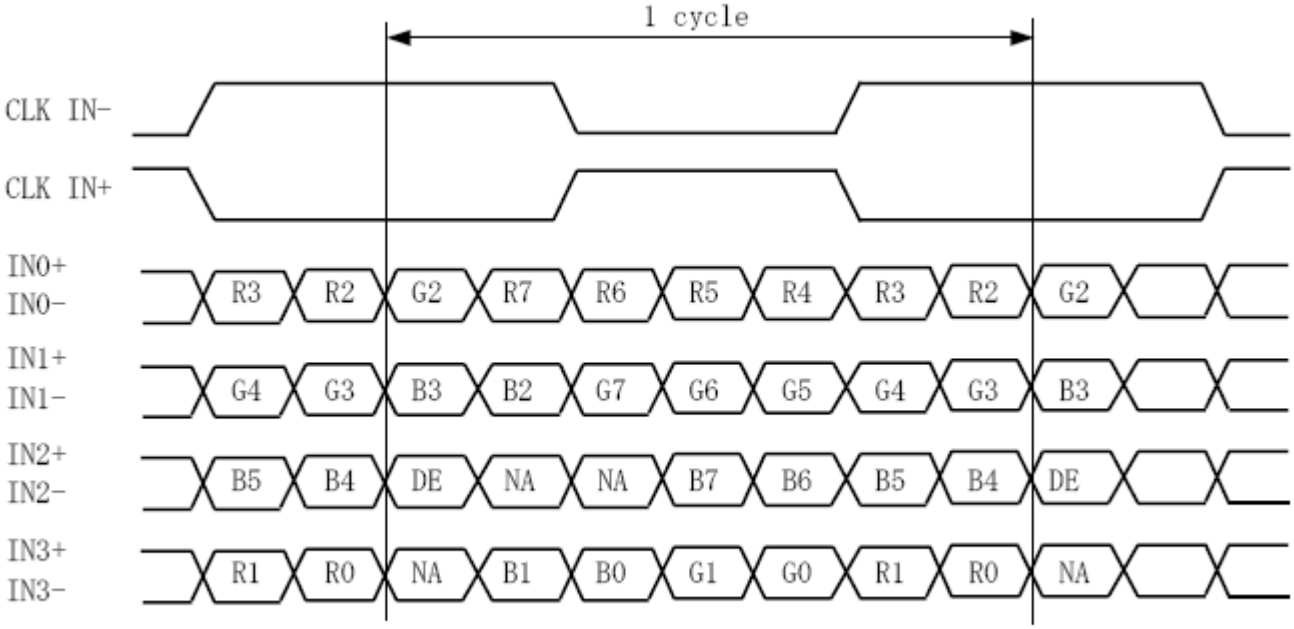
＜MSL=High＞



DE : Display Enable

NA : Not Available

＜MSL=Low＞



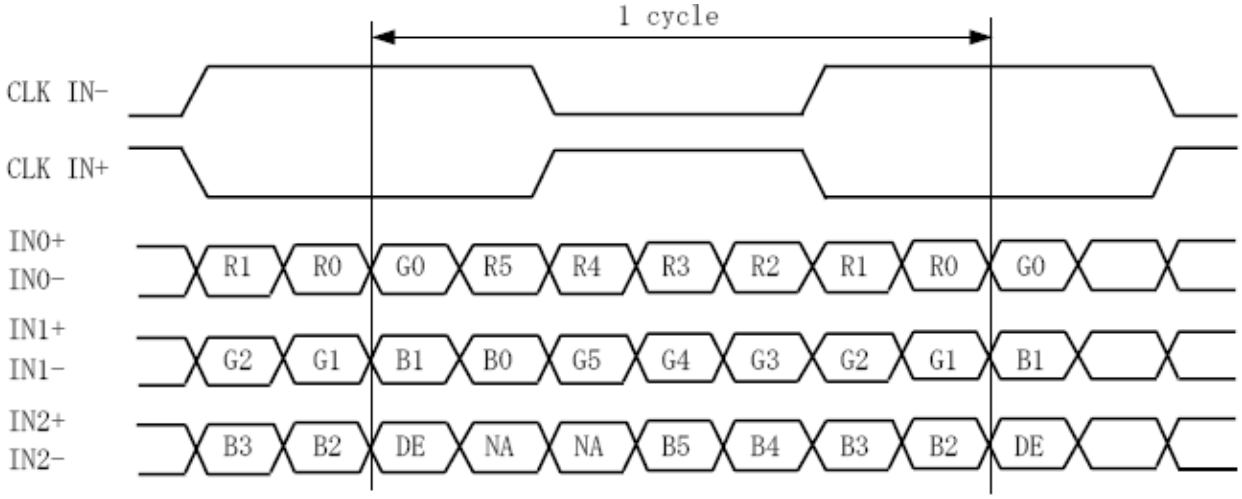
DE : Display Enable

NA : Not Available

2) 6 Bit Mode

Note : Assignment in the Mode A(THC63LVDM83R)

Transmitter		MSL	
Pin No.	Date	=High	=Low
51	TA0	R0 (LSB)	R0 (LSB)
52	TA1	R1	R1
54	TA2	R2	R2
55	TA3	R3	R3
56	TA4	R4	R4
3	TA5	R5 (MSB)	R5 (MSB)
4	TA6	G0 (LSB)	G0 (LSB)
6	TB0	G1	G1
7	TB1	G2	G2
11	TB2	G3	G3
12	TB3	G4	G4
14	TB4	G5 (MSB)	G5 (MSB)
15	TB5	B0 (LSB)	B0 (LSB)
19	TB6	B1	B1
20	TC0	B2	B2
22	TC1	B3	B3
23	TC2	B4	B4
24	TC3	B5 (MSB)	B5 (MSB)
27	TC4	(NA)	(NA)
28	TC5	(NA)	(NA)
30	TC6	DE	DE
50	TD0	(NA)	(NA)
2	TD1	(NA)	(NA)
8	TD2	(NA)	(NA)
10	TD3	(NA)	(NA)
16	TD4	(NA)	(NA)
18	TD5	(NA)	(NA)
25	TD6	(NA)	(NA)

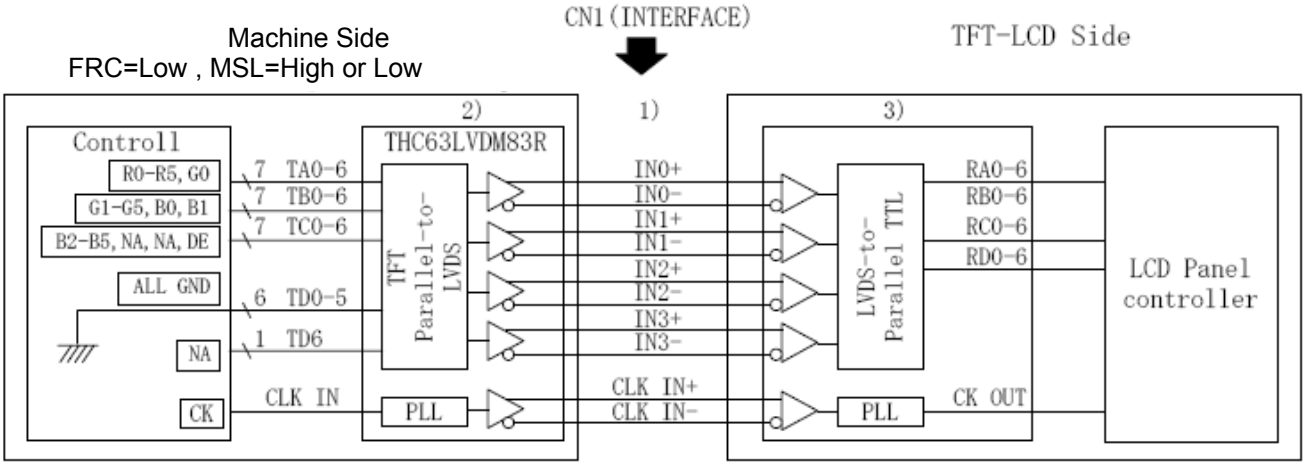


DE : Display Enable

NA : Not Available

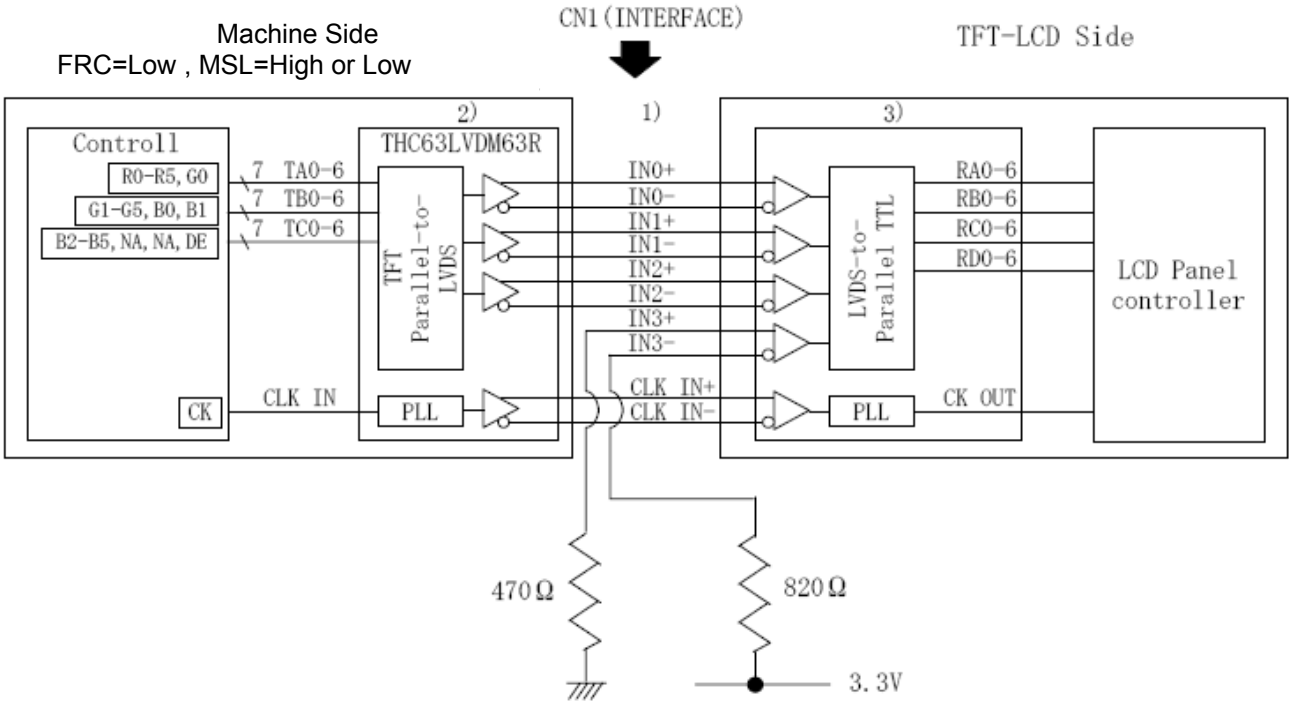
＊ Connection circuit of IN3-, IN3+ for 6 bit mode

① Connect TD0～TD5 to GND



② Connect IN3+ by 3.3V resistor 820Ω and connect IN3- to GND by resistor 470Ω as below circuit.

Never turn on LCD when IN3+ and IN3- are Open.



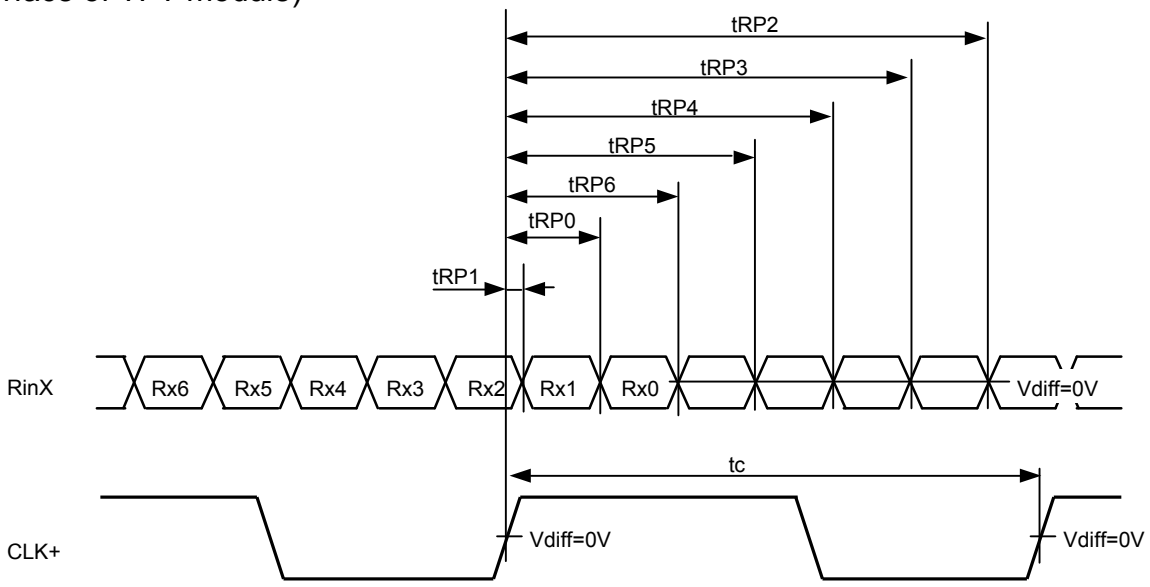
Note 1 : The impedance between differential signal pair should be 100 ohms.

Note 2 : Transmitter is not contained in module.

The recommended transmitter is Thine THC63LVDM83R or equivalent.

8.6 LVDS RECEIVER TIMING

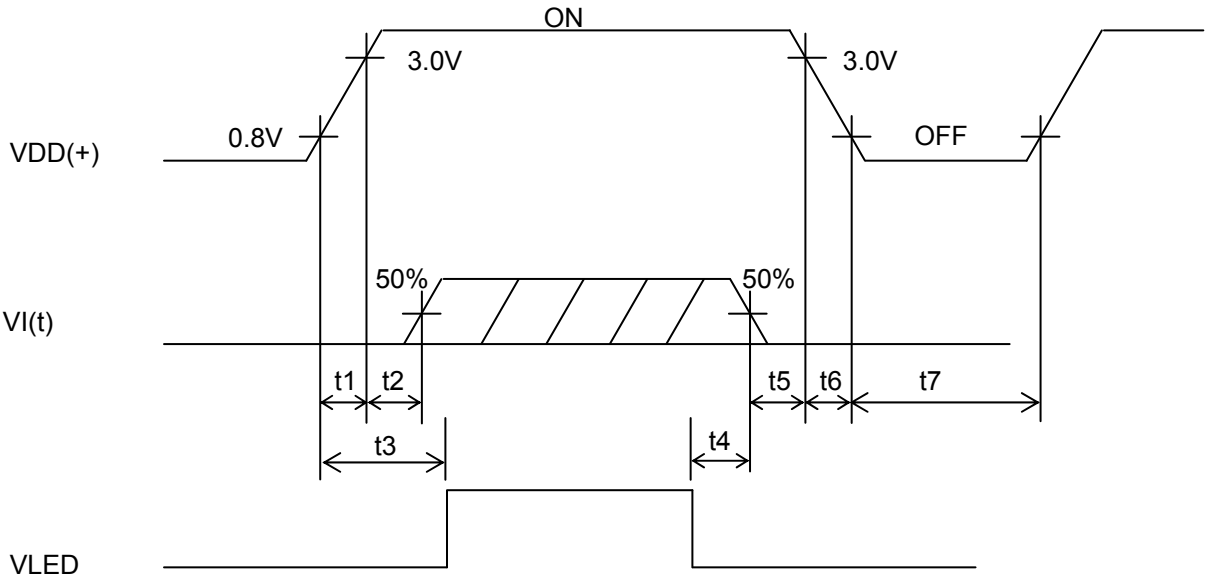
(Interface of TFT module)



RinX=(RinX+)-(RinX-) (X=0,1,2,3)

Item		Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	FREQUENCY	1/tc	-	(25)	(29)	MHz	
RinX (X=0,1,2,3)	0 data position	tRP0	1/7*tCLK -0.65	1/7*tCLK	1/7tCLK +0.65	ns	
	1st data position	tRP1	-0.65	0	+0.65		
	2nd data position	tRP2	6/7*tCLK -0.65	6/7*tCLK	6/7*tCLK +0.65		
	3rd data position	tRP3	5/7*tCLK -0.65	5/7*tCLK	5/7*tCLK +0.65		
	4th data position	tRP4	4/7*tCLK -0.65	4/7*tCLK	4/7*tCLK +0.65		
	5th data position	tRP5	3/7*tCLK -0.65	3/7*tCLK	3/7*tCLK +0.65		
	6th data position	tRP6	2/7*tCLK -0.65	2/7*tCLK	2/7*tCLK +0.65		

8.7 POWER SEQUENCE



POWER ON

0ms＜ t1≦15ms

0ms＜ t2 ≦45ms

100ms≦t3

POWER OFF

5ms≦t4

0ms＜ t5 ≦45ms

0ms＜ t6 ≦20ms

500ms≦t7

Note 1: VDD(+)=Power supply voltage

VI(t)=LVDS Interface Signal

VLED=Back-Light Power Supply voltage

Note 2: 0V≦VI(t)≦VDD(t)

VI(t) and VDD(t) is a surfeit of condition for power on/off.

Note 3: Input Voltage (Signal) should not be set high impedance when power on.

8.8 DATA INPUT for DISPLAY COLOR(8 BIT MODE)

Input color		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB							LSB	MSB							LSB	MSB							LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note 1: Definition of gray scale : Color(n) Number in parenthesis indicates gray scale level. Larger number corresponds to brighter level.

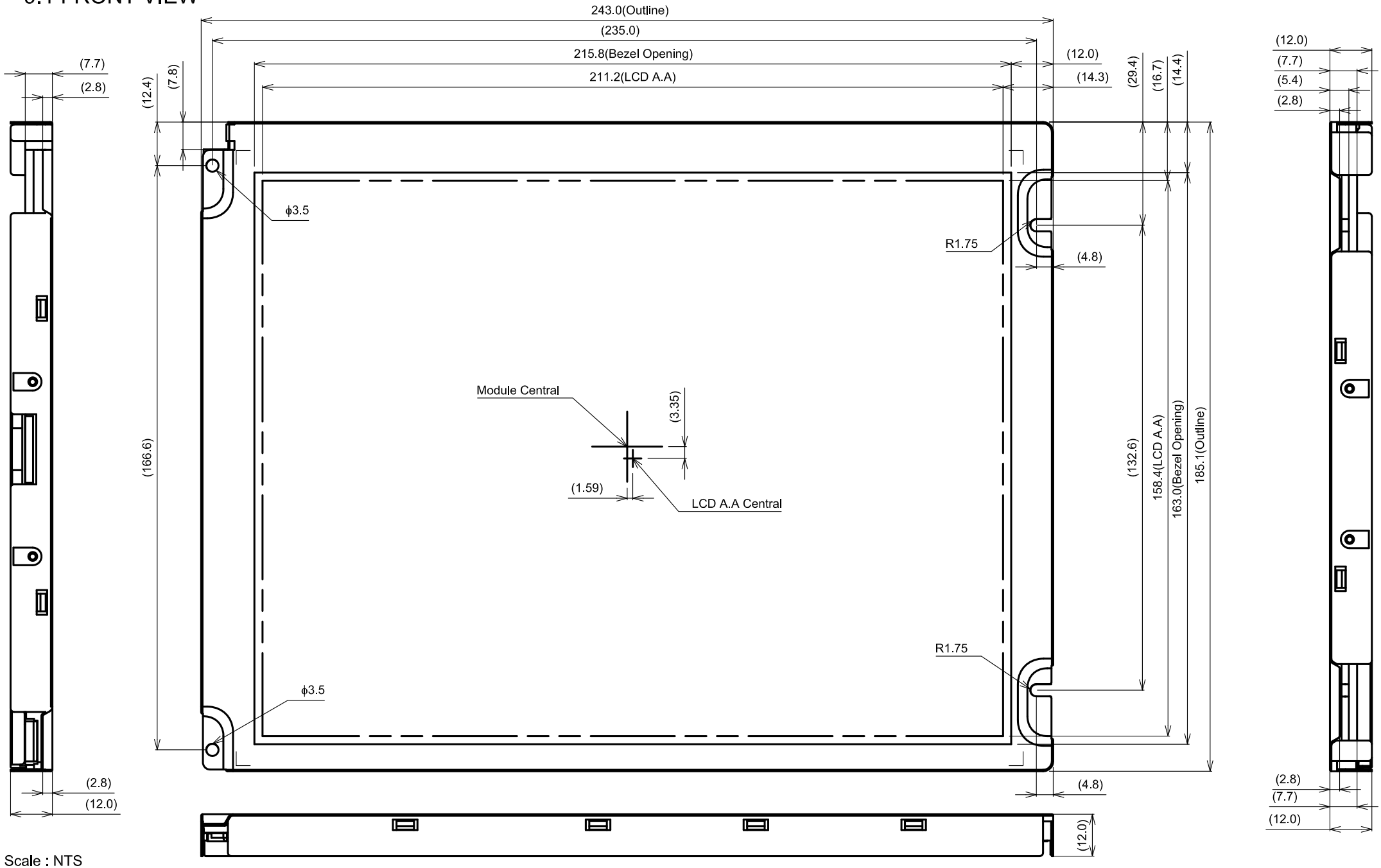
Note 2: Data Signal : 1 : High, 0 : Low

8.9 DATA INPUT for DISPLAY COLOR (6 BIT MODE)

	COLOR & Gray Scale	Data Signal																	
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

9. OUTLINE DIMENSIONS

9.1 FRONT VIEW



Scale : NTS
Unit : mm

Note 1:The unspecified tolerance ±0.5mm

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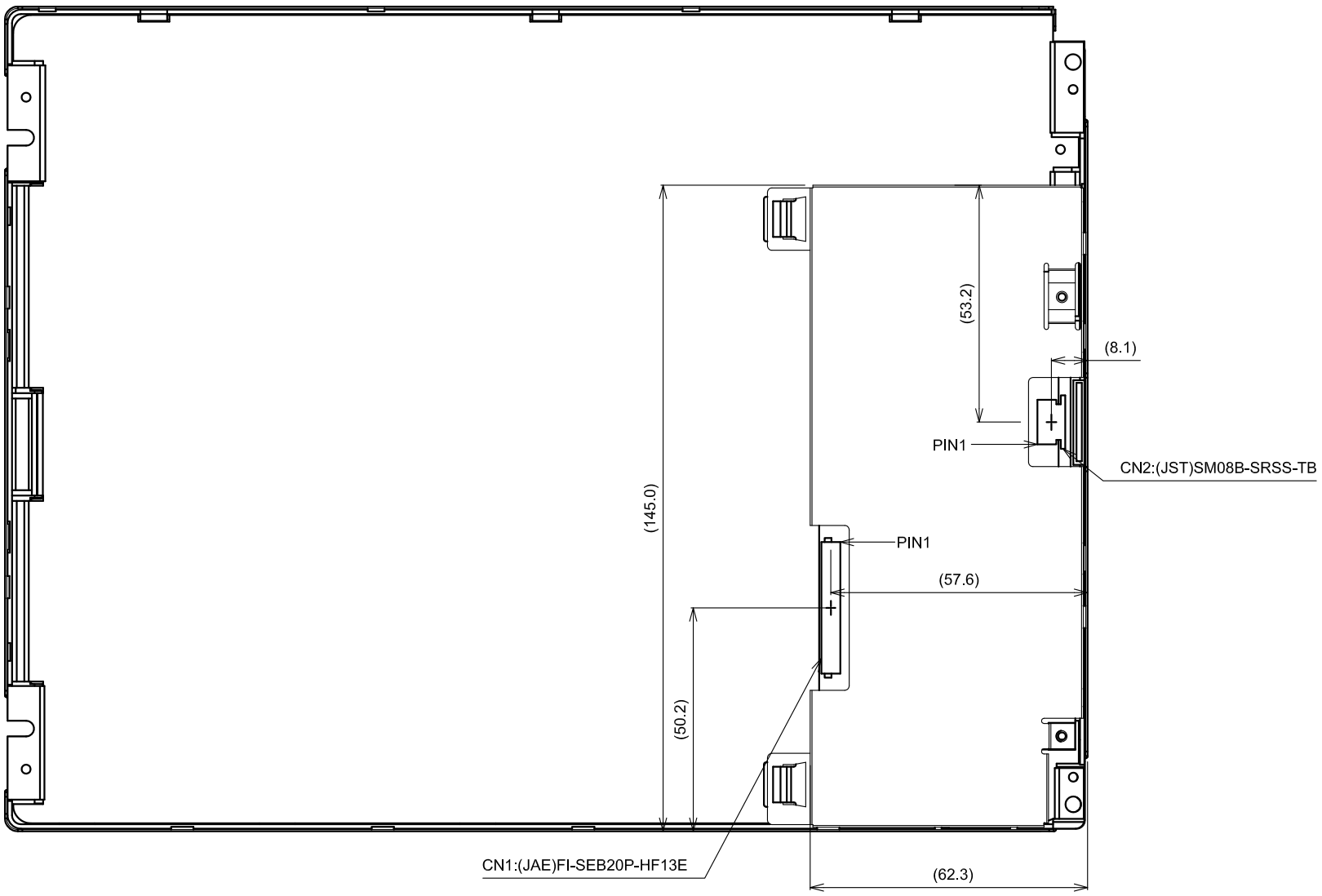

Scale : NTS
Unit : mm

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