LIQUID CRYSTAL DISPLAY MODULE TECHNICAL DATA
(TENTATIVE)

LTPMD0625

Date : Apr 10, 2009

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RECORD OF REVISIONS

Date	Sheet No.	Summary

3. GENERAL SPECIFICATIONS

(1)	Product Name	LTPMD0625
(2)	Module Dimensions	60.17 (W) mm × 43.78 (H) mm × 2.85 (t) mm (typ)
(3)	Active Area Dimensions	49.92(W) mm × 37.44 (H) mm, 2.46" diagonally
(4)	Dot Pitch	0.052 (W) mm × 0.156 (H) mm
(5)	Resolution	960 (W) × 240 (H) dots
(6)	Color Pixel Arrangement	RGB Delta Arrangement
(7)	Display Mode	Transmissive Type, Normally Black Mode
(8)	Upper Polarizer	with HC
(9)	Number of Colors	16M Colors (Dithering)
(10)	Viewing Direction	Especially none
(11)	Backlight	Four LEDs
(12)	Weight	22 g (typ) (Excluded protective sheet)
(13)	Power Supply Voltage	Vcc=3.0 V (typ)
(14)	Interface	RGB Interface (8 bits)

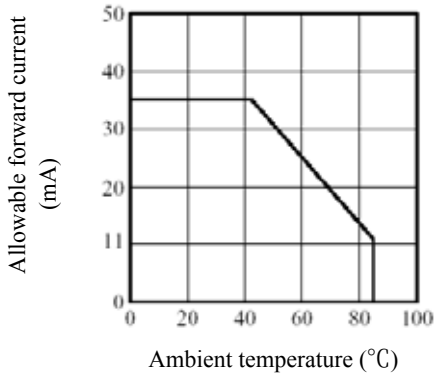
4. ABSOLUTE MAXIMUM RATINGS

4.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS OF LCD

PGND, GND=0 V

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VCC VCCIO PVCC	-0.3	4.0	V	(1)
Input Voltage	V_{t1}	-0.3	VCCI/O+0.3	V	(1), (2)
LED Reverse Voltage	VR	-	20	V	
LED Forward Current	ILED	-	Note (3)	mA	

Notes (1) Each voltage refers to GND and PGND.
(2) Applies to the VSYNC, HSYNC, DCLK, DIN0 to DIN7, SDI, SCL and CS pins.
(3) Ambient Temperature vs. Allowable Forward Current



4.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

Item	Operating		Storage		Comment
	Min.	Max.	Min.	Max.	
Ambient Temperature (Ta)	0°C	40°C	0°C	40°C	Note (1)
Humidity	Note (2)		Note (2)		No condensation
Corrosive Gas	Not Acceptable		Not Acceptable		

Notes (1) Background color, hue and contrast ratio may slightly change depending on ambient temperature and viewing angle.
The temperatures for operating in the table above apply to operation only.
Visual qualities, such as contrast and response time, are to be evaluated at Ta=25°C.
(2) Ta $\leq$ 40°C : 85%RH Max.
(3) Refer to Note (3) of Item 4.1 for the LED current of the backlight unit.

5. ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS OF LCD

Ta=25°C, GND=0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	VCC	-	2.9	3.3	3.6	V	(5)
Power Supply Voltage for Step-up Circuit	PVCC	-	2.9	3.3	3.6	V	(5)
Power Supply Voltage for Control Signal Interface	VCCIO	-	1.8	3.3	3.6	V	(5)
Input Voltage for Logic Circuits	Vi	"H" level	0.8 × VCCIO	-	VCCIO	V	(1)
		"L" level	GND	-	0.2 × VCCIO	V	
Input Leak current	I_{Li}	-	-5.0	-	+5.0	μA	(1)
Consumption Current	ICC	RGB vertical stripe	-	6.0	11.0	mA	(2)
LED Current	ILED	-	-	24.0	Note (3)	mA	(3)
LED Forward Voltage	VF	ILED=24mA	(10.8)	(13.2)	(14.4)	V	

The values with parentheses are just for reference.

Notes (1) Applies to the VSYNC, HSYNC, DCLK, DIN0 to DIN7, SDI, SCL and CS pins.
(2) PVCC=VCCIO=VCC=3.0 V, f_{FLM}=59.94 Hz
(3) Refer to Item 4.1, Electrical Absolute Maximum Ratings of LCD on Page 4-1/1.
(4) The metal frame must be connected to GND level to prevent static electricity affecting the screen performance.
(5) Voltage fluctuation of power supply must be maintained within ±0.1 V while the LCD module is operated.

6. OPTICAL CHARACTERISTICS

6.1 OPTICAL CHARACTERISTICS OF LCD (Transmissive type)

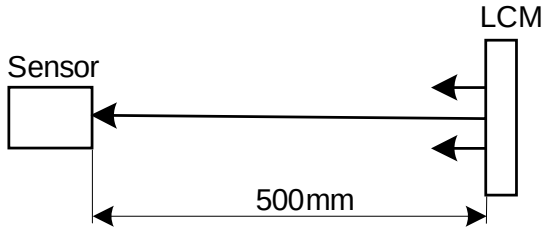
Ta=25℃

ITEM		SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
Brightness		B	ϕ=0°, θ=0°	400	550	-	cd/m^2	1)
Uniformity		-	ϕ=0°, θ=0°	-	-	±30	%	3), 5)
Viewing angle		ϕ2-ϕ1	θ=0°, CR≧2.0	-	170	-	°	4), 6), 7)
			ϕ=90°, CR≧2.0	-	170	-		
Contrast ratio		CR	ϕ=0°, θ=0°	(300)	500	-	-	6)
Response time (rise+fall)		tr+tf	ϕ=0° θ=0° Ta=25°C	-	(30)	(45)	ms	8)
Color tone (Primary Color)	Red	x	ϕ=0°, θ=0°	0.520	0.570	0.620	-	1)
		y		0.290	0.340	0.390		
	Green	x		0.290	0.340	0.390		
		y		0.520	0.570	0.620		
	Blue	x		0.100	0.150	0.200		
		y		0.080	0.130	0.180		
	White	x		0.260	0.310	0.360		
		y		0.280	0.330	0.380		

(Measurement condition: Hitachi standard)

The values with parentheses are just for reference.

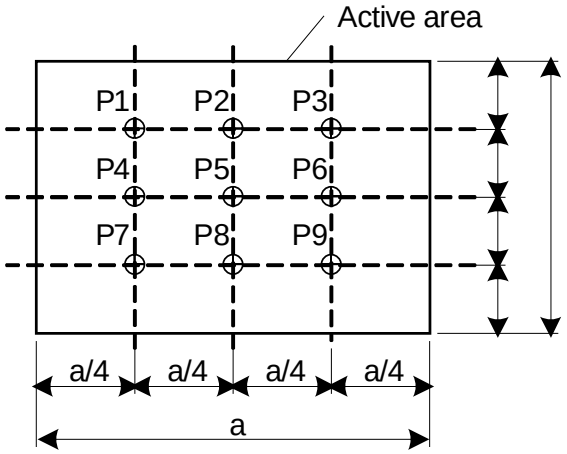
Note 1. Definition of Brightness "B"



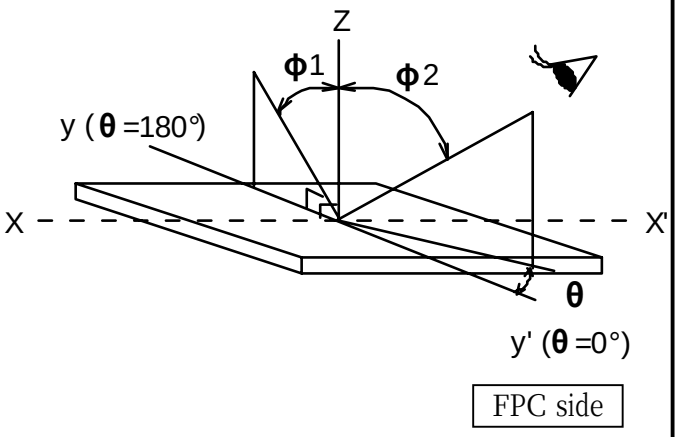
Sensor: CS-1000A
or equivalent

Measuring point: Active area center

Note 3. Measuring point



Note 4. Definition of θ and φ



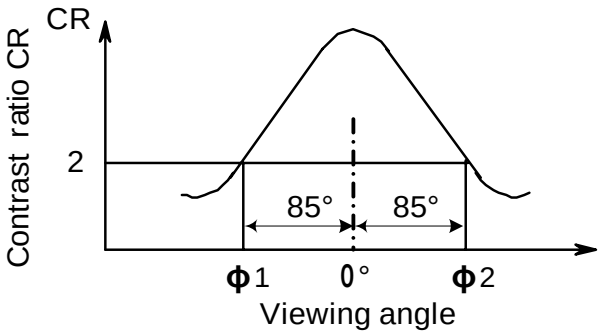
Note 5. Definition of the brightness uniformity

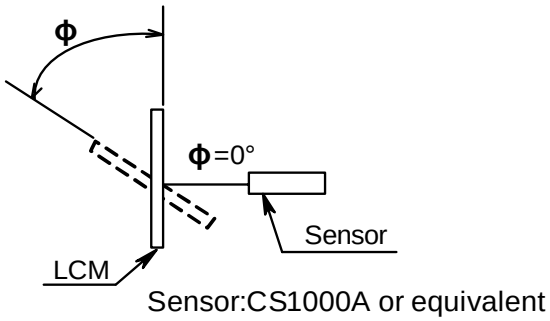
$$\frac{\text{(Max brightness or Min brightness) - (Average brightness)}}{\text{(Average brightness)}} \times 100$$

Note 6. Definition of Contrast ratio "CR"

$$CR = \frac{\text{Brightness when displaying White raster}}{\text{Brightness when displaying Black raster}}$$

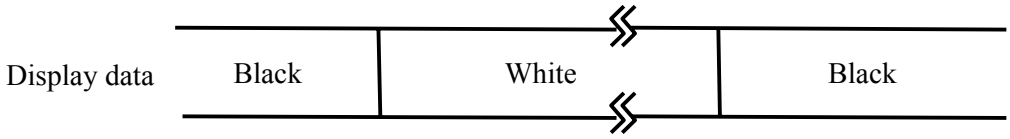
Note 7. Definition of viewing angle φ1and φ2

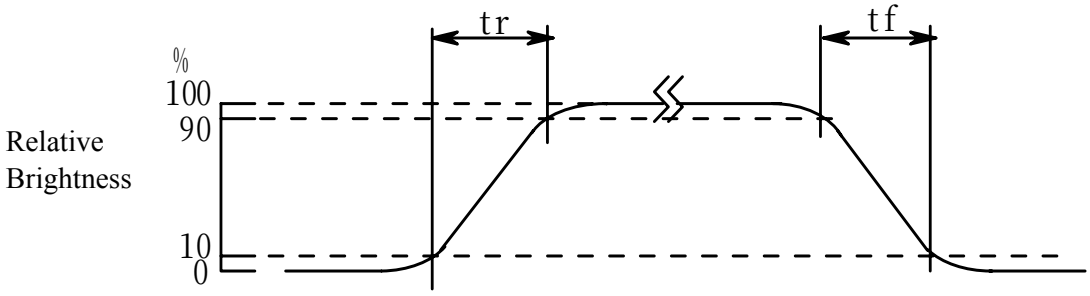




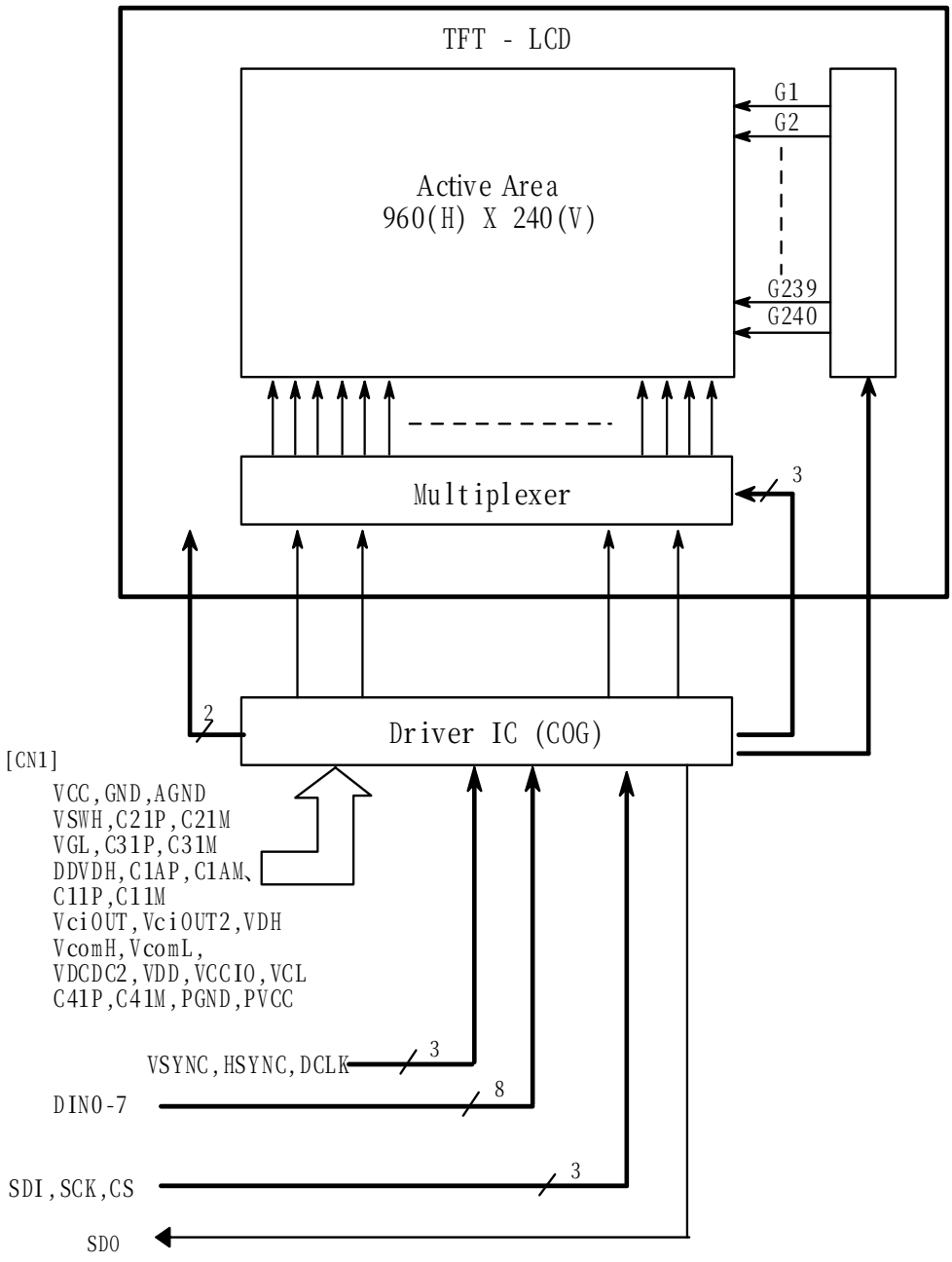
Sensor:CS1000A or equivalent

Note 8. Definition of optical response time

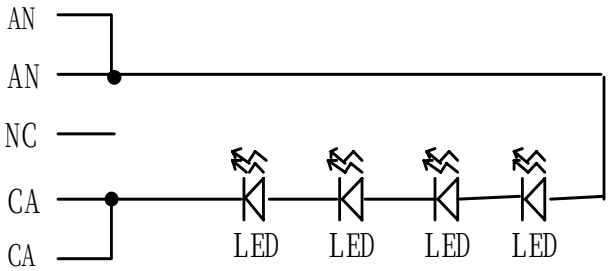




7. BLOCK DIAGRAM



[CN2]



8. INTERFACE

8.1 INTERNAL PIN CONNECTION

CN1

No.	Signal Name	Function	Remarks
1	C11M	Step-up capacitor	
2	C11P	Step-up capacitor	
3	C1AP	Step-up capacitor	
4	C1AM	Step-up capacitor	
5	PVCC	Power supply for step-up circuit	To be same potential as VCC
6	PGND	Ground for step-up circuit	To be same potential as GND
7	VciOUT	Reference voltage	
8	C41M	Step-up capacitor	
9	C41P	Step-up capacitor	
10	VCL	Reference voltage	
11	C31M	Step-up capacitor	
12	C31P	Step-up capacitor	
13	VGL	Negative voltage for panel circuit/VCOM drive	
14	VciOUT2	Reference voltage	
15	C21M	Step-up capacitor (C21-)	
16	C21P	Step-up capacitor (C21+)	
17	VSWH	Positive voltage for panel circuit	
18	VDCDC2	Reference voltage	
19	GND	Ground	
20	AGND	Ground for analog circuit	To be same potential as GND
21	DDVDH	Reference voltage	
22	VCCIO	Power supply for control data interface	
23	VCC	Power supply for analog circuit	
24	VDD	Internal power supply	
25	DIN7	Display data(MSB)	
26	DIN6	Display data	
27	DIN5	Display data	
28	DIN4	Display data	
29	DIN3	Display data	
30	DIN2	Display data	
31	DIN1	Display data	
32	DIN0	Display data(LSB)	
33	HSYNC	Horizontal synchronous for display data	
34	VSYNC	Vertical synchronous for display data	
35	GND	(DCLK shield)	
36	DCLK	Clock signal for display data	
37	GND	(DCLK shield)	
38	CS	Chip select for serial communication	
39	SCL	Clock for serial communication	
40	SDI	Data for serial communication	
41	SDO	Data for serial communication	
42	VDH	Reference voltage for gray scale/VCOM amplitude	
43	VCOML	Power supply for common low level	
44	VCOMH	Power supply for common high level	
45	GND	Ground	

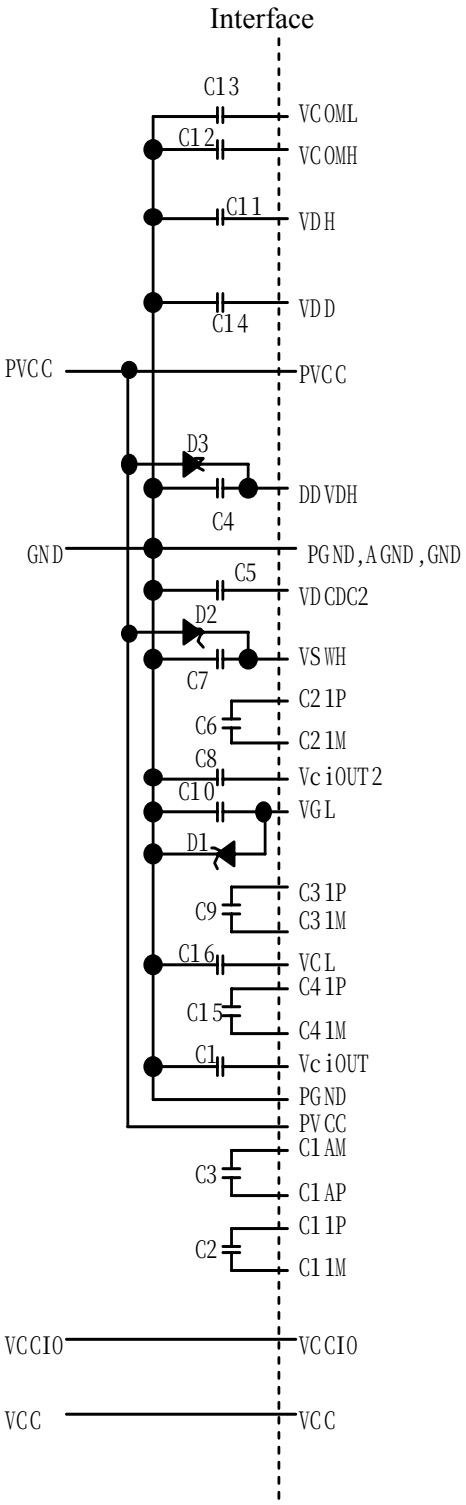
CN2

№	Pin Name	Description
1	CA	Cathode
2	CA	Cathode
3	NC	Open
4	AN	Anode
5	AN	Anode

8.2 SUITABLE CONNECTOR

CN1：molex SD-501616-001(45pins、0.3pictch zig-zag arrangement)
CN2：JST 05FHJ-SM1-GB(LF)(GB)(5pins、0.5pitch)

8.3 RECOMMENDED POWER CIRCUIT



Capacitor	Capacitance/Applied Voltage	Withstanding Voltage	Wiring Resistance
(C1)VciOUT	1μF/VciOUT	6VMin	3ΩMax
(C2)C11P/M	1μF/VciOUT	6VMin	3ΩMax
(C3)C1AP/M	1μF/VciOUT	6VMin	3ΩMax
(C4)DDVDH	1μF/DDVDH	10VMin	3ΩMax
(C5)VDCDC2	1μF/VDCDC2	10VMin	10ΩMax
(C6)C21P/M	1μF/VDCDC2	10VMin	10ΩMax
(C7)VSWH	1μF/VSWH	16VMin	10ΩMax
(C8)VciOUT2	1μF/VciOUT2	6VMin	10ΩMax
(C9)C31P/M	1μF/VciOUT2	6VMin	10ΩMax
(C10)VGL	1μF/VciOUT2	6VMin	10ΩMax
(C11)VDH	1μF/VDH	10VMin	20ΩMax
(C12)VcomH	1μF/VCOMH	10VMin	6ΩMax
(C13)VcomL	1μF/VCOML	6VMin	6ΩMax
(C14)VDD	1μF/VDD	3VMin	3ΩMax
(C15)C41P/M	1μF/VciOUT	6VMin	6ΩMax
(C16)VCL	1μF/VciOUT	6VMin	6ΩMax

Use a Capacitor with Characterstic "B".

Other parts	Spec	Remarks
D1～D3	VF＜0.4／20mA@25°C	Connect a Schottky diode.

8.4 INTERFACE TIMING

GND=0V, PVCC=VCC=VCCIO=2.9V to 3.6V,tr=tf=4ns, (at 25 deg Cenvironment)

* : Depending on input signal

= : Limited to typical values

(1) Horizontal Timing

Item	Symbol	Scope	Min	Typ	Max	Unit	Remarks	Note
Clock cycle time	Trate	DCLK	34	37	-	ns	Typ:f=27MHz	
Clock "Low" level pulse width	Tcwl	DCLK	12			ns		
Clock "High" level pulse width	Tcwh	DCLK	12			ns		
Data set up time	Tds	DIN0-7, DCLK	7			ns		
Data hold time	Tdh	DIN0-7, DCLK	8			ns		
Horizontal scanning period	Th	HSYNC	*	63.556	*	ns		
Horizontal effective display period	Thd	HSYNC, DCLK, DIN0-7	=	960	=	DCLK		
Horizontal front porch	Thf	HSYNC, DCLK	0			DCLK		
Horizontal synchronizing pulse width	Thp	HSYNC, DCLK	1			DCLK		
Horizontal back porch	Thb	HSYNC, DCLK	15	162	486	DCLK		
DOTCLK setup time	Tdcs	HSYNC, DCLK	8			ns		
DOTCLK hold time	Tdch	HSYNC, DCLK	8			ns		

(2) Vertical Timing

Item	Symbol	Scope	Min	Typ	Max	Unit	Remarks	Note
Vertical scanning period	Tv	VSYNC	*	16.68	*	ms	f=60Hz	
			250	262	264	HSYNC		
Vertical effective display period	Tvd	VSYNC, HSYNC	=	240	=	HSYNC		
Vertical front porch	Tvf	VSYNC, HSYNC	1	-	15	HSYNC		
Vertical "Low" level pulse width	Tvp	VSYNC, HSYNC	1	-	12	HSYNC		
Vertical back porch	Tvb	VSYNC, HSYNC	9	9	12	HSYNC		

(3) Serial Interface Timing (Write)

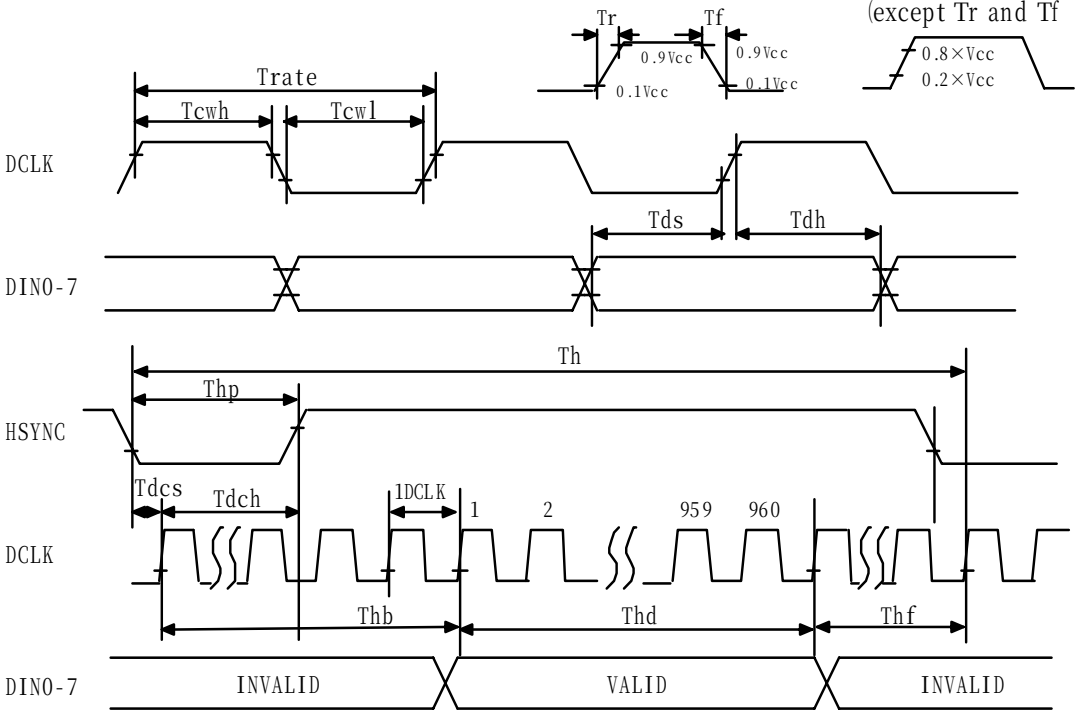
Item	Scope	Scope	Min	Typ	Max	Unit	Remarks	Note
Serial clock cycle time	Tcycs	SCL	300			ns		
Serial clock "Low" level pulse width	Tscwl	SCL	120			ns		
Serial clock "High" level pulse width	Tscwh	SCL	120			ns		
Serial data setup time	Tsds	SDI,SCL	100			ns		
Serial data hold time	Tsdh	SDI,SCL	100			ns		
Chip select setup time	Tess	CS,SCL	100			ns		
Chip select hold time	Tcsh	CS,SCL	100			ns		

(4) Serial Interface Timing (Read)

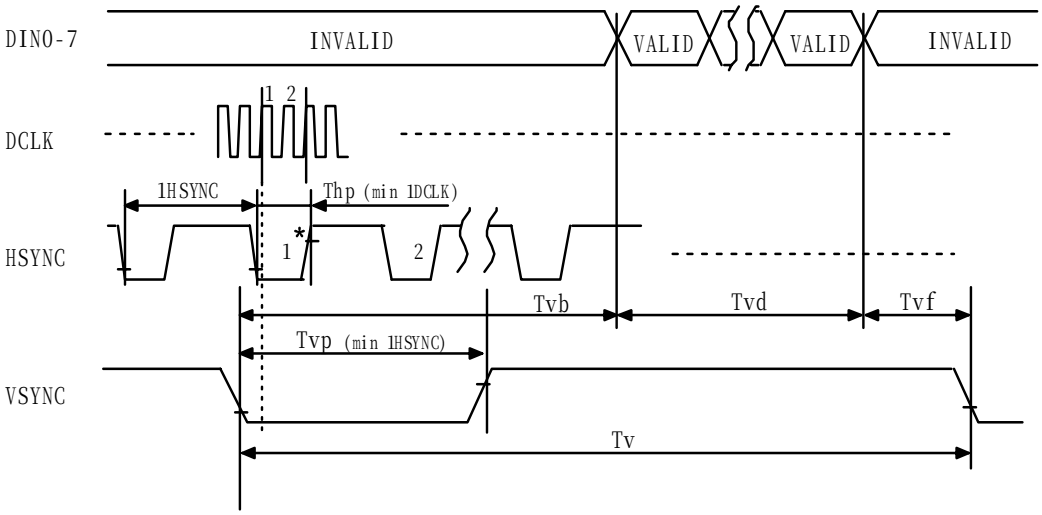
Item	Scope	Scope	Min	Typ	Max	Unit	Remarks	Note
Serial clock cycle time	Tcycs	SCL	500			ns		
Serial clock "Low" level pulse width	Tscwl	SCL	230			ns		
Serial clock "High" level pulse width	Tscwh	SCL	230			ns		
Serial data setup time	Tsds	SD0,SCL	200			ns		

[Horizontal Timing]

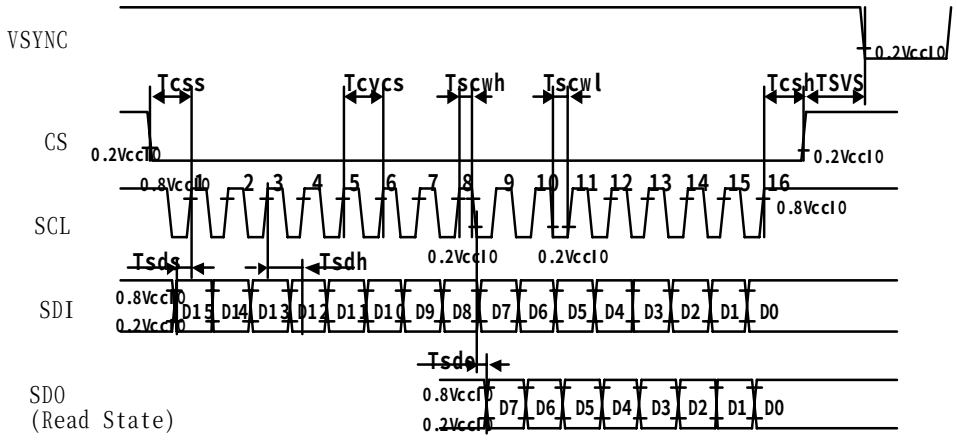
Measurement point
(except Tr and Tf)



[Vertical Timing]

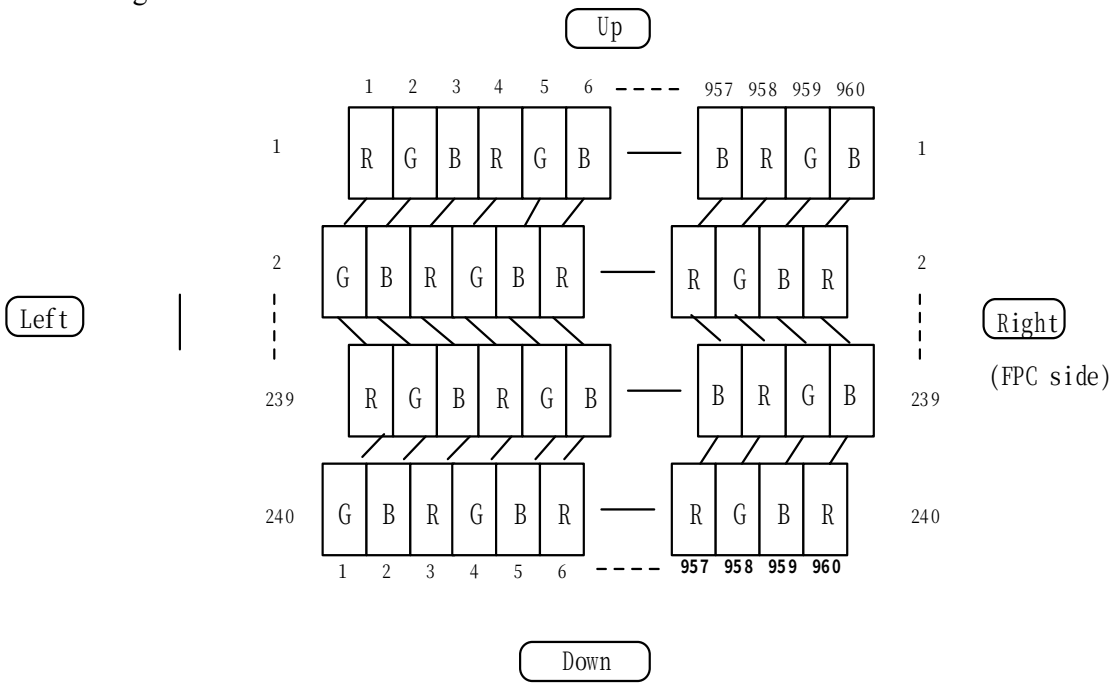


[Serial Interface Timing]

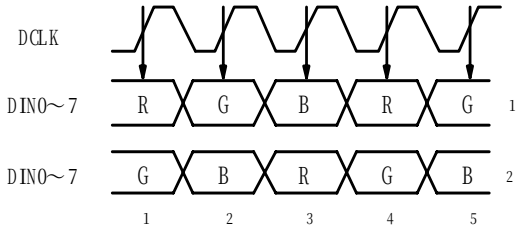


8.5 DOTS ARRANGEMENT AND DATA INPUT

(1)Dots Arrangement



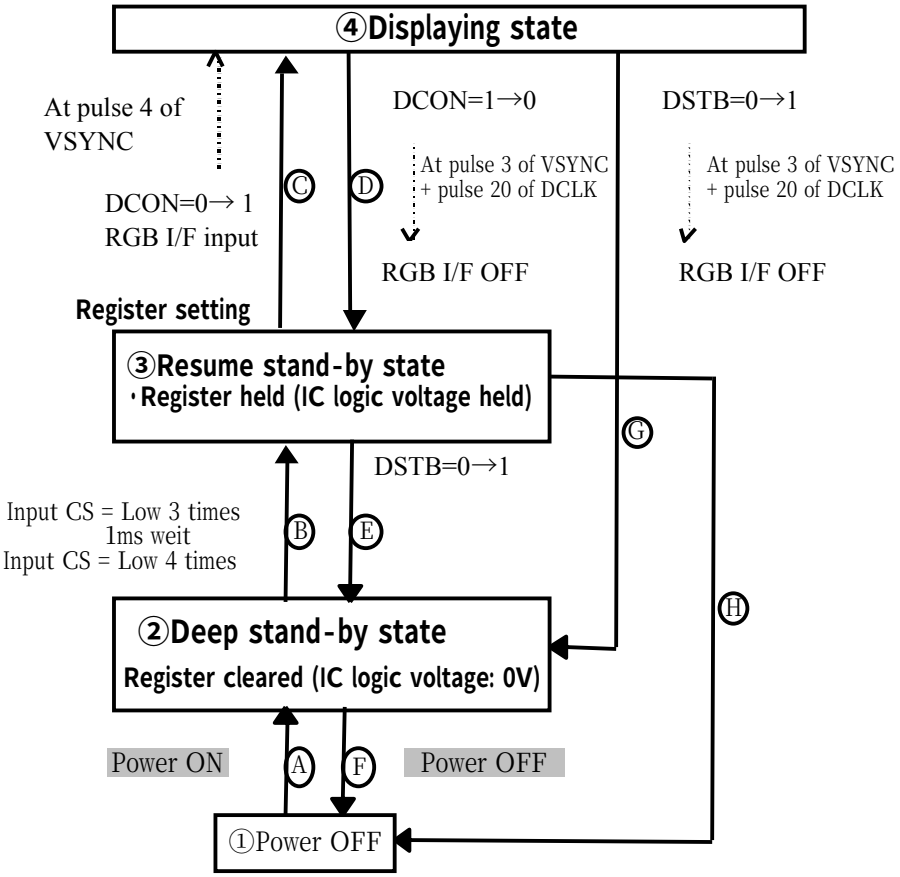
(2)Data input



8.6 POWER SUPPLY SEQUENCE

(1) ON-OFF States Transition

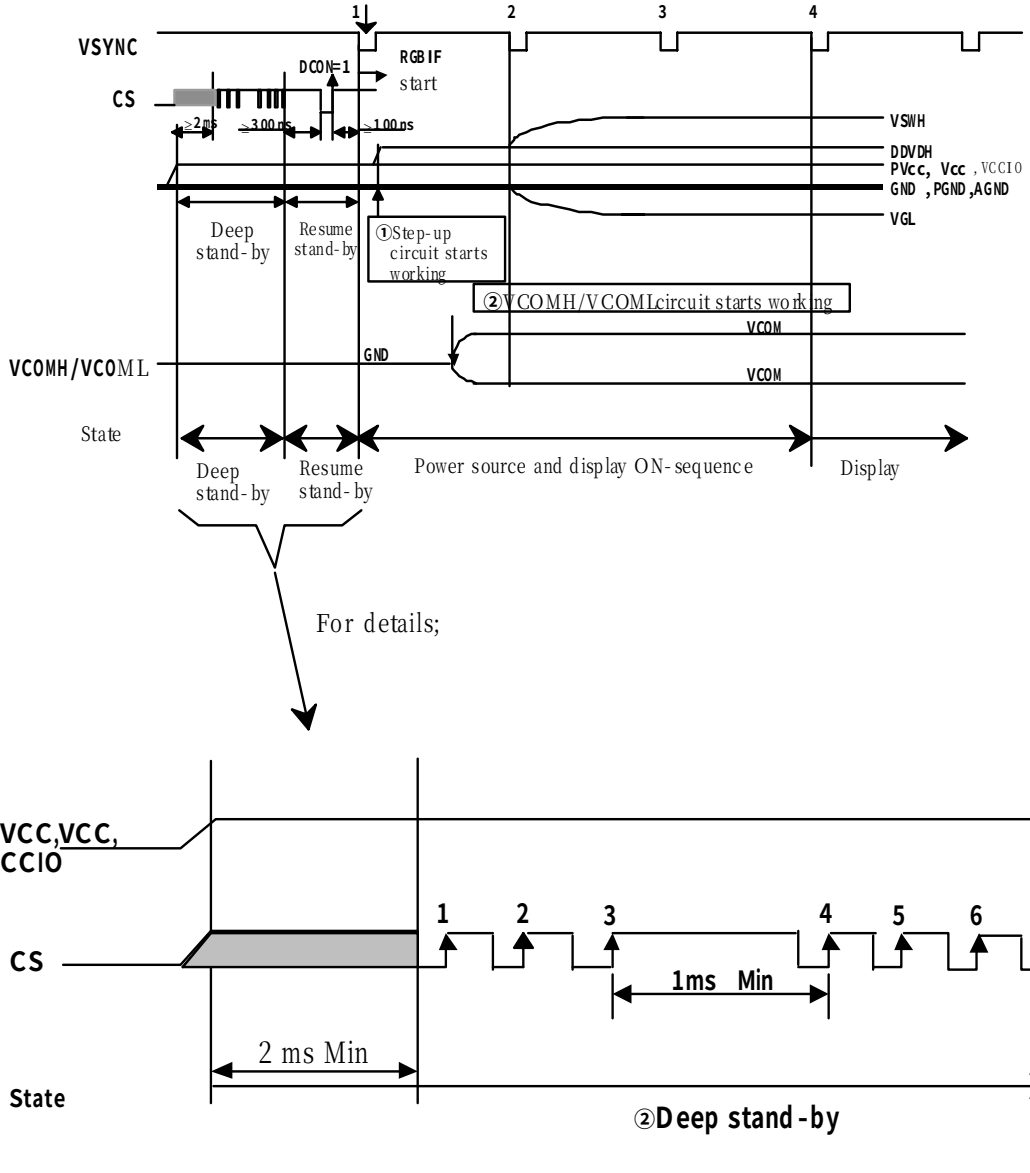
The following shows the state chart of power supply (ON and OFF).
There are two stand-by states between ON and OFF.
Timing charts for each transition are given in (2) and following items.



(2) On sequence（(A) -> (B) -> (C)）

When DCON=0 turns DCON=1, the auto-sequence shown below is available.

Display starts at the fourth of VSYNC after DCON=1 is made.



(1)To cancel the deep stand-by and make resume stand-by available, seven lows of CS are necessary.

(2)Keep 2 ms or more after VCC reaches specified voltage till the first CS rise edge.
CS can be either high or low, but no rise edge must stay in this period.

(3)The width of high/low CS pulse must be 300 ns or more.

(4)Keep 1 ms or more between the third and the fourth of CS rise edge.

(5)At the seventh CS rise edge, deep stand-by is canceled and then resume stand-by is available.

(6)When DCON=0, it is in resume stand-by mode. VSYNC, HSYNC, DIN and DCLK cannot be accepted.

(7)When DCON=1, resume stand-by is canceled. VSYNC, HSYNC, DIN and DCLK can be accepted.

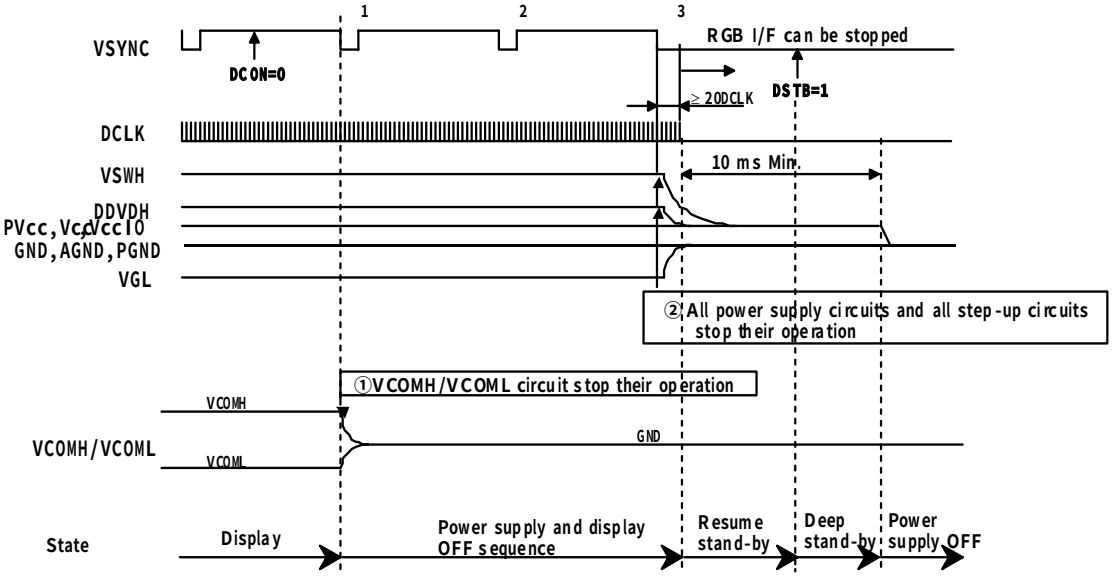
(8)Data are loaded from the fuse to the register by inputting the second HSYNC after the first VSYNC input while DCON=1.

(3) Resume Stand-by OFF Sequence（(D) -> (E) -> (F)）

When DCON=1 turns DCON=0, the OFF-sequence shown below is available. It is the resume stand-by mode. The operation of the internal circuit stops at the third pulse VSYNC and the 20th pulse of DCLK after DCON=0 is set.

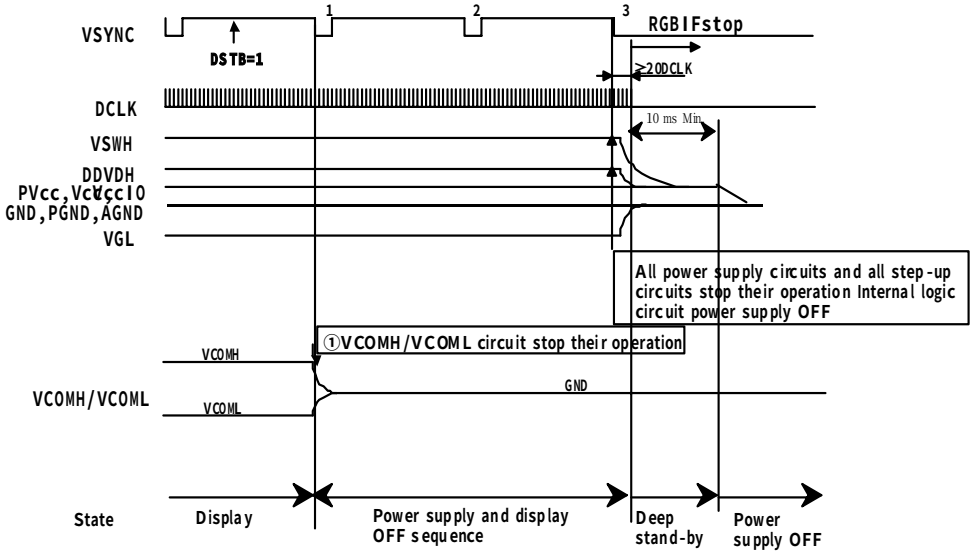
As the internal logic circuit is on, register can be accepted and register data can be held as well.

When DSTB=0 turns DSTB=1 during the resume stand-by mode, deep stand-by mode is set. In this mode, the register cannot be accepted, nor the resister can be held.



(4)Deep Stand-by Incoming Sequence Timing [(G) -> (F)]

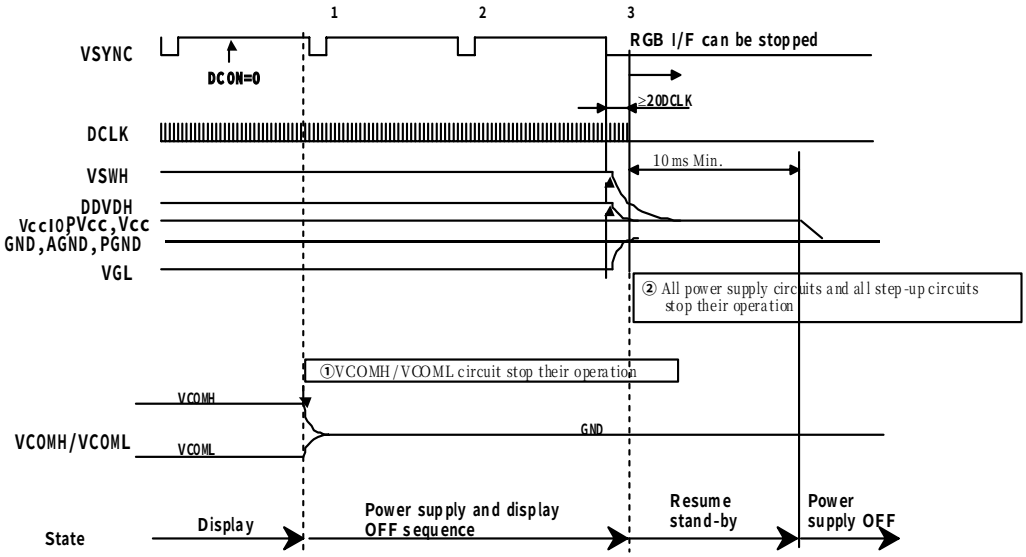
When DCON=0 turns DCON=1, the OFF-sequence shown below is available. It is the deep stand-by mode. The operation of the internal circuit of the LCD driver IC stops the third pulse of VSYNC and the 20th pulse of DCLK after DCON=1 is set. The internal logic circuit is completely off. In this state, the register cannot be accepted, nor the register data can be held. Please refer to (2), ON- sequence for recovery from the deep stand-by mode.



※ The period of 10 ms minimum after 20 pulses of DCLK is the time to release residual electricity charged in external capacitors.

(5) Resume Stand-by OFF-sequence [(D) -> (H)]

When DCON=1 turns DCON=0, the auto-sequence shown below is available.
The operation stops at the third pulse of VSYNC and the 20th pulse of DCLK after DCON=0 is set.
This is the resume stand-by mode. Register data holding and register acceptance are both available in this mode.
During resume stand-by, RGBIF can be accepted as internal data after DCON=1 is issued.



※ The period of 10 ms minimum after 20 pulses of DCLK is the time to release residual electricity charged in external capacitors.

8.7 INSTRUCTION SPECIFICATIONS

This LCD has 58 internal registers. The data writing to these internal registers is performed using serial interface. Upper seven bits of transmission data are the index code of a register, and lower eight bits are instruction data. D8 is a R/W bit.

8.7.1 Instructions and Initial Value

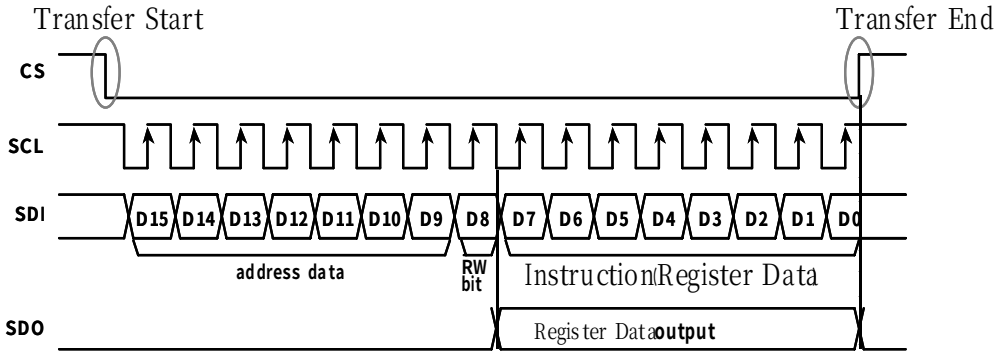
Instruction data is set as the following value at the time of power on.

Register Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
(Hexadecimal)	Register Address Code							RW(0:W/1:R)	Register Data							
00	0	0	0	0	0	0	0	0						1	0	0
01	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0
02	0	0	0	0	0	1	0	0		0	0	1	1	1	0	0
03	0	0	0	0	0	1	1	0					0	0	0	0
04	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1
05	0	0	0	0	1	0	1	0				1	0	0	1	0
06	0	0	0	0	1	1	0	0							0	0
09	0	0	0	1	0	0	1	0						0	0	0
0A	0	0	0	1	0	1	0	0		0	0	0	0	0	0	0
0B	0	0	0	1	0	1	1	0						0	0	0
10	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
11	0	0	1	0	0	0	1	0		1	0	0	0	0	0	0
12	0	0	1	0	0	1	0	0		1	0	0	0	0	0	0
13	0	0	1	0	0	1	1	0				1	0	0	0	0
14	0	0	1	0	1	0	0	0		1	0	0	0	0	0	0
15	0	0	1	0	1	0	1	0				1	0	0	0	0
16	0	0	1	0	1	1	0	0	0	0	1	0	0	0	0	0
17	0	0	1	0	1	1	1	0	0	1	0	0	0	0	0	0
18	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0
19	0	0	1	1	0	0	1	0	1	1	0	0	0	0	0	0
1A	0	0	1	1	0	1	0	0	0	0	1	0	0	0	0	0
1B	0	0	1	1	0	1	1	0	0	1	0	0	0	0	0	0
1C	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0
1D	0	0	1	1	1	0	1	0	1	1	0	0	0	0	0	0
1E	0	0	1	1	1	1	0	0	0	0	1	0	0	0	0	0
1F	0	0	1	1	1	1	1	0	0	1	0	0	0	0	0	0
20	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0
21	0	1	0	0	0	0	1	0	1	1	0	0	0	0	0	0
22	0	1	0	0	0	1	0	0	1	0	0	0	0	0	0	0
23	0	1	0	0	0	1	1	0	1	0	0	0	0	0	0	0
24	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0
25	0	1	0	0	1	0	1	0		1	0	0	0	0	0	0
26	0	1	0	0	1	1	0	0		1	0	0	0	0	0	0
27	0	1	0	0	1	1	1	0		1	0	0	0	0	0	0
2F	0	1	0	1	1	1	1	0		0	0	0	0	0	0	0
30	0	1	1	0	0	0	0	0					1	1	0	0
31	0	1	1	0	0	0	1	0	0	1	1	1	1	0	1	1
32	0	1	1	0	0	1	0	0	0	1	1	1	0	1	1	1
33	0	1	1	0	0	1	1	0			0	1	0	0	1	0
40	1	0	0	0	0	0	0	0		1	1	1		1	1	1
41	1	0	0	0	0	0	1	0				0	1	0	1	1
42	1	0	0	0	0	1	0	0		0	1	1	0	1	0	0
43	1	0	0	0	0	1	1	0	1	0	0	0	0	1	1	0
44	1	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0
45	1	0	0	0	1	0	1	0	0	0	1	1		0	1	1
46	1	0	0	0	1	1	0	0				0	0	0	0	1
47	1	0	0	0	1	1	1	0				0	0	1	0	1
48	1	0	0	1	0	0	0	0					0	0	1	0
49	1	0	0	1	0	0	1	0		1	0	0		1	1	1
4A	1	0	0	1	0	1	0	0				0	0	0	0	0
4B	1	0	0	1	0	1	1	0		0	0	1	0	0	1	0
4C	1	0	0	1	1	0	0	0	1	0	1	0	0	1	0	0
4D	1	0	0	1	1	0	1	0	0	0	1	0	0	1	1	0
4E	1	0	0	1	1	1	0	0	0	1	0	0		0	1	0
4F	1	0	0	1	1	1	1	0				0	0	1	0	1
50	1	0	1	0	0	0	0	0				0	0	1	0	1
51	1	0	1	0	0	0	1	0					0	0	1	1

: "0" or "1

8.7.2 SERIAL INTERFACE

Instructions are transmitted by CS, SCL, SDI and SDO.
Data transfer starts at the falling edge of CS, and ends at its rising edge.
When R/W bit (D8) is "0", it is in the writing mode and the D7 to D0 data of SDI are transmitted as register data.
The data are transmitted by 16-bit unit. The transmitted data format is in the order of MSB and then LSB.
The transmitted data is invalid if 16 bits or more SCL is not inputted in the low period of CS.
The inputted 16-bit unit data are effective from the falling edge of CS if 16 bits or more SCL is inputted.
When the register data are read out, intended address is written by SDI and then the first 8-bit of SDO from the falling edge of SCL is outputted as a register value with R/W bit (D8) set to "1".
SCL cycle time at reading out must be longer than the cycle time for writing.



8.7.3 INSTRUCTION VALUE

Address data	Register Data
R01h	20h
R02h	1Ch
R03h	00h
R04h	11h
R05h	12h
R06h	01h
R09h	00h
R0Ah	01h
R0Bh	00h
R16h	20h
R17h	40h
R18h	80h
R19h	C0h
R1Ah	20h
R1Bh	40h
R1Ch	80h
R1Dh	C0h
R1Eh	20h
R1Fh	40h

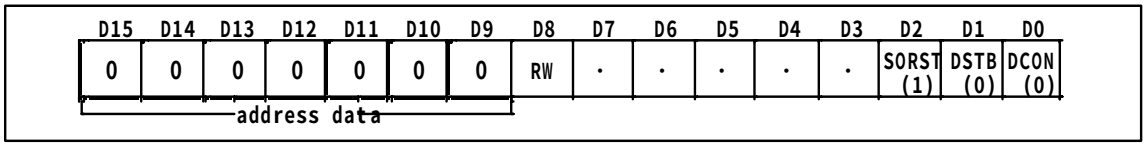
Address data	Register Data
R20h	80h
R21h	C0h
R22h	80h
R23h	80h
R24h	80h
R25h	40h
R26h	40h
R27h	40h
R30h	0Ah
R31h	8Ah
R32h	77h
R33h	04h
R40h	77h
R41h	06h
R42h	46h
R43h	96h
R44h	BBh
R45h	24h
R46h	02h
R47h	00h
R48h	04h

Address data	Register Data
R49h	63h
R4Ah	00h
R4Bh	14h
R4Ch	66h
R4Dh	45h
R4Eh	23h
R4Fh	04h
R50h	06h
R51h	00h
R00h	05h

8.7.4 INSTRUCTIONS

The description of each instruction is explained here. The code in parentheses following to the instruction is the default index after reset. The hyphen "-" shows it can be either "0" or "1".

(1) Display Control (R00h)

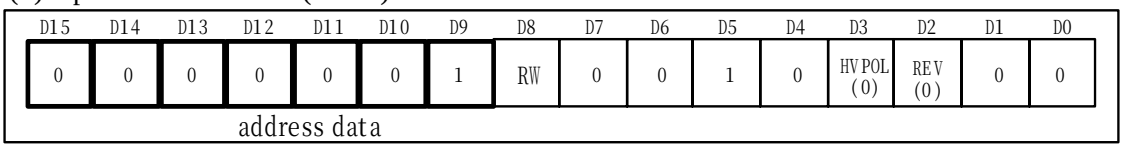


SORST:System reset. It resets the system and brings each instruction to default by setting SORST="0". Every operation is reset.

DSTB:Deep standby mode setting. By setting DSTB1="1", display becomes OFF.
After power sequence, the internal power is off and it goes to deep stand-by mode.
Inputting seven rising edges of SC makes it to recover from deep stand-by mode.
Refer to Item 8.6, Power Supply Sequence.

DCON:Power supply and display control bit.
At the 4th VSYNC after DCON="1", display is ON and displaying starts.
At the 3rd VSYNC after DCON="0", display is OFF and then power is OFF.
When Vcc is ON and DCON="0", it is in stand-by mode. VSYNC, HSYNC, DCLK and DIN7-0 are not accepted.

(2)Input Data Control (R01h)



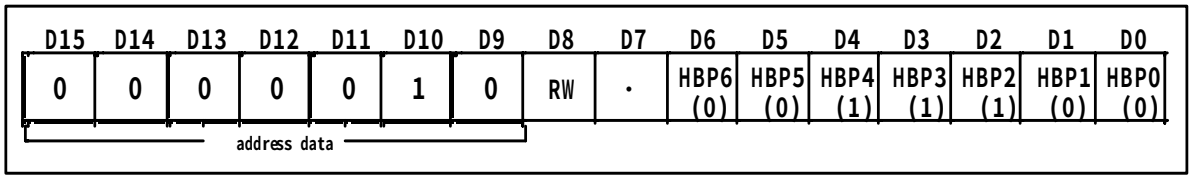
HVPOL: Switch for HSYNC and VSYNC.
When HSYCN/VSYNC is inputted with positive pulse, HVPOL="1" should be set.

REV:Switch of positive and negative for input data. Refer to the following table.

REV	Internal data polarity
0	As its polarity
1	Opposite polarity

(3) Horizontal Back Porch Setting (R02h)

This is to define horizontal back porch. Setting in the following table is available.
It does not depend on interface mode, output number mode and clock frequency mode.



n: Decimal number of HBP

HBP[6]	HBP[5]	HBP[4]	HBP[3]	HBP[2]	HBP[1]	HBP[0]	Horizontal back porch	Remarks
0	0	0	0	0	0	0	15	
0	0	0	0	0	0	1	21	
0	0	0	0	0	1	0	27	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	(Once every 6 pulses)
0	0	1	0	0	1	1	129	
0	0	1	0	1	0	0	135	
0	0	1	0	1	0	1	141	6n+15
0	0	1	0	1	1	0	144	
0	0	1	0	1	1	1	147	
0	0	1	1	0	0	0	150	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	(Once every 3 pulses)
0	0	1	1	1	0	0	162	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	3(n- 22)+144
0	1	1	0	1	0	0	234	
0	1	1	0	1	0	1	237	
0	1	1	0	1	1	0	240	
0	1	1	0	1	1	1	241	
0	1	1	1	0	0	0	244	
0	1	1	1	0	0	1	247	(Once every 3 pulses)
0	1	1	1	0	1	0	250	
0	1	1	1	0	1	1	253	3(n- 55)+241
0	1	1	1	1	0	0	255	
0	1	1	1	1	0	1	258	
0	1	1	1	1	1	0	261	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	(Once every 3 pulses)
1	0	0	0	1	0	1	282	
1	0	0	0	1	1	0	285	3(n- 60)+255
1	0	0	0	1	1	1	288	
1	0	0	1	0	0	0	294	
1	0	0	1	0	0	1	300	
1	0	0	1	0	1	0	306	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	(Once every 6 pulses)
1	1	0	0	1	1	0	474	
1	1	0	0	1	1	1	480	6(n- 72)+294
1	1	0	1	0	0	0	486	

(4) Vertical Back Porch Setting (R03h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	RW	·	·	·	·	0	0	VBP[1] 0	VBP[0] (0)

address data

VBP [1:0] : This is to define vertical back porch.

VBP1	VBP0	Backporch Setting(RGB) (Hsync)
0	0	9
0	1	10
1	0	11
1	1	12

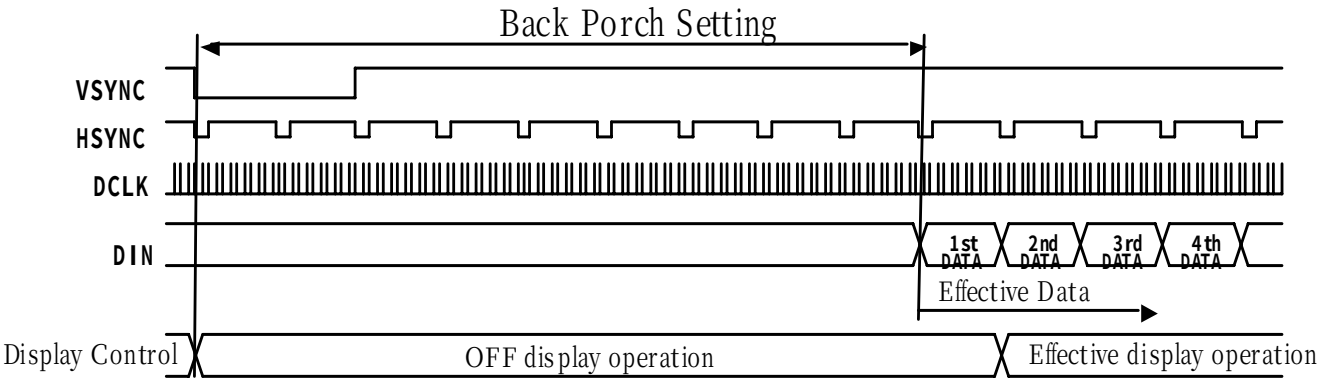


Figure ertical Back Porch Setting Position