HITACHI

Hitachi Displays, Ltd.

Date; November 28, 2008

TECHNICAL DATA

TX06D105VM0AAA

CONTENTS

RECORD OF REVISIONS

Date	Sheet No.	Summary

3. GENERAL SPECIFICATIONS

(1)	Product Name	TX06D105VM0AAA
(2)	Module Dimensions	40.0 (W) mm × 57.0 (H) mm × 1.5 (t) mm (Excluding FPC)
(3)	Active Area Dimensions	33.84 (W) mm × 45.12 (H) mm
(4)	Pixel Pitch	0.141 (W) mm × 0.141 (H) mm
(5)	Resolution	240 × 3 (R, G, B) (W) × 320 (H) dots
(6)	Color Pixel Arrangement	RGB Vertical Stripe
(7)	Display Mode	Transmissive Type, Normally Black Mode, IPS
(8)	Number of Colors	65,536 Colors / 262,144 Colors (8-bit, 16-bit CPU-I/F)
(9)	Viewing Direction	-
(10)	Backlight	Light Emitting Diode (LED), Five LEDs connected in parallel Backlight current : 20mA/LED(typ)
(11)	Weight	6.1 g (typ)
(12)	Power Supply Voltage	Vcc=2.8 V (typ)
(13)	Interface I/O Power Supply Note (1)	$1.8V \leq I/OVcc \leq Vcc$ The same voltage as "H" level of a customer's interface signal must be supplied to I/OVcc.
(14)	LCD Driver IC	R61505U (Source, Gate and Power IC)
(15)	Interface	8-bit / 16-bit / CPU bus (80 CPU series)

Note (1) I/OVcc is reference voltage for adjusting I/O signal level of R61505U.
I/OVcc voltage must be determined according to a customer's system.

4. ABSOLUTE MAXIMUM RATINGS

4.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS OF LCD VSS=0 V

Item	Symbol	Min.	Max.	Unit	Note
Power Supply for Logic and Analog	Vcc	-0.3	4.6	V	(1), (2)
Power Supply for Interface	I/OVcc	-0.3	4.6	V	(1), (2)
Input Voltage	V_t	-0.3	I/OVcc+0.3	V	(1), (3)
LED Reverse Voltage	V_R	-	5	V	(1), (4)
LED Forward Current	I_{LED}	-	35	mA	(4), (5)
Static Electricity	-	-	±2	kV	(6)

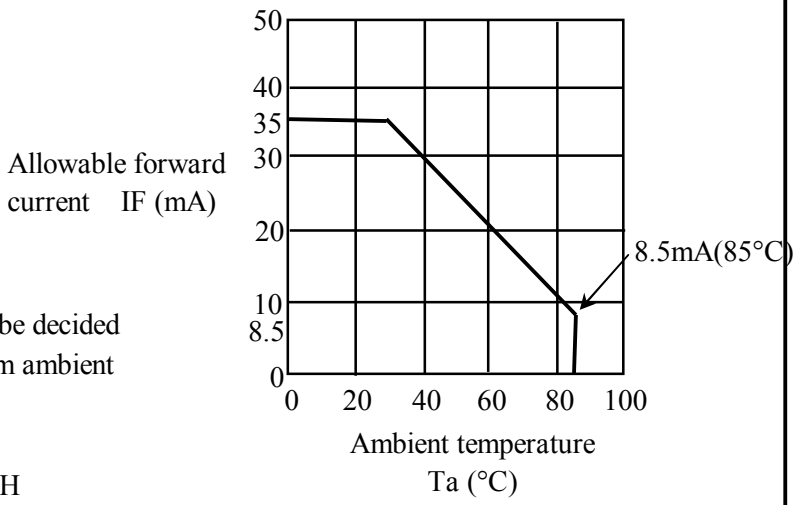
Notes (1) All voltage values are referred to GND.

(2) I/OVcc ≤ Vcc

(3) Applies to the RESET*, RD*, WR*, CS*, RS, IFMODE, VSYNC-IN and D15 to D0 pins.

(4) Ta=25°C, per LED

(5) Relationship between ambient temperature and allowable forward current



The operating current should be decided after considering the maximum ambient temperature of LEDs.

(6) 100 pF, 1.5 kΩ, 25°C, 70%RH
Static electricity discharge is to be given at the center of the active area.

4.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

Item	Operating		Storage		Comment
	Min.	Max.	Min.	Max.	
Ambient Temperature	-20°C	70°C	-30°C	80°C	Note (2)
Humidity	Note (1)		Note (1)		No condensation
Corrosive Gas	Not Acceptable		Not Acceptable		

Notes (1) Ta ≤ 40°C : 85%RH Max.
Ta > 40°C : Absolute humidity must be lower than the humidity of 85%RH at 40°C.
The polarizer's quality is not assured by the above values.

(2) Background color slightly changes depending on ambient temperature and viewing angle.

5. ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS OF LCD

Ta=25°C, VSS=0 V

	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage for Logic and Analog	Vcc	-	2.7	2.8	2.9	V	
Power Supply Voltage for Interface	I/OVcc	-	1.8	-	Vcc	V	
Input Voltage for Logic Circuits	Vi	"H" level	0.85 × I/OVcc	-	I/OVcc	V	(1)
		"L" level	-0.3	-	0.15 × I/OVcc		
Output Voltage for Logic Circuits	Vo	"H" level	0.75 × I/OVcc	-	-	V	(2)
		"L" level	-	-	0.2 × I/OVcc		
Input / Output Leak current	I_{LI}	-	-1.0	-	1.0	µA	
Power Supply Current	Icc	All White	-	2.8	5.1	mA	(3)(6)
		8-Color Partial	-	1.1	2.0	mA	(4)(6)
		Deep Standby	-	1	15	µA	(5)(6)
LED Forward Voltage	V_{LED}	-	2.8	3.2	3.5	V	(7)
LED Forward Current	I_{LED}	-	-	20	Note (8)	mA/LED	(7)
LED Reverse Current	I_R	-	-	-	50	µA	(7)

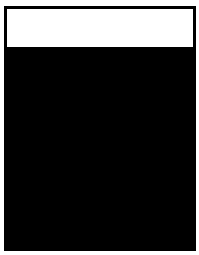
Notes (1) Applies to the RESET, RD*, WR*, CS*, RS, IFMODE, VSYNC-IN and D15 to D0 pins.

(2) Applies to the VSYNC-OUT and D15 to D0 pins.

(3) Vcc=2.8 V, I/OVcc=1.8 V, f_{FLM}=85 Hz, Frame inversion mode.

(4) Partial Pattern

Vcc=2.8 V
I/OVcc=1.8 V
f_{FLM}=60 Hz
40 Lines: White
280 Lines: Black
8-color mode



40 Lines: White

280 Lines: Black

(5) Vcc=2.8 V, I/OVcc=1.8 V, fFLM=85 Hz, Deep standby mode

(6) Operation Mode: Refer to Item 8.4.1

(7) Shows the value per LED.

(8) Refer to Item 4.1

6. OPTICAL CHARACTERISTICS

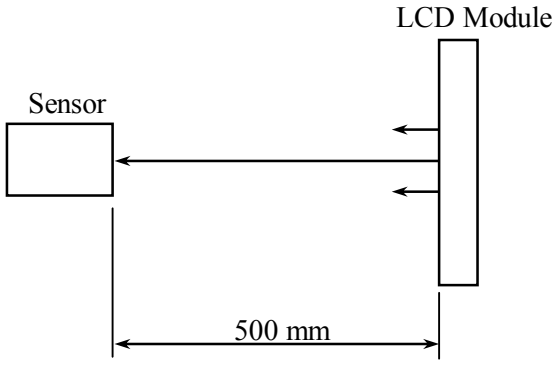
OPTICAL CHARACTERISTICS OF LCD (BACKLIGHT ON)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Brightness		B	φ=0°, θ=0°	-	400	-	cd/m²	(1), (2)
Contrast ratio		CR	φ=0°, θ=0°	-	400	-	-	(1), (6)
Viewing angle		φ1+φ2	θ=0°, CR≥10	-	170	-	deg	(4), (6), (7)
			θ=90°, CR≥10	-	170	-		
Brightness uniformity		-	φ=0°, θ=0°	-	80	-	%	(2), (3), (5)
Response time		tr + tf	φ=0°, θ=0° Ta=25°C	-	40	-	ms	(8)
Color tone (Primary Color)	Red	x	φ=0°, θ=0° Maximum Gradient	-	-	-	-	(1)
		y		-	-	-		
	Green	x		-	-	-		
		y		-	-	-		
	Blue	x		-	-	-		
		y		-	-	-		
	White	x		-	(0.32)	-		
		y		-	(0.33)	-		
NTSC Ratio		-		-	70	-	%	-

Common conditions for measurement

Measurement environment : Dark room
Ambient temperature : Ta=25°C
Sequence : Refer to Item 8.4.2, Sequence.
Power supply voltage : Vcc=2.8 V, I/OVcc=1.8 V
Backlight current : ILED = 20 mA/1LED

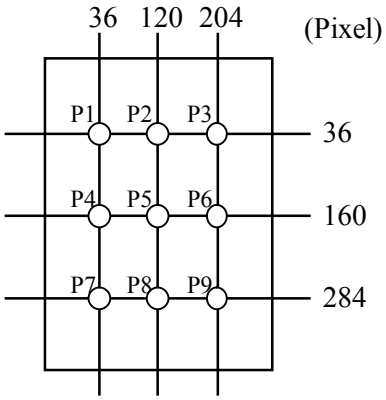
Notes (1) Definition of Brightness "B"



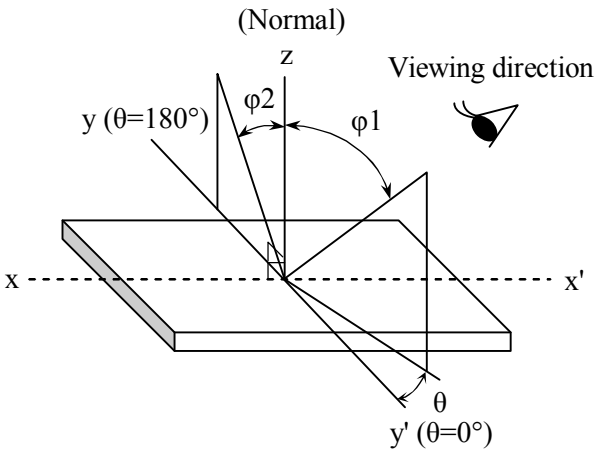
Sensor : TOPCON / BM-5A or equivalent
Measurement point : Center of LCD's active area

(2) Display image for measurement : White

Notes (3) Measurement point



(4) Definition of θ and φ



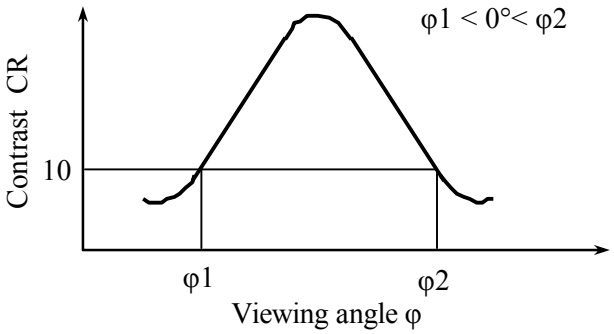
(5) Definition of brightness uniformity

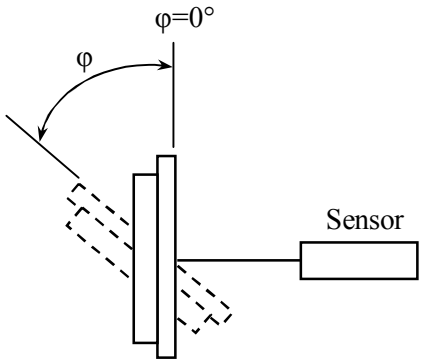
$$\text{Brightness uniformity} = \frac{\text{Minimum brightness}}{\text{Maximum brightness}} \times 100\ (\%)$$

(6) Definition of Contrast "CR"

$$\text{CR} \quad \frac{\text{Brightness when displaying White raster}}{\text{Brightness when displaying Black raster}}$$

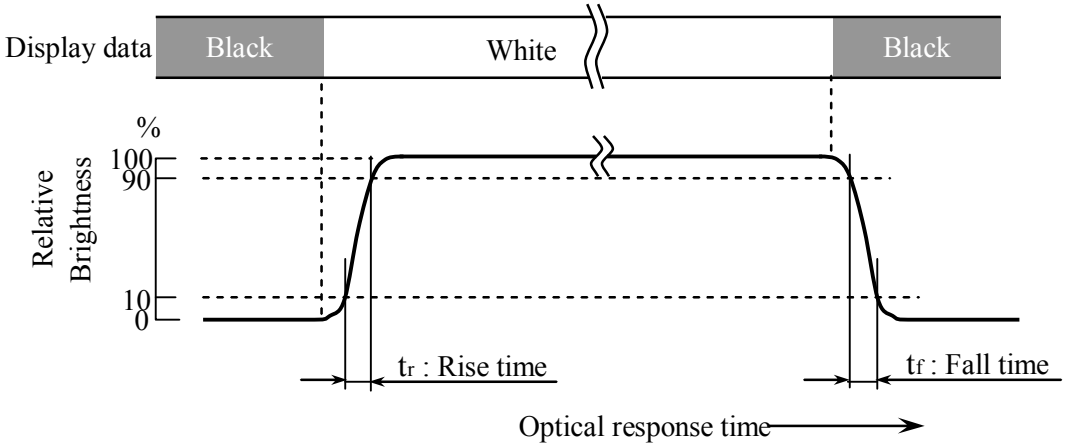
(7) Definition of viewing angle φ1and φ2



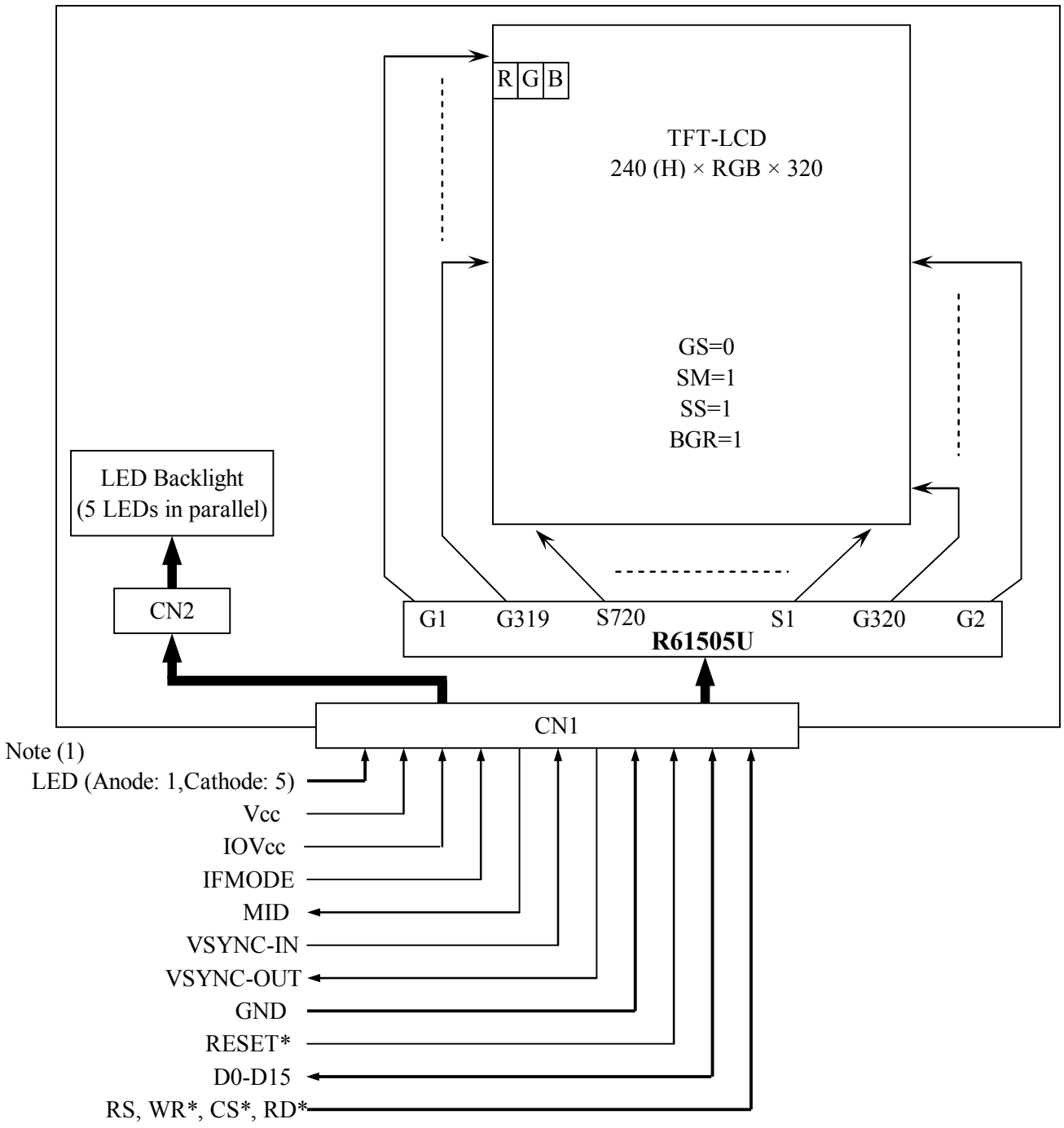


Sensor : TOPCON / BM-5A or equivalent

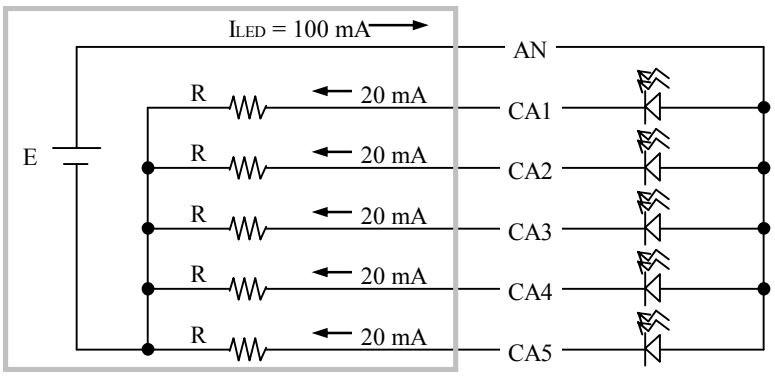
(8) Definition of optical response time



7. BLOCK DIAGRAM



Note (1) Please connect the resistor (R = 200Ω) for current control between LED (cathode) and GND in the customer's system.



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8. INTERFACE

8.1 INTERNAL PIN CONNECTION

Pin No.	Signal	I/O	Function	Driver's Signal Name
1	Vcc (2.8V)	-	Power Supply for Logic and Analog	VCC
2	I/OVcc (1.8V)	-	Power Supply for Interface	IOVCC
3	Maker ID (Low)	O	Maker ID (Low : Ground level)	-
4	VSYNC-IN Note(1)	I	Frame Synchronizing Signal	VSYNC
5	D0	I/O	Data Bus (Instruction & Display Data)	DB1
6	D1	I/O	Data Bus (Instruction & Display Data)	DB2
7	D2	I/O	Data Bus (Instruction & Display Data)	DB3
8	D3	I/O	Data Bus (Instruction & Display Data)	DB4
9	D4	I/O	Data Bus (Instruction & Display Data)	DB5
10	D5	I/O	Data Bus (Instruction & Display Data)	DB6
11	D6	I/O	Data Bus (Instruction & Display Data)	DB7
12	D7	I/O	Data Bus (Instruction & Display Data)	DB8
13	D8	I/O	Data Bus (Instruction & Display Data)	DB10
14	D9	I/O	Data Bus (Instruction & Display Data)	DB11
15	D10	I/O	Data Bus (Instruction & Display Data)	DB12
16	D11	I/O	Data Bus (Instruction & Display Data)	DB13
17	D12	I/O	Data Bus (Instruction & Display Data)	DB14
18	D13	I/O	Data Bus (Instruction & Display Data)	DB15
19	D14	I/O	Data Bus (Instruction & Display Data)	DB16
20	D15	I/O	Data Bus (Instruction & Display Data)	DB17
21	GND	-	Ground	-
22	RESET*	I	Reset	RESET*
23	WR*	I	Write Strobe	WR*
24	RD*	I	Read Strobe	RD*
25	CS*	I	Chip Select	CS*
26	RS	I	Register Select	RS
27	IFMODE	I	Interface mode Select	IM0
28	GND	-	Ground	-
29	VSYNC-OUT	O	Frame Head Pulse Signal	FMARK
30	LED(CA5)	-	Ground for LED	-
31	LED(CA4)	-	Ground for LED	-
32	LED(CA3)	-	Ground for LED	-
33	LED(CA2)	-	Ground for LED	-
34	LED(CA1)	-	Ground for LED	-
35	LED(AN)	-	Power Supply for LED	-

Suitable Connector : KYOCERA ELCO 04-6293-035-001-829+

Note (1) When not using VSYNC-IN (pin No.4), connect it to GND.

8.2 CPU INTERFACE MODE SETTING

8.2.1 CPU Interface Mode Selection

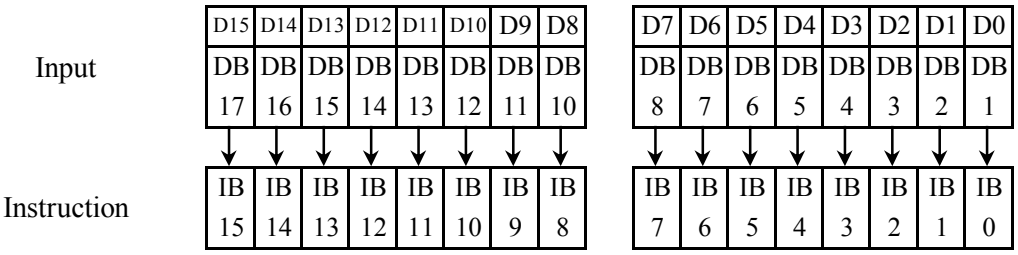
Mode Select IFMODE	System Interface	DB Pin	RAM Write Data	Color	Note
0	16-bit Interface	D15-D0	Single transfer (16 bits)	65k	
			2 transfers (1st: 2 bits, 2nd: 16 bits)	262k	
			2 transfers (1st: 16 bits, 2nd: 2 bits)	262k	
1	8-bit Interface	D15-D8	2 transfers (1st: 8 bits, 2nd: 8 bits)	65k	(1)
			3 transfers (1st: 2 bits, 2nd: 8 bits, 3rd: 8 bits)	262k	(1)
			3 transfers (1st: 6 bits, 2nd: 6 bits, 3rd: 6 bits)	262k	(1)

Note (1) Unused data bus pins are to be set at "GND" or "IOVcc".

8.2.2 Data Format of CPU Interface

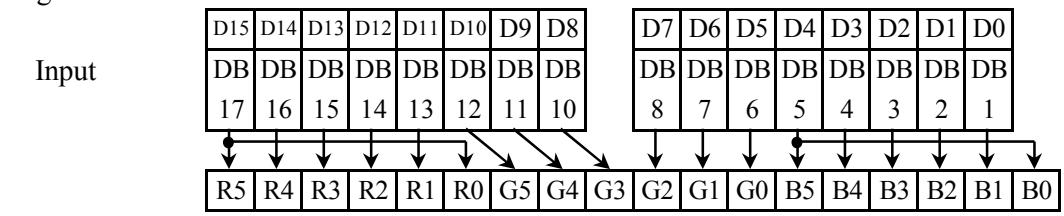
<16-bit Interface mode>

Instruction data format

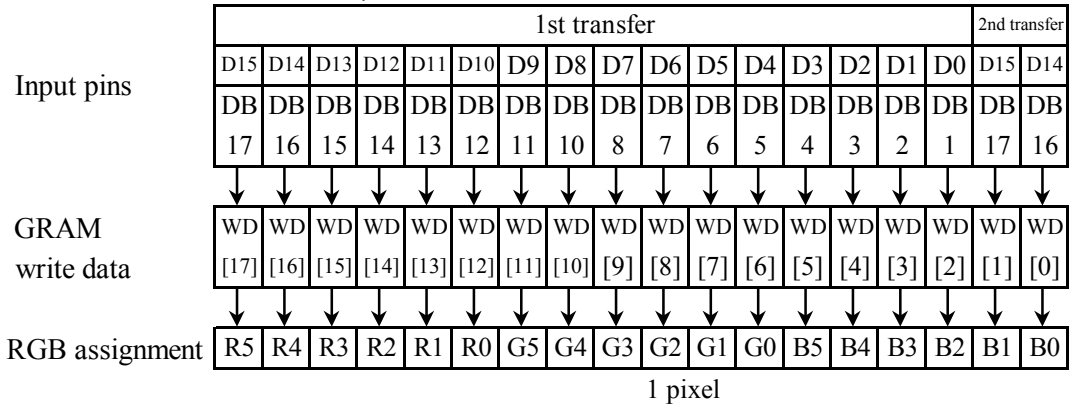


RAM data write data fotmat

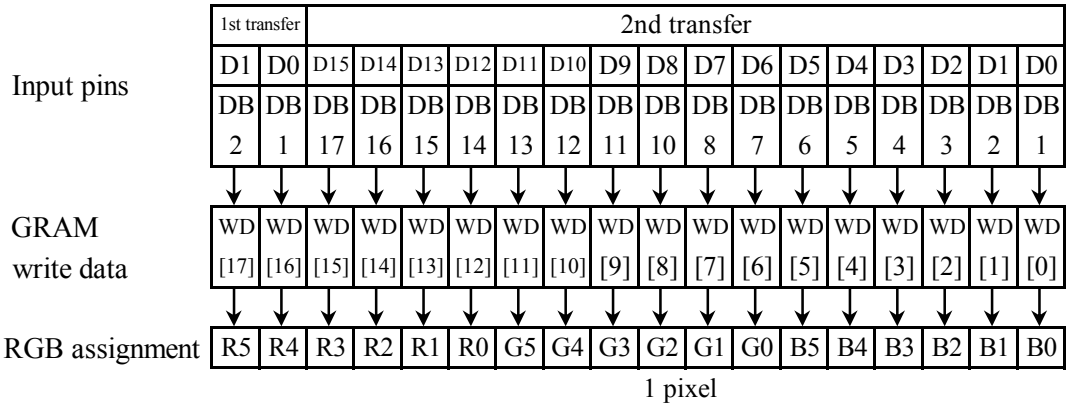
Single transfer mode : TRIREG=0



2 transfers mode : TRIREG=1, DFM=0

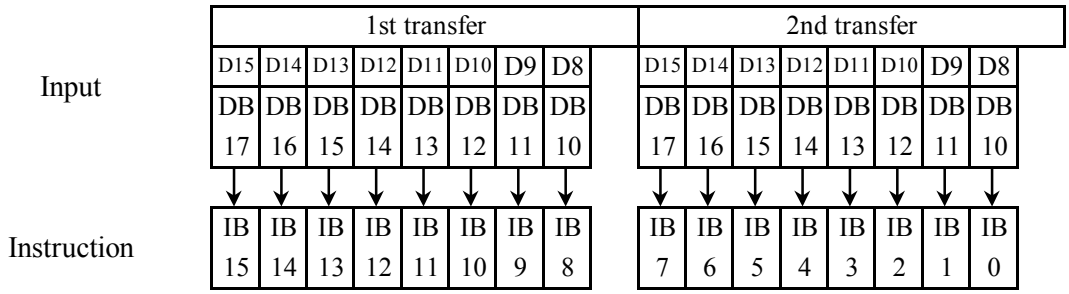


2 transfers mode : TRIREG=1, DFM=1



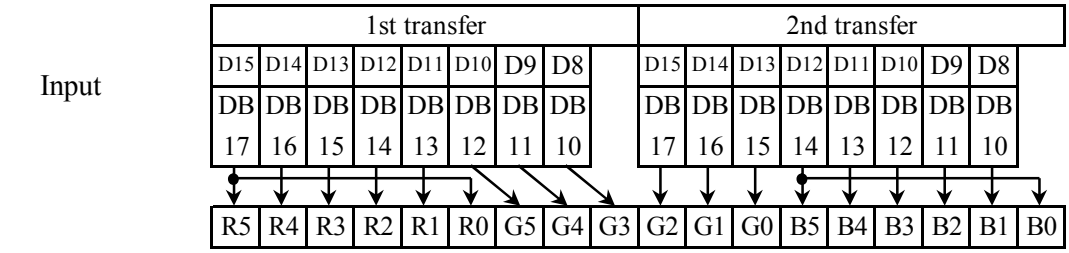
<8-bit Interface mode>

Instruction data format

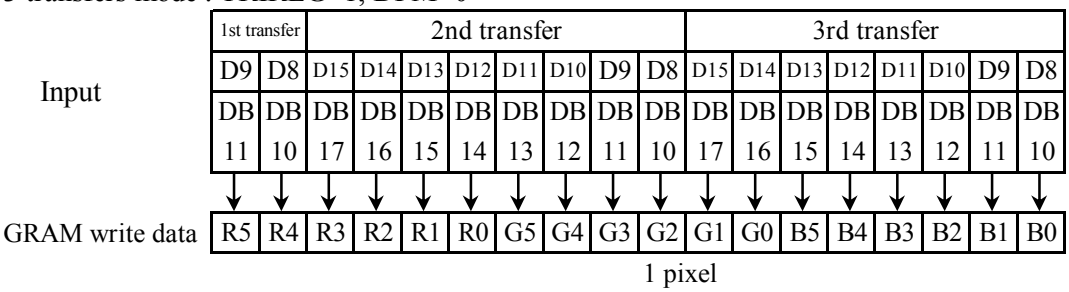


RAM data write data fotmat

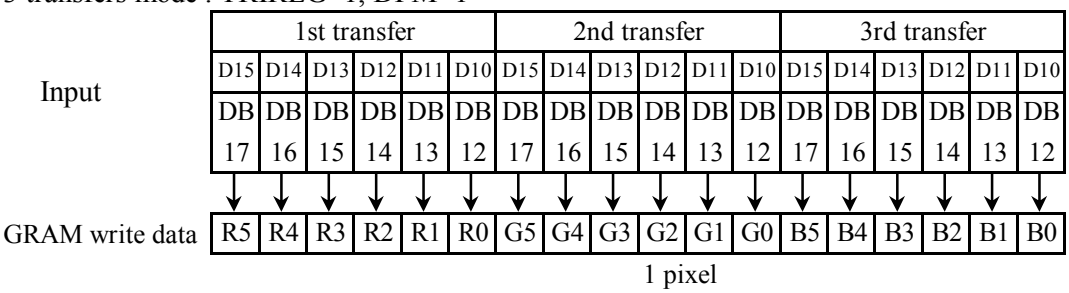
2 transfers mode : TRIREG=0



3 transfers mode : TRIREG=1, DFM=0



3 transfers mode : TRIREG=1, DFM=1



8.3 INTERFACE TIMING

8.3.1 80-System Bus Interface Timing Characteristics

<<16-/18-bits, Normal write mode (HWM=0), IOVcc=1.8V to Vcc>>

Vcc=2.8 V

Item		Symbol	Unit	Min.	Typ.	Max.
Bus cycle time	Write	t_{CYCW}	ns	132	-	-
	Read	t_{CYCR}	ns	473	-	-
Write low-level pulse width		PWLW	ns	48	-	-
Read low-level pulse width		PWLR	ns	179	-	-
Write high-level pulse width		PWHW	ns	74	-	-
Read high-level pulse width		PWHR	ns	263	-	-
Write/Read rise/fall time		t_{WRr}, t_{WRf}	ns	-	-	23
Setup time	Write (RS to CS*, WR*)	t_{AS}	ns	0	-	-
	Read (RS to CS*, RD*)		ns	11	-	-
Address hold time		t_{AH}	ns	2	-	-
Write data setup time		t_{DSW}	ns	27	-	-
Write data hold time		t_H	ns	11	-	-
Read data delay time		t_{DDR}	ns	-	-	142
Read data hold time		t_{DHR}	ns	5	-	-

Timing Diagram : Fig.1

<<16-/18-bits, High-speed write mode (HWM=1), IOVcc=1.8V to Vcc>>

Vcc=2.8 V

Item		Symbol	Unit	Min.	Typ.	Max.
Bus cycle time	Write	t_{CYCW}	ns	79	-	-
	Read	t_{CYCR}	ns	473	-	-
Write low-level pulse width		PWLW	ns	42	-	-
Read low-level pulse width		PWLR	ns	179	-	-
Write high-level pulse width		PWHW	ns	27	-	-
Read high-level pulse width		PWHR	ns	263	-	-
Write/read rise/fall time		t_{WRr}, t_{WRf}	ns	-	-	23
Setup time	Write (RS to CS*, WR*)	t_{AS}	ns	0	-	-
	Read (RS to CS*, RD*)		ns	11	-	-
Address hold time		t_{AH}	ns	2	-	-
Write data setup time		t_{DSW}	ns	27	-	-
Write data hold time		t_H	ns	11	-	-
Read data delay time		t_{DDR}	ns	-	-	142
Read data hold time		t_{DHR}	ns	5	-	-

Timing Diagram : Fig.1

<<8-bits, Normal write mode (HWM=0) / High-speed write mode (HWM=1), IOVcc=1.8V to Vcc>>

Vcc=2.8 V

Item		Symbol	Unit	Min.	Typ.	Max.
Bus cycle time	Write	t_{CYCW}	ns	74	-	-
	Read	t_{CYCR}	ns	473	-	-
Write low-level pulse width		PWLW	ns	32	-	-
Read low-level pulse width		PWLR	ns	179	-	-
Write high-level pulse width		PWHW	ns	27	-	-
Read high-level pulse width		PWHR	ns	263	-	-
Write/Read rise/fall time		t_{WRr}, t_{WRf}	ns	-	-	23
Setup time	Write (RS to CS*, WR*)	t_{AS}	ns	0	-	-
	Read (RS to CS*, RD*)	t_{AS}	ns	11	-	-
Address hold time		t_{AH}	ns	2	-	-
Write data setup time		t_{DSW}	ns	27	-	-
Write data hold time		t_{H}	ns	11	-	-
Read data delay time		t_{DDR}	ns	-	-	142
Read data hold time		t_{DHR}	ns	5	-	-

Timing Diagram : Fig.1

8.3.2 Reset Timing Characteristics

<<IOVcc=1.8V to Vcc>>

Vcc=2.8 V

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	t_{RES}	ms	1	-	-
Reset rise time	t_{rRES}	µs	-	-	9

Timing Diagram : Fig.2

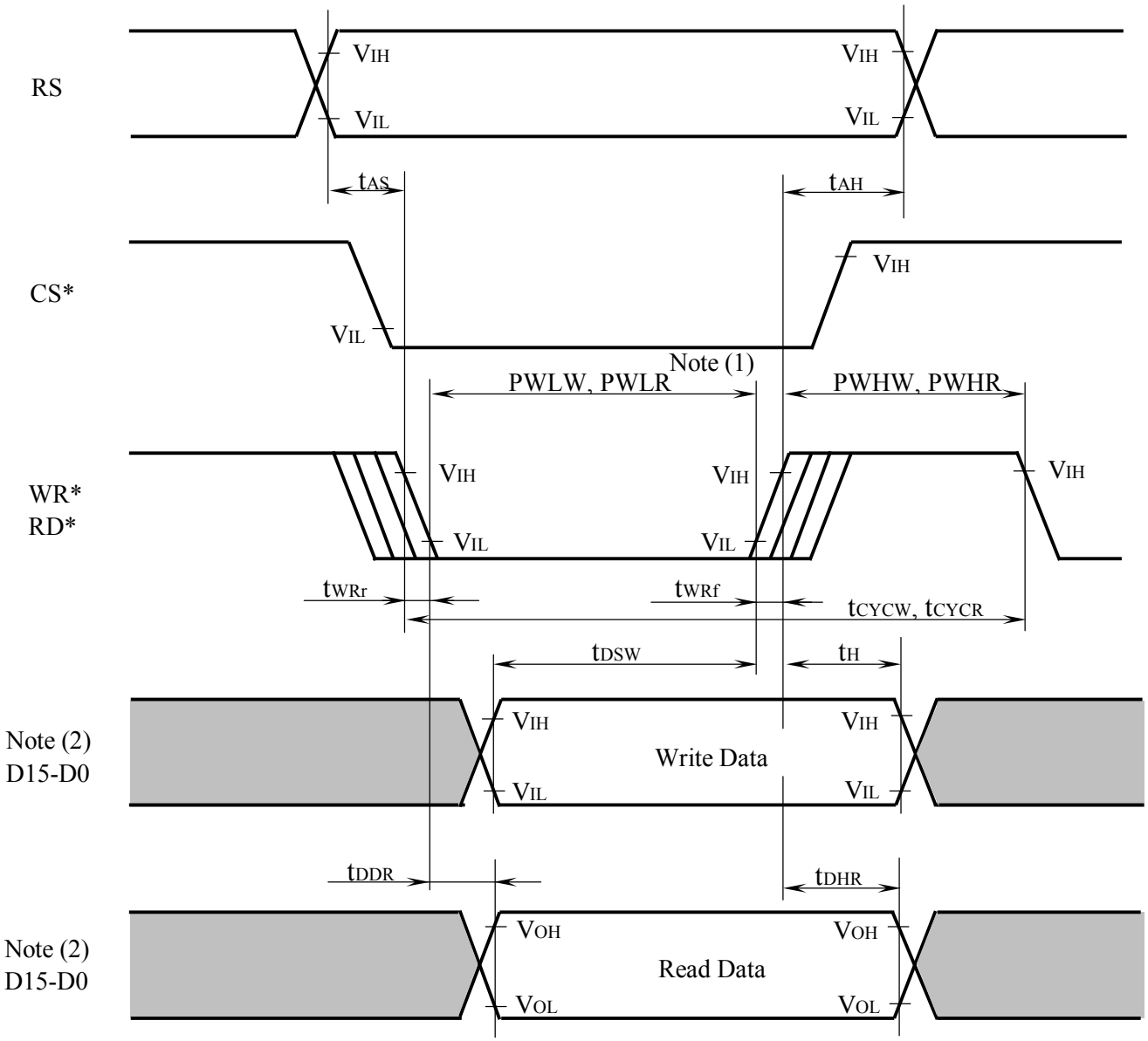


Fig.1 Bus Timing

Notes (1) PWLW and PWLR are defined by the overlapped period when CS* is low and WR* or RD* is low as well.

(2) Fix unused DB pins to either IOVcc or GND level.

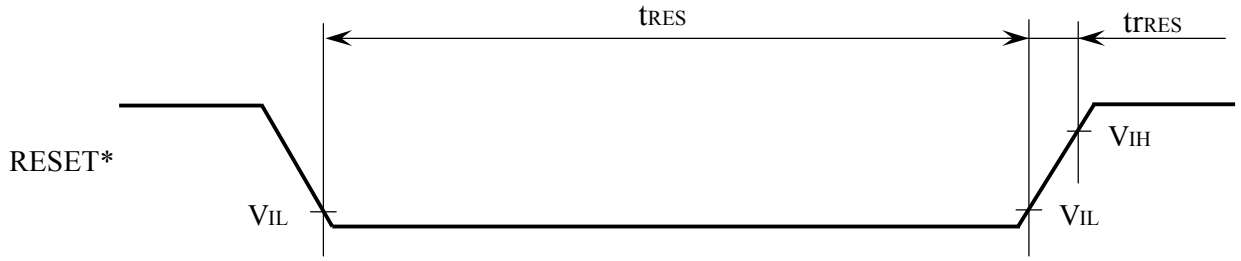
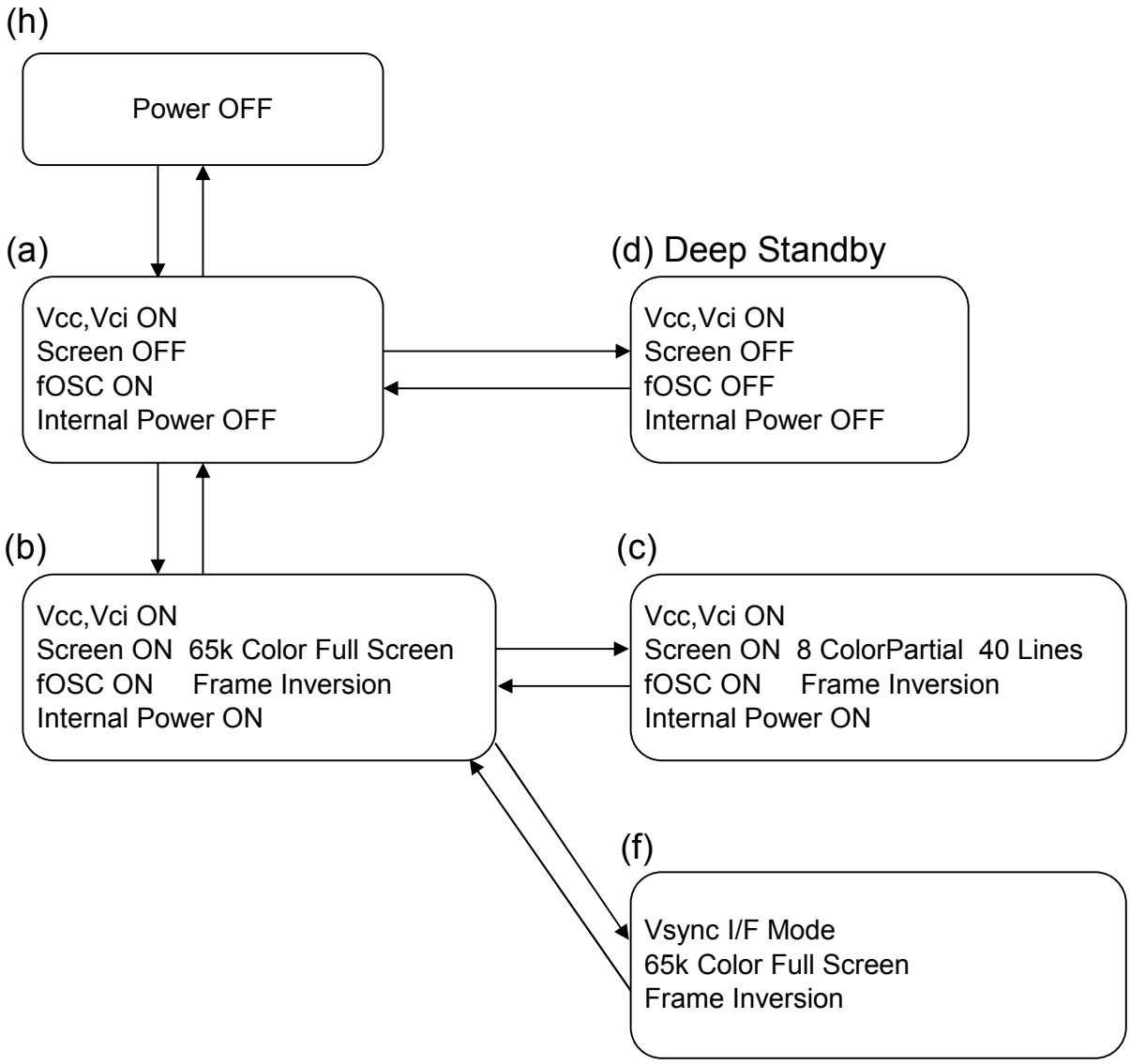
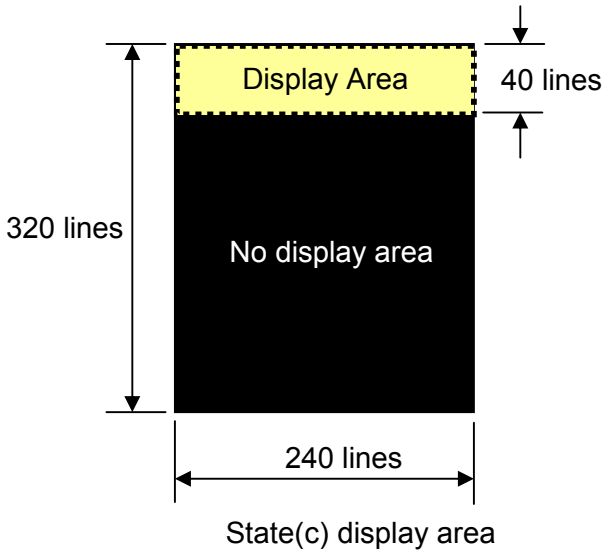


Fig.2 Reset Timing

8.4 REGISTER SETTING

8.4.1 State Transition Diagram of Operation Mode





State(c) display area

8.4.2 Sequence

State (h) → (a)

1	Power ON	Vcc ON	
2		ioVcc ON	
3		Vci ON	
4		reset* = "L"	
5	Reset	wait	1 ms min
6		reset* = "H"	
7		wait	2 ms min
8	Transfer synchronization	RS=0,DB=0x0000	
9		RS=0,DB=0x0000	
10		RS=0,DB=0x0000	
11		RS=0,DB=0x0000	

State (a) → (h)

1	Power OFF	Vci OFF	
2		ioVcc OFF	
3		Vcc OFF	

State (b) → (a)

1	Screen OFF	R07h	0x0072
2		wait	2 frame min
3		R07h	0x0001
4		wait	8 line min
5		R07h	0x0000
6	AMP OFF	R09h	0x0000
7		R10h	0x0080
8		R11h	0x0660
9		R12h	0x0000
10		wait	30 ms min
11		R10h	0x0000

State (a) → (d)

1	Deep Standby	R10h	0x0004

State (d) → (a)

DSTB Mode Cancellation(1)	Index Write(Data=8'h00)		Sequential control
DSTB Mode Cancellation(2)	Index Write(Data=8'h00)		
	wait	1ms min	
DSTB Mode Cancellation(3)	Index Write(Data=8'h00)		*1
DSTB Mode Cancellation(4)	Index Write(Data=8'h00)		
DSTB Mode Cancellation(5)	Index Write(Data=8'h00)		
DSTB Mode Cancellation(6)	Index Write(Data=8'hF0)		
Transfer synchronization	Index Write(Data=8'h00)		
	Index Write(Data=8'h00)		
	Index Write(Data=8'h00)		
	Index Write(Data=8'h00)		
	wait	50ms min	

State (b) → (f)

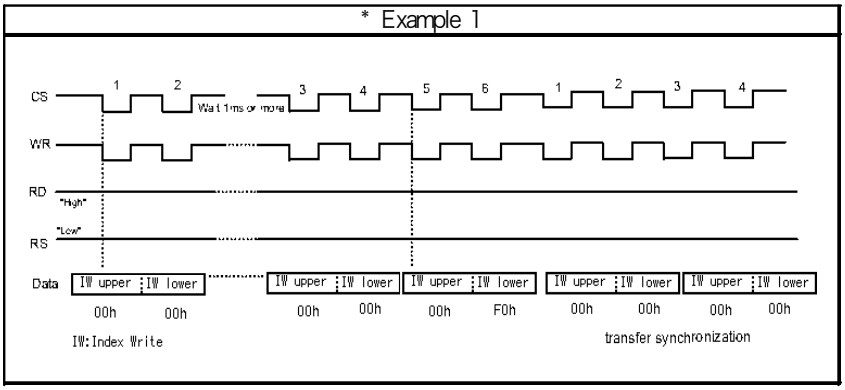
1		Vsync input ON		
2	Frame cycle control	R90h	0x0012	
3	Vsync I/F	R0Ch	0x0020	
4	GRAM write	R22h	-	
5		wait	1frame min	
6		Display data write		

fFLM:85Hz max

State (f) → (b)

1	CPUI/F	R0Ch	0x0000	
2		wait	1frame min	
3		Vsync input OFF		
4	Frame cycle control	R90h	0x0015	
5	GRAM address	R20h	0x0000	
6		R21h	0x0000	
7	GRAM write	R22h	-	
8		Display data write		Image size 240x320
9	Image refresh	R20h	0x0000	
10		R21h	0x0000	
11		R22h	-	
12		Display data write		Image size 240x320

* Example 1



State (a) → (b)

1		RA4h	0x0001	
2		wait	1ms min	
3	Power Screen control	R07h	0x0021	
4		wait	10 ms min	
5		R17h	0x0001	
6		wait	10 ms min	
7	Power start 1	R19h	0x0000	
8		R10h	0x17B0	
9		R11h	0x0016	
10		R12h	0x019C	
11		R13h	0x1100	
12		R14h	0x8000	
13		wait	10 ms min	
14	Power start 2	R12h	0x01BC	
15		wait	120 ms min	
16	Driver output control	R01h	0x0500	
17	LCD driving wave control	R02h	0x0400	
18	Entry mode	R03h	0x1230	
19	Display control 2	R08h	0x0808	(FP=8, BP=8)
20	ISC control	R09h	0x0000	
21	Display control 4	R0Ah	0x0008	
22	External display interface control 1	R0Ch	0x0000	
23	Frame marker control	R0Dh	0x0000	
24	Gamma settig	R30h	0x0606	
25		R31h	0x0002	
26		R32h	0x0200	
27		R33h	0x0201	
28		R34h	0x0001	
29		R35h	0x0205	
30		R36h	0x0717	
31		R37h	0x0606	
32		R38h	0x0002	
33		R39h	0x0200	
34		R3Ah	0x0201	
35		R3Bh	0x0001	
36		R3Ch	0x0205	
37		R3Dh	0x0818	
38	Horizontal RAM Address S	R50h	0x0000	
39	Horizontal RAM Address E	R51h	0x00EF	
40	Vertical RAM Address S	R52h	0x0000	
41	Vertical RAM Address E	R53h	0x013F	
42		R60h	0x2700	
43		R61h	0x0000	
44		R6Ah	0x0000	
45	Frame Frequency control	R90h	0x0015	fFLM85Hz
46		R92h	0x0000	
47		R93h	0x0001	
48	GRAM address set	R20h	0x0000	
49		R21h	0x0000	
50	GRAM write	R22h	-	
51		Display data write		Image size 240x320
52	Display ON	R07h	0x0021	
53		wait	8 line min	
54		R10h	0x17B0	
55		R11h	0x0017	
56		R07h	0x0061	
57		wait	2 frame min	
58		R07h	0x0173	
59	Image refresh	R20h	0x0000	
60		R21h	0x0000	
61		R22h	-	
62		Display data write		Image size 240x320

State (b) → (c)

1	Dsiplay OFF	R07h	0x0073	
2		wait	2 frame min	
3		R02h	0x0400	
4		R10h	0x17A0	
5	Horizontal RAM Address S	R50h	0x0000	
6	Horizontal RAM Address E	R51h	0x00EF	
7	Vertical RAM Address S	R52h	0x0000	
8	Vertical RAM Address E	R53h	0x0027	
9	Partial display position	R80h	0x0000	
10	Partial 1 RAM address S	R81h	0x0000	
11	Partial 2 RAM address E	R82h	0x0027	
12	ISC ON	R09h	0x0401	
13	Frame cycle control	R90h	0x001E	fFLM=60Hz
14		wait	2frame min	
15	GRAM Address	R20h	0x0000	
16		R21h	0x0000	
17	GRAM write	R22h	-	
18		Display data write		Image size 240x40
19	Display ON	R07h	0x107B	
20	Image refresh	R20h	0x0000	
21		R21h	0x0000	
22		R22h	-	
23		Display data write		Image size 240x40

State (c) → (b)

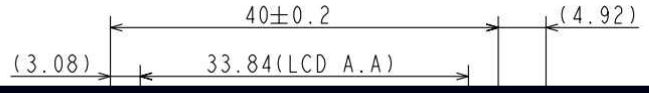
1	Dsiplay OFF	R07h	0x0073	
2		wait	2 frame min	
3	ISC OFF	R09h	0x0000	
4		R02h	0x0400	
5		R10h	0x17B0	
6	Horizontal RAM Address S	R50h	0x0000	
7	Horizontal RAM Address E	R51h	0x00EF	
8	Vertical RAM Address S	R52h	0x0000	
9	Vertical RAM Address E	R53h	0x013F	
10	Frame cycle control	R90h	0x0015	fFLM85Hz
11		wait	2frame min	
12	GRAM address	R20h	0x0000	
13		R21h	0x0000	
14	GRAM write	R22h	-	
15		Display data write		Image size 240x320
16	Diplay ON	R07h	0x0173	
17	Image refresh	R20h	0x0000	
18		R21h	0x0000	
19		R22h	-	
20		Display data write		Image size 240x320

Notes

Gamma and power control is Hitachi standard proposal.

We can optimize for this sequence for your evaluation.

9. Dimensional outline



IFMODE PIN	System Interface	Data Transfer	Display Colors
L	16bit	single	65k
		2transfers	262k
H	8bit	2transfers	65k
		3transfers	262k

No.	SIGNAL
1	Vcc(2.8V)
2	I/OVcc(1.8V)
3	Maker ID(Low)