

HITACHI

LIQUID CRYSTAL DISPLAY MODULE TECHNICAL DATA

TX07D24VM0AAA

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(NOTES)

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RECORD OF REVISIONS

| Date | Sheet No. | Summary |
|------|-----------|---------|
| | | |

3. GENERAL DATA

| | |
|---------------------------------|-------------------------------------------------------------------------------------|
| (1) Product Name | TX07D24VM0AAA |
| (2) Module Dimensions | 50.0 (W) mm x 70.0(H) mm x 2.15 (t) mm |
| (3) Active Area Dimensions | 43.2 (W) mm x 57.6 (H) mm |
| (4) Pixel Pitch | 0.18 (W) mm x 0.18 (H) mm |
| (5) Resolution | 240 x 3 (R, G, B) (W) x 320 (H) dots |
| (6) Color Pixel Arrangement | RGB Vertical Stripe |
| (7) Display Mode | Transmissive Type, Normally Black Mode, IPS |
| (8) Number of Colors | 65,536 Colors (8-bit, 16-bit CPU - I/F) 262,144 Colors (9-bit, 18-bit CPU - I/F) |
| (9) Viewing Direction | - |
| (10) Backlight | Light Emitting Diode (LED) Five LEDs connected in Series |
| (11) Weight | 14.5g |
| (12) Power Supply Voltage | V _{cc} = 2.8 V (typ) |
| (13) Interface I/O power supply | 1.75V ≤ V _{DDI/O} ≤ V _{cc} |
| (14) LCD Driver IC | S6D0154 |
| (15) Interface | 8-bit / 9-bit / 16-bit / 18-bit CPU bus (80 CPU series) |

4. ABSOLUTE MAXIMUM RATINGS

4. 1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS OF LCD

VSS = 0 V

| Item | Symbol | Min | Max | Unit | Note |
|-----------------------------------|------------------|------|------------|------|----------|
| Power Supply for Logic and Analog | Vcc | -0.3 | 4.6 | V | (1), (2) |
| Power Supply for Interface | VDDI/O | -0.3 | 4.6 | V | (1), (2) |
| Input Voltage | V _{IN} | -0.3 | VDDI/O+0.3 | V | (1), (3) |
| LED Reverse Voltage | VR | - | 5 | V | (1), (4) |
| LED Forward Current | I _{LED} | - | 35 | mA | (4), (5) |
| Static Electricity | - | - | ±2 | kV | (6) |

Notes (1) All voltage values are referred to GND.

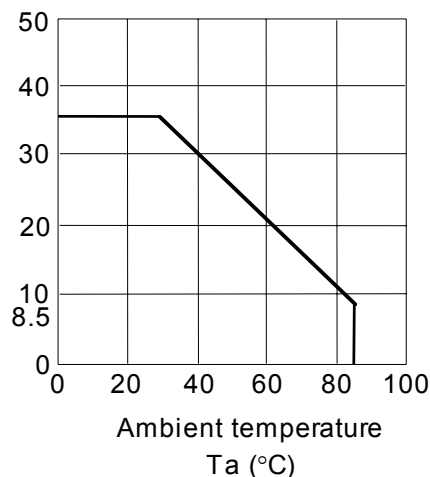
(2) $VDDI/O \leq Vcc$

(3) Applies to the RESET*, RD*, WR*, CS*, RS, VSYNC*, IM0, IM3 and DB17-0 pins.

(4) Ta = 25 deg C, per piece of LED.

(5) Relationship between ambient temperature and allowable forward current

Allowable forward current I_F (mA)



The operating current should be decided after considering the ambient maximum temperature of LEDs.

(6) 100 pF, 1.5 kohm, 25°C, 70% RH.

Static electricity discharge point is the center of LCD's surface.

4. 2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

| Item | Operating | | Storage | | Comment |
|---------------------|----------------|------|----------------|------|-----------------|
| | Min | Max | Min | Max | |
| Ambient Temperature | -20°C | 70°C | -30°C | 80°C | Note (2) |
| Humidity | Note (1) | | Note (1) | | No condensation |
| Corrosive Gas | Not Acceptable | | Not Acceptable | | |

Notes (1) Ta ≤ 40°C: 85% RH max.

Ta > 40°C: Absolute humidity must be lower than the humidity of 85%RH at 40°C.

The polarizer quality is not assured by the above values.

(2) Background color slightly changes depending on ambient temperature and viewing angle.

5. ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS OF LCD

Ta = 25°C, VSS = 0 V

| Item | Symbol | Condition | Min | Typ | Max | Unit | Note |
|-------------------------------------------|--------|-----------|--------------|-----|--------------|--------|------|
| Power Supply Voltage for Logic and Analog | Vcc | - | 2.72 | 2.8 | 2.88 | V | |
| Power Supply Voltage for Interface | VDDI/O | - | 1.75 | - | Vcc | | |
| Input Voltage for Logic Circuits | Vi | "H" level | 0.8 x VDDI/O | - | VDDI/O | V | (1) |
| | | "L" level | 0 | - | 0.2 x VDDI/O | | |
| Output Voltage for Logic Circuits | Vo | "H" level | 0.8 x VDDI/O | - | - | V | (2) |
| | | "L" level | - | - | 0.2 x I/OVcc | | |
| Input/Output Leak current | ILi | - | -1.0 | - | 1.0 | μA | |
| Power Supply Current | Icc | All White | - | 9.3 | 12.0 | mA | (3) |
| | | Partial | - | 6.0 | 8.0 | mA | (4) |
| | | Standby | - | 0.1 | 1.0 | μA | (5) |
| LED Forward Voltage | VLED | - | - | 3.2 | 3.5 | V | |
| LED Forward Current | I LED | - | - | 20 | Note (6) | mA/LED | |
| Frame Frequency | fFLM | - | - | 85 | - | Hz | |

Notes (1) Applies to the RESET*, RD*, WR*, CS*, RS, VSYNC*, IM0, IM3 and DB17-0 pins.

(2) Applies to the FLM and DB17-0 pins.

(3) Vcc = VDDI/O = 2.8 V, fFLM = 85 Hz

(4) Partial Pattern

40 Lines: White
280 Lines: Black
fFLM = 85 Hz
8-color mode



40 Lines: White

280 Lines: Black

(5) Vcc = VDDI/O = 2.8 V, Standby mode

(6) Refer to Item 4.1

6. OPTICAL CHARACTERISTICS

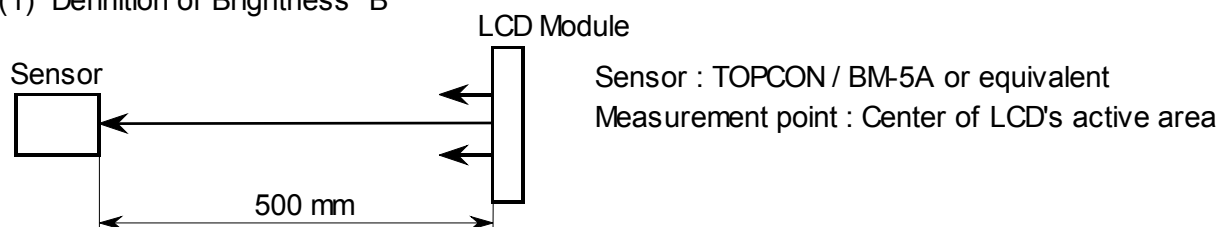
OPTICAL CHARACTERISTICS OF LCD (BACKLIGHT ON)

| Item | Symbol | Condition | Min | Typ | Max | Unit | Note | |
|-------------------------------|-------------------|-------------------------------------------|--------------------------------------------------------|------|------|-------------------|---------------|-----|
| Brightness | B | $\phi=0^\circ, \theta=0^\circ$ | 200 | 300 | - | cd/m ² | (1), (2) | |
| Contrast ratio | K | $\phi=0^\circ, \theta=0^\circ$ | 200 | 400 | - | - | (1), (6) | |
| Viewing angle | $\phi_1 + \phi_2$ | $\theta=0^\circ, K \geq 10$ | - | 160 | - | deg | (4), (6), (7) | |
| | | $\theta=90^\circ, K \geq 10$ | - | 160 | - | | | |
| Brightness uniformity | - | $\phi=0^\circ, \theta=0^\circ$ | 70 | 80 | - | % | (2), (3), (5) | |
| Response time | tr + tf | $\phi=0^\circ, \theta=0^\circ$ Ta=25°C | - | 40 | 70 | ms | (8) | |
| Color tone (Primary Color) | Red | x | Maximum Gradient $\phi=0^\circ$ $\theta=0^\circ$ | 0.57 | 0.63 | 0.69 | - | (1) |
| | | y | | 0.29 | 0.35 | 0.41 | | |
| | Green | x | | 0.28 | 0.34 | 0.40 | | |
| | | y | | 0.53 | 0.59 | 0.65 | | |
| | Blue | x | | 0.08 | 0.14 | 0.20 | | |
| | | y | | 0.04 | 0.10 | 0.16 | | |
| | White | x | | 0.25 | 0.31 | 0.37 | | |
| | | y | | 0.26 | 0.32 | 0.38 | | |

Common conditions for measurement

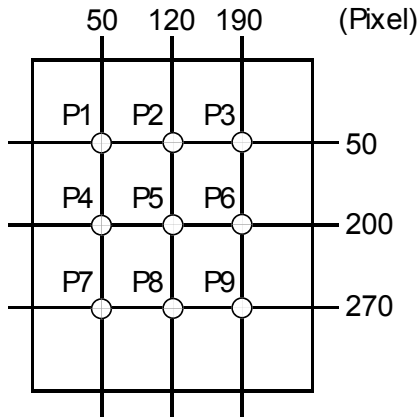
Measurement environment : Dark room
 Ambient temperature : Ta = 25°C
 Sequence : Follow Item 8.4.2, SEQUENCE.
 Power supply voltage : Vcc = VDD/O = 2.8 V
 Backlight current : 20 mA

Notes (1) Definition of Brightness "B"

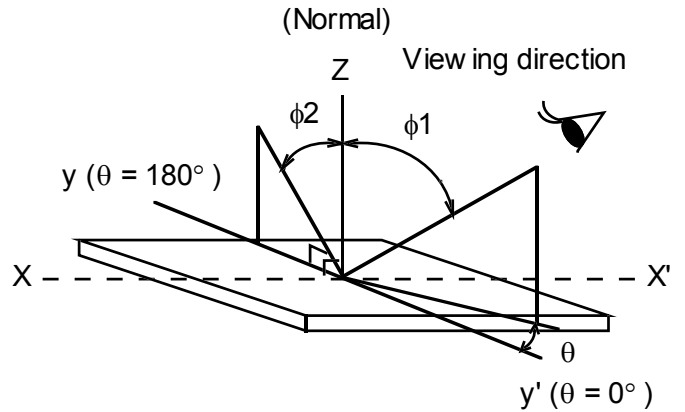


(2) Display image for measurement : White

Notes (3) Measurement point



(4) Definitions of θ and ϕ



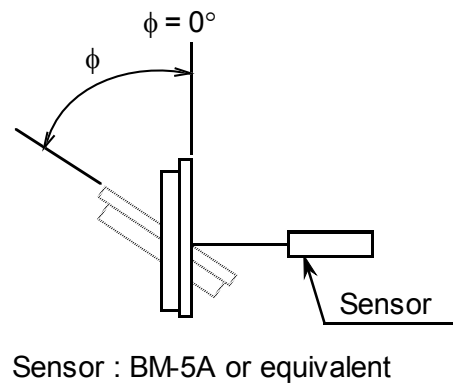
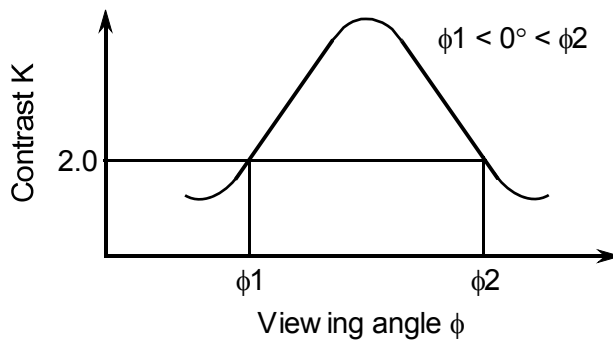
(5) Definition of the brightness uniformity

$$\text{Uniformity} = \text{Brightness (min.)} / \text{Brightness (max.)} \times 100(\%)$$

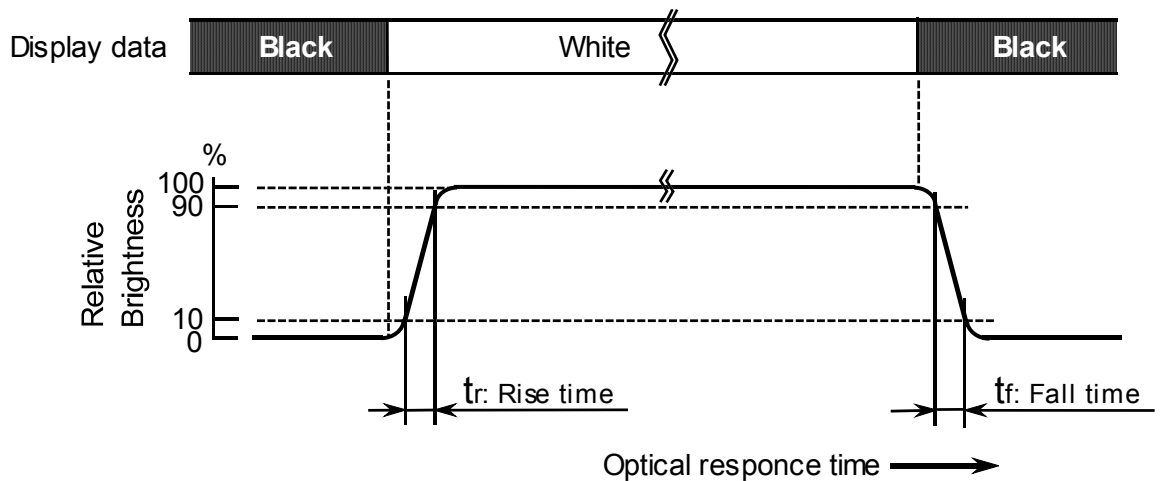
(6) Definition of Contrast "K"

$$K = \frac{\text{Brightness when displaying White raster}}{\text{Brightness when displaying Black raster}}$$

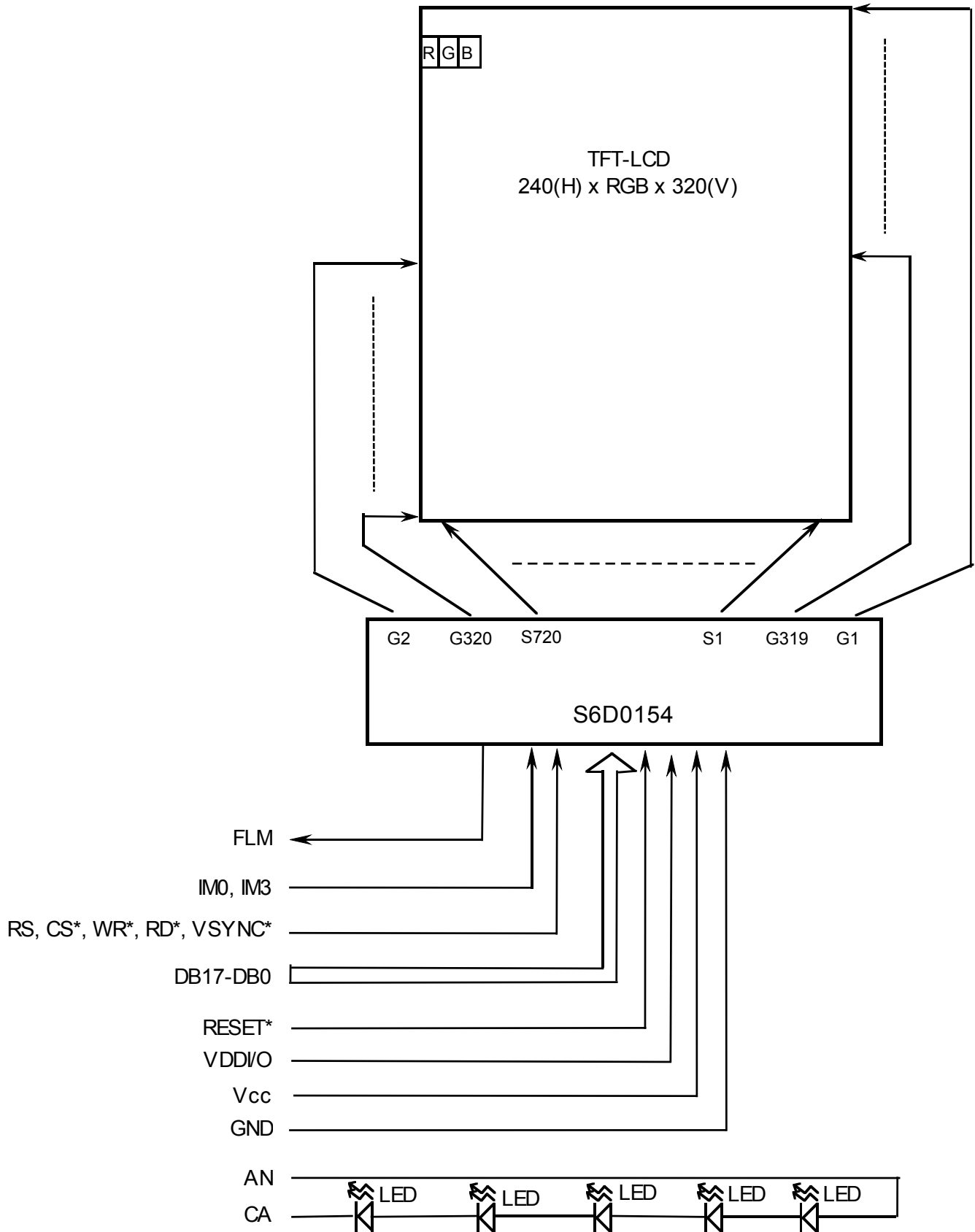
(7) Definition of viewing angle ϕ_1 and ϕ_2



(8) Definition of optical response time



7. BLOCK DIAGRAM



8. INTERFACE

8.1 INTERNAL PIN CONNECTION (8 / 9 / 16/18-bit CPU bus correspondence)

| Pin No. | Signal | Function | Pin No. | Signal | Function |
|---------|--------|---------------------------------------|---------|---------------------|---------------------------------------|
| 1 | GND | GND | 21 | DB3 | Data Bus (Instruction & Display Data) |
| 2 | GND | GND | 22 | DB2 | Data Bus (Instruction & Display Data) |
| 3 | ID | ID(VDD/O) | 23 | DB1 | Data Bus (Instruction & Display Data) |
| 4 | IM0 | MPU Interface Sw itching | 24 | DB0 | Data Bus (Instruction & Display Data) |
| 5 | IM3 | MPU Interface Sw itching | 25 | RD* | Read |
| 6 | RESET* | Reset | 26 | WR* | Write |
| 7 | DB17 | Data Bus (Instruction & Display Data) | 27 | RS | Data/Command Identification |
| 8 | DB16 | Data Bus (Instruction & Display Data) | 28 | CS* | Chip Select |
| 9 | DB15 | Data Bus (Instruction & Display Data) | 29 | VDD/O | Power Supply for Interface |
| 10 | DB14 | Data Bus (Instruction & Display Data) | 30 | VDD/O | Power Supply for Interface |
| 11 | DB13 | Data Bus (Instruction & Display Data) | 31 | V _{cc} | Power Supply for Logic and Analog |
| 12 | DB12 | Data Bus (Instruction & Display Data) | 32 | V _{cc} | Power Supply for Logic and Analog |
| 13 | DB11 | Data Bus (Instruction & Display Data) | 33 | NC | NC (No Connection) |
| 14 | DB10 | Data Bus (Instruction & Display Data) | 34 | AN | Power Supply for LED |
| 15 | DB9 | Data Bus (Instruction & Display Data) | 35 | CA | GND for LED |
| 16 | DB8 | Data Bus (Instruction & Display Data) | 36 | VS _{YNC} * | Line synchronous signal |
| 17 | DB7 | Data Bus (Instruction & Display Data) | 37 | FLM | Frame head pulse signal |
| 18 | DB6 | Data Bus (Instruction & Display Data) | 38 | NC | NC (No Connection) |
| 19 | DB5 | Data Bus (Instruction & Display Data) | 39 | GND | GND |
| 20 | DB4 | Data Bus (Instruction & Display Data) | | | |

Suitable Connector : HIROSE FH26-39S-0.3SHW(5)

8.2 CPU INTERFACE MODE SETTING

8.2.1 CPU Interface Mode Selection

| PIN No. | SIGNAL | 80-System Bus Interface | | | |
|---------|--------|-------------------------|------------|-------------|------------|
| | | 18-bit | 16-bit | 9-bit | 8-bit |
| | | 262k Colors | 65k Colors | 262k Colors | 65k Colors |
| 4 | IM0 | GND | GND | VDDI/O | VDDI/O |
| 5 | IM3 | VDDI/O | GND | VDDI/O | GND |

Select the interface mode and colors by setting bits of IM0 and IM3.

8.2.2 Unused Data Bus Connection

| Bus Interface | | 18-bit | 16-bit | 9-bit | 8-bit |
|----------------------|--------|--------|---------------|---------------|---------------|
| Data Bus Pins | | DB17-0 | DB17-10 DB8-1 | DB17-9 | DB17-10 |
| Unused Data Bus Pins | | - | DB9,DB0 | DB8-0 | DB9-0 |
| Pin No. | Signal | | | | |
| 7 | DB17 | | | | |
| 8 | DB16 | | | | |
| 9 | DB15 | | | | |
| 10 | DB14 | | | | |
| 11 | DB13 | | | | |
| 12 | DB12 | | | | |
| 13 | DB11 | | | | |
| 14 | DB10 | | | | |
| 15 | DB9 | | GND or VDDI/O | | GND or VDDI/O |
| 16 | DB8 | | | GND or VDDI/O | GND or VDDI/O |
| 17 | DB7 | | | GND or VDDI/O | GND or VDDI/O |
| 18 | DB6 | | | GND or VDDI/O | GND or VDDI/O |
| 19 | DB5 | | | GND or VDDI/O | GND or VDDI/O |
| 20 | DB4 | | | GND or VDDI/O | GND or VDDI/O |
| 21 | DB3 | | | GND or VDDI/O | GND or VDDI/O |
| 22 | DB2 | | | GND or VDDI/O | GND or VDDI/O |
| 23 | DB1 | | | GND or VDDI/O | GND or VDDI/O |
| 24 | DB0 | | GND or VDDI/O | GND or VDDI/O | GND or VDDI/O |

Unused data bus pins are to be set at GND or VDDI/O.

8.2.3 Display Data Input

| Data Bus | | DB 17 | DB 16 | DB 15 | DB 14 | DB 13 | DB 12 | DB 11 | DB 10 | DB 9 | DB 8 | DB 7 | DB 6 | DB 5 | DB 4 | DB 3 | DB 2 | DB 1 | DB 0 |
|----------|------------|----------|-------|-------|----------|-------|-------|-------|-------|------|------|------|------|----------|------|------|------|------|------|
| 18-bit | Transfer 1 | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 |
| 16-bit | Transfer 1 | R5 R0 | R4 | R3 | R2 | R1 | G5 | G4 | G3 | - | G2 | G1 | G0 | B5 B0 | B4 | B3 | B2 | B1 | - |
| 9-bit | Transfer 1 | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | - | - | - | - | - | - | - | - | - |
| | Transfer 2 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 | - | - | - | - | - | - | - | - | - |
| 8-bit | Transfer 1 | R5 R0 | R4 | R3 | R2 | R1 | G5 | G4 | G3 | - | - | - | - | - | - | - | - | - | - |
| | Transfer 2 | G2 | G1 | G0 | B5 B0 | B4 | B3 | B2 | B1 | - | - | - | - | - | - | - | - | - | - |

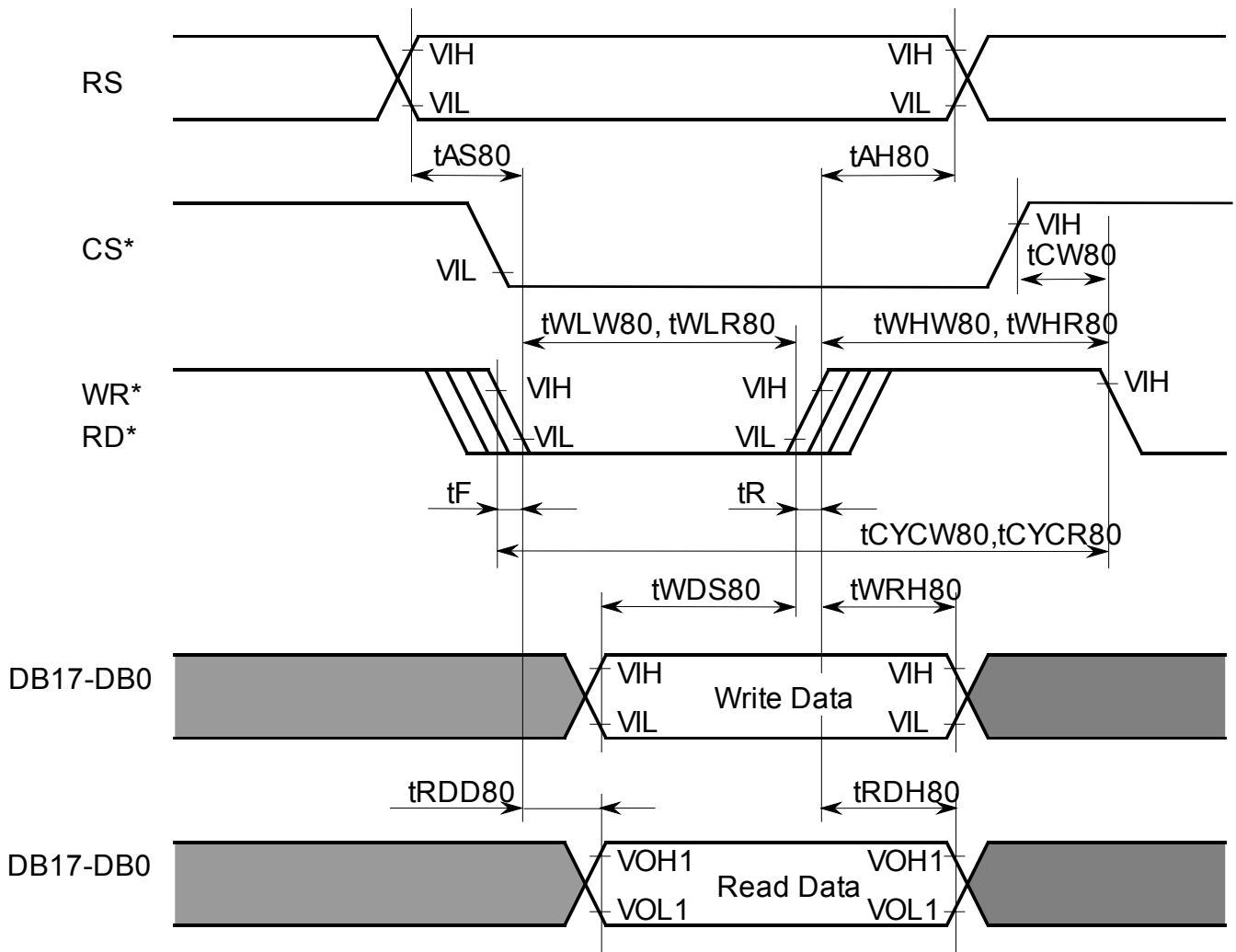
8.3 INTERFACE TIMING

8.3.1 80-System Bus Interface Timing Characteristics <<18 bits / 16 bits / 9 bits / 8 bits>>

[Normal Write Mode, VDD/I/O = 1.75 to 2.8 V]

V_{CC} = 2.8 V

| Item | | Symbol | Unit | Min | Typ | Max |
|-----------------------------|-------|---------|------|-----|-----|-----|
| Cycle time | Write | tCYCW80 | ns | 105 | - | - |
| | Read | tCYCR80 | ns | 525 | - | - |
| Pulse rise / fall time | | tR, tF | ns | - | - | 14 |
| Pulse width low | Write | tWLW80 | ns | 35 | - | - |
| | Read | tWLR80 | ns | 263 | - | - |
| Pulse width high | Write | tWHW80 | ns | 35 | - | - |
| | Read | tWHR80 | ns | 263 | - | - |
| RS to CS, WR(RD) setup time | | tAS80 | ns | 11 | - | - |
| RS to CS, WR(RD) hold time | | tAH80 | ns | 3 | - | - |
| CS to WR(RD) time | | tCT80 | ns | 16 | - | - |
| Write data set up time | | tWDS80 | ns | 21 | - | - |
| Write data hold time | | tWDH80 | ns | 11 | - | - |
| Read data delay time | | tRDD80 | ns | - | - | 190 |
| Read data hold time | | tRDH80 | ns | 11 | - | - |



Bus Timing

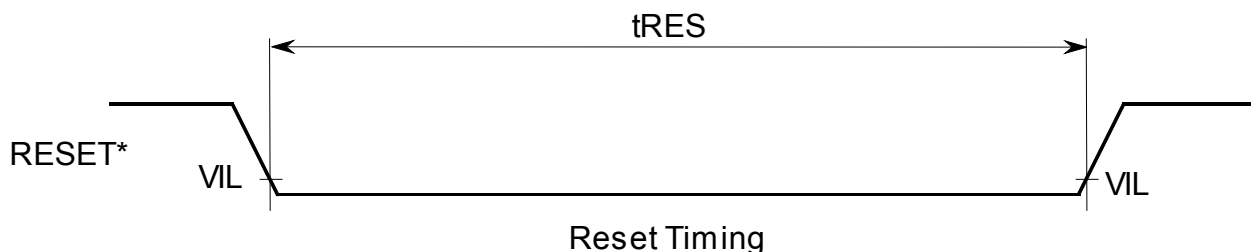
Notes (1) t_{WLW80} and t_{WLR80} are determined by the overlap period of low CS and low WR or low CS and low RD.

8.3.2 Reset Timing Characteristics

[VDD/O=1.75 to 2.8V]

V_{CC} = 2.8 V

| Item | Symbol | Unit | Min | Typ | Max |
|-----------------------|------------------|------|-----|-----|-----|
| Reset low pulse width | t _{RES} | ms | 10 | - | - |

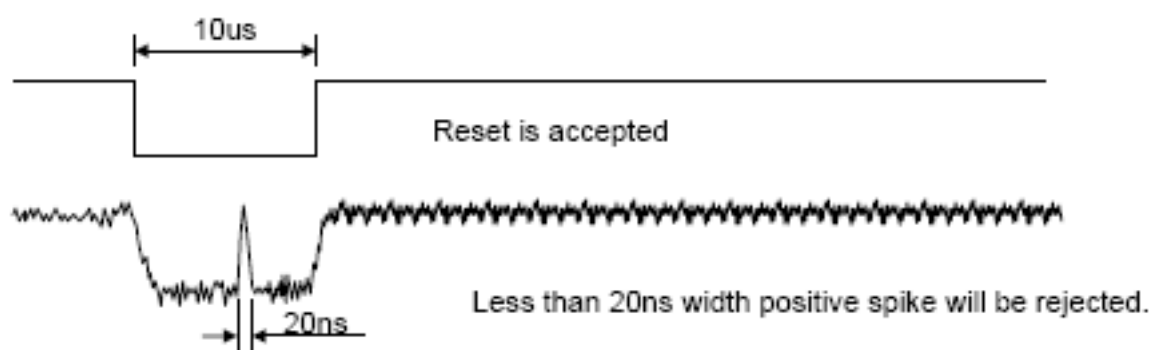


Notes (1) Reset low pulse width shorter than 10us do not make reset. It means undesired short pulse such as glitch, bouncing noise or electrostatic discharge do not cause irregular system reset. Please refer to the table below.

| ItRES Pulse | Action |
|------------------------|----------------|
| Shorter than 5 us | No reset |
| Longer than 10 us | Reset |
| Between 5 us and 10 us | Not determined |

1. User may or may not use RESETB pin. In order to use it, user should satisfy the conditions described in the above tables. But when not wants to use RESETB, user may fix this pin to VDD3 level because internally generated POR (Power-On-Reset) is used.

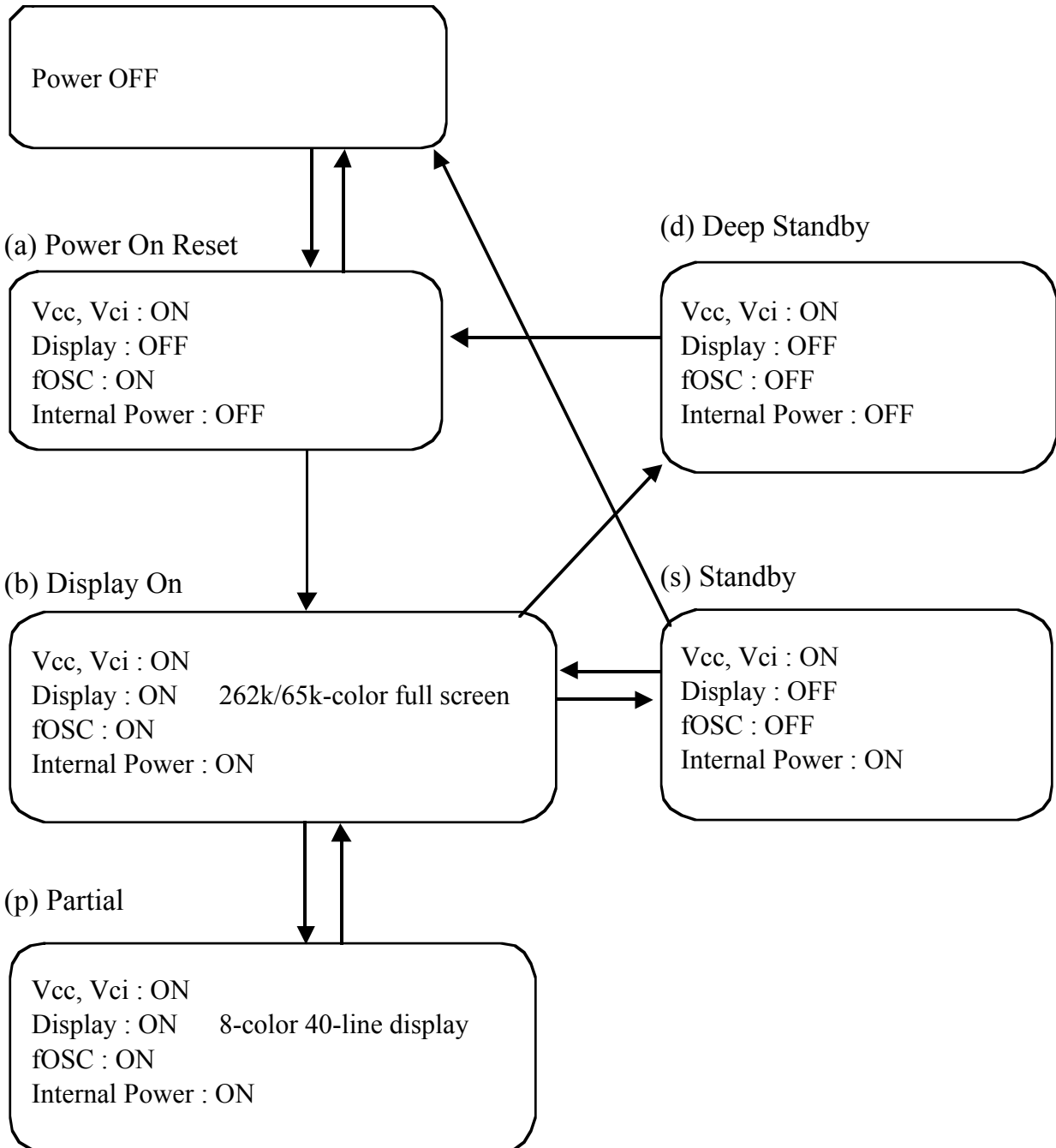
2. Spike Rejection also applies during a valid reset pulse as shown below:



8.4 REGISTER SETTING

8.4.1 State Transition Diagram of Operation Mode

(h) External Power Off



8.4.2 Sequence

| State (h) to (a) | | | Last proposal |
|------------------|----------|-------------------|---------------|
| 1 | Power ON | Vcc ON | |
| 2 | | ioVcc ON | |
| 3 | | Vci ON | |
| 4 | Reset | wait 1 ms Min. | |
| 5 | | reset* = "L" | |
| 6 | | wait 1 ms Min. | |
| 7 | | reset* = "H" | |
| 8 | | wait 10 ms Min. | |

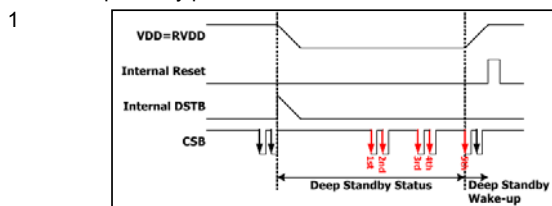
| State (a) to (h) | | | Last proposal |
|------------------|-----------|-----------|---------------|
| 1 | Power OFF | Vci OFF | |
| 2 | | ioVcc OFF | |
| 3 | | Vcc OFF | |

| State (s) to (h) | | | Last proposal |
|------------------|-------------|-------------------|---------------|
| 1 | Display OFF | wait 20 ms Min. | |
| 2 | Power OFF | Vci OFF | |
| 3 | | ioVcc OFF | |
| 4 | | Vcc OFF | |

| State (b) to (d) | | | Last proposal |
|------------------|--------------|----------------------|---------------|
| 1 | Display OFF | R15h 0x0000 | |
| 2 | | R07h 0x0012 | |
| 3 | | wait 2 frames Min. | |
| 4 | | R07h 0x0000 | |
| 5 | | wait 1 frame Min. | |
| 6 | Deep Standby | R10h 0x0002 | |

| State (d) to (a) | | | Last proposal |
|------------------|-------|------------------------|---------------|
| 1 | Reset | reset* = "L" | |
| 2 | | wait 10 μ s Min. | |
| 3 | | reset* = "H" | |
| 4 | | wait 10 ms | |

Otherwise, set CSB as follows (Low pulse width >10 μ s) and sequentially put "Wait 10ms".



| | | | |
|---|--|-------------|--|
| 2 | | wait 10ms | |
|---|--|-------------|--|

| State (b) to (s) | | | Last proposal |
|------------------|-------------|----------------------|---------------|
| 1 | Display OFF | R15h 0x0000 | |
| 2 | | R07h 0x0012 | |
| 3 | | wait 2 frames Min. | |
| 4 | | R07h 0x0000 | |
| 5 | | wait 1 frame Min. | |
| 6 | Standby | R10h 0x0001 | |

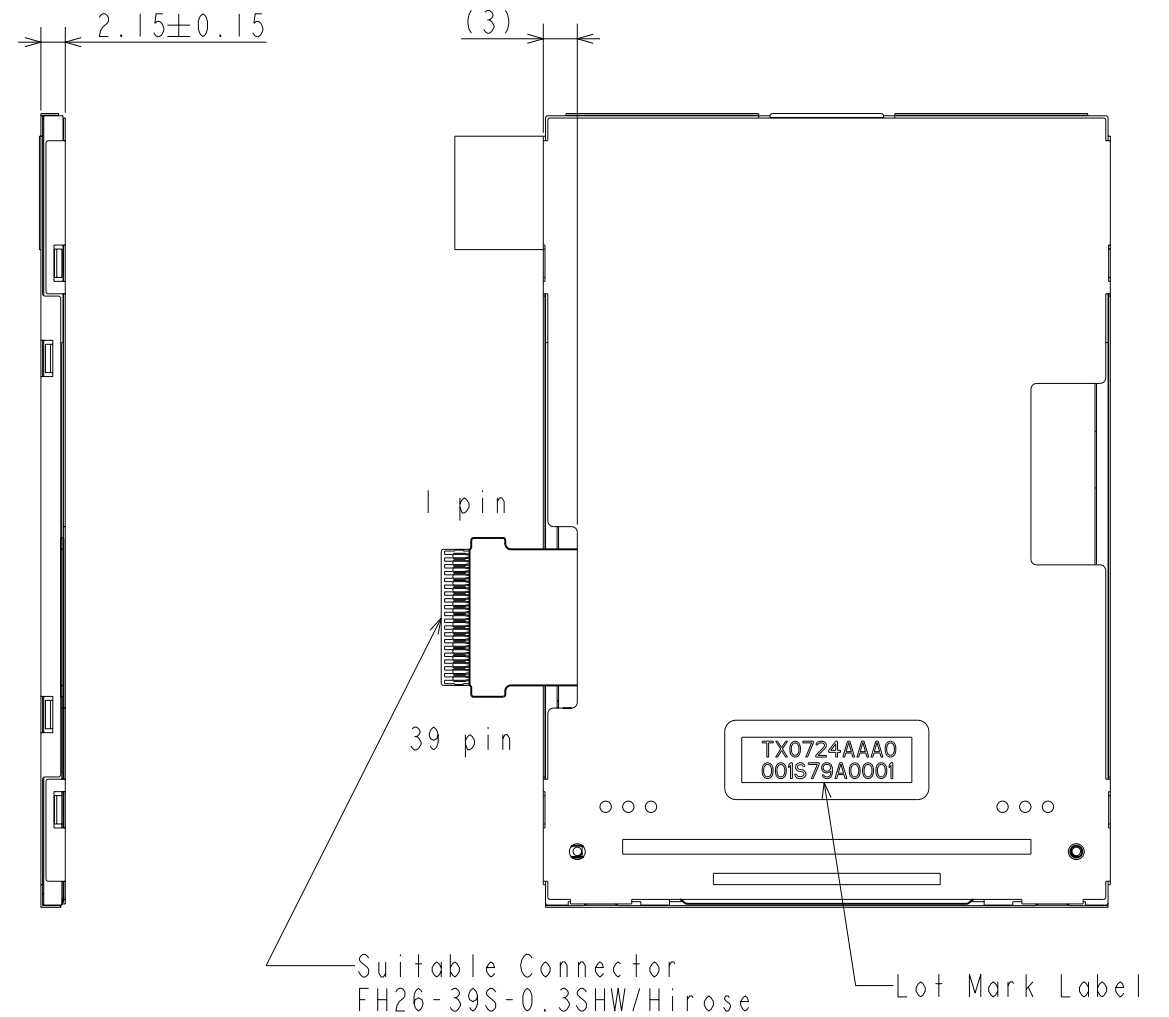
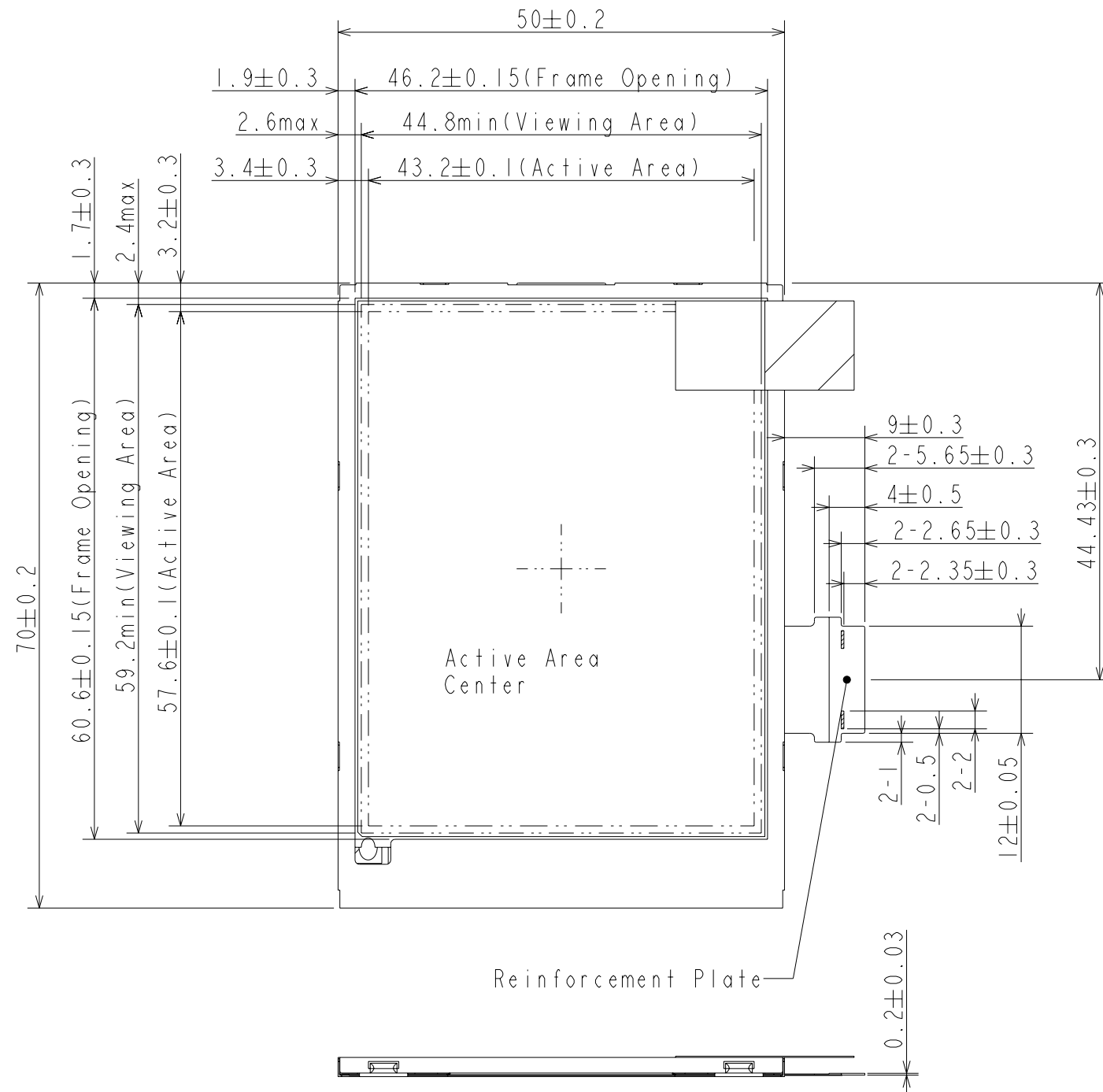
| State (b) to (p) | | | Last proposal |
|------------------|---------------------------------------|----------------------|---------------|
| 1 | Display OFF | R07h 0x0012 | |
| 2 | Power control | R10h 0x0100 | |
| 3 | | R12h 0x2232 | |
| 4 | Vertical scroll control | R30h 0x0000 | |
| 5 | Vertical scroll control E | R31h 0x0027 | |
| 6 | Vertical scroll control S | R32h 0x0000 | |
| 7 | Vertical scroll control S | R33h 0x0000 | |
| 8 | Partial screen driving position END | R34h 0x0027 | |
| 9 | Partial screen driving position Start | R35h 0x0000 | |
| 10 | Horizontal RAM address position E | R36h 0x00EF | |
| 11 | Horizontal RAM address position S | R37h 0x0000 | |
| 12 | Vertical RAM address position E | R38h 0x0027 | |
| 13 | Vertical RAM address position S | R39h 0x0000 | |
| 14 | | wait 2 frames Min. | |
| 15 | 8-color | R07h 0x001A | |
| 16 | | wait 2 frames Min. | |
| 17 | Display ON | R07h 0x101B | |
| 18 | Image refresh | R20h 0x0000 | |
| 19 | | R21h 0x0000 | |
| 20 | | R22h - | |
| 21 | | Display data write | 240x40 |

| State (p) to (b) | | | Last proposal |
|------------------|---------------------------------------|----------------------|---------------|
| 1 | Display OFF | R07h 0x0012 | |
| 2 | Power control | R10h 0x0710 | |
| 3 | Power control | R12h 0x2000 | |
| 4 | Vertical scroll control | R30h 0x0000 | |
| 5 | Vertical scroll control E | R31h 0x013F | |
| 6 | Vertical scroll control S | R32h 0x0000 | |
| 7 | Vertical scroll control S | R33h 0x0000 | |
| 8 | Partial screen driving position END | R34h 0x013F | |
| 9 | Partial screen driving position Start | R35h 0x0000 | |
| 10 | Horizontal RAM address position E | R36h 0x00EF | |
| 11 | Horizontal RAM address position S | R37h 0x0000 | |
| 12 | Vertical RAM address position E | R38h 0x013F | |
| 13 | Vertical RAM address position S | R39h 0x0000 | |
| 14 | | wait 2 frames Min. | |
| 15 | 262k-color | R07h 0x1012 | |
| 16 | | wait 2 frames Min. | |
| 17 | Display ON | R07h 0x1013 | |
| 18 | Image refresh | R20h 0x0000 | |
| 19 | | R21h 0x0000 | |
| 20 | | R22h - | |
| 21 | | Display data write | 240x320 |

| State (a) to (b) | | Last proposal | |
|------------------|------------------------------------|--------------------|---------------------|
| 1 | Power setting (1) | R11h | 0x001A |
| 2 | | R12h | 0x2000 |
| 3 | | R13h | 0x0070 |
| 4 | | R14h | 0x24E9 |
| 5 | Equalizing control | R15h | 0x0070 |
| 6 | | R10h | 0x0710 |
| 7 | | wait | 10ms |
| 8 | Power control (1) | R11h | 0x0110 |
| 9 | | wait | 10ms |
| 10 | Power control (2) | R11h | 0x0312 |
| 11 | | wait | 10ms |
| 12 | Power control (3) | R11h | 0x0712 |
| 13 | | wait | 10ms |
| 14 | Power control (4) | R11h | 0x0F1A |
| 15 | | wait | 20ms |
| 16 | Power control (5) | R11h | 0x0F3A |
| 17 | | wait | 30ms |
| 18 | Driver output control | R01h | 0x0528 |
| 19 | LCD-driving-waveform control | R02h | 0x0100 |
| 20 | Entry mode | R03h | 0x1130 |
| 21 | Display control (1) | R07h | 0x0000 |
| 22 | Display control (2) | R08h | 0x0808 (FP=8, BP=8) |
| 23 | Frame cycle control | R0Bh | 0x2102 |
| 24 | External display interface control | R0Ch | 0x0000 |
| 25 | | R0Eh | 0x0200 |
| 26 | | R0Fh | 0x1801 |
| 27 | | wait | 10ms |
| 28 | Gamma setting | R50h | 0x0500 |
| 29 | | R51h | 0x000B |
| 30 | | R52h | 0x0200 |
| 31 | | R53h | 0x0003 |
| 32 | | R54h | 0x0002 |
| 33 | | R55h | 0x0B00 |
| 34 | | R56h | 0x0005 |
| 35 | | R57h | 0x0300 |
| 36 | | R58h | 0x0000 |
| 37 | | R59h | 0x0000 |
| 38 | Vertical scroll control | R30h | 0x0000 |
| 39 | Vertical scroll control E | R31h | 0x013F |
| 40 | Vertical scroll control S | R32h | 0x0000 |
| 41 | Vertical scroll control S | R33h | 0x0000 |
| 42 | Horizontal RAM address position E | R36h | 0x00EF |
| 43 | Horizontal RAM address position S | R37h | 0x0000 |
| 44 | Vertical RAM address position E | R38h | 0x013F |
| 45 | Vertical RAM address position S | R39h | 0x0000 |
| 46 | | wait | 2 frames Min. |
| 47 | | R07h | 0x0012 |
| 48 | | wait | 2 frames Min. |
| 49 | Display ON | R07h | 0x1013 FLM ON |
| 50 | Image refresh | R20h | 0x0000 |
| 51 | | R21h | 0x0000 |
| 52 | | R22h | - |
| 53 | | Display data write | 240x320 |

| State (s) to (b) | | Last proposal | |
|------------------|------------------------------------|--------------------|---------------|
| 1 | Standby return | R10h | 0x0000 |
| 2 | | wait | 10ms |
| 3 | Power setting (1) | R11h | 0x001A |
| 4 | | R12h | 0x2000 |
| 5 | | R13h | 0x0070 |
| 6 | | R14h | 0x24E9 |
| 7 | Equalizing control | R15h | 0x0070 |
| 8 | | R10h | 0x0710 |
| 9 | | wait | 10ms |
| 10 | Power control (1) | R11h | 0x0110 |
| 11 | | wait | 10ms |
| 12 | Power control (2) | R11h | 0x0312 |
| 13 | | wait | 10ms |
| 14 | Power control (3) | R11h | 0x0712 |
| 15 | | wait | 10ms |
| 16 | Power control (4) | R11h | 0x0F1A |
| 17 | | wait | 20ms |
| 18 | Power control (5) | R11h | 0x0F3A |
| 19 | | wait | 30ms |
| 20 | Driver output control | R01h | 0x0528 |
| 21 | LCD-driving-waveform control | R02h | 0x0100 |
| 22 | Entry mode | R03h | 0x1130 |
| 23 | Display control (1) | R07h | 0x0000 |
| 24 | Display control (2) | R08h | 0x0808 |
| 25 | Frame cycle control | R0Bh | 0x2102 |
| 26 | External display interface control | R0Ch | 0x0000 |
| 27 | | R0Eh | 0x0200 |
| 28 | | R0Fh | 0x1801 |
| 29 | | wait | 10ms |
| 30 | Gamma setting | R50h | 0x0500 |
| 31 | | R51h | 0x000B |
| 32 | | R52h | 0x0200 |
| 33 | | R53h | 0x0003 |
| 34 | | R54h | 0x0002 |
| 35 | | R55h | 0x0B00 |
| 36 | | R56h | 0x0005 |
| 37 | | R57h | 0x0300 |
| 38 | | R58h | 0x0000 |
| 39 | | R59h | 0x0000 |
| 40 | Vertical scroll control | R30h | 0x0000 |
| 41 | Vertical scroll control E | R31h | 0x013F |
| 42 | Vertical scroll control S | R32h | 0x0000 |
| 43 | Vertical scroll control S | R33h | 0x0000 |
| 44 | | R36h | 0x00EF |
| 45 | | R37h | 0x0000 |
| 46 | | R38h | 0x013F |
| 47 | | R39h | 0x0000 |
| 48 | | wait | 2 frames Min. |
| 49 | Display ON | R07h | 0x0012 |
| 50 | | wait | 2 frames Min. |
| 51 | Display ON | R07h | 0x1013 |
| 52 | Image refresh | R20h | 0x0000 |
| 53 | | R21h | 0x0000 |
| 54 | | R22h | - |
| 55 | | Display data write | 240x320 |

9. Dimensional Outline



Unit:mm
 Note
 (1) The unspecified tolerance:±0.2