TENTATIVE

Sep. 12, 2006

No.3284TTD 2597 - 2

HITACHI

Hitachi Displays, Ltd.

LIQUID CRYSTAL DISPLAY MODULE TECHNICAL DATA

TX18D30VM2FAA

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DESCRIPTION

This specifications is applied to the following TFT module.

Note : Inverter for back light unit is not built in this module.

Product Name : TX18D30VM2FAA

General Specifications

Effective Display Area	: (H)153.4 × (V)86.4	(mm)
Number of Pixels	: (H)480 × (V)234	(pixels)
Pixel Pitch	: (H)0.3195 × (V)0.3690	(mm)
Color Pixel Arrangement	: R,G,B Vertical Stripe	
Display Mode	: Transmissive Mode Normally White Mode	
Top Polarizer Type	: Anti-Glare and Anti-Reflective Polarizer Film	
Number of Colors	: 262,144	(colors)
Viewing Angle	: (Azimuth ϕ =270°)	
Input Signal	: C-MOS (R,G,B 6 bit Digital)	
Back Light	: 1pc. of CCFL	
External Dimensions	: (H)167.0 × (V)102.0 × (t)14.3 typ.	(mm)
Weight	: 240 typ.	(g)

1. ABSOLUTE MAXIMUM RATINGS

1.1 Environmental Absolute Maximum Ratings

ITEM		Operating		Storage		Unit	Note
		Min.	Max.	Min.	Max.		
Temperature	ambient	-30	85	-40	95	℃	1)
	surface	-30	85	-			
Humidity		2)		2)		%RH	1),2)
Vibration		-	4.9(0.5G)	-	19.6 (2G)	m/s2	3)
Shock		-	29.4(3G)	-	490 (50G)	m/s2	4)
Corrosive Gas		Not Acceptable		Not Acceptable		-	

Note 1) The brightness of CCFL tends to degrade at low temperature and the life-time becomes shorter at low temperature.

2) Ta≦40 ℃ · · · · · · Relative humidity should be less than 85%RH. Dew is prohibited.
Ta＞40 ℃ · · · · · · Relative humidity should be lower than the moisture of the 85%RH at 40℃.

3) Frequency of the vibration is between 20Hz and 100Hz. (Except the resonance point)

4) Pulse width of the shock is 10 ms.

1.2 Electrical Absolute Maximum Ratings

(1)TFT Module

ITEM	SYMBOL	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	0	5.5	V	
Input Voltage for logic	V_I	-0.3	3.6	V	1)
Electrostatic Durability	V_{ESD0}	±100		V	2),3)
	V_{ESD1}	±8		kV	2),4)

Note 1)It is applied to pixel data signal and clock signal.
2)Discharge Coefficient : 200pF-250Ω, Environmental : 25℃-70%RH
3)It is applied to I/F connector pins.
4)It is applied to the surface of a metallic bezel and a LCD panel.

(2) Back-light

ITEM	SYMBOL	Min.	Max.	Unit	Note
Input Current	IL	-	7.0	mArms	1)
Input Voltage	VL	-	1,800	Vrms	2)

Note 1)The specification is defined at ground line.
2)The specification shall be applied at connector pins for a CCFL at start-up.

2. OPTICAL CHARACTERISTICS

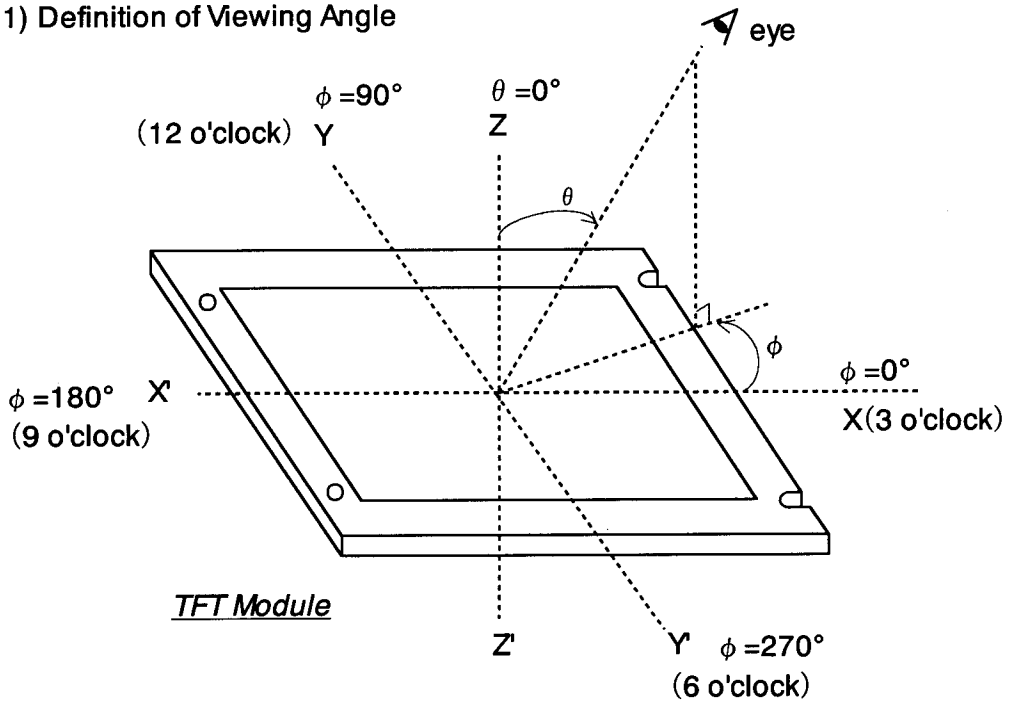
2.1 OPTICAL CHARACTERISTICS

The following optical characteristics are measured under stable conditions. It takes about 15 minutes to reach stable conditions. The measuring point is the center of display area unless otherwise noted. The optical characteristics should be measured in a dark room or equivalent state.

Measuring equipment: KONICA MINOLTA CS-1000A, or equivalent
Temperature =25℃、VDD=5.0V、fV=60Hz、IL=6.0mA

ITEM		SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT	NOTE
Contrast Ratio		CR		250	400	-	-	2)
Brightness of white		Bwh		400	500	-	cd/m^2	
Brightness uniformity		Buni		75	-	-	%	4)
Color Chromaticity (CIE)	Red	χ	θ =0° 1)	0.55	0.60	0.65	-	
		y		0.28	0.33	0.38		
	Green	χ		0.28	0.33	0.38		
		y		0.49	0.54	0.59		
	Blue	χ		0.10	0.15	0.20		
		y		0.08	0.13	0.18		
	White	χ		0.30	0.33	0.36		
		y		0.30	0.33	0.36		
Response Time	Rise	ton	Ta=25℃ θ =0° 1)	-	15	25	ms	3)
	Fall	toff		-	5	15		
	Rise	ton	Ta=-25℃ θ =0° 1)	-	270	500		
	Fall	toff		-	80	200		
	Rise	ton	Ta=-30℃ θ =0° 1)	-	390	750		
	Fall	toff		-	110	250		
Viewing Angle (CR≧10)	X-X'	θ X	ϕ =0°	25	35	-	deg	1)
		θ X'	ϕ =180°	25	35	-		
	Y-Y'	θ Y	ϕ =90°	20	25	-		
		θ Y'	ϕ =270°	20	25	-		
Surface reflection	-			-	-	3.0	%	
Gamma	-			-	2.5	-		

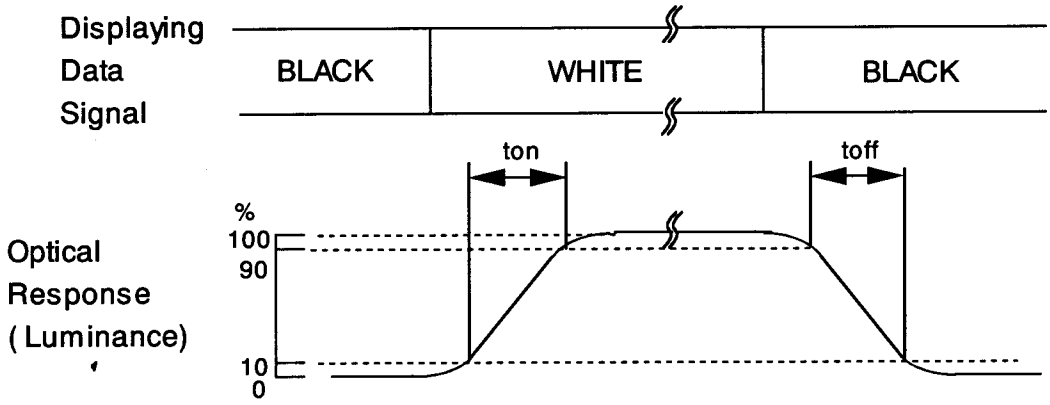
Note 1) Definition of Viewing Angle



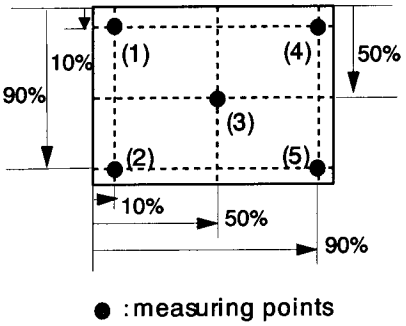
2) Definition of Contrast Ratio (CR)

$$CR = \frac{\text{(Luminance at displaying WHITE)}}{\text{(Luminance at displaying BLACK)}}$$

3) Definition of Response Time



4) Definition of Brightness Uniformity



● : measuring points

Display pattern is white (63 level) . The brightness uniformity is defined as the following equation. Brightness at each point is measured, and maximum and minimum brightness is calculated.

$$Buni = \frac{Bmin}{Bmax} \times 100$$

3. ELECTRICAL CHARACTERISTICS

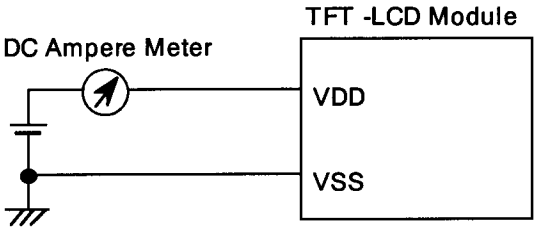
3.1 TFT-LCD Module

Ta=25℃, Vss=0V

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage		VDD	4.5	5	5.5	V	
Input Voltage for Logic Circuits	Hi	VIH	2.0	—	3.6	V	1)
	Lo	VIL	VSS	—	0.8	V	1)
Power Supply Current		IDD	—	150	280	mA	2), 3)
VSYNC Frequency		fV	47	60	72	Hz	

Notes 1) The specification is applied to pixel data signal,timing signal and clock signal.

2) fV=60Hz, fCLK=9 MHz, VDD=5.0V, DC Current.



Typical value is measured when displaying Black raster.

Maximum is measured when displaying Vertical-stripe pattern of 2 pixel pitch.

3) Current capacity for VDD power source should be larger than 2A.

This TFT-LCD Module has a fuse(1A).

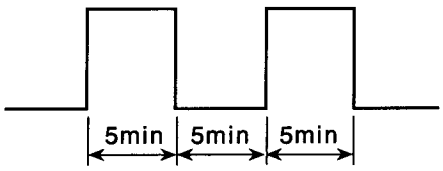
3.2 Back Light

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Input Voltage (IL=6mA)		VL	-	600	1000	Vrms	3),4)
Input Current		IL	5.0	6.0	7.0	mArms	1)
Established Starting	at 25℃	Vs	-	-	1450	Vrms	3),7)
Voltage	at -30℃		-	-	1500	Vrms	
Operating Frequency		fL	40	-	60	kHz	2)
CCFL Life Time (IL=6mA at 25℃)		-	15000	-	-	h	6)
CCFL Life Time intermittent		-	20000	-	-	cycle	6),10)
Start-up brightness		LLOW	-	100	-	cd/m^2	11)

Note :

1) The specification is defined at low voltage line.
2) Frequency of power supply for a CCFL may cause the interference with HSYNC frequency and cause beat or flicker on the display. Therefore, lamp frequency shall be as different as possible from HSYNC frequency in order to avoid the interference.
3) It is applied between each terminal in CCFL.
4) Operating voltage is measured at 25 ± 2℃. The variance of the voltage is (± 10%).
5) The lamp power consumption shown above does not include loss of external inverter.
6) Life time of a lamp is defined. The life is determined as the time at which brightness of the lamp is 50% compared to that of initial value at the typical lamp current on condition of continuous operating at 25 ± 2℃.
7) Max frequency is 70kHz at starting time only.
8) The Voltage Vs should be applied to the lamps for more than 1.0 second for start up.
9) The burst frequency may produce interference with Vsync frequency and it may cause beat noise on the display. So please set the burst frequency to avoid the interference.
10) Intermission cycle (TA=25℃)

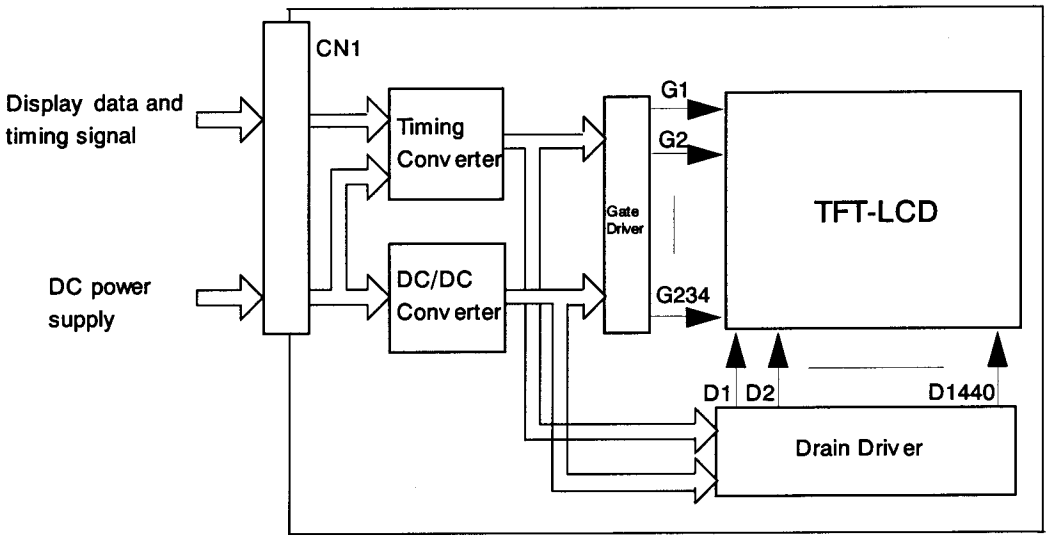
High (7mA)



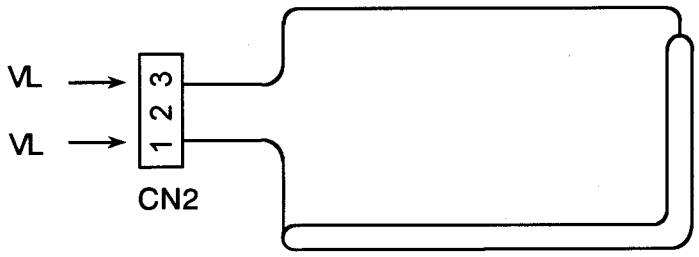
11) Starting temperature -20℃
Lamp current boost current ILBOOST=9mArms
Warm up time 1minute

4. BLOCK DIAGRAM

(1) TFT Module



(2) Back light unit



Color of Wires from CCFL to CN2

1(VL) :Pink

3(VL) :White

5. INTERFACE PIN ASSIGNMENT

5.1 TFT-LCD MODULE

(Connector 1 :IRISO 9633S-38A-T)

Pin No.	Symbol	Description	Note
1	VSS	Ground	2)
2	CLK	Clock	
3	VSS	Ground	
4	HSync	Horizontal Sync	
5	VSync	Vertical Sync	
6	VSS	Ground	2)
7	R0	Red Data Signal 0 (LSB)	
8	R1	Red Data Signal 1	
9	R2	Red Data Signal 2	
10	R3	Red Data Signal 3	
11	R4	Red Data Signal 4	
12	R5	Red Data Signal 5 (MSB)	
13	VSS	Ground	2)
14	G0	Green Data Signal 0 (LSB)	
15	G1	Green Data Signal 1	
16	G2	Green Data Signal 2	
17	G3	Green Data Signal 3	
18	G4	Green Data Signal 4	
19	G5	Green Data Signal 5 (MSB)	
20	VSS	Ground	2)
21	B0	Blue Data Signal 0 (LSB)	
22	B1	Blue Data Signal 1	
23	B2	Blue Data Signal 2	
24	B3	Blue Data Signal 3	
25	B4	Blue Data Signal 4	
26	B5	Blue Data Signal 5 (MSB)	
27	VSS	Ground	2)
28	DTMG	Data Enable	
29	VDD	Power Supply	1)
30	VDD	Power Supply	1)
31	VSS	Ground	2)
32	VSS	Ground	2)
33	HR	Horizontally inverted	3)
34	VR	Vertically inverted	3)
35	NTC+	Temperature Sensor Pos	
36	NTC-	Temperature Sensor Neg	
37	BRT+	Brightness Sencor Pos	
38	BRT-	Brightness Sencor Neg	

Notes 1) All VDD pins shall be connected to +5.0V(Typ.).

2) All VSS pins shall be grounded. Metal bezel is internally connected to VSS.

3) HR, VR signal change isn't allowed during TFT Module power on.

5.2 BACK-LIGHT UNIT

(Connector 2:JST BHR-03VS-1)

Pin No.	SYMBOL	Function	Note
1	VL	Power Supply (High Voltage)	
2	NC	No Connection	
3	VL	Power Supply (Low Voltage)	

RELATIONSHIP BETWEEN DISPLAY COLORS AND INPUT SIGNALS

Color \ Input		R Data						G Data						B Data					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
		MSB					LSB	MSB					LSB	MSB					LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	:	:		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Blue(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
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	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Notes 1) Definition of gray scale:

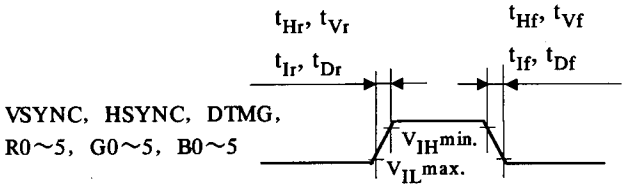
Color(n) · · · · Number in parenthesis indicates gray scale level.
Larger n corresponds to brighter level.

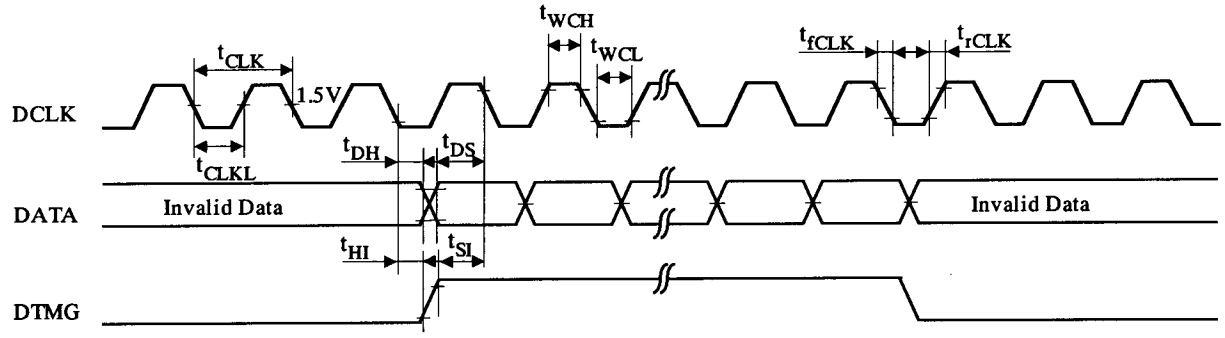
2) Data: 1:High, 0:Low

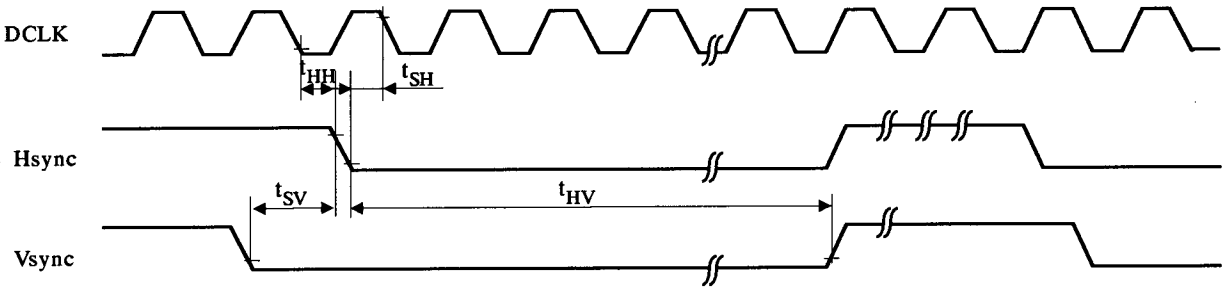
6. INTERFACE TIMING

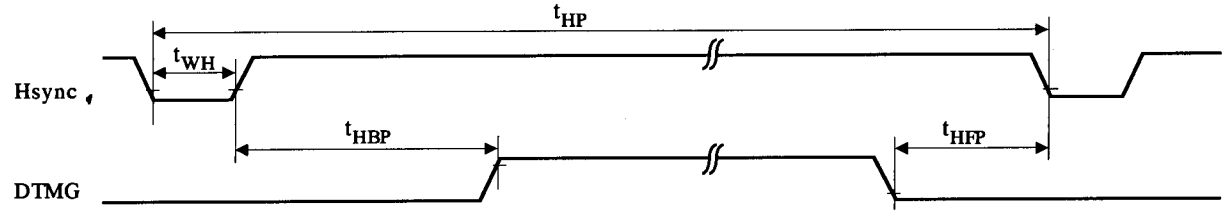
6.1 TIMING CHART

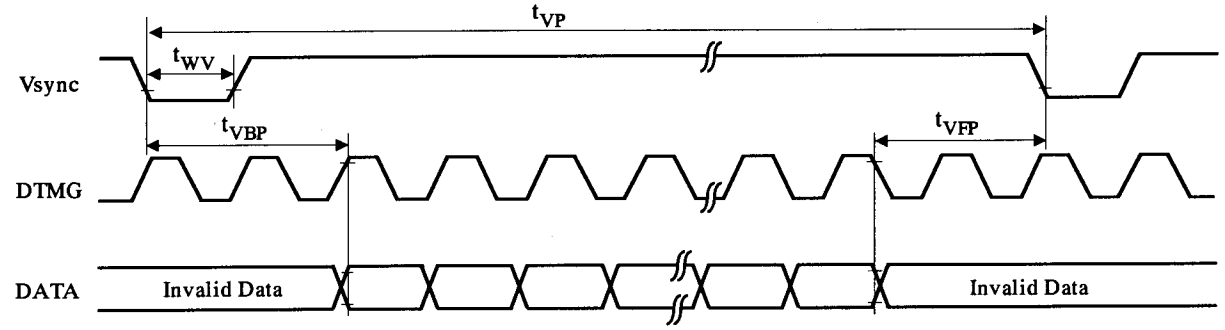
(Data : Latched at Fall edge of DCLK)







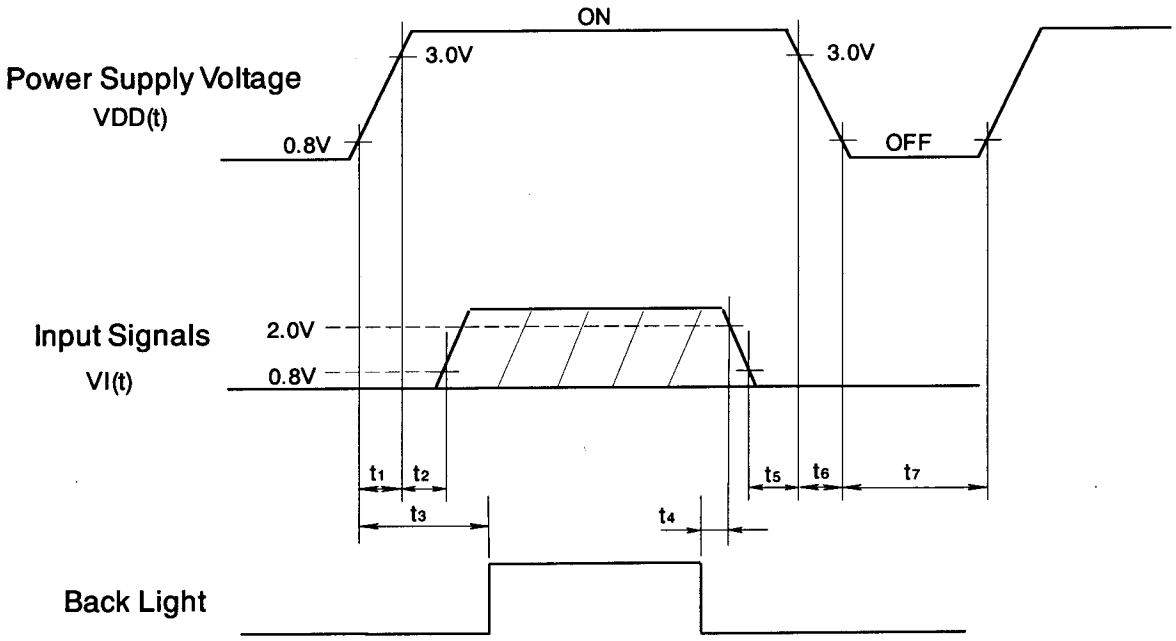




6.2 INTERFACE TIMING SPECIFICATIONS

Item		Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Period	t_{CLK}	7	11	25	MHz	
	Width-Low	t_{WC}	12	—	—	ns	
	Width-Hi	t_{WCH}	12	—	—		
	Rise Time	t_{rCLK}	—	—	25		
	Fall Time	t_{fCLK}	—	—	25		
	Duty	D	0.45	0.5	0.55	—	$D=t_{CLKL}/t_{CLK}$
Hsync	Set up Time	t_{SH}	5	—	—	ns	for DCLK
	Hold Time	t_{HH}	10	—	—		
	Period	t_{HP}	545	650	1300	t_{CLK}	
	Width-Active	t_{WH}	4	6	—		
	Rise/Fall Time	t_{Hr},t_{Hf}	—	—	30	ns	for DCLK
Vsync	Set up Time	t_{SV}	0	—	—	t_{CLK}	for Hsync
	Hold Time	t_{HV}	2	—	—		
	Period	t_{VP}	265	270	1023	t_{HP}	
	Width-Active	t_{WV}	3	3	3		
	Rise/Fall Time	t_{Vr},t_{Vf}	—	—	50	ns	for DCLK
DTMG	Set up Time	t_{SI}	5	—	—	ns	for DCLK
	Hold Time	t_{HI}	10	—	—		
	Rise/Fall Time	t_{Ir},t_{If}	—	—	30	ns	
	Horizontal Back porch	t_{HBP}	7	48	—	t_{CLK}	
	Horizontal Front porch	t_{HFP}	—	116	—		
	Vertical Back porch	t_{VBP}	21	21	21	t_{HP}	
	Vertical Front porch	t_{VFP}	—	15	—		
DATA	Set up Time	t_{DS}	5	—	—	ns	for DCLK
	Hold Time	t_{DH}	10	—	—		
	Rise/Fall Time	t_{Dr},t_{Df}	—	—	25	ns	

6.3 TIMING BETWEEN INTERFACE SIGNALS AND POWER SUPPLY



POWER ON

$t_1 \leqq 15ms$

$0ms < t_2 \leqq 45ms$

$100ms \leqq t_3$

POWER OFF

$5ms \leqq t_4$

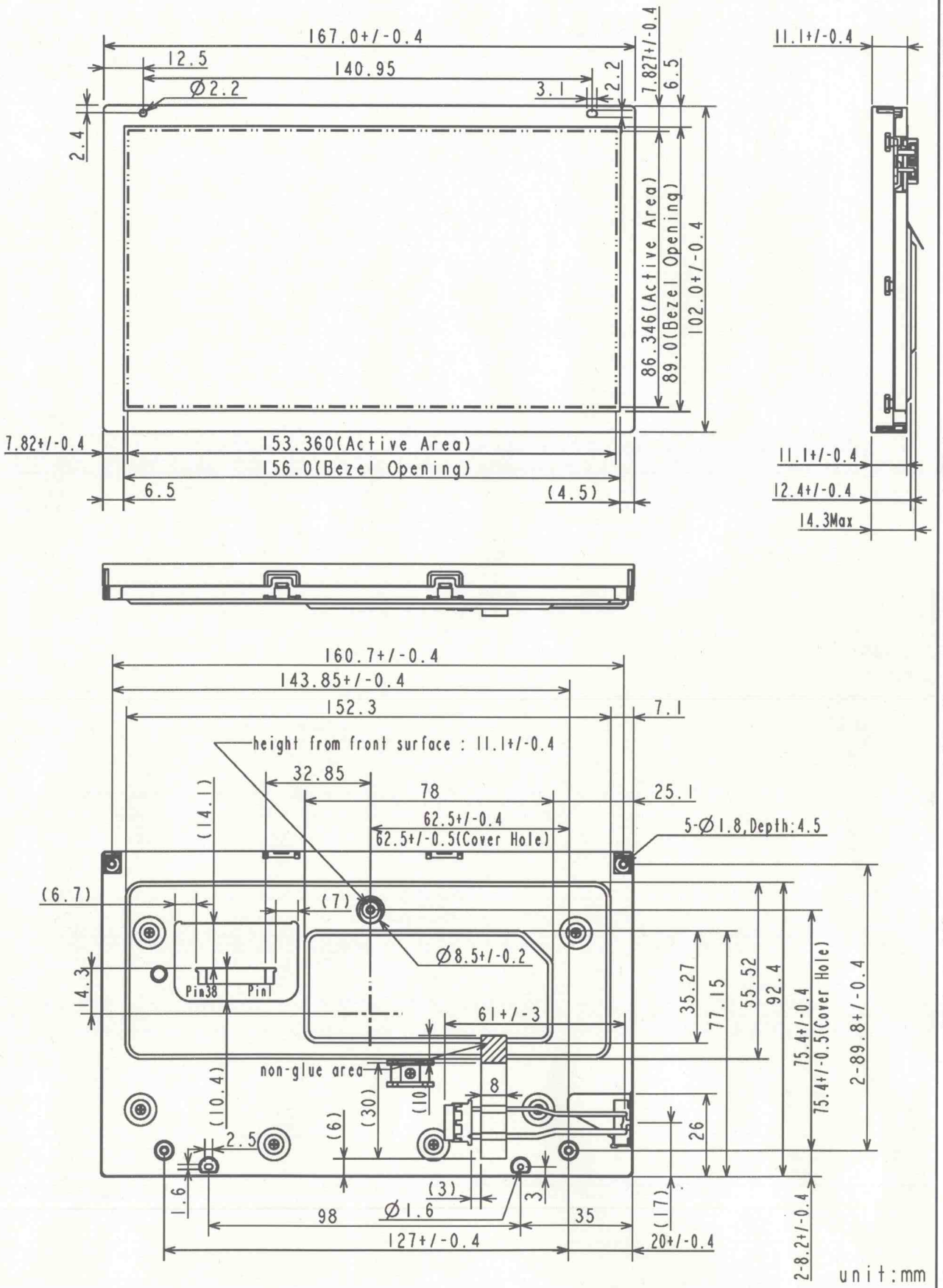
$0ms \leqq t_5 \leqq 45ms$

$0ms \leqq t_6 \leqq 20ms$

$400ms \leqq t_7$

Note 1) Set $0V \leqq VI(t) \leqq VDD(t)$.
Here, VI(t), VDD(t) indicate the transitional state of VI, VDD when power supply is turned ON or OFF.
2) Do not keep interface signal high-impedance when power on.

Outline Dimensions



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