

Specification

TX

Spec No: TX

Date: th, 2012

HITACHI

KAOHSIUNG HITACHI ELECTRONICS CO., LTD.

CUSTOMER'S ACCEPTANCE SPECIFICATIONS

TX23D86VM0BAA

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ACCEPTED BY:	PROPOSED BY:	Lenken
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2. REC	CORD OF I	REVISI	ON				
DATE	SHEET No	o.		S	SUMMARY		
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KAOHSIU ELECTRON	NG HITACHI ICS CO., LTD.	SHEET NO.	7B64F	S 2702-TX2	3D86VM0BAA-1	PAGE	2-1/1

3. GENERAL DATA

3.1 DISPLAY FEATURES

This module is a 9" WXGA of 16:9 format amorphous silicon TFT. The pixel format is vertical stripe and sub pixels are arranged as R(red), G(green), B(blue) sequentially. This display is RoHS compliant, and COG (chip on glass) technology and LED backlight are applied on this display.

Part Name	TX23D86VM0BAA
Module Dimensions	216.0(W) mm x 142.0(H) mm x 11.7 (D) mm
LCD Active Area	193.920(W) mm x 116.352(H) mm
Pixel Pitch	0.1515(W) mm x 0.1515(H) mm
Resolution	1280 x 3(RGB)(W) x 768(H) dots
Color Pixel Arrangement	R, G, B Vertical stripe
LCD Type	Transmissive Color TFT; Normally Black
Display Type	Active Matrix
Number of Colors	16.7M Colors(6-bit + FRC)
Backlight	White LED
Weight	380g (typ.)
Interface	1ch-LVDS/Receiver ; 30 pins
Power Supply Voltage	3.3V for LCD; 12V for Backlight
Power Consumption	2.31 W for LCD ; 5.76W for backlight
Viewing Direction	Super Wide Version (In Plane Switching)

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	VDD	0	4.0	>	-
Input Voltage of Logic	VI	-0.3	VDD+0.3	>	Note 1
Operating Temperature	Тор	-20	70	°C	Note 2
Storage Temperature	Tst	-30	80	°C	Note 2
Backlight Input Voltage	VLED	-	15	٧	-

- Note 1: The rating is defined for the signal voltages of the interface such as CLK, and pixel data pairs.
- Note 2: The maximum rating defined as above is based on the chamber temperature, which might be different from ambient temperature after assembling the panel into the application. Moreover, some temperature-related phenomenon as below needed to be noticed:
 - Background color, contrast and response time would be different in temperatures other than $25\,^{\circ}\mathrm{C}_{\,\cdot}$
 - Operating under high temperature will shorten LED lifetime.

5. ELECTRICAL CHARACTERISTICS

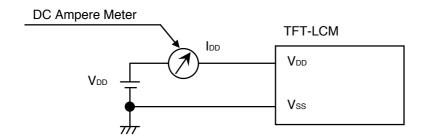
5.1 LCD CHARACTERISTICS

 $T_a = 25$ °C, VSS = 0V

Item	Symbol	Condition	Min.	Тур.	Max.	Unit	Remarks
Power Supply Voltage	VDD	-	3.0	3.3	3.6	V	-
Differential Input Voltage for LVDS Receiver Threshold	VI	"H" level	-	-	+100	mV	VCM
		"L" level	-100	-	-		=1.2V
Power Supply Current	IDD	VDD=3.3V	-	700	-	mA	Note 1,2
Vsync Frequency	f_v	-	ı	60	65	Hz	Note 3
Hsync Frequency	$f_{\scriptscriptstyle H}$	-	ı	49.5	ı	KHz	Note 3
DCLK Frequency	$f_{\it CLK}$	-	71.4	74.25	77.5	MHz	Note 3

Note 1: fV=60Hz, fCLK=74.25MHz, VDD=3.3V, DC Current.

Typical value is measured when displaying vertical 256 gray scale. Maximum is measured when displaying Vertical-stripe.



Note 2: 1.6A fuse is applied in the module for IDD. For display activation and protection purpose, power supply is recommended larger than 4.0A to start the display and break fuse once any short circuit occurred.

Note 3: For LVDS Transmitter Input

5.2 BACKLIGHT CHARACTERISTICS

Item	Symbol	Condition	Min.	Тур.	Max.	Unit	Remarks
LED Input Voltage	VLED	-	10.8	12.0	13.2	V	-
LED Forward Current	ILED	-	-	480	-	mA	Note1
PWM Frequency	fPWM	-	0.2	-	10.0	kHz	-
PWM Signal Voltage	VPH	High	3.1	3.3	-	V	-
	VPL	Low	-	0	0.8	V	-
PWM Duty	DPWM	-	1	-	100	%	-
LED lifetime	-	480 mA	-	70K	-	hrs	Note 2

- Note 1: LED current is constant, 480 mA, controlled by the LED driver when applying 12V VLED.
- Note 2: The estimated lifetime is specified as the time to reduce 50% brightness by applying 480 mA at $25\,^{\circ}\mathrm{C}$.
- Note 3: Dimming function can be obtained by applying DC voltage or PWM signal from the display interface CN2. The recommended PWM signal is $0.2K \sim 10K$ Hz with 3.3V amplitude.

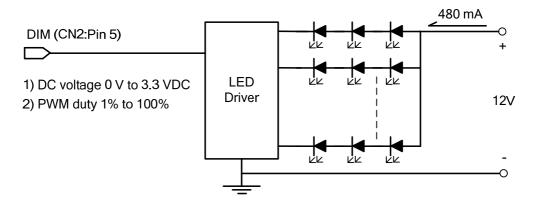


Fig. 5.1

6. OPTICAL CHARACTERISTICS

The optical characteristics are measured based on the conditions as below:

- Supplying the signals and voltages defined in the section of electrical characteristics.
- The backlight unit needs to be turned on for 30 minutes.
- The ambient temperature is 25 $^{\circ}\mathrm{C}\,.$
- In the dark room around 500~1000 lx, the equipment has been set for the measurements as shown in Fig 6.1.

T - 2	25 °C	f	= 60 Hz,	עחח –	3 3V
$I_a = 2$	20 C	, I w	= 00 112,	۷ D =	J.J V

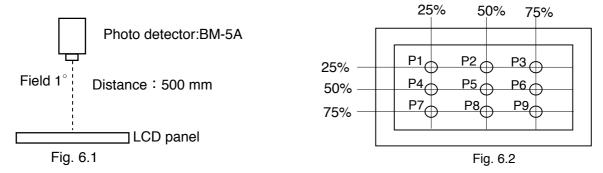
Item Brightness of White Brightness Uniformity Contrast Ratio		Symbol	Condition	Min.	Тур.	Max.	Unit	Remarks
		-	4 00 0 00	200	350	-	cd/m ²	Note 1
		-	$\phi = 0^{\circ}, \theta = 0^{\circ},$ ILED= 480 mA	75	-	-	%	Note 2
		CR	ILED= 480 MA	600	1000	-	-	Note 3
Response	Time	Rise + Fall	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	22	50	ms	Note 4
NTSC R	atio	-	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	72	-	%	-
\(\(\)		θ x	$\phi = 0^{\circ}, CR \ge 10$	-	85	-		
	$\theta x'$		$\phi = 180^{\circ}, CR \ge 10$	-	85	-	D	Note 5
Viewing Angle		θ y	φ = 90°, CR ≥ 10	-	85	-	Degree	
		θ y'	φ = 270°, CR ≥ 10	-	85	-		
	Dod	X		0.595	0.650	0.705		
	Red	Υ		0.275	0.330	0.385		
	0.42.242	X		0.235	0.290	0.345		
Color	Green	Υ		0.535	0.590	0.645		
Chromaticity	Blue	Х	$\phi = 0^{\circ}, \theta = 0^{\circ}$	0.095	0.150	0.205	-	Note 6
	Diue	Υ		0.005	0.060	0.115		
	\\/hito	Х		0.245	0.300	0.355		
	White	Y		0.245	0.300	0.355		

Note 1: The brightness is measured from 9 point of the panel, P1~P9 in Fig. 6.2, for the average value.

Note 2: The brightness uniformity is calculated by the equation as below:

Brightness uniformity =
$$\frac{\text{Min. Brightness}}{\text{Max. Brightness}}$$
 X100%

, which is based on the brightness values of the 9 points measured by BM-5 as shown in Fig. 6.2.

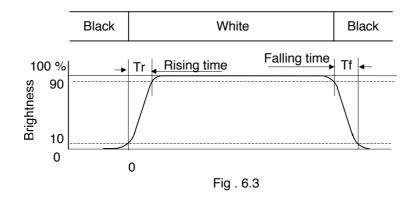


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Note 3: The Contrast ratio is measured from the center point of the panel, P5, and defined as the following equation:

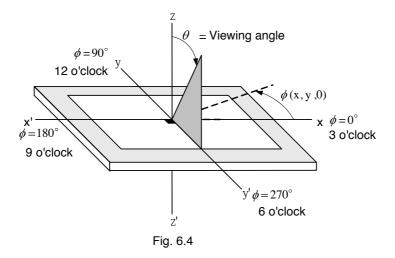
CR = Brightness of White
Brightness of Black

Note 4: The definition of response time is shown in Fig. 6.3. The rising time is the period from 10% brightness to 90% brightness when the data is from white to black. Oppositely, Falling time is the period from 90% brightness rising to 10% brightness.



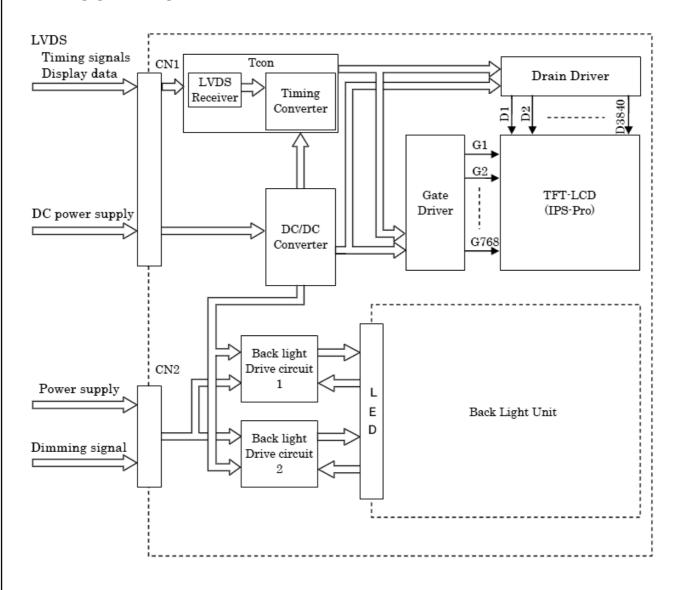
Note 5: The definition of viewing angle is shown in Fig. 6.4. Angle ϕ is used to represent viewing directions, for instance, $\phi = 270^{\circ}$ means 6 o'clock, and $\phi = 0^{\circ}$ means 3 o'clock. Moreover, angle θ is used to represent viewing angles from axis Z toward plane XY.

The display is super wide viewing angle version; 85° viewing angle can be obtained from each viewing direction.



Note 6: The color chromaticity is measured from the center point of the panel, P5, as shown in Fig. 6.2.

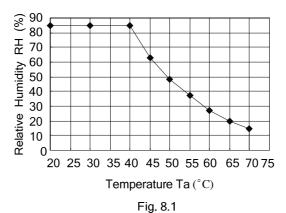
7. BLOCK DIAGRAM



8. RELIABILITY TESTS

Test Item	Condition	
High Temperature	1) Operating 2) 70 °C	240 hrs
Low Temperature	1) Operating 2) -20°C	240 hrs
High Temperature	1) Storage 2) 80 °C	240 hrs
Low Temperature	1) Storage 2) -30 °C	240 hrs
Heat Cycle	1) Operating 2) -20°C ~70°C 3) 3hrs~1hr~3hrs	240 hrs
Thermal Shock	 1) Non-Operating 2) -35 °C ↔ 85 °C 3) 0.5 hr ↔ 0.5 hr 	240 hrs
High Temperature & Humidity	1) Operating2) 40°C & 85%RH3) Without condensation4) Note 3	240 hrs
Vibration	1) Non-Operating 2) 20~200 Hz 3) 2G 4) X, Y, and Z directions	1 hr for each direction
Mechanical Shock	1) Non-Operating 2) 10 ms 3) 50G 4) ±X,±Y and ±Z directions	Once for each direction
ESD	1) Glass: 9 points 2) Metal frame: 8 points	

- Note 1: Display functionalities are inspected under the conditions defined in the specification after the reliability tests.
- Note 2: The display is not guaranteed for use in corrosive gas environments.
- Note 3: Under the condition of high temperature & humidity, if the temperature is higher than 40° C, the humidity needs to be reduced as Fig. 8.1 shown.
- Note 4: All pins of LCD interface (CN1) have been tested by ± 100 V contact discharge of ESD under non-operating condition.



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9. LCD INTERFACE

9.1 INTERFACE PIN CONNECTIONS

The display interface connector is FI-XB30SL-HF10 made by JAE. More details of the connector are shown in the section of outline dimension.

Pin assignment of LCD interface is as below:

Pin No.	Symbol	Description	Note	Pin No.	Symbol	Description	Note
1	VDD			16	RX1+	Pixel Data	4
2	VDD	Power Supply	4	17	VSS	GND (0V)	2
3	VDD	(3.3V)	I	18	RX2-	Divel Date	4
4	VDD			19	RX2+	Pixel Data	4
5	VSS			20	VSS	GND (0V)	2
6	VSS	CND (OV)	2	21	CLK-	Clock	4
7	VSS	GND (0V)	2	22	CLK+	Clock	4
8	VSS			23	VSS	GND (0V)	2
9	TEST1	Toot Din	0	24	RX3-	Pixel Data	4
10	TEST2	Test Pin	3	25	RX3+	Pixei Dala	4
11	VSS	GND (0V)	2	26	VSS	GND (0V)	2
12	RX0-	Divol Data	4	27	TEST3		3
13	RX0+	Pixel Data	4	28	TEST4	Test Pin	3
14	VSS	GND (0V)	2	29	TEST5	I est Fill	3
15	RX1-	Pixel Data	4	30	TEST6		3

Note 1: All VDD pins must be connected to +3.3V.

Note 2: All VSS pins must be connected to GND(0V). Metal bezel is connected internally to VSS.

Note 3: Please keep this pin open.

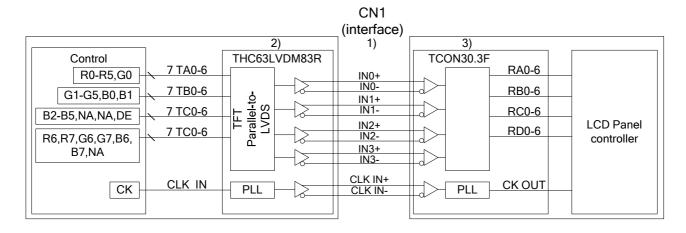
Note 4: In n⁻ and n⁺ (n=0,1,2,3),CLK IN- and CLK IN+ must be wired by twist-pairs or side by side FPC patterns, respectively.

The backlight interface connector is SM08B-SHLS (LF) (SN) made by JST, and pin assignment of backlight is as below:

Pin No.	Signal	Function			
1~3	V_{LED} +	Power Supply for LED (12V)			
4	NC	No Connection			
5	DIM	Backlight Brightness Dimming			
6~8	V _{LED} -	GND (0V)			

Note 1: In case Pin5 is not used, please apply 3.3V.

9.2 LVDS INTERFACE



Note 1: 100 Ω impedance of LVDS cable is recommended for best optical performance.

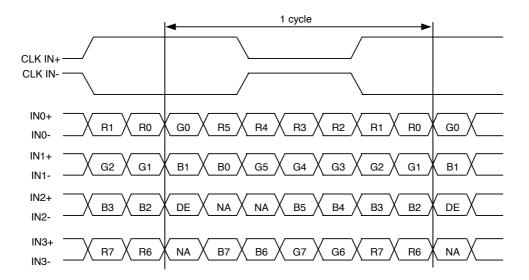
Note 2: Transmitter Made by THine: THC63LVDM83R or equivalent.

Note 3: Receiver (TCON30.3-F) • Made by THine: THC63LVDF84B equivalent.

9.3 DATA MAPPING

Pin No.	Pin name	Data	Pin No.	Pin name	Data
TA0	51	R0(LSB)	TC0	20	B2
TA1	52	R1	TC1	22	В3
TA2	54	R2	TC2	23	B4
TA3	55	R3	TC3	24	B5
TA4	56	R4	TC4	27	(NA)
TA5	3	R5	TC5	28	(NA)
TA6	4	G0(LSB)	TC6	30	DE
TB0	6	G1	TD0	50	R6
TB1	7	G2	TD1	2	R7(MSB)
TB2	11	G3	TD2	8	G6
TB3	12	G4	TD3	10	G7(MSB)
TB4	14	G5	TD4	16	B6
TB5	15	B0(LSB)	TD5	18	B7(MSB)
TB6	19	B1	TD6	25	(NA)

9.4 LVDS DATA FORMAT



DE : Display Enable NA : Not In Use

9.5 INTERFACE TIMING SPECIFICATIONS

The column of timing sets including minimum, typical, and maximum as below are based on the best optical performance, frame frequency (Vsync) = 60 Hz to define. If 60 Hz is not the aim to set, less than 65 Hz for Vsync is recommended to apply for better performance by other parameter combination as the definitions in section 5.1.

	Item		Min.	Тур.	Max.	Unit
	Cycle frequency	1/t _{CLK}	71.4	74.25	77.5	MHz
	Low level width	t _{WCL}	10	-	-	
DCLK	High level width	t _{WCH}	10	-	-	ns
	Rise / Fall time	t_{rCLK} , t_{fCLK}	-	-	12	
	Duty	D	0.45	0.5	0.55	-
	Set up time	t _{SI}	8	-	-]
	Hold time	t _{HI}	8	-	-	ns
	Rise / Fall time	t _{ir} ,t _{if}	-	-	12	ns
	Horizontal cycle	t _H	1450	1500	1550	
DE	Horizontal valid data width	t _{HD}	1280	1280	1280	t _{CLK}
	Horizontal porch width	t _{HB}	170	220	270	
	Vertical cycle	tv	820	825	833	
	Vertical valid data width	t _{VD}	768	768	768	t _H
	Vertical porch width	t _{VB}	52	57	65	
	Set up time	t _{SD}	8	-	-	
Data	Hold time	t _{HD}	8	-	-	ns
	Rise / Fall time	t_{Dr}, t_{Df}	-	-	12	ns

9.6 TIMING CHART

DE (Data Enable) is the signal to determine valid data, and the timing of DE can be determined from Hsync and Vsync as below. For this display, only DE and DCLK are the essential signals. Hsync and Vsync are not necessary to connect to display interface after DE has been generated and input.

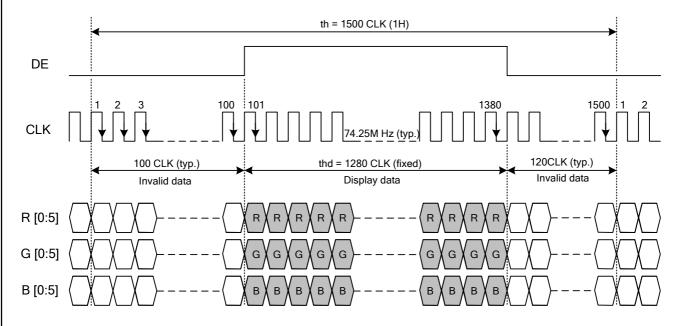


Fig. 9.1 Horizontal Timing

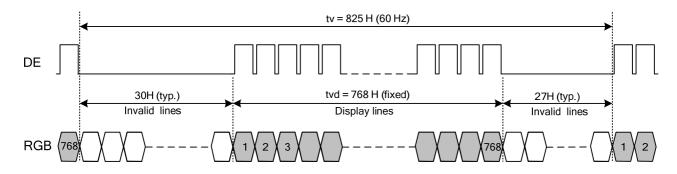
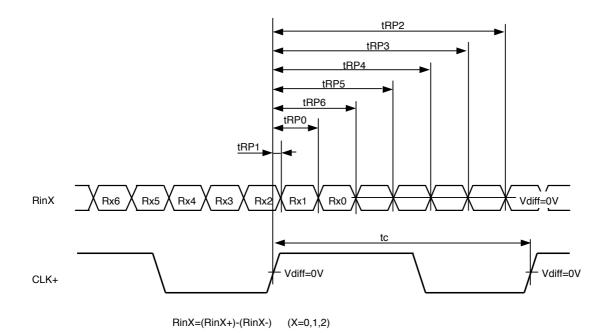


Fig. 9.2 Vertical Timing

9.7 INTERFACE TIMING

(1) LVDS Receiver Timing

(Interface of TFT module)



	Item	Symbol	Min.	Тур.	Max.	Unit
DCLK	Frequency	1/t _{CLK}	71.4	74.25	77.5	MHz
RinX	0 data position	t _{RP0}	1/7t _{CLK} -0.4	1/7*t _{CLK}	1/7t _{CLK} +0.4	
(X=0,1,2)	1st data position	t _{RP1}	-0.4	0	+0.4	
	2nd data position	t _{RP2}	6/7t _{CLK} -0.4	6/7*t _{CLK}	6/7t _{CLK} +0.4	
	3rd data position	t _{RP3}	5/7t _{CLK} -0.4	5/7*t _{CLK}	5/7t _{CLK} +0.4	ns
	4th data position	t _{RP4}	4/7t _{CLK} -0.4	4/7*t _{CLK}	4/7t _{CLK} +0.4	
	5th data position	t _{RP5}	3/7t _{CLK} -0.4	3/7*t _{CLK}	3/7t _{CLK} +0.4	
	6th data position	tppe	2/7tcur-0.4	2/7*t _{CLK}	2/7tc.r+0.4	1

9.8 DATA INPUT for DISPLAY COLORS

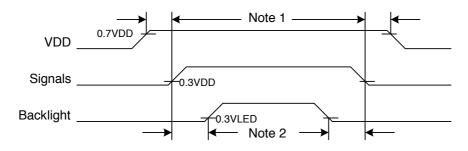
					Red	Data	ı					G	ireen	Dat	а					ı	Blue	Data	ì		
Input	,	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	В6	B5	B4	В3	B2	B1	В0
color	r	MSB							LSB	MSB							LSB	MSB							LSB
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Basic	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Color	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Red	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	•	:	•	:	:	:	:	:	:
	:	:	•	:	:	:	:	:	:	:	:	:	:	•	:	:	•	:	•	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Green	:	:	:	:	:	:	:	:	:	:	••	:	:	:	:	;	•	;	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)		0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254) Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			0	0	0		0			0			0			0	0	0	0	0	0	0	0		
	Blue(1) Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	: :	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	
Blue		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	•	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
L N	nte 1: Def																								

Note 1: Definition of gray scale : Color(n) Number in parenthesis indicates gray scale level. Larger number corresponds to brighter level.

Note 2: Data Signal : 1 : High, 0 : Low

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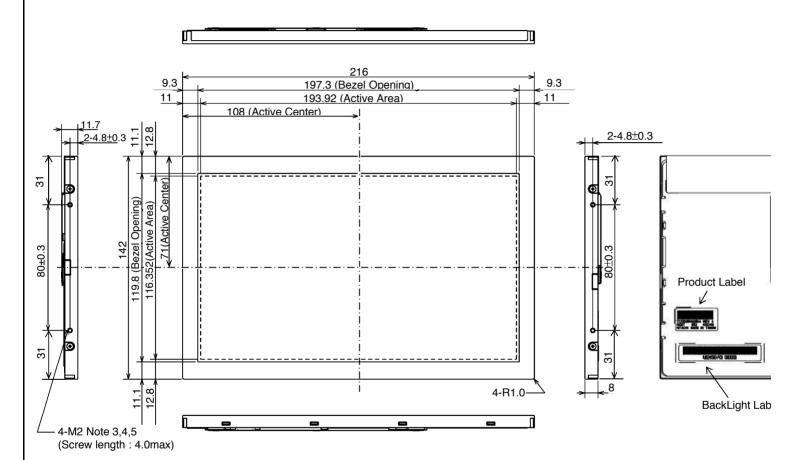
9.9 POWER SEQUENCE



Power Sequence Timing

- Note 1: In order to avoid any damages, VDD has to be applied before all other signals. The opposite is true for power off where VDD has to be remained on until all other signals have been switch off. The recommended time period is 1 second. Hot plugging might cause display damage due to incorrect power sequence, please pay attention on interface connecting before power on.
- Note 2: In order to avoid showing uncompleted patterns in transient state. It is recommended that switching the backlight on is delayed for 1 second after the signals have been applied. The opposite is true for power off where the backlight has to be switched off 1 second before the signals are removed.

10. OUTLINE DIMENSIONS



Note 1: Interface connector (CN1)

JAE: F1 - XB30SL - HF10 or equivalent.

Note 2: Backlight connector (CN2)

JST: SM08B - SHLS (LF) (SN)

Note 3: The unspecified tolerance: ±0.5.

Note 4: Fixation mounting hole: Each 2 points on right and left side (total 4 points)

Note 5: Maximum torque for screw: 0.196N • M (2kgf • cm)

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11. APPEARANCE STANDARD

The appearance inspection is performed in a dark room around 500lx~1000lx based on the conditions as below:

- The distance between inspector's eyes and display is 30 cm.
- The viewing zone is defined with angle θ shown in Fig. 11.1 The inspection should be performed within 45° when display is shut down. The inspection should be performed within 5° when display is power on.

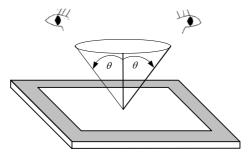


Fig. 11.1

11.1 THE DEFINITION OF LCD ZONE

LCD panel is divided into 3 areas as shown in Fig.11.2 for appearance specification in next section. A zone is the LCD active area (dot area); B zone is the area, which extended 1 mm out from LCD active area; C zone is the area between B zone and metal frame.

In terms of housing design, B zone is the recommended window area customers' housing should be located in.

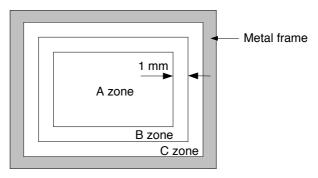


Fig. 11.2

11.2 LCD APPEARANCE SPECIFICATION

The specification as below is defined as the amount of unexpected phenomenon or material in different zones of LCD panel. The definitions of length, width and average diameter using in the table are shown in Fig. 11.3 and Fig. 11.4.

Item			Cri	teria			Applied zone		
	Length (mm)	Widtl	h (mm)	Maximum nu	umber	Minimum space			
	Ignored	W≦	≦0.01	Ignored	t	-			
	L≦40	W≦	≦0.02	10		-			
0	L≦20	W≦	<u></u> 0.04	10		-	A D		
Scratches		Α、B							
	Average diameter	(mm)	Maxim	um number	Mir	nimum space			
	D≦0.2		ļ	gnore		-			
	D≦0.4			10		-			
Dent		Se	erious one	is not allowed			Α		
Wrinkles in polarizer		Se	erious one	is not allowed			Α		
	Average diam	eter (m	nm)	Max	kimum n	umber			
Bubbles on polarizer	D≦0.	.3			Ignore	d	Α		
Dubbles on polarizer	D≦0.	.5			10		^		
	D≦1.	.0			5				
	Length (mm)		Widtl	n (mm)	Max	imum number			
	Ignored		W≦	_0.02		Ignored	Α·Β		
	L≦2.0		W≦	≦0.03		10			
1) Ctains	L≦1.0		W≦	≦0.06		10			
Stains Foreign Materials									
3) Dark Spot	Average diameter (n	nm)	Maximu	m number	Min	imum Space			
o) Dark Spot	D≦0.22		lgn	ored		-			
	D≦0.33			5		-	Α·Β		
	D>0.33			0	-				
	In total								
		Those	wiped out e	asily are accept	able				
			T	ype	Max	imum number			
			1	dot		4			
			2 adja	cent dot		1			
	Bright dot-defect	: 3	3 adjacent	dot or above	N	lot allowed			
			De	nsity	:	2/φ 20mm			
Dot-Defect			In	total		5	Α		
(Note 1)			1	dot		5	^		
			2 adja	cent dot		2			
	Dark dot-defect	3	3 adjacent	dot or above	N	lot allowed			
			De	nsity	;	3/φ 20mm			
			In	total		5			
		In tot	al			10			

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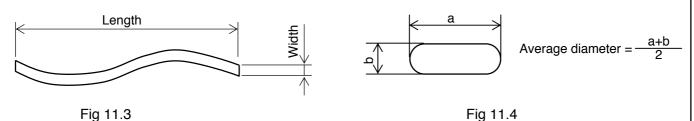


Fig 11.3

Note 1: The definitions of dot defect are as below:

- The defect area of the dot must be bigger than half of a dot.
- For bright dot-defect, showing black pattern, the dot's brightness must be over 30% brighter than others.
- For dark dot-defect, showing white pattern, the dot's brightness must be under 70% darker than others.
- The definition of 1-dot-defect is the defect-dot, which is isolated and no adjacent defect-dot.
- The definition of adjacent dot is shown as Fig. 11.5.
- The Density of dot defect is defined in the area within diameter ϕ =20mm.

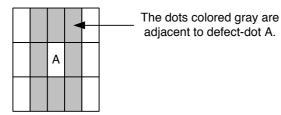


Fig. 11.5

12. PRECAUTIONS

12.1 PRECAUTIONS OF ESD

- 1) Before handling the display, please ensure your body has been connected to ground to avoid any damages by ESD. Also, do not touch display's interface directly when assembling.
- 2) Please remove the protection film very slowly before turning on the display to avoid generating ESD.

12.2 PRECAUTIONS OF HANDLING

- 1) In order to keep the appearance of display in good condition, please do not rub any surfaces of the displays by sharp tools harder than 3H, especially touch panel, metal frame and polarizer.
- 2) Please do not pile the displays in order to avoid any scars leaving on the display. In order to avoid any injuries, please pay more attention for the edges of glasses and metal frame, and wear finger cots to protect yourself and the display before working on it.
- 3) Touching the display area or the terminal pins with bare hand is prohibited. This is because it will stain the display area and cause poor insulation between terminal pins, and might affect display's electrical characteristics furthermore.
- 4) Do not use any harmful chemicals such as acetone, toluene, and isopropyl alcohol to clean display's surfaces.
- 5) Please use soft cloth or absorbent cotton with ethanol to clean the display by gently wiping. Moreover, when wiping the display, please wipe it by horizontal or vertical direction instead of circling to prevent leaving scars on the display's surface, especially polarizer.
- 6) Please wipe any unknown liquids immediately such as saliva, water or dew on the display to avoid color fading or any permanently damages.
- 7) Maximum pressure to the surface of the display must be less than $1,96 \times 10^4$ Pa. If the area of adding pressure is less than $1 \, \text{cm}^2$, the maximum pressure must be less than 1.96×10^4 Pa.

12.3 PRECAUTIONS OF OPERATING

- 1) Please input signals and voltages to the displays according to the values defined in the section of electrical characteristics to obtain the best performance. Any voltages over than absolute maximum rating will cause permanent damages to this display. Also, any timing of the signals out of this specification would cause unexpected performance.
- 2) When the display is operating at significant low temperature, the response time will be slower than it at $25\,\mathrm{C}^\circ$. In high temperature, the color will be slightly dark and blue compared to original pattern. However, these are temperature-related phenomenon of LCD and it will not cause permanent damages to the display when used within the operating temperature.
- 3) The use of screen saver or sleep mode is recommended when static images are likely for long periods of time. This is to avoid the possibility of image sticking.
- 4) Spike noise can cause malfunction of the circuit. The recommended limitation of spike noise is no bigger than ± 100 mV.

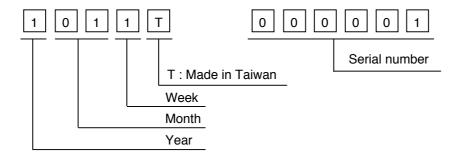
12.4 PRECAUTIONS OF STORAGE

If the displays are going to be stored for years, please be aware the following notices.

- 1) Please store the displays in a dark room to avoid any damages from sunlight and other sources of UV light.
- 2) The recommended long term storage temperature is between 10 °C ~35 °C and 55%~75% humidity to avoid causing bubbles between polarizer and LCD glasses, and polarizer peeling from LCD glasses.
- 3) It would be better to keep the displays in the container, which is shipped from Hitachi, and do not unpack it.
- 4) Please do not stick any labels on the display surface for a long time, especially on the polarizer.

13. DESIGNATION of LOT MARK

1) The lot mark is showing in Fig.13.1. First 4 digits are used to represent production lot, T represented made in Taiwan, and the last 6 digits are the serial number.



2) The tables as below are showing what the first 4 digits of lot mark are shorted for.

Year	Mark
2011	1
2012	2
2013	3
2014	4
2015	5

Month	Mark	Month	Mark
1	01	7	07
2	02	8	08
3	03	9	09
4	04	10	10
5	05	11	11
6	06	12	12

Week (Days)	Mark	
1~7	1	
8~14	2	
15~21	3	
22~28	4	
29~31	5	

- 3) Except letters I and O, revision number will be shown on lot mark and following letters A to Z.
- 4) The location of the lot mark is on the back of the display shown in Fig. 13.1.



Fig 13.1