HITACHI

Electron Tube & Devices
Division, Hitachi, Ltd.

Date; Jun. 05, '97

TECHNICAL DATA

TENTATIVE

TX31D62VC1CAA

3284TTD 0572-1

CONTENTS

Note) The information contained herein is tentative and may be changed without prior notice due to development stage.
Consequently it is better to contact to Hitachi before proceeding with the design of your product in corporating this TFT-LCD Module.

RECORD OF REVISION

Date	Sheet No.	Summary

APPLICATIONS

This specification is applied to the following TFT Liquid Crystal Display Module with Back-light unit and LVDS (Low Voltage Differential Signaling) Interface.

Note : Inverter device for Back-light is not built in so it should be prepared by yourself.

• Type name	: TX31D62VC1CAA
• Display Area	: H245.8×V184.3[mm]
• Display Dots (Display Pixels)	: H(1024×3)×V768 [dots] (H1024×V768 pixels)
• Pixel Pitch	: H 0.24×V 0.24[mm]
• Color Pixel Arrangement	: R•G•B Vertical Stripe
• Display Mode	: Transmissive Mode Normally White Mode
• Color Number	: 262k Colors
• Dimensions Outlines	: H275.5(typ.)×V199(typ.)t7(max.)[mm]
• Weight	: Approximately 470 [g]
• Power Supply	: 3.3V
• Interface	: LVDS Receiver SN75LVDS86 in Module.

1. ABSOLUTE MAXIMUM RATINGS

1.1 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

ITEM	OPERATING		STORAGE		UNIT	NOTE
	MIN.	MAX.	MIN.	MAX.		
Ambient Temperature	10	40	−20	60	℃	1)
Humidity	2)		2)		—	1)
Vibration	—	4.9 (0.5G)	—	19.6 (2G)	m/s2	3)
Shock	—	29.4(3G)	—	490 (50G)		4)
Corrosive Gas	NOT ACCEPTABLE		NOT ACCEPTABLE		—	
Illuminance of LCD surface	—	50,000	—	50,000	lx	

Note 1) Environmental temperature and humidity of this unit, not of system installed with this unit.
At low temperature the brightness of CFL drop and the life time of CFL become to be short.

2) Ambient temp. Ta≦40℃ : 85%RH MAX. without condensation
Ta>40℃ : Absolute humidity must be lower than the humidity of 85%RH at 40℃. without condensation

3) 20~50Hz.

4) 7ms.

1.2 ELECTRICAL ABSOLUTE MAXIMUM RATINGS

(1) TFT LIQUID CRYSTAL DISPLAY MODULE

Vss=0V

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTE
Power Supply Voltage	VDD	0	4.0	V	
Input Voltage	VI	− 0.2	VDD+0.2	V	
Electrostatic Durability	VESD0	±100		V	1), 2)
	VESD1	± 8		kV	1), 3)

Note 1) 200pF-250Ω, 25℃-70%RH.
2) I/F Connector pins are subjected.
3) The Surface of Metal bezel and LCD are subjected.

(2) BACK-LIGHT UNIT

GND=0V

ITEM	SYMBOL	MIN.	MAX.	UNIT
Lamp Current	IL	0	5.5	mArms
Lamp Voltage	VL	0	2000	Vrms

2. OPTICAL CHARACTERISTICS

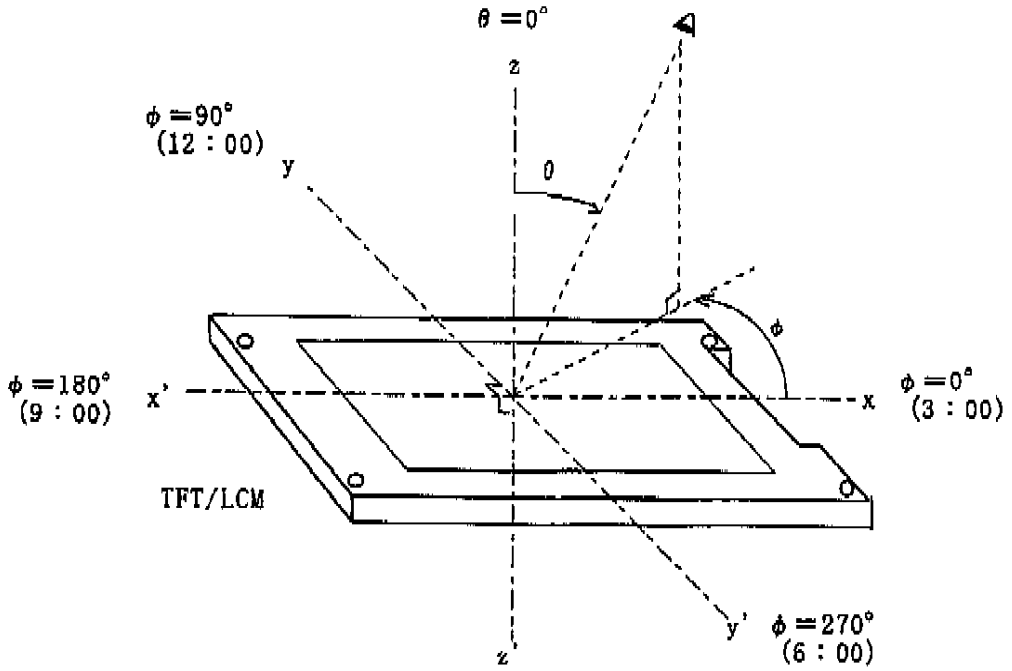
The following items are measured when the conditions of this unit (TFT panel and Back-light) and measuring systems are stable.
The ambient light excluding Back-light is nothing.

- Measuring equipment : TOPCON BM-7, Prichard 1980A, or equivalent

Temperature of LCD=25℃, VDD=3.3V, fV=60Hz, IL=3.1mA

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Contrast Ratio		CR		30	80	—	—	2)
Response Time	RISE	tr		—	40	90	ms	3)
	FALL	tf		—	20	60		
Brightness(White)		Twh		50	70	—	cd/m²	
Color of CIE	Red	x	θ =0° Note 1)	—	(0.54)	—	—	
		y			(0.34)	—		
	Green	x		—	(0.28)	—		
		y			(0.52)	—		
	Blue	x		—	(0.15)	—		
		y			(0.16)	—		
	White	x		—	(0.30)	—		
		y			(0.33)	—		

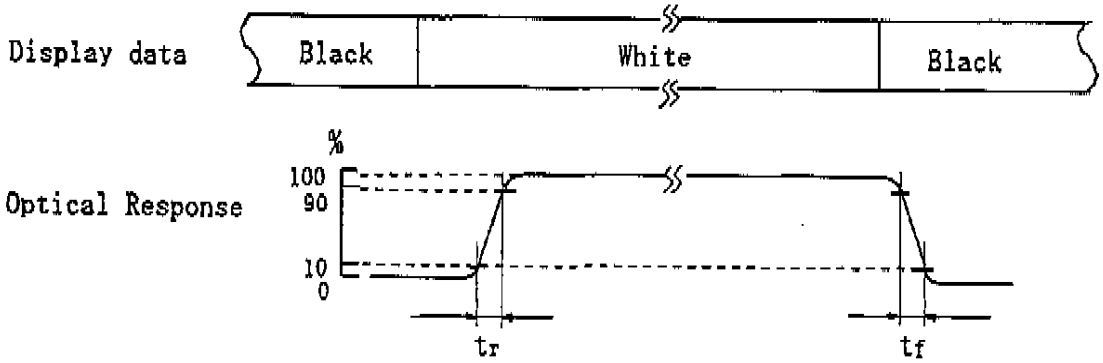
Note 1) Definition of Viewing Angle



Note 2) Definition of Contrast Ratio (CR)

$$CR = \frac{\text{Brightness when displaying White raster}}{\text{Brightness when displaying Black raster}}$$

Note 3) Definition of Response Time



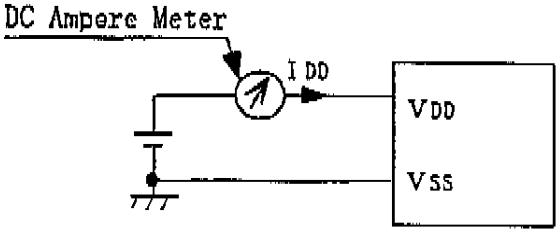
3. ELECTRICAL CHARACTERISTICS

(1) TFT LIQUID CRYSTAL DISPLAY MODULE

Ta=25℃, Vss=0V

ITEM		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Power Supply Voltage		V_{DD}	3.0	3.3	3.6	V	
Differential Input Voltage for LVDS Receiver Threshold	Hi	V_{IH}	—	—	+100	mV	1)
	Lo	V_{IL}	-100	—	—		
Power Supply Current		I_{DD}	—	350	630	mA	2), 3)
Vsync Frequency		f_V	59	60	65	Hz	4)
Hsync Frequency		f_H	45.5	48.4	52.1	kHz	4)
DCLK Frequency		f_{CLK}	60	65	68	MHz	4)

Note 1) VCM=+1.125 ~ +1.375V
2) fv=60Hz, f_{CLK}=65MHz, V_{DD}=3.3V, DC Current.



Typical value is measured when displaying Black raster.
Maximum value is measured when displaying Vertical-stripe pattern

3) As this module contains current fuse, prepare current source that is enough for cutting current fuse when a truble happens.
4) For LVDS Transmitter Input

(2) BACK-LIGHT UNIT

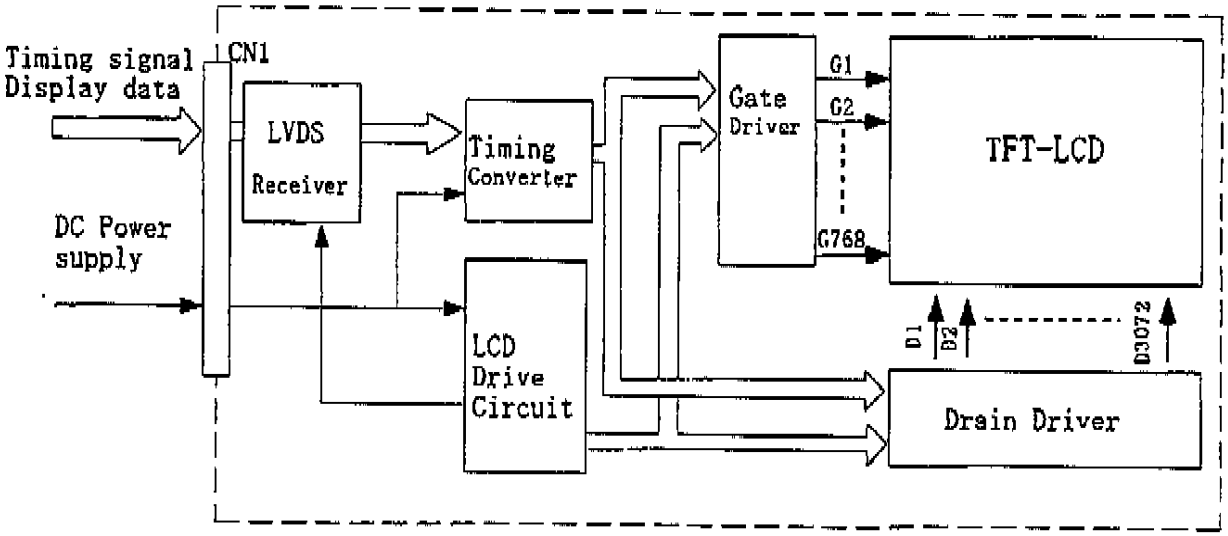
Ta=25℃

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Lamp Current	I_L	—	3.1	5.0	mArms	1)
		—	—	7.0	mA0-peak	
Lamp Voltage	V_L	—	590	—	Vrms	
Frequency	f_L	—	(50)	—	kHz	2)
Starting Lamp Voltage	V_S	930	—	—	Vrms	3)
		1620	—	—		3), 4)

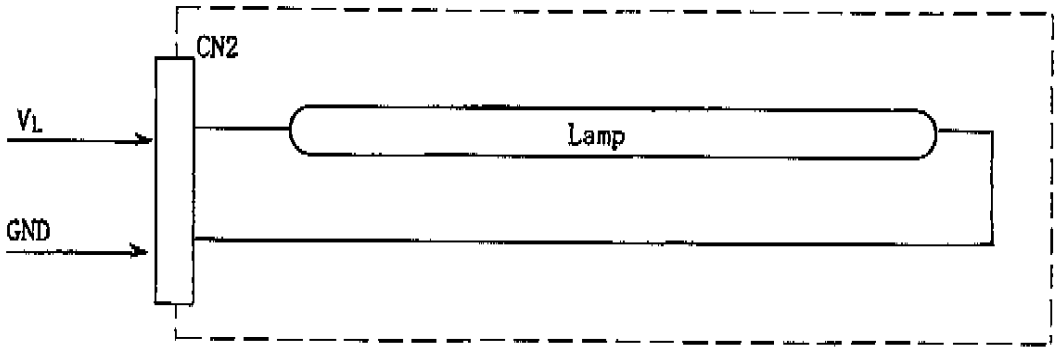
Note 1) Higher I_L cause the short life time of CFL.
2) Lamp frequency may produce interference with Hsync frequency, causing beat or flicker on the display. Therefore lamp frequency shall be as different as possible from Hsync frequency, to avoid interference.
3) Lamp voltage when starting lamp.
4) Ta=10℃

4. BLOCK DIAGRAM

(1) TFT LIQUID CRYSTAL DISPLAY MODULE



(2) BACK-LIGHT UNIT



5. INTERFACE PIN CONNECTION

(1) TFT LIQUID CRYSTAL DISPLAY MODULE

CN1

Pin No	SYMBOL	DESCRIPTION	NOTE
1	—	—	3)
2	—		
3	—		
4	VDD	Power Supply (Typ. +3.3V)	2)
5			
6			
7	CLK IN+	Pixel Clock	
8	CLK IN−		
9	VSS	GND (0V)	1)
10	IN0+	Pixel Data	
11	IN0−		
12	VSS	GND (0V)	1)
13	IN1+	Pixel Data	
14	IN1−		
15	VSS	GND (0V)	1)
16	IN2−	Pixel Data	
17	IN2+		
18	VSS	GND (0V)	1)
19	—	—	3)
20	—		
21	VSS	GND (0V)	1)

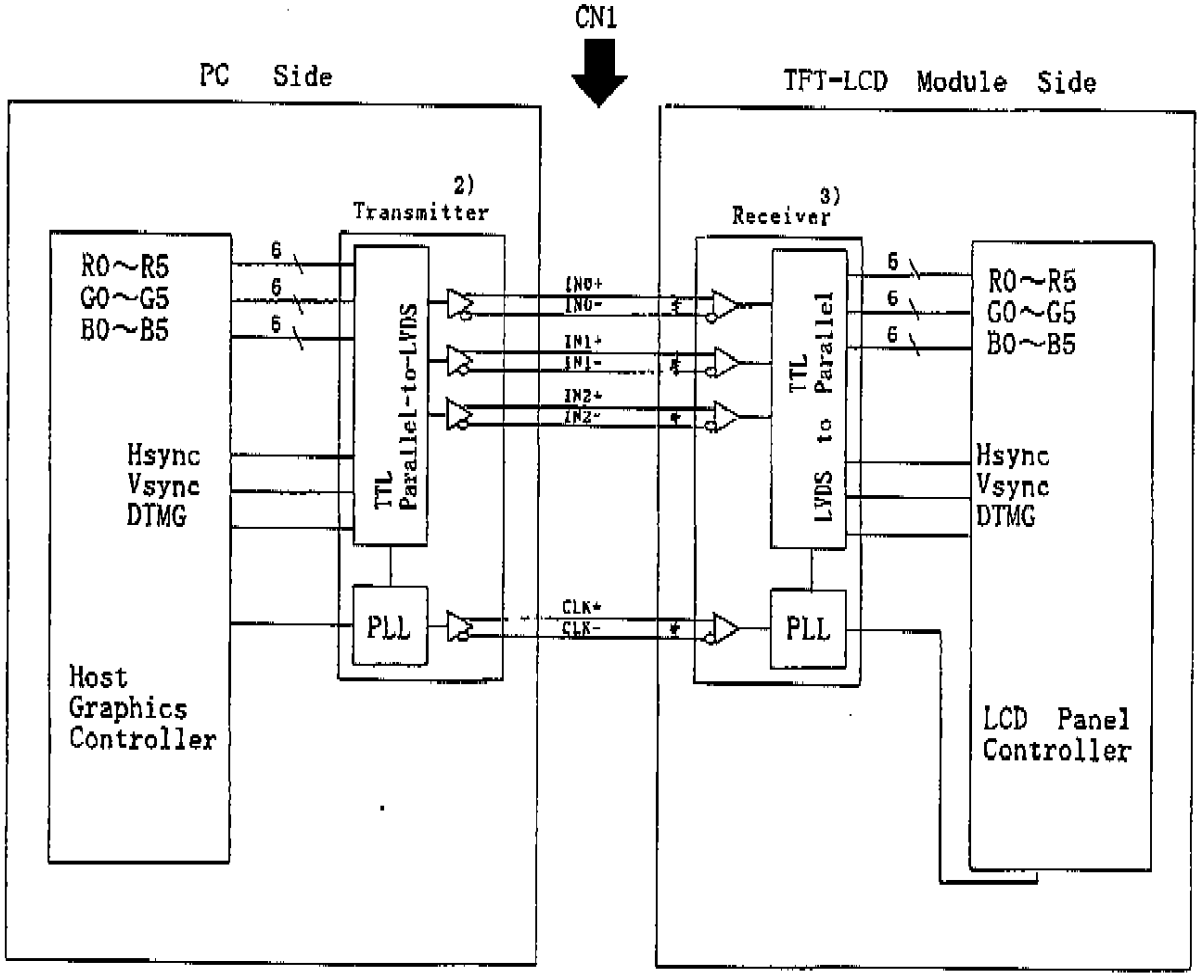
Note 1) All Vss pins should be connected to GND (0V).
Metal bezel is connected internally to Vss.
2) All V_{DD} pins should be connected to V_{DD} (Typ. +3.3V).
3) Don't use. Keep open.

(2) BACK-LIGHT UNIT

CN2

Pin No	SYMBOL	DESCRIPTION
1	V_L	Power Supply
2	(NC)	
3	GND	GND (0V)

LVDS INTERFACE



NOTE: 1) LVDS cable impedance is 50 ohms per signal line or about 100 ohms when two are used differentially.

2) LVDS Transmitter : SN75LVDS84, SN75LVDS81

3) LVDS Receiver : SN75LVDS86 (in Module)

INPUT SIGNAL FOR LVDS

	INPUT SIGNAL	TRANSMITTER SN75LVDS81	TRANSMITTER SN75LVDS84	INTERFACE CONNECTOR (CN1)		Receiver SN75LVDS86
				PC	TFT-LCD	
LVDS	R0	IN0	IN0 (44)	OUT0+	IN0+	OUT0
	R1	IN1	IN1 (45)			OUT1
	R2	IN2	IN2 (47)			OUT2
	R3	IN3	IN3 (48)			OUT3
	R4	IN4	IN4 (1)			OUT4
	R5	IN6	IN5 (3)	OUT0-	IN0-	OUT5
	G0	IN7	IN6 (4)			OUT6
	G1	IN8	IN7 (6)	OUT1+	IN1+	OUT7
	G2	IN9	IN8 (7)			OUT8
	G3	IN12	IN9 (9)			OUT9
	G4	IN13	IN10 (10)			OUT10
	G5	IN14	IN11 (12)			OUT11
	B0	IN15	IN12 (13)	OUT1-	IN1-	OUT12
	B1	IN18	IN13 (15)			OUT13
	B2	IN19	IN14 (16)			OUT14
	B3	IN20	IN15 (18)	OUT2+	IN2+	OUT15
	B4	IN21	IN16 (19)			OUT16
	B5	IN22	IN17 (20)			OUT17
	HSYNC	IN24	IN18 (22)			OUT18
	VSYNC	IN25	IN19 (23)			OUT19
	DTMG	IN26	IN20 (25)	OUT2-	IN2-	OUT20
	DCLK	CLK IN	CLK IN (26)	CLK OUT+ CLK OUT-	CLK IN+ CLK IN-	CLK OUT

NOTE : 1) Numbers in parenthesis are IC pin No.

RELATIONSHIP BETWEEN DISPLAYED COLOR AND INPUT DATA

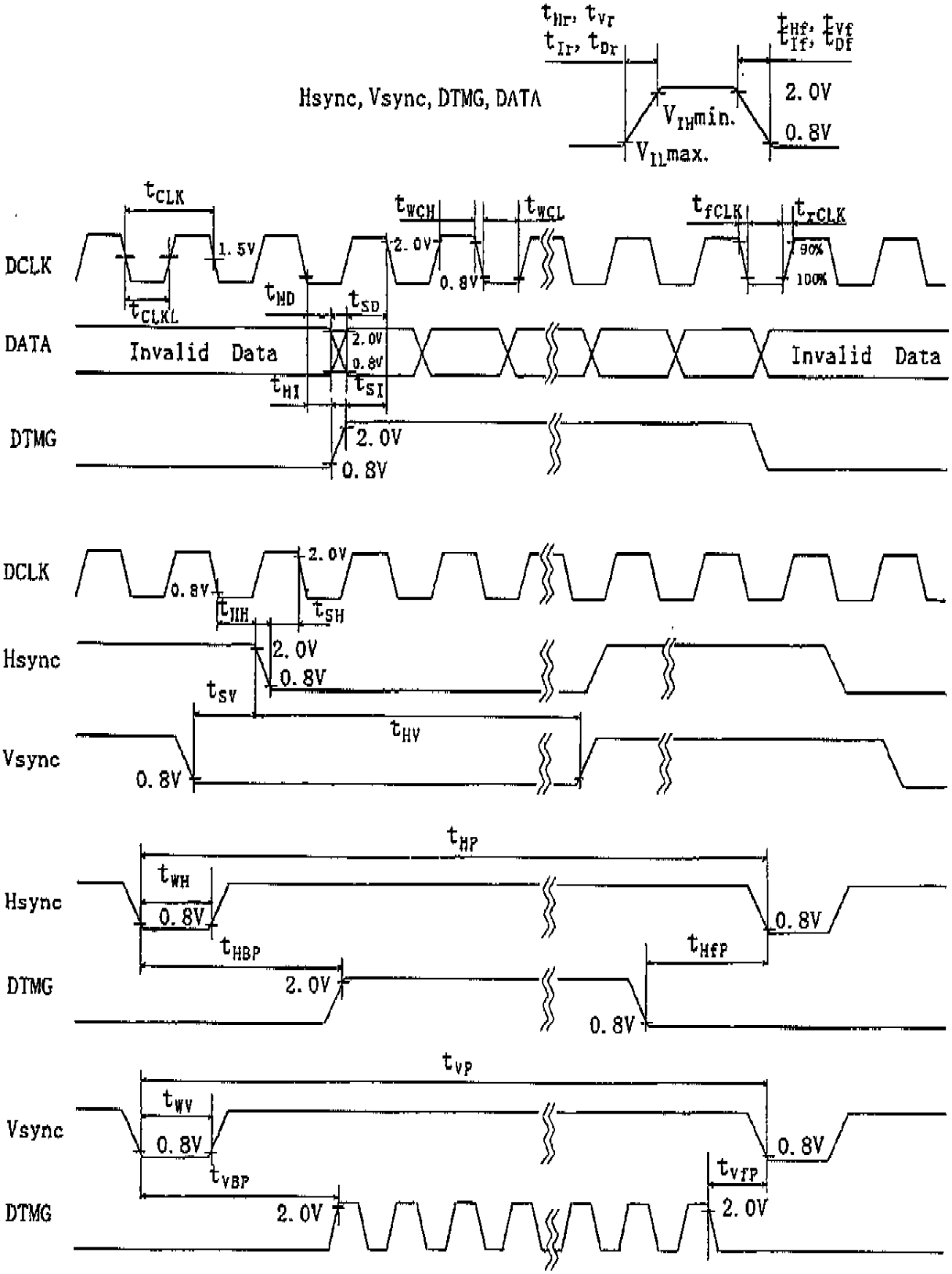
COLOR \ INPUT DATA		R DATA						G DATA						B DATA					
		RA5	RA4	RA3	RA2	RA1	RA0	GA5	GA4	GA3	GA2	GA1	GA0	BA5	BA4	BA3	BA2	BA1	BA0
		RB5	RB4	RB3	RB2	RB1	RB0	GB5	GB4	GB3	GB2	GB1	GB0	BB5	BB4	BB3	BB2	BB1	BB0
		MSB					LSB	MSB					LSB	MSB					LSB
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	BLUE(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	CYAN	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	MAGENTA	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	YELLO	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	RED(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	RED(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	RED(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	GREEN(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	GREEN(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	GREEN(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	GREEN(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
BLUE	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	BLUE(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	BLUE(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	BLUE(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	BLUE(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note 1) Definition of gray scale :
Color(n) --- n indicates gray scale level.
Higher n means brighter level.
2) Data : 1:Hi, 0:Lo

6. INTERFACE TIMING

6.1 TIMING CHART (FOR LVDS TRANSMITTER)

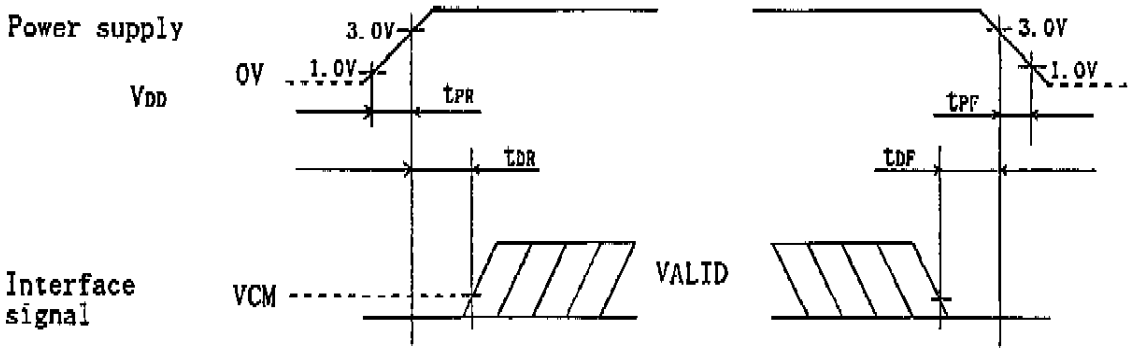
(Data : Latched at Fall edge of DCLK)



6.2 INTERFACE TIMING SPECIFICATION (FOR LVDS TRANSMITTER)

ITEM		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
DCLK	Period	t_{CLK}	14.7	15.4	16.7	ns	
	Width-Low	t_{WCL}	0.4	0.5	0.6	t_{CLK}	
	Width-High	t_{WCH}	0.4	0.5	0.6		
	Rise Time	t_{rCLK}	—	—	5	ns	
	Fall Time	t_{fCLK}	—	—	5		
	Duty	D	0.45	0.5	0.55	—	$D=t_{CLKL}/t_{CLK}$
Hsync	Set up Time	t_{SH}	5	—	—	ns	for DCLK
	Hold Time	t_{HH}	4	—	—		
	Period	t_{HP}	1072	—	2400	t_{CLK}	
	Width-Active	tWH	8	—	480		
	Rise/Fall Time	t_{Hr}, t_{Hf}	—	—	5	ns	
Vsync	Set up Time	t_{SV}	-8	—	—	t_{CLK}	for Hsync
	Hold Time	t_{HV}	2	—	—		
	Period	t_{VP}	771	—	1000	t_{HP}	
	Width-Active	t_{WV}	1	—	120		
	Rise/Fall Time	t_{Vr}, t_{Vf}	—	—	5	ns	
DTMG	Set up Time	t_{SI}	5	—	—	ns	for DCLK
	Hold Time	t_{HI}	4	—	—		
	Rise/Fall Time	t_{Ir}, t_{If}	—	—	5	ns	
	Horizontal Back Porch	t_{HBP}	32	—	416	t_{CLK}	
	Horizontal Front Porch	t_{HFP}	16	—	—		
	Vertical Back Porch	t_{VBP}	1	—	—	t_{HP}	
	Vertical Front Porch	t_{VFP}	3	—	—		
DATA	Set up Time	t_{SD}	5	—	—	ns	for DCLK
	Hold Time	t_{HD}	4	—	—		
	Rise/Fall Time	t_{Dr}, t_{Df}	—	—	5	ns	

6.3 TIMING BETWEEN INTERFACE SIGNAL AND POWER SUPPLY



POWER ON

$0 \leqq t_{DR} \leqq 0.5s$

$40ms \geqq t_{PR}$

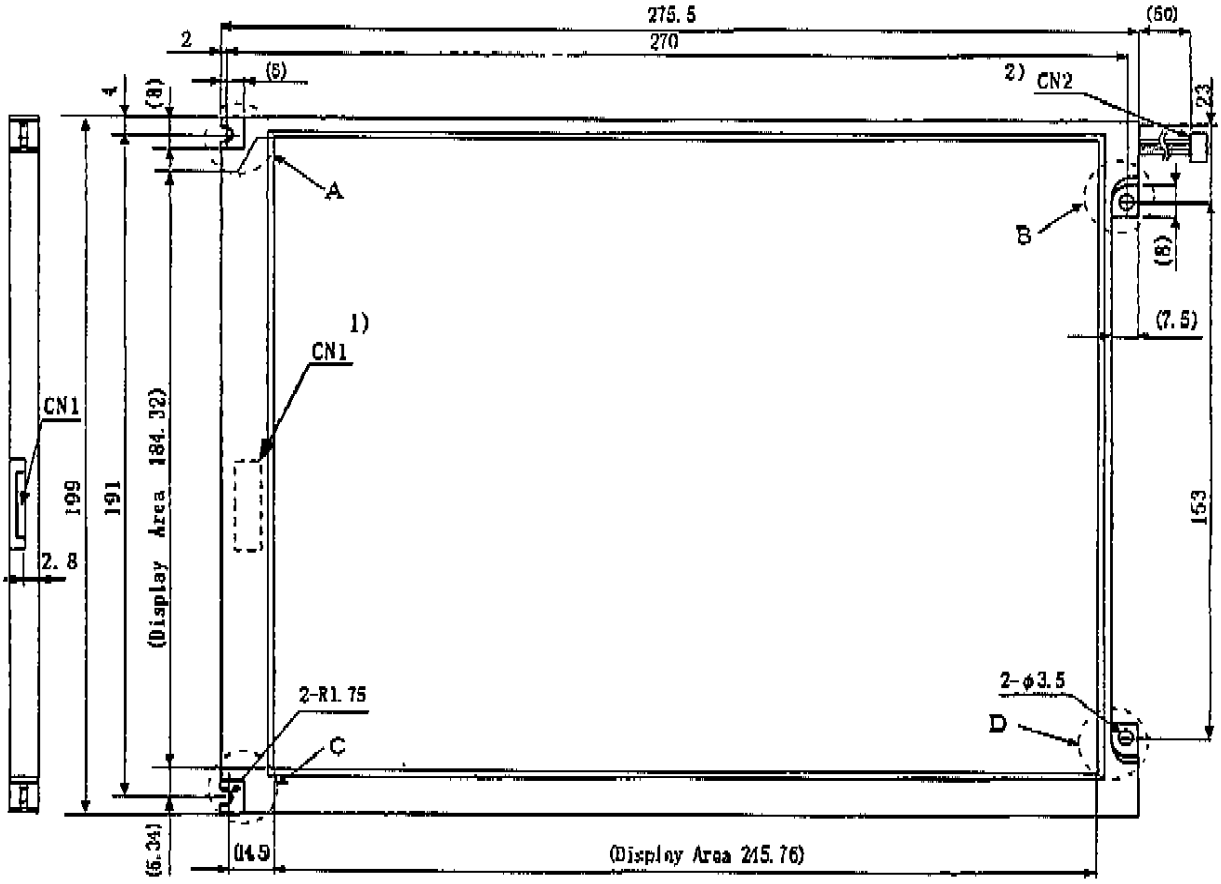
POWER OFF

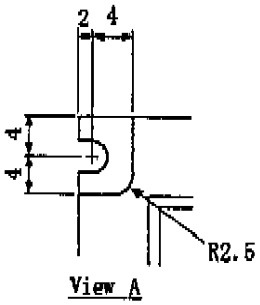
$0 \leqq t_{DF} \leqq 0.5s$

$40ms \geqq t_{PF}$

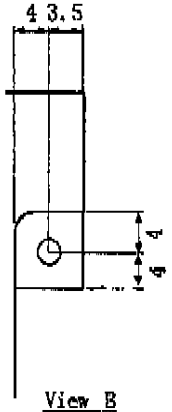
7. DIMENSIONAL OUTLINE

(1) Front View

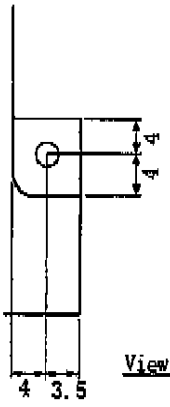




View A

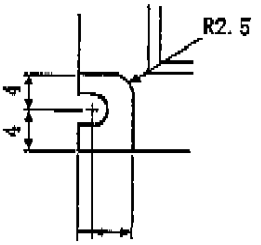


View B



View C

Unit : mm
Scale : NTS



View C

Note 1) CN1 : JAE FI-WE21P-HF
2) CN2 : JST BHR-03VS-1 cable length : about 50mm.
3) Tolerance not specified is ±0.5mm.
4) Dimensions in parenthesis are reference value.
5) Position, size and form of tab and grooves on Metal bezal not specified.

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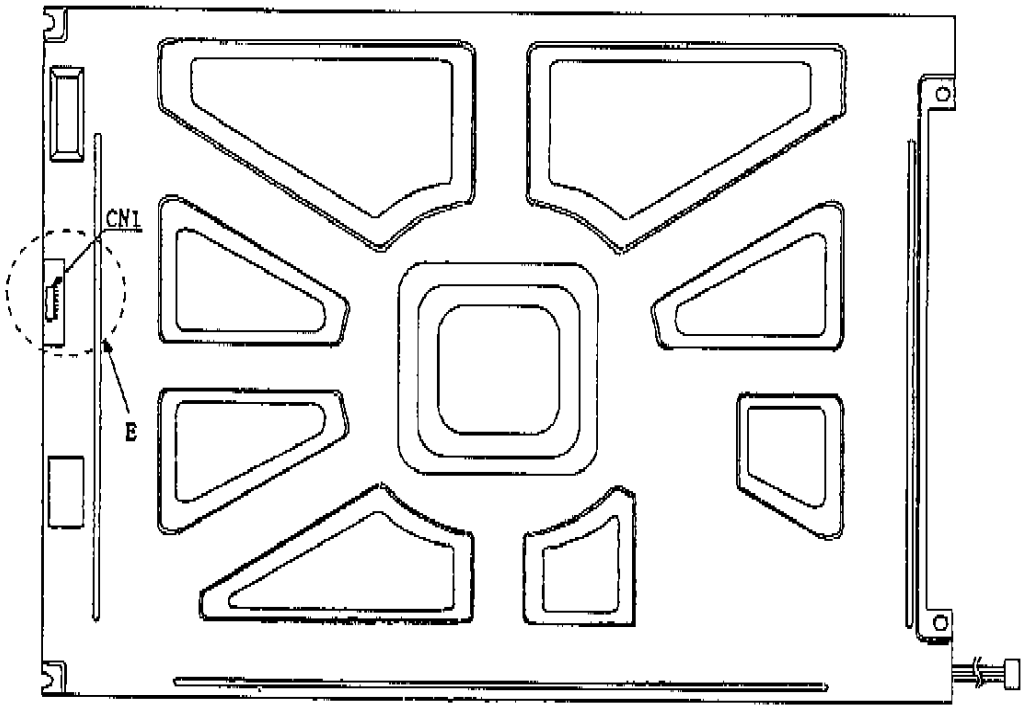
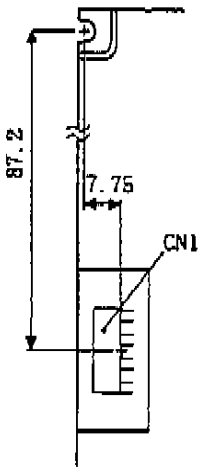
(2) Back View





View E

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