

**Engineering Specification**

**Type 20.12 WSXGA+ Color TFT/LCD Module  
Model Name:IAWS64**

**Document Control Number : OEM I-964-01**

**Note:Specification is subject to change without notice. Consequently it is better to contact to International Display Technology before proceeding with the design of your product incorporating this module.**

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## ii Record of Revision

Date	Document Revision	Page	Summary
June 10,2002	OEM I-964-01	All	First Edition for customer. Based on Internal Spec. as of June 7,2002.

## 1.0 Handling Precautions

- If any signal or power line deviates from the power on/off sequence, it may cause shortening the life of the LCD module and/or damage the electrical components. Also, hot plug-in operation may cause the similar damages as above.
- The LCD panel and the CCFL (Cold Cathode Fluorescent Lamp)s are made of glass and may break or crack if dropped on a hard surface. Handling with care is necessary.
- The fluorescent lamp in the liquid crystal display (LCD) contains mercury. Do not put it in trash that is disposed of in landfills. Dispose of it as required by local ordinances or regulations.
- Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be applied to exemption conditions of the flammability requirements (4.4.3.3, EN60950 or UL1950) in an end product.
- Please handle with care when mounted in the system cover. Mechanical damage for the lamp cable / lamp connector may cause safety problems.
- After installation of the TFT Module into an enclosure (Monitor frame, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/ twisting forces are applied to the TFT Module from out side. Otherwise the TFT Module may be damaged.
- Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- Also, when removing a protection sheet from the module surface, please take some actions against static electricity, like earth band, ionic shower, etc.
- Since front polarizer is easily damaged, pay attention not to scratch it.
- Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- Do not open nor modify the Module Assembly.
- Prevent continuous 10 hours or over same pattern displaying, to avoid image sticking.

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- The information contained herein may be changed without prior notice. It is therefore advisable to contact International Display Technology before proceeding with the design of equipment incorporating this product.

## 2.0 General Description

This specification applies to the Type 20.12 Color TFT/LCD Module 'IAWS64'.

This module is designed for a display unit of a monitor application.

The screen format and electrical interface are intended to support the WSXGA+ (1680(H) x 1050(V)) screen.

Supported color is native 24bit colors (8-bit per RGB-subpixels data driver).

All input signals are TMDS (Transition Minimized Differential Signaling) interface compatible.

This module does not contains an inverter card for backlight.

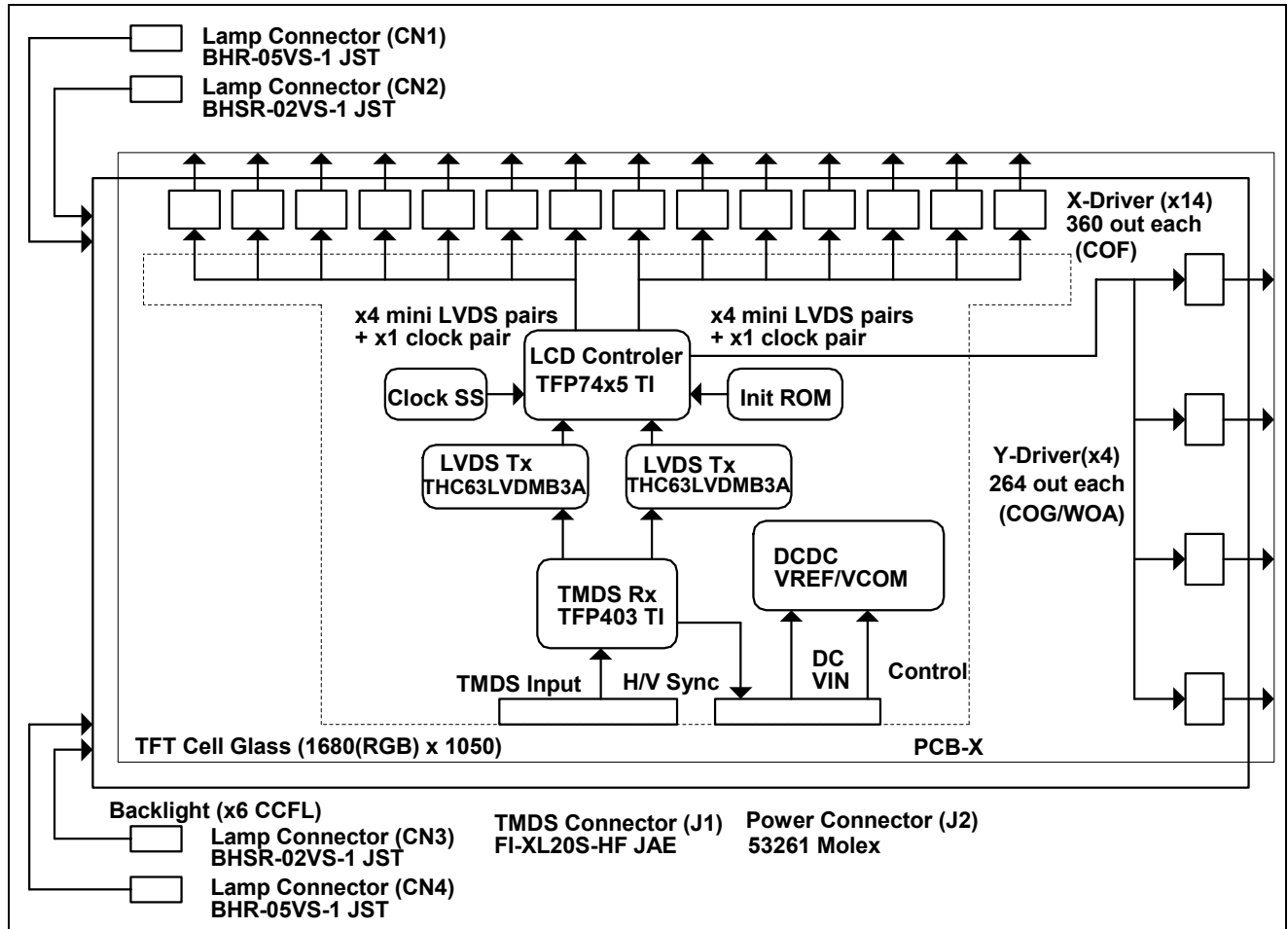
## 2.1 Characteristics

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [cm]	51.11 (16:10)
Pixels	1680(H) x 1050(V)
Active Area [mm]	433.44(H) x 270.90(V)
Pixel Pitch [mm]	0.258 x 0.258
Pixel Arrangement	RGB-subpixels per one Pixel, Vertical Stripe
Weight [K grams]	3.80 <b>(TBD)</b> Typ. <b>(TBD)</b> Max.
Physical Size [mm]	486.2(W) x 307.0(H) x 17.8 Typ./ 18.3 Max. (D)
Display Mode	Dual Domain IPS, Normally Black
Supported Color	Native 24bit colors (RGB 8-bits per each subpixel)
White Luminance [cd/m <sup>2</sup> ]	210 Typ., 180 Min.
Contrast Ratio	350:1 Typ. 250:1 Min. (In the Dark room)
Optical Rise Time+Fall Time [msec]	45 Typ. <b>(TBD)</b>
Input Voltage [V]	+18 +5/-5% (Logic)
Power Consumption [W]	Logic 15 Typ. <b>(TBD)</b> , Backlight 32 Typ. <b>(TBD)</b>
Electrical Interface	Single Link TMDS (Clock Freq.:117.13[MHz])
Temperature Range [degree C] Operating Storage (Shipping)	0 to +50 <b>(Note)</b> -20 to +60

**Note** : Max. Operating Temperature 50 deg.C in the spec means the temperature measured at the point of the front surface of the LCD glass cell.

## 2.2 Functional Block Diagram

The following diagram shows the functional block diagram for the Type 20.12 Color TFT/LCD Module.



### 3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module are as follows;

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vcc	-0.3	+21.0	V	<b>(TBD)</b>
Input Voltage of Signal		-0.3	+4.0	V	<b>(TBD)</b> (TMDS pins)
Input Voltage of Signal		-0.3	+5.3	V	<b>(TBD)</b> (PWR_CTRL)
CFL Ignition Voltage	Vinv	-	2,000	Vrms	Ta=0[deg. C] <b>(Note 1)</b>
CFL Current	ICFL	7.0	-	mArms	
CFL Peak Current	ICFLP	20	-	mArms	Ta=25[deg. C] <b>(Note 1)</b>
Operating Temperature	TOP	0	+50	deg.C	<b>(Note 2)</b>
Operating Relative Humidity	HOP	8	80	%RH	<b>(Note 2)</b>
Storage Temperature	TST	-20	+60	deg.C	<b>(Note 2)</b>
Storage Relative Humidity	HST	5	95	%RH	<b>(Note 2)</b>
Vibration			1.5	G Hz	
Shock			50 11	G ms	Half sine wave

**Note :**

1. Duration : 50[mS] Max.
2. Maximum Wet-Bulb should be 39 degree C and No condensation.  
Max. Operating Temperature 50 deg. C in the spec means the temperature measured for the point of the front surface of the LCD glass cell.

## 4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

Item	Conditions	Specification	
		Typ.	Note
Viewing Angle (Degrees)	Horizontal (Right)	85	-
	$K \geq 10$ (Left)	85	-
K:Contrast Ratio	Vertical (Upper)	85	-
	$K \geq 10$ (Lower)	85	-
Contrast ratio		350	-
Response Time (ms)	Rising + Falling	45	-
Color Chromaticity (CIE)	Red x	0.640	-
	Red y	0.330	-
	Green x	0.290	-
	Green y	0.600	-
	Blue x	0.150	-
	Blue y	0.060	-
	White x	0.313	-
	White y	0.329	-
White Luminance (cd/m <sup>2</sup> )		210 (Center)	-
White point tracking (K)	L64 (TBD) - L255 (TBD)	Less than 400	



## 5.0 Signal Interface

Physical interface is described in accordance with the connectors on the LCD module.

These connectors are capable of accommodating the following signals and will be the following components or IDT approved types.

### 5.1 Connectors

All video signals are provided through the LVDS cable from Monitor Card. These connectors are the input connector of video signals. The LVDS signals, which are provided from monitor card, are described on the following table.

#### Signal Connectors

Connector	Function	Type	Manufacturer	Mating Connector
J1	TMD5 Connector	FI-XL20S-HF	JAE	
J2	Power Connector	53261	Molex	

#### Lamp Connectors

Connector	Function	Connector Type	Manufacturer	Mating Connector
CN1	Lamp Connector (Upper1)	BHR-05VS-1	JST	SM04(9-E2)B-BHS-1
CN2	Lamp Connector (Upper2)	BHSR-02VS-1	JST	SM02B-BHSS-1
CN3	Lamp Connector (Lower1)	BHSR-02VS-1	JST	SM02B-BHSS-1
CN4	Lamp Connector (Lower2)	BHR-05VS-1	JST	SM04(9-E2)B-BHS-1

## 5.2 Interface Signal Connector

### TMDS Connector Signals Pin Assignment (J1)

Pin #	Signal Name
1	GND
2	GND
3	GND
4	GND
5	SHLD2
6	TX2+
7	TX2-
8	SHLD1
9	TX1+
10	TX1-
11	SHLD0
12	TX0+
13	TX0-
14	SHLDC
15	TXC+
16	TXC-
17	GND
18	GND
19	GND
20	GND

Voltage levels of all input signals are TMDS compatible in this connector, J1.

### Power Connector Signals Pin Assignment (J2)

Pin #	Signal Name
1	GND
2	Reserved
3	PWR_CTRL
4	GND
5	Vcc
6	Vcc
7	Vcc
8	Vcc
9	GND
10	NC
11	NC
12	GND
13	HS_OUT
14	VS_OUT
15	GND

**Lamp Connectors Pin Assignment (CN1)**

Pin #	Signal Name	CFL Position <b>(Note)</b>	Voltage	Wire Color
1	Lamp High	HIGH	HV	PINK
2	Lamp High	MID	HV	BLUE
3				
4	Lamp Low	HIGH	LV	WHITE
5	Lamp Low	MID	LV	WHITE

**Lamp Connectors Pin Assignment (CN2)**

Pin #	Signal Name	CFL Position <b>(Note)</b>	Voltage	Wire Color
1	Lamp High	LOW	HV	GRAY
2	Lamp Low	LOW	LV	WHITE

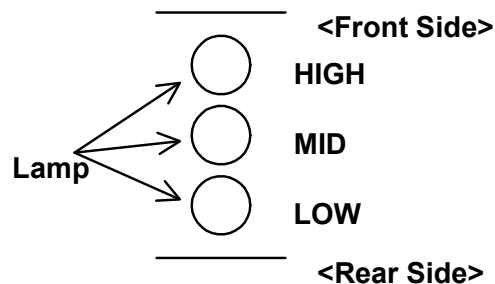
**Lamp Connectors Pin Assignment (CN3)**

Pin #	Signal Name	CFL Position <b>(Note)</b>	Voltage	Wire Color
1	Lamp High	LOW	HV	GRAY
2	Lamp Low	LOW	LV	WHITE

**Lamp Connectors Pin Assignment (CN4)**

Pin #	Signal Name	CFL Position <b>(Note)</b>	Voltage	Wire Color
1	Lamp High	HIGH	HV	PINK
2	Lamp High	MID	HV	BLUE
3				
4	Lamp Low	HIGH	LV	WHITE
5	Lamp Low	MID	LV	WHITE

**Note :** CFL Position is defined as follows.



### 5.3 Interface Signal Description

#### TMDS Connector Signal Description (J1)

SIGNAL NAME	Description
TX0+	TMDS positive differential Input (Channel 0)
TX0-	TMDS negative differential Input (Channel 0)
TX1+	TMDS positive differential Input (Channel 1)
TX1-	TMDS negative differential Input (Channel 1)
TX2+	TMDS positive differential Input (Channel 2)
TX2-	TMDS negative differential Input (Channel 2)
TXC+	TMDS positive differential Input (Channel C)
TXC-	TMDS negative differential Input (Channel C)
SHLD0	Shield for TMDS channel 0
SHLD1	Shield for TMDS channel 1
SHLD2	Shield for TMDS channel 2
SHLDC	Shield for TMDS channel C
GND	Ground

#### Power Connector Signal Description (J2)

SIGNAL NAME	Description
Vcc	+18V Power Supply
GND	Ground
PWR_CTRL	LCD Module Power Control Signal Input ( <b>Note</b> )
HS_OUT	Hsync Output
VS_OUT	Vsync Output
Reserved	No Connect LCD panel internal use

**Note** : PWR\_CTRL is used to control the power to the LCD drivers. The actual control circuit is on the LCD module.

#### Lamp Connector Signal Description (CN1, CN2, CN3, CN4)

SIGNAL NAME	Description
Lamp High	Lamp Electrode at High Voltage Side
Lamp Low	Lamp Electrode at Low Voltage Side

**Signal Description**

SIGNAL NAME	Description
+Red7 (QE23, QO23) +Red6 (QE22, QO22) +Red5 (QE21, QO21) +Red4 (QE20, QO20) +Red3 (QE19, QO19) +Red2 (QE18, QO18) +Red1 (QE17, QO17) +Red0 (QE16, QO16)	Red Sub Pixel Data 7 (MSB) Red Sub Pixel Data 6 Red Sub Pixel Data 5 Red Sub Pixel Data 4 Red Sub Pixel Data 3 Red Sub Pixel Data 2 Red Sub Pixel Data 1 Red Sub Pixel Data 0 (LSB) Red Sub Pixel Data: Each Red Sub pixel's brightness data consists of these 8 bits pixel data.
+Green7 (QE15, QO15) +Green6 (QE14, QO14) +Green5 (QE13, QO13) +Green4 (QE12, QO12) +Green3 (QE11, QO11) +Green2 (QE10, QO10) +Green1 (QE9, QO9) +Green0 (QE8, QO8)	Green Sub Pixel Data 7 (MSB) Green Sub Pixel Data 6 Green Sub Pixel Data 5 Green Sub Pixel Data 4 Green Sub Pixel Data 3 Green Sub Pixel Data 2 Green Sub Pixel Data 1 Green Sub Pixel Data 0 (LSB) Green Sub Pixel Data: Each Green Sub pixel's brightness data consists of these 8 bits pixel data.
+Blue7 (QE7, QO7) +Blue6 (QE6, QO6) +Blue5 (QE5, QO5) +Blue4 (QE4, QO4) +Blue3 (QE3, QO3) +Blue2 (QE2, QO2) +Blue1 (QE1, QO1) +Blue0 (QE0, QO0)	Blue Sub Pixel Data 7 (MSB) Blue Sub Pixel Data 6 Blue Sub Pixel Data 5 Blue Sub Pixel Data 4 Blue Sub Pixel Data 3 Blue Sub Pixel Data 2 Blue Sub Pixel Data 1 Blue Sub Pixel Data 0 (LSB) Blue Sub Pixel Data: Each Blue Sub pixel's brightness data consists of these 8 bits pixel data.
DTCLK	Data Clock: The typical frequency is 117.13MHz. The signal is used to strobe the pixel +data and the +DSPTMG
+DSPTMG (DSP)	When the signal is high, the pixel data shall be valid to be displayed.
VSYNC (V-S)	Vertical Sync: This signal is synchronized with DTCLK. Both active high/low signals are acceptable.
HSYNC (H-S)	Horizontal Sync: This signal is synchronized with DTCLK. Both active high/low signals are acceptable.

## **5.4 Interface Signal Electrical Characteristics**

### **5.4.1 Signal Electrical Characteristics for TMDS Receiver**

Please refer to TI TFP403 datasheet (SLDS 125 December 2000)

### **5.4.2 Recommended Guidelines for Motherboard PCB Design and Cable Selection**

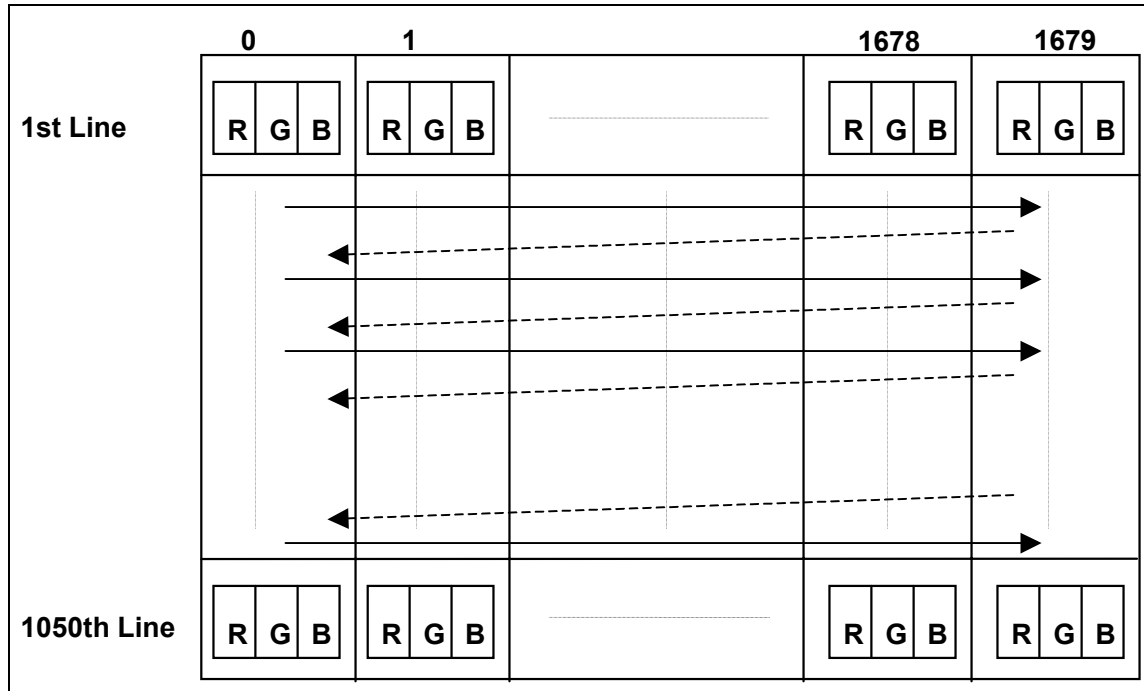
Following the suggestions below will help to achieve optimal results.

- Use controlled impedance media for TMDS signals.
- Match electrical lengths between traces to minimize signal skew.
- Isolate TTL signals from TMDS signals.
- For cables, twisted pair, twinax, or flex circuit with close coupled differential traces are recommended.

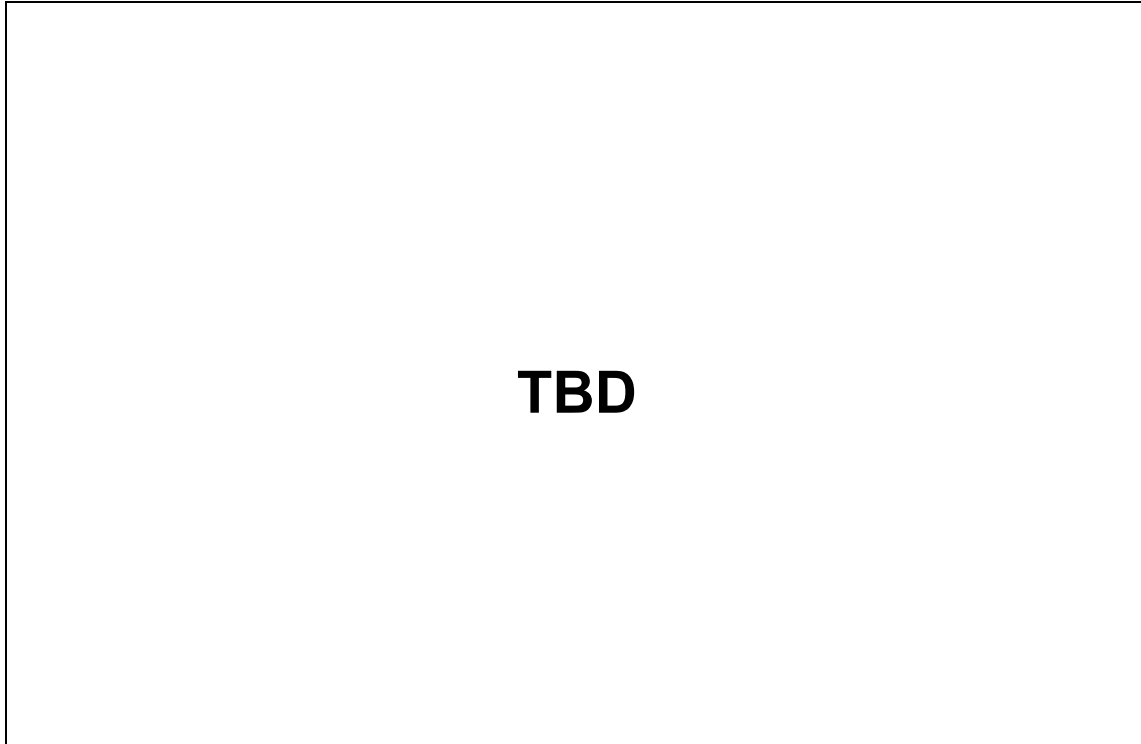
## 6.0 Pixel format image

Following figure shows the relationship between the input signals and the LCD pixel format image. IAWS64 has a TMDS interface. Following figure shows the relationship of the input signals and LCD pixel format image.

Screen Format



The following chart is the ICFL versus Brightness for your reference.





## 7.0 Interface Timings

### 7.1 Timing Characteristics

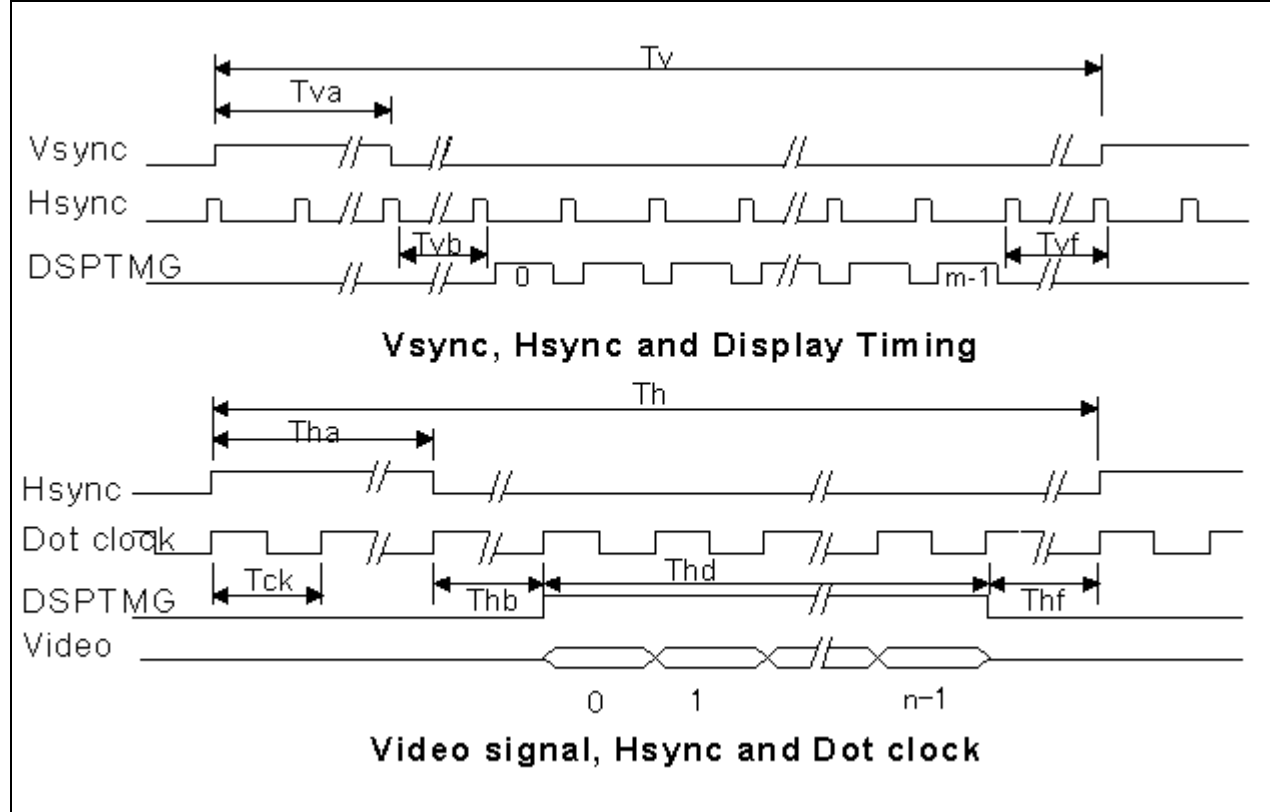
#### Timing Characteristics (TBD)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit
DTCLK	Dot Clock Freq.	Fdck	111.0	117.13	124.0	[MHz] +/- 5%
DTCLK	Dot Clock period	Tck	8.06	8.54	9.01	[ns]
+V-Sync	Refresh Rate	1/Tv		59.94		[Hz]
+V-Sync	Frame period	Tv		16.68		[ms]
+V-Sync	Total line	Tv		1062	2303	[lines]
+V-Sync	V-front porch	Tvf	1	3		[lines]
+V-Sync	V-active level	Tva	1	3		[lines]
+V-Sync	V-back porch	Tvb	(6)	6	127	[lines]
+V-Sync	V-Blank	Tvf+Tva+Tvb	8	12	255	[lines]
+DSPTMG	Display Lines / frame	m	-	1050	-	[lines]
+H-Sync	H-Scan Rate	1/Th		63.7		[kHz]
+H-Sync	H-Scan Rate	Th		15.71		[us]
+H-Sync	Cycle	Th		1840		[tck]
+H-Sync	H-front porch	Thf	64	64		[tck]
+H-Sync	H-active level	Tha	8	32		[tck]
+H-Sync	H-back porch	Thb	8	64		[tck]
+H-Sync	H-Blank	Thf+Tha+Thb	80	160		[tck]
+DSPTMG	Display clocks	Thd	-	1680	-	[tck]
+DSPTMG	Display Pixels	n	-	1680	-	[pixels]

#### Note :

1. H/V sync Polarity will be acceptable both positive and negative. DSPTMG (Data Enable) should be Active High.
2. Vsync should not be changed at Hsync leading edge (+/- 6 [tck]). (TBD)
3. All channels should be activated any time after Power On (because it does not have Auto Refresh protection).

Following is the Video timing per channel to be converted to/from TMDS interface.



## 8.0 Power Consumption

### Power Characteristics

SYMBOL	PARAMETER	Min.	Typ.	Max.	UNITS	CONDITION
Vcc	Logic/LCD Drive Voltage	17.0	18.0	19.0	[V]	Load Capacitance <b>(TBD)</b> [uF]
Icc	Vcc Current	<b>(TBD)</b>	<b>(TBD)</b>	<b>(TBD)</b>	[A]	Vcc=18.0[V]
Pin	Vcc Power	<b>(TBD)</b>	15.0 <b>(TBD)</b> <b>(Note 1)</b>	<b>(TBD)</b> <b>(Note 2)</b>	[W]	Vcc=18.0[V]
Vcc rp	Allowable Logic/LCD Drive Ripple Voltage			100	[mVp-p]	
Vcc ns	Allowable Logic/LCD Drive Ripple Noise			100	[mVp-p]	

**Note :**

1. Vertical Color Bar **(TBD)**
2. Sub Pixel Checker **(TBD)**

### CFL Characteristics

Symbol	Parameter	Min.	Max.	Units	Conditions
ICFL	CFL Current	2.0	6.5	[mArms]	Ta=25 [deg. C] <b>(Note 1)</b>
FCFL	CFL Frequency	35	80	[kHz]	Ta=25 [deg. C] <b>(Note 2)</b>
Vinv	CFL Ignition Voltage	-	1350	[Vrms]	Ta=25 [deg. C]
		-	1650	[Vrms]	Ta=0 [deg. C]

**Note :**

1. CFL current exceeds Min./Max. values, then "CFL life", "ON/OFF Cycle" and "Safety" will not be guaranteed.
2. CFL frequency should be carefully determined to avoid interference between inverter and TFT LCD.

**Inverter Design Point**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
(L255)	White Luminance (center) (Reference)	-	210	-	[cd/m <sup>2</sup> ]	Ta=25 [deg. C]
ICFL	CFL Current	2.0	6.0	6.5	[mArms]	Ta=25 [deg. C] <b>(Note 1)</b>
ICFLP	CFL Peak Inrush Current			20	[mA]	Ta=25 [deg. C] <b>(Note 1)</b>
FCFL	CFL Frequency	35		60	[kHz]	Ta=25 [deg. C] <b>(Note 2)</b>
Vinv	Inverter Ignition Voltage *5	1500			[Vrms]	Ta=25 [deg. C]
		1700			[Vrms]	Ta=10 [deg. C]
		1850			[Vrms]	Ta=0 [deg. C]
VCFL	CFL Voltage (Reference)		860		[Vrms]	Ta=25 [deg. C]
PCFL	CFL Power Consumption		5.2	5.6	[W]	Ta=25 [deg. C] <b>(Note 3)</b>
	Total CFL Power Consumption (6 lamps)		32	34	[W]	Ta=25 [deg. C]

**Note :**

1. If it exceeds Min./Max. values, then "CFL Life", "ON/OFF Cycle" and "Safety" will not be guaranteed.
2. CFL Frequency should be carefully determined to avoid interference between inverter and TFT LCD.
3. Calculated value for reference (ICFL x VCFL = PCFL)
4. It should be employed the inverter which has 'Duty Dimming', if ICFL is less than 4.0 **(TBD)**[mA].
5. Please keep balancing of all CFL currents.

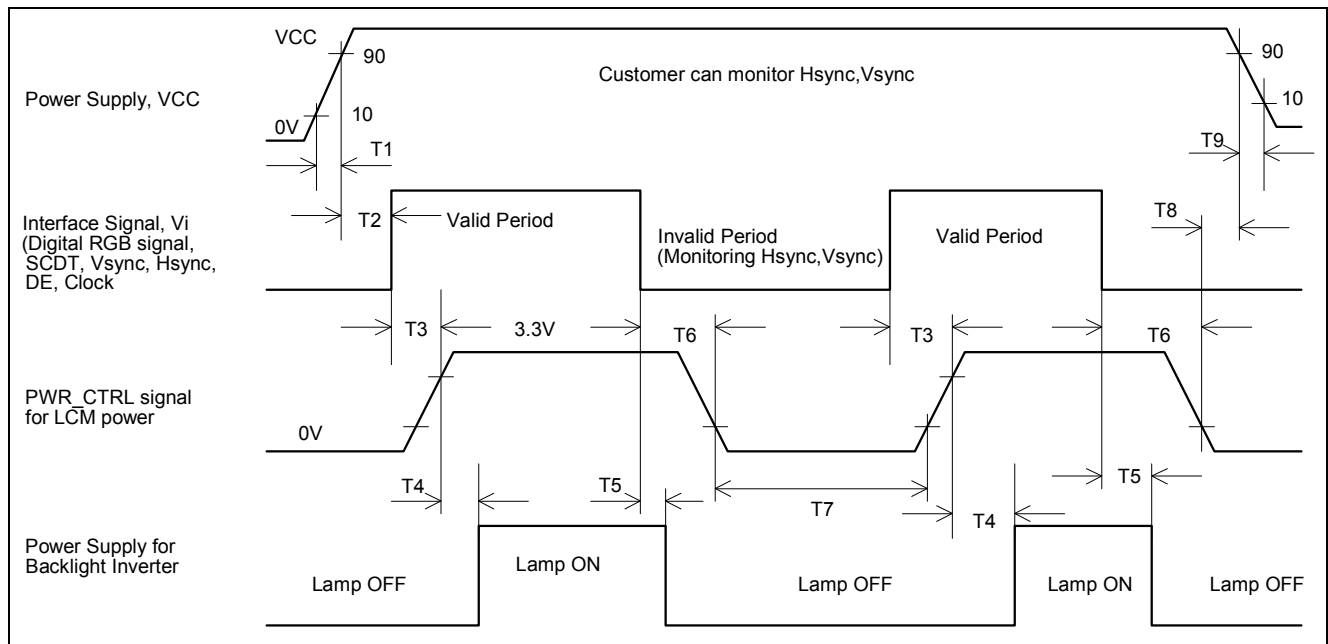
## 9.0 Power ON/OFF Sequence

Vcc power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when Vcc is off.

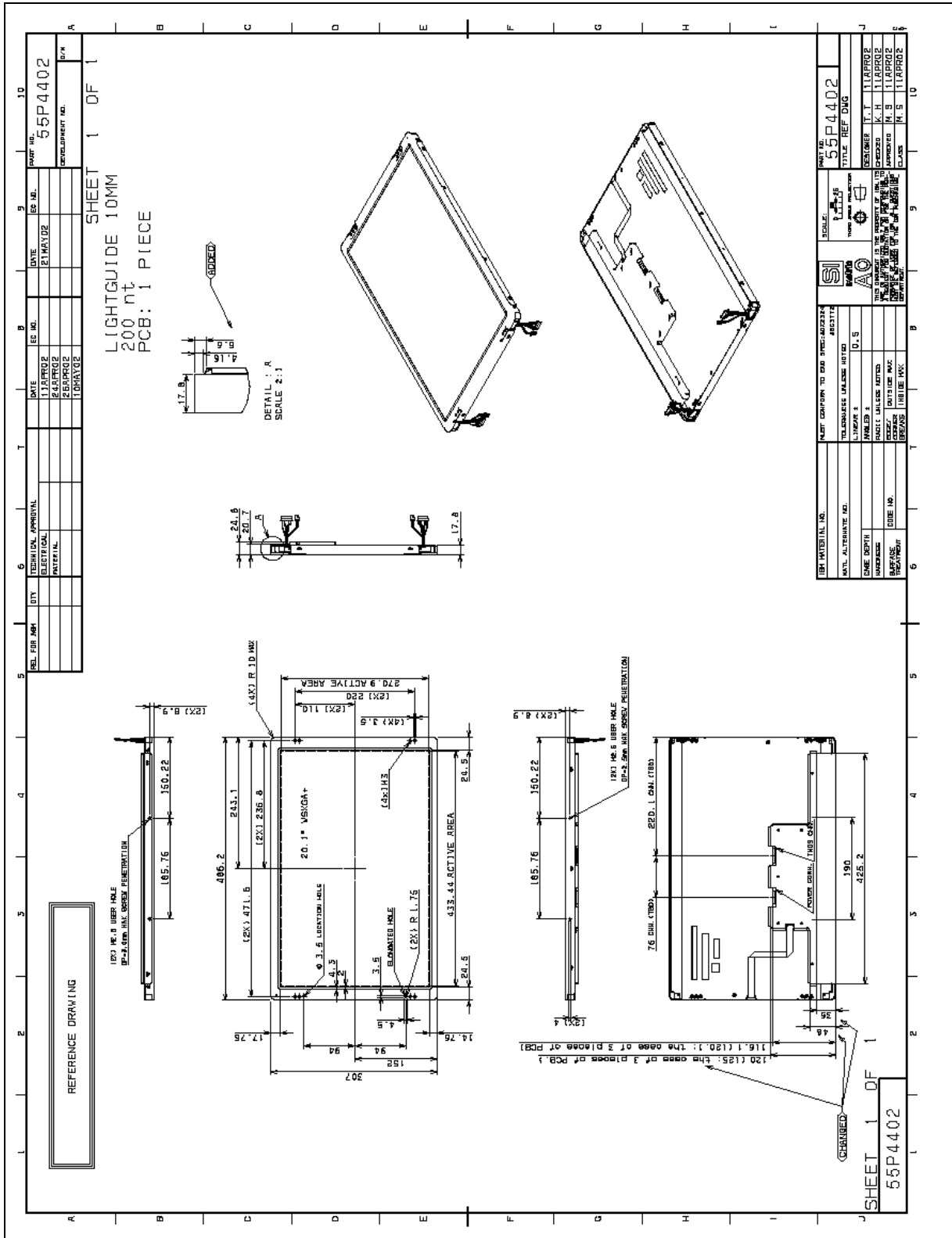
Power On/Off Sequence

Parameter	Min.	Typ.	Max.	Unit
T1	-		10	[ms]
T2	0		-	[ms]
T3	-		50	[ms]
T4	100		-	[ms]
T5	-		50	[ms]
T6	-		80	[ms]
T7	400		-	[ms]
T8	0		-	[ms]
T9	-		10	[ms]

Vcc/TMDS Signals/Lamp Voltage On/Off Sequence Requirements



# 10.0 Mechanical Characteristics



## 11.0 National Test Lab Requirement

The display module is authorized to Apply the UL Recognized Mark.

### Conditions of Acceptability

- This component has been judged on the basis of the required spacings in the Standard for Safety of Information Technology Equipment, Including Electrical Business Equipment, CAN/CSA C22.2 No.950-00,UL60950, 3rd Edition, IEC 60950 (3rd. Ed.) and EN 60950 (3rd. Ed.), which would cover the component itself if submitted for Listing.
- CF Lamp circuit for this model should be supplied from Limited Current Circuit.
- The units are supplied by Limited Power Sources.
- The terminals and connectors are suitable for factory wiring only.
- The terminals and connectors have not been evaluated for field wiring.
- A suitable Electrical and Fire enclosure shall be provided.

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