

Engineering Specification

**Type 15.0 SXGA+ Color TFT/LCD Module
Model Name:ITSX95**

Document Control Number : OEM I-95-04

Note:Specification is subject to change without notice. Consequently it is better to contact to International Display Technology before proceeding with the design of your product incorporating this module.

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ii Record of Revision

| Date | Document Revision | Page | Summary |
|------------------|-------------------|---|---|
| June 1,2000 | OEM95-01 | All | First Edition for customer. Based on Internal Spec. as of March 10,2000. Based on Mechanical Drawing as of 24APR00. |
| August 4,2000 | OEM95-02 | 6 12 14 19 21 22 23,24 | Based on Internal Specification EC F78951 as of July 12,2000. To update Characteristics. To add Note for Even/Odd. To update LVDS Macro AC characteristics. To update Timing Characteristics. To update Power Consumption. To update Power ON/OFF Sequence. To update Reference Drawing as of June 5,2000. |
| October 10,2000 | OEM95-03 | 8 9 14,15,16,17,18 21 25 27,28 | Based on Internal Specification EC F78952 as of September 6,2000. To update Absolute Maximum Ratings (VDD). To update Optical Characteristics. To update Interface Signal Electrical Characteristics. To update Parameter guide line for CFL Inverter. To update Power Consumption. To update Reference Drawing as of September 1,2000. |
| April 24,2001 | OEM95-04 | 1,5,6,7 6 27,28 | Based on Internal Specification EC H30700 as of January 31,2001. To avoid using "inch" indication. To update Weight. To update Reference Drawings. |
| February 22,2002 | OEM I-95-04 | | Updated by establishment of the New Company as "International Display Technology". |

1.0 Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) Do not stick the adhesive tape on the reflector sheet at the back of the LCD module.
- 10) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CFL Reflector edge.
Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
- 11) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 12) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 13) The fluorescent lamp in the liquid crystal display (LCD) contains mercury. Do not put it in trash that is disposed of in landfills. Dispose of it as required by local ordinances or regulations.
- 14) Small amount of materials having no flammability grade is used in the LCD module.
The LCD module should be supplied by power complied with requirements of Limited Power Source (2.11, IEC60950 or UL1950), or be applied exemption conditions of flammability requirements (4.4.3.3, IEC60950 or UL1950) in an end product.
- 15) The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit (2.4, IEC60950 or UL1950). Do not connect the CFL in Hazardous Voltage Circuit.

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- The information contained herein may be changed without prior notice. It is therefore advisable to contact International Display Technology before proceeding with the design of equipment incorporating this product.

2.0 General Description

This specification applies to the Type 15.0 Color TFT/LCD Module 'ITSX95'.

This module is designed for a display unit of notebook style personal computer.

The screen format and electrical interface are intended to support the SXGA+(1400(H) x 1050(V)) screen.

Support color is native 262K colors(RGB 6-bit data driver).

All input signals are LVDS(Low Voltage Differential Signaling) interface compatible.

This module does not contain an inverter card for backlight.

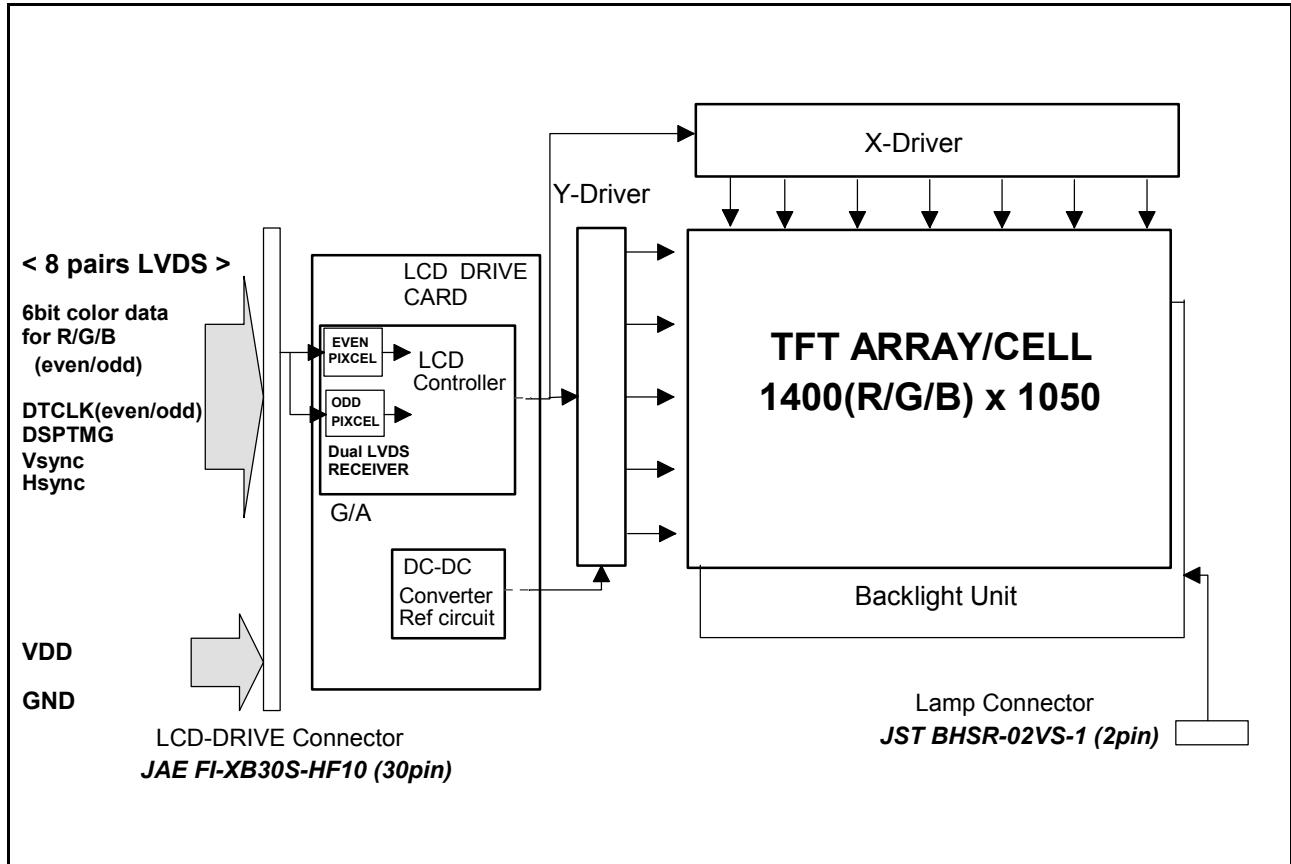
2.1 Characteristics

The following items are characteristics summary on the table under 25 degree C condition:

| CHARACTERISTICS ITEMS | SPECIFICATIONS |
|--|---|
| Screen Diagonal [mm] | 381 |
| Pixels H x V | 1400(x3) x 1050 |
| Active Area [mm] | 304.5(H) x 228.375(V) |
| Pixel Pitch [mm] | 0.2175(per one triad) x 0.2175 |
| Pixel Arrangement | R,G,B Vertical Stripe |
| Weight [grams] | 590 Typ.,625 MAX. |
| Physical Size [mm] | 317.3(W) x 242.0(H) x 6.0(D) typ./6.3(D) MAX. |
| Display Mode | Normally White |
| Support Color | Native 262K colors(RGB 6-bit data driver) |
| White Luminance [cd/m ²] Design Point 1:(ICFL=3.5mA) Design Point 2:(ICFL=6.5mA) | 90 Typ(center) 85 Typ(5 points average) 150 Typ(center)140 Typ(5 points average) |
| Contrast Ratio | 200 : 1 Typ. |
| Optical Rise Time/Fall Time [msec] | 30Typ.,50 Max. |
| Nominal Input Voltage VDD [Volt] | +3.3 Typ. |
| Power Consumption [Watt](VDD Line) | 1.8 Typ.,3.2MAX. |
| Lamp Power Consumption [Watt] (VCFL Line) Design Point 1:(ICFL=3.5mA) Design Point 2:(ICFL=6.5mA) | 2.6Typ.,(W/o inverter loss) 4.2Typ.,(W/o inverter loss) |
| Typical Power Consumption [Watt] (VDD Line + VCFL Line) Design Point 1:(ICFL=3.5mA) Design Point 2:(ICFL=6.5mA) | 4.5Typ.5.9MAX,(W/o inverter loss) 6.0Typ.7.7MAX,(W/o inverter loss) |
| Electrical Interface | 8 pairs LVDS(Even/Odd R/G/B Data(6bit), 3sync signals, Clock) |
| Temperature Range [degree C] Operating Storage (Shipping) | 0 to +50 -20 to +60 |

2.2 Functional Block Diagram

The following diagram shows the functional block of this Type 15.0 Color TFT/LCD Module. The first LVDS port transmits even pixels while the second LVDS port transmits odd pixels.



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

| Item | Symbol | Min | Max | Unit | Conditions |
|-----------------------------|--------|------|------------|-------|----------------|
| Logic/LCD Drive Voltage | VDD | -0.3 | +4.0 | V | |
| Input Signal Voltage | VIN | -0.3 | VDD+0.3 | V | |
| CFL Ignition Voltage | Vs | - | +1,600 | Vrms | Note 2 |
| CFL Current | ICFL | - | +7 | mAms | |
| CFL Peak Inrush Current | ICFLP | - | 20 | mA | |
| Operating Temperature | TOP | 0 | +50 | deg.C | Note 1 |
| Operating Relative Humidity | HOP | 8 | 95 | %RH | Note 1 |
| Storage Temperature | TST | -20 | +60 | deg.C | Note 1 |
| Storage Relative Humidity | HST | 5 | 95 | %RH | Note 1 |
| Vibration | | | 1.5 10-200 | G Hz | |
| Shock | | | 50 18 | G ms | Rectangle wave |

Note 1 : Maximum Wet-Bulb should be 39 degree C and No condensation.

Note 2 : Duration : 50msec Max. Ta=0 degree C

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

| Item | Conditions | Specification | |
|---|---------------------|---|-------|
| | | Typ. | Note |
| Viewing Angle (Degrees) | Horizontal (Right) | 40 | - |
| | $K \geq 10$ (Left) | 40 | - |
| K:Contrast Ratio | Vertical (Upper) | 15 | - |
| | $K \geq 10$ (Lower) | 30 | - |
| Contrast ratio | | 200 | - |
| Response Time (ms) | Rising | 30 | 50Max |
| | Falling | 30 | 50Max |
| Color Chromaticity (CIE) | Red x | 0.569 | - |
| | Red y | 0.332 | - |
| | Green x | 0.312 | - |
| | Green y | 0.544 | - |
| | Blue x | 0.149 | - |
| | Blue y | 0.132 | - |
| | White x | 0.313 | - |
| | White y | 0.329 | - |
| White Luminance (cd/m ²) ICFL 6.5 mA | | 150Typ. Center 140Typ. 5 points average | |

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

| | |
|-------------------------------|----------------------|
| Connector Name / Designation | For Signal Connector |
| Manufacturer | JAE |
| Type / Part Number | FI-XB30S-HF10 |
| Mating Receptacle Manufacture | JAE |
| Mating Receptacle/Part Number | FI-X30M |

| | |
|------------------------------|--------------------|
| Connector Name / Designation | For Lamp Connector |
| Manufacturer | JST |
| Type / Part Number | BHSR-02VS-1 |
| Mating Type / Part Number | SM02B-BHSS-1 |

5.2 Interface Signal Connector

| Pin # | Signal Name |
|-------|-------------|
| 1 | FG (GND) |
| 2 | GND |
| 3 | VDD |
| 4 | VDD |
| 5 | Reserved |
| 6 | Reserved |
| 7 | Reserved |
| 8 | Reserved |
| 9 | ReIN0- |
| 10 | ReIN0+ |
| 11 | GND |
| 12 | ReIN1- |
| 13 | ReIN1+ |
| 14 | GND |
| 15 | ReIN2- |
| 16 | ReIN2+ |

| Pin # | Signal Name |
|-------|-------------|
| 17 | GND |
| 18 | ReCLKIN- |
| 19 | ReCLKIN+ |
| 20 | GND |
| 21 | RoIN0- |
| 22 | RoIN0+ |
| 23 | GND |
| 24 | RoIN1- |
| 25 | RoIN1+ |
| 26 | GND |
| 27 | RoIN2- |
| 28 | RoIN2+ |
| 29 | GND |
| 30 | RoCLKIN- |
| 31 | RoCLKIN+ |
| 32 | FG (GND) |

Note:

'Reserved' pins are not allowed to connect any other line.

Voltage levels of all input signals are LVDS compatible (except VDD). Refer to "Signal Electrical Characteristics for LVDS(*)", for voltage levels of all input signals.

5.3 Interface Signal Description

The module uses a pair of LVDS receiver SN75LVDS86(Texas Instruments) compatible. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84/85 or compatible.

| PIN # | SIGNAL NAME | Description |
|-------|-------------|--|
| 1 | FG | Frame Ground |
| 2 | GND | Ground |
| 3 | VDD | +3.3V Power Supply |
| 4 | VDD | +3.3V Power Supply |
| 5 | Reserved | Reserved |
| 6 | Reserved | Reserved |
| 7 | Reserved | Reserved |
| 8 | Reserved | Reserved |
| 9 | ReIN0- | Negative LVDS differential data input (Even R0-R5, G0) |
| 10 | ReIN0+ | Positive LVDS differential data input (Even R0-R5, G0) |
| 11 | GND | Ground |
| 12 | ReIN1- | Negative LVDS differential data input (Even G1-G5, B0-B1) |
| 13 | ReIN1+ | Positive LVDS differential data input (Even G1-G5, B0-B1) |
| 14 | GND | Ground |
| 15 | ReIN2- | Negative LVDS differential data input (Even B2-B5, HSYNC, VSYNC, DSPTMG) |
| 16 | ReIN2+ | Positive LVDS differential data input (Even B2-B5, HSYNC, VSYNC, DSPTMG) |
| 17 | GND | Ground |
| 18 | ReCLKIN- | Negative LVDS differential clock input (Even) |
| 19 | ReCLKIN+ | Positive LVDS differential clock input (Even) |
| 20 | GND | Ground |
| 21 | RoIN0- | Negative LVDS differential data input (Odd R0-R5, G0) |
| 22 | RoIN0+ | Positive LVDS differential data input (Odd R0-R5, G0) |
| 23 | GND | Ground |
| 24 | RoIN1- | Negative LVDS differential data input (Odd G1-G5, B0-B1) |
| 25 | RoIN1+ | Positive LVDS differential data input (Odd G1-G5, B0-B1) |
| 26 | GND | Ground |
| 27 | RoIN2- | Negative LVDS differential data input (Odd B2-B5) |
| 28 | RoIN2+ | Positive LVDS differential data input (Odd B2-B5) |
| 29 | GND | Ground |
| 30 | RoCLKIN- | Negative LVDS differential clock input (Odd) |
| 31 | RoCLKIN+ | Positive LVDS differential clock input (Odd) |
| 32 | FG | Frame Ground |

Note:

Input signals of odd and even clock shall be the same timing.

The module uses a 100ohm resistor between positive and negative data lines of each receiver input.

Even : First Pixel data

Odd : Second Pixel Data

| SIGNAL NAME | Description |
|--|---|
| +RED 5 +RED 4 +RED 3 +RED 2 +RED 1 +RED 0 (EVEN/ODD) | RED Data 5 (MSB) RED Data 4 RED Data 3 RED Data 2 RED Data 1 RED Data 0 (LSB) Red-pixel Data: Each red pixel's brightness data consists of these 6 bits pixel data. |
| +GREEN 5 +GREEN 4 +GREEN 3 +GREEN 2 +GREEN 1 +GREEN 0 (EVEN/ODD) | GREEN Data 5 (MSB) GREEN Data 4 GREEN Data 3 GREEN Data 2 GREEN Data 1 GREEN Data 0 (LSB) Green-pixel Data: Each green pixel's brightness data consists of these 6 bits pixel data. |
| +BLUE 5 +BLUE 4 +BLUE 3 +BLUE 2 +BLUE 1 +BLUE 0 (EVEN/ODD) | BLUE Data 5 (MSB) BLUE Data 4 BLUE Data 3 BLUE Data 2 BLUE Data 1 BLUE Data 0 (LSB) Blue-pixel Data: Each blue pixel's brightness data consists of these 6 bits pixel data. |
| -DTCLK (EVEN/ODD) | Data Clock: The typical frequency is 54MHz. The signal is used to strobe the pixel +data and the +DSPTMG |
| +DSPTMG | Display Timing: When the signal is high, the pixel data shall be valid to be displayed. |
| VSYNC | Vertical Sync: This signal is synchronized with -DTCLK. Both active high/low signals are acceptable. |
| HSYNC | Horizontal Sync: This signal is synchronized with -DTCLK. Both active high/low signals are acceptable. |
| VDD | +3.3V Power Supply |
| GND | Ground |

Note: Output signals from any system shall be Hi-Z state when VDD is off.

5.4 Interface Signal Electrical Characteristics

5.4.1 Signal Electrical Characteristics for LVDS Receiver

Table . Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|--------------------------------------|-----------------|-------------------|-----|-----------------|------|------------|
| Differential Input High Threshold | Vth | | | +100 | mV | |
| Differential Input Low Threshold | Vtl | -100 | | | mV | |
| Magnitude Differential Input Voltage | Vid | 100 | | 600 | mV | |
| Common Mode Voltage | Vcm | 0.825 + Vid /2 | | 2.4 - Vid /2 | V | |
| Common Mode Voltage Offset | ΔV_{cm} | -50 | | +50 | mV | |

Note:

- Input signals shall be low or Hi-Z state when VDD is off.

Figure . Voltage Definitions

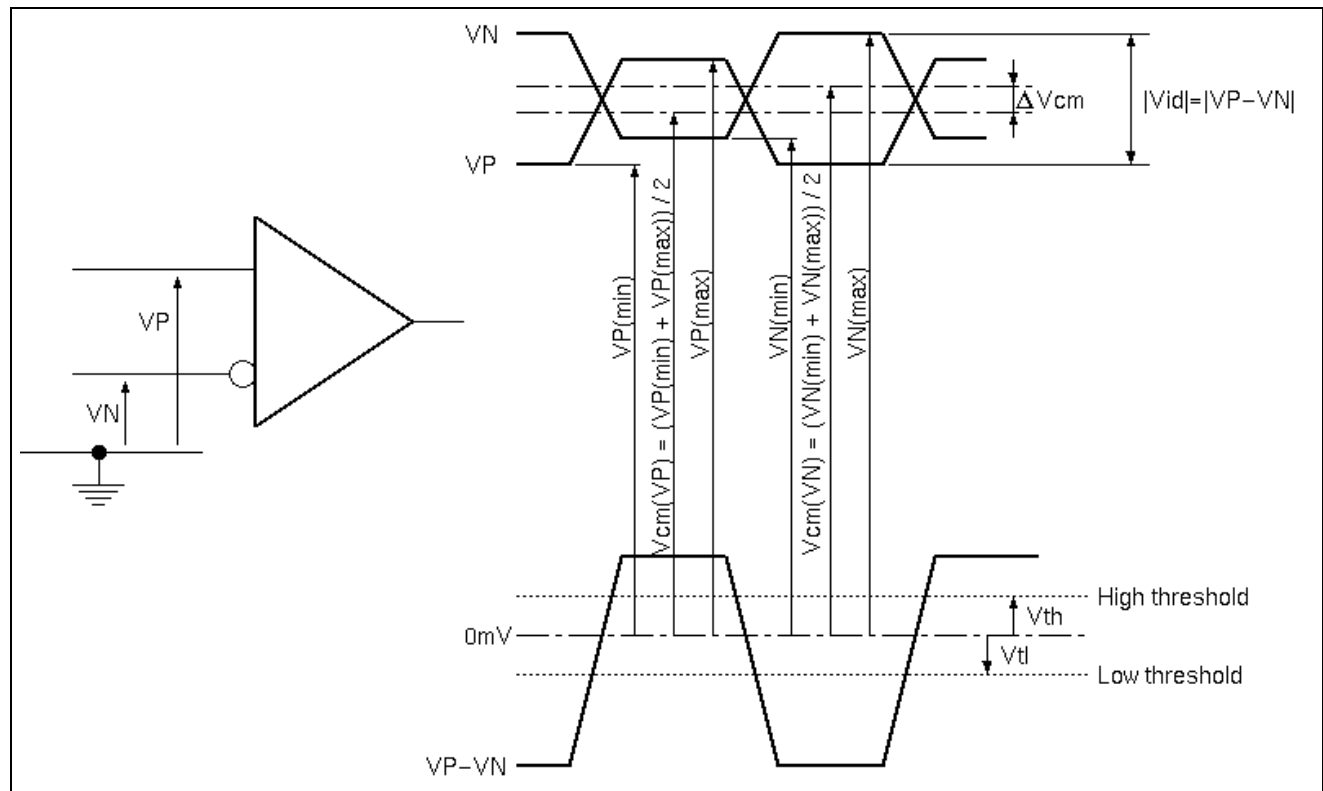


Table . Switching Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|-----------------------------|--------|------|------|------|----------|---------------------------|
| Clock Frequency | fc | 51 | 54 | 57 | MHz | |
| Cycle Time | tc | 17.5 | 18.5 | 19.6 | ns | |
| Data Setup Time | Tsu | 700 | | | ps | fc = 54MHz, jitter < 50ps |
| Data Hold Time | Thd | 700 | | | ps | |
| Cycle modulation rate(Note) | tCJavg | | | 20 | ps/clock | |

Note: This specification defines maximum average cycle modulation rate in peak-to-peak transition within any 100 clock cycles. This specification is applied only if input clock peak jitter within any 100 clock cycles is greater than 300ps.

Figure . Timing Definition (Even)

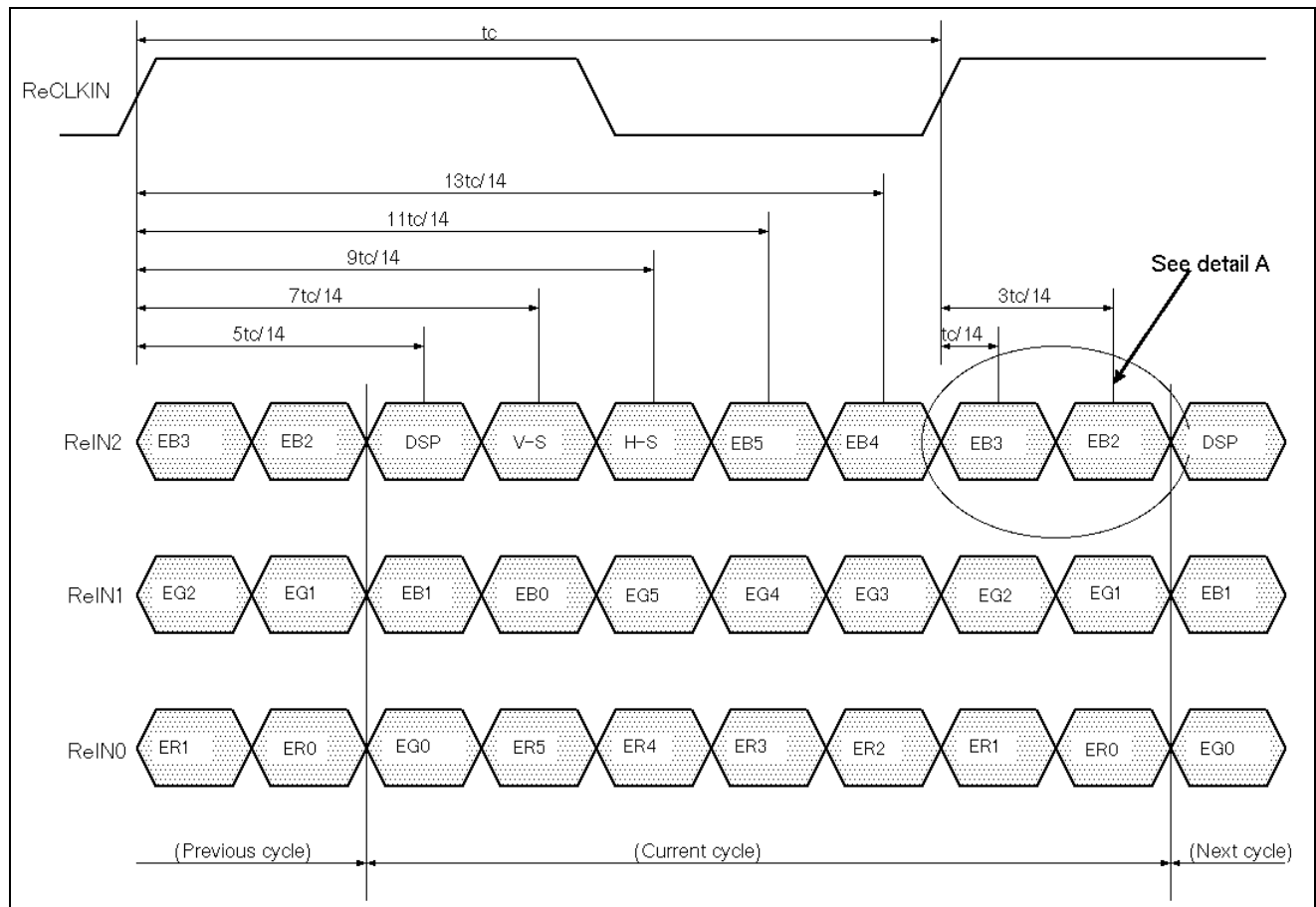


Figure . Timing Definition (Odd)

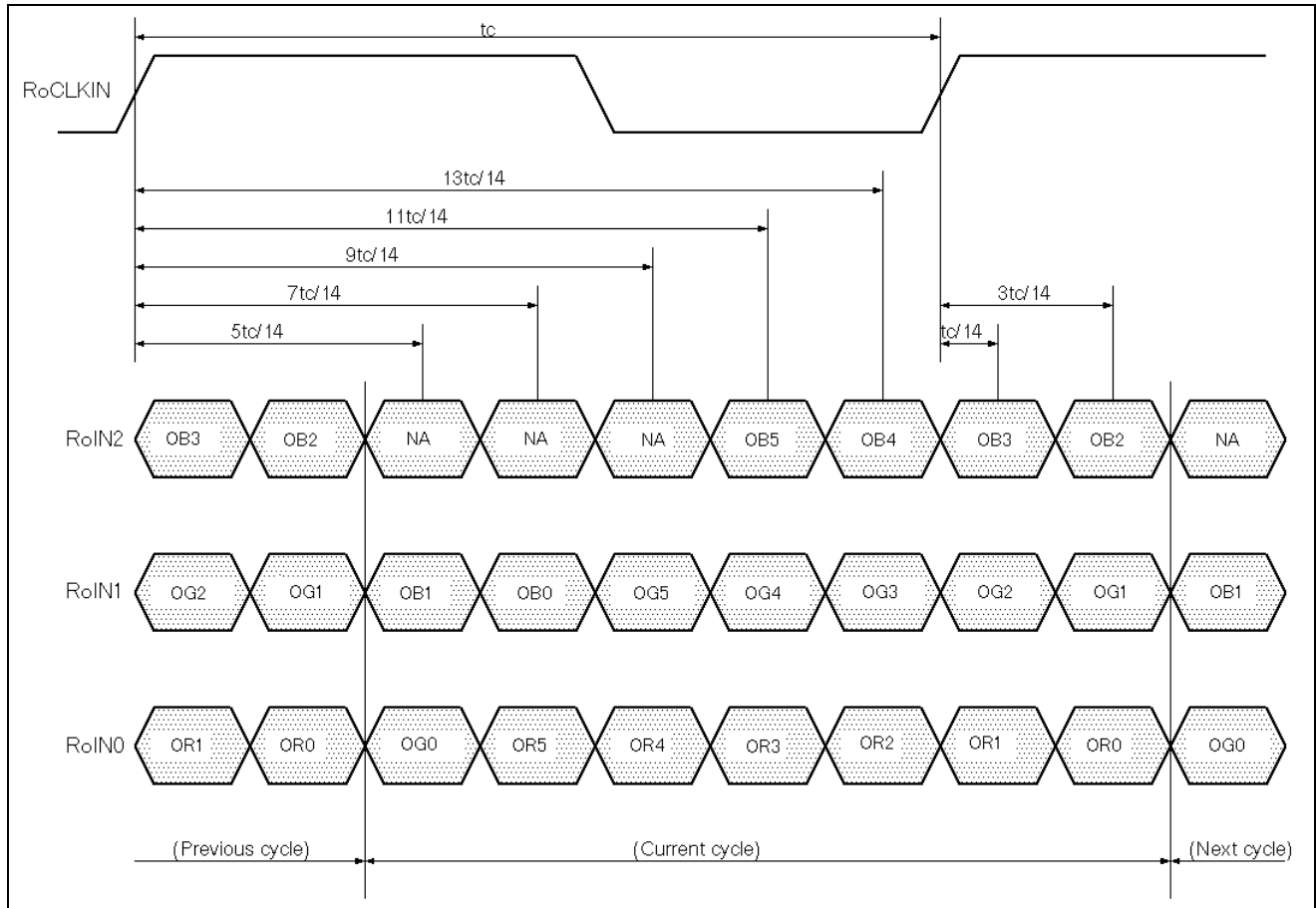
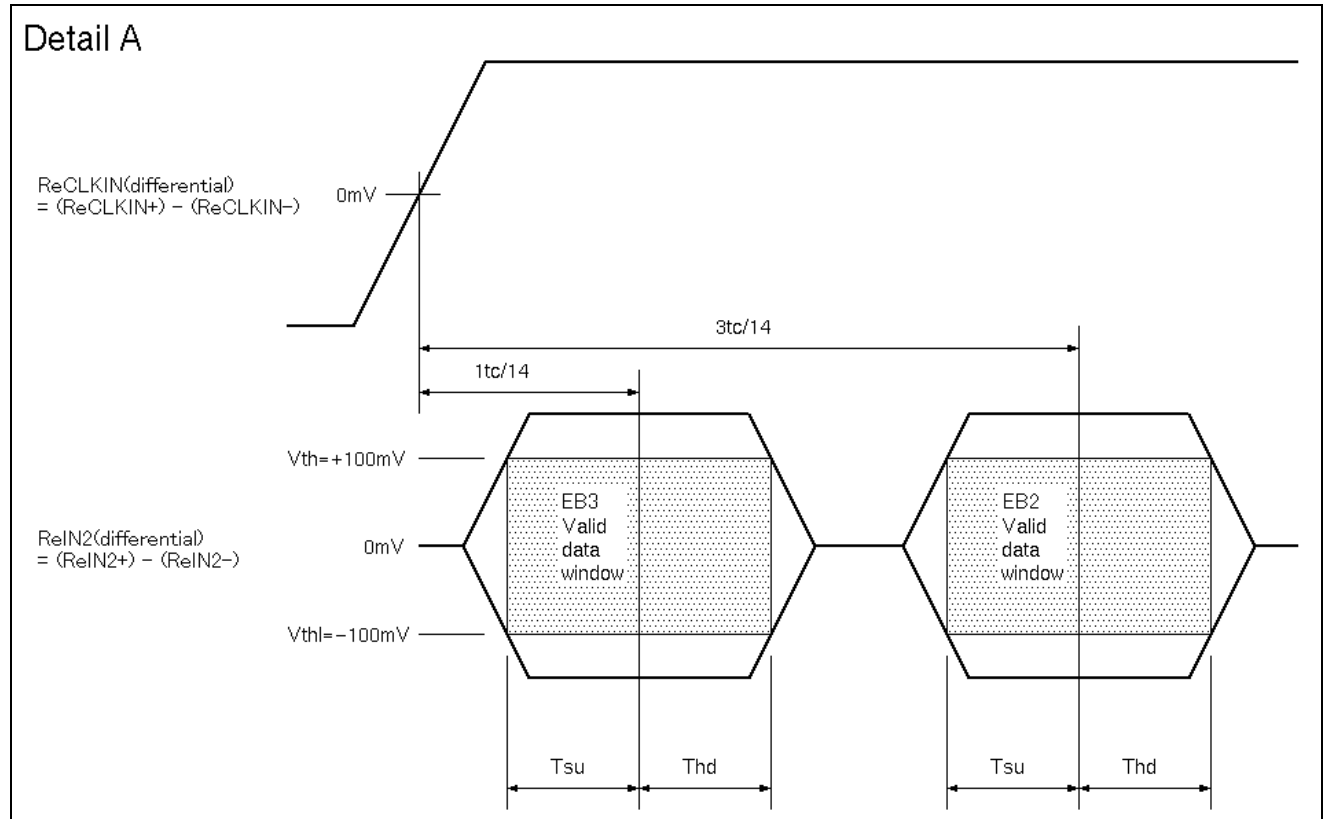
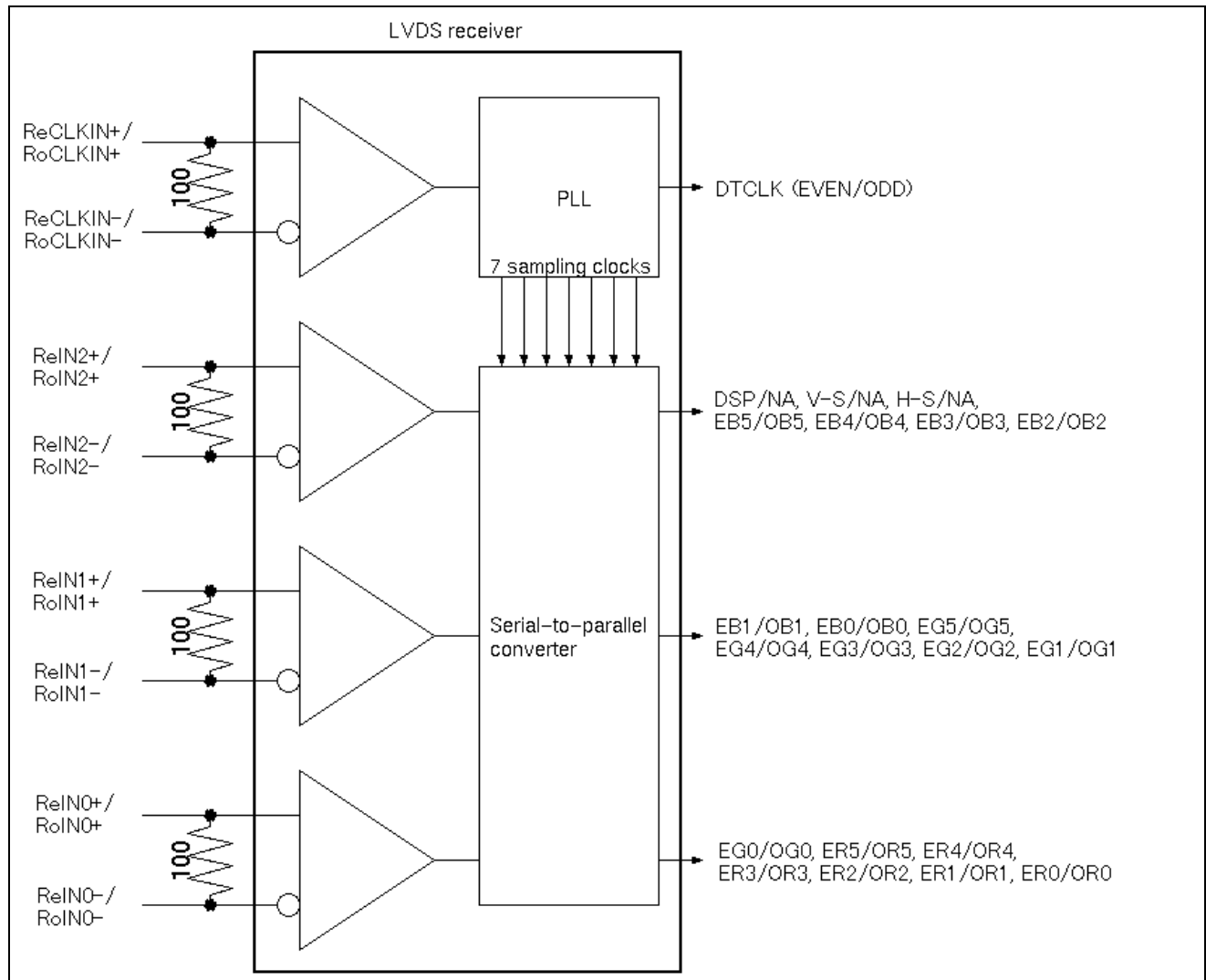


Figure . Timing Definition(detail A)



5.4.2 LVDS Receiver Internal Circuit

Below figure shows the internal block diagram of the LVDS receiver.

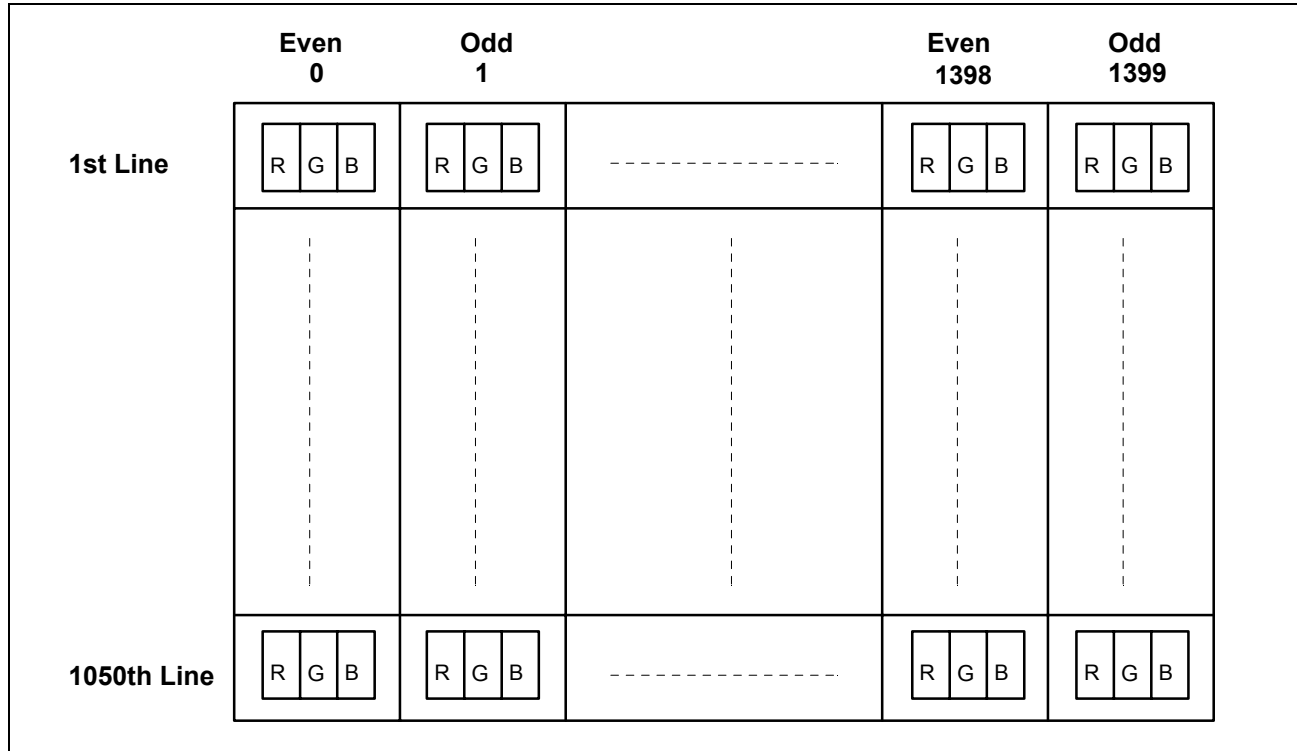


5.5 Signal for Lamp Connector

| Pin # | Signal Name |
|-------|-------------------|
| 1 | Lamp High Voltage |
| 2 | Lamp Low Voltage |

6.0 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format image. Even and odd pair of RGB data are sampled at a time.



7.0 Parameter guide line for CFL Inverter

| PARAMETER | MIN | DP-1 | DP-2 | MAX | UNITS | CONDITION |
|---|--------|----------|------------|--------|-------------------|--------------------------------|
| White Luminance (Center) (5 Points average) | - - | 90 85 | 150 140 | - - | cd/m ² | (Ta=25 deg.C) |
| CFL current(ICFL) | 3.0 | 3.5 | 6.5 | 7.0 | mArms | (Ta=25 deg.C) |
| CFL Frequency(FCFL) | 40 | | | 60 | KHz | (Ta=25 deg.C) Note 1 |
| CFL Ignition Voltage(Vs) | 1,500 | - | - | - | Vrms | (Ta= 0 deg.C) Note 3 |
| CFL Voltage (Reference)(VCFL) | - | 730 | 635 | - | Vrms | (Ta=25 deg.C) Note 2 |
| CFL Power consumption(PCFL) | - | 2.6 | 4.2 | - | W | (Ta=25 deg.C) Note 2 |

Note 1: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

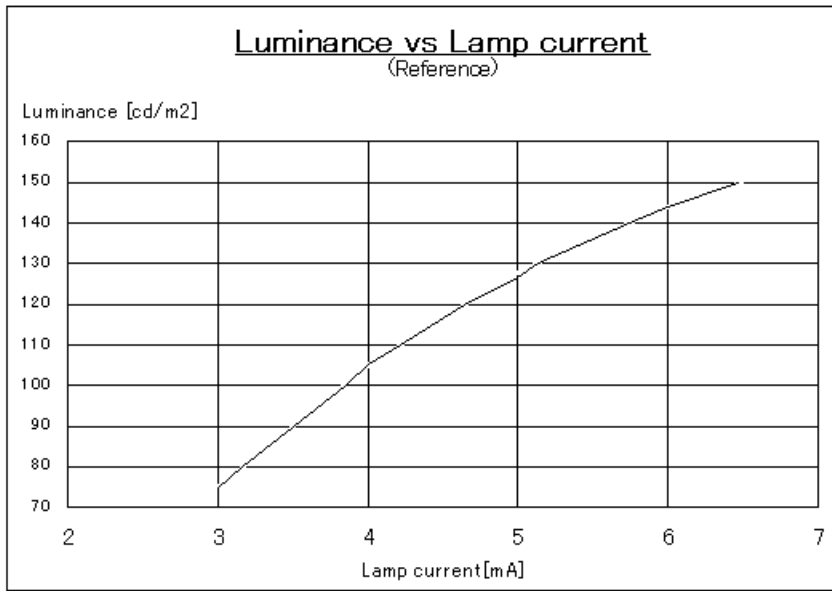
Note 2: Calculated value for reference (ICFL x VCFL = PCFL).

Note 3: CFL inverter should be able to give out a power that has a generating capacity of over 1,500 voltage. Lamp units need 1,500 voltage minimum for ignition.

Note 4: DP-1 and DP-2 are recommended Design Points.

- *1 All of characteristics listed are measured under the condition using the Test inverter.
- *2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.
- *3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.
- *4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.
- *5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.
- *6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.
- *7 It should be employed the inverter which has 'Duty Dimming', if ICFL is less than 4[mA].

The following chart is CFL current versus the luminance for your reference.



8.0 Interface Timings

Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS86(Texas Instruments) or equivalent.

8.1 Timing Characteristics

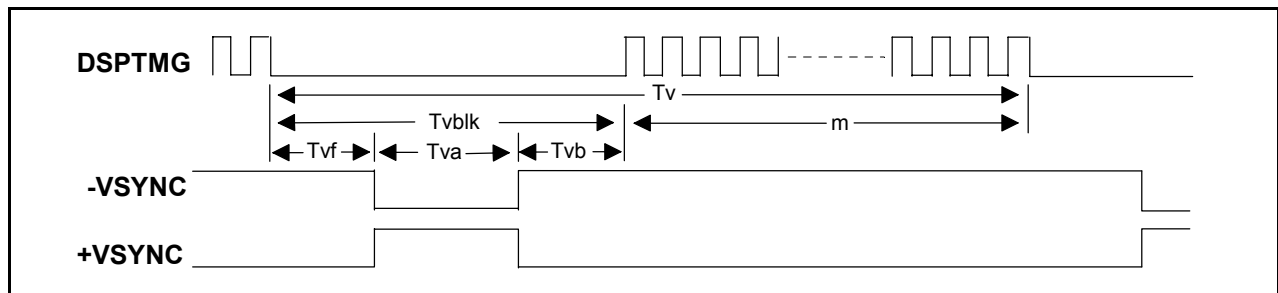
| Signal | Item | Symbol | MIN. | TYP. | MAX. | Unit |
|---------|----------------|--------|-------|-------|------|---------|
| DTCLK | Frequency | Fdck | 51 | 54 | 57 | [MHz] |
| | | Tck | | 18.5 | | [ns] |
| +V-Sync | Frame Rate | Fv | | 60 | | [Hz] |
| | | Tv | | 16.67 | | [ms] |
| | | Nv | 1058 | 1066 | 2046 | [lines] |
| | V-Active Level | Tva | 15.78 | 46.7 | | [us] |
| | | Nva | 1 | 3 | 62 | [lines] |
| | V-Back Porch | Nvb | 6 | 12 | 125 | [lines] |
| | V-Front Porch | Nvf | 1 | 1 | | [lines] |
| +DSPTMG | V-Line | m | | 1050 | | [lines] |
| +H-Sync | Scan Rate | Fh | | 63.98 | | [KHz] |
| | | Th | | 15.63 | | [usec] |
| | | Nh | 762 | 844 | 1023 | [Tck] |
| | H-Active Level | Tha | | 1.037 | | [usec] |
| | | Tha | 8 | 56 | 250 | [Tck] |
| | H-Back Porch | Thb | 26 | 64 | 300 | [Tck] |
| | H-Front Porch | Thf | 8 | 24 | | [Tck] |
| +DSPTMG | Display | Thd | | 12.96 | | [usec] |
| +DATA | Data Even/Odd | n | | 1400 | | [dots] |

Note:Both positive Hsync and positive Vsync polarity is recommended

8.2 Timing Definition

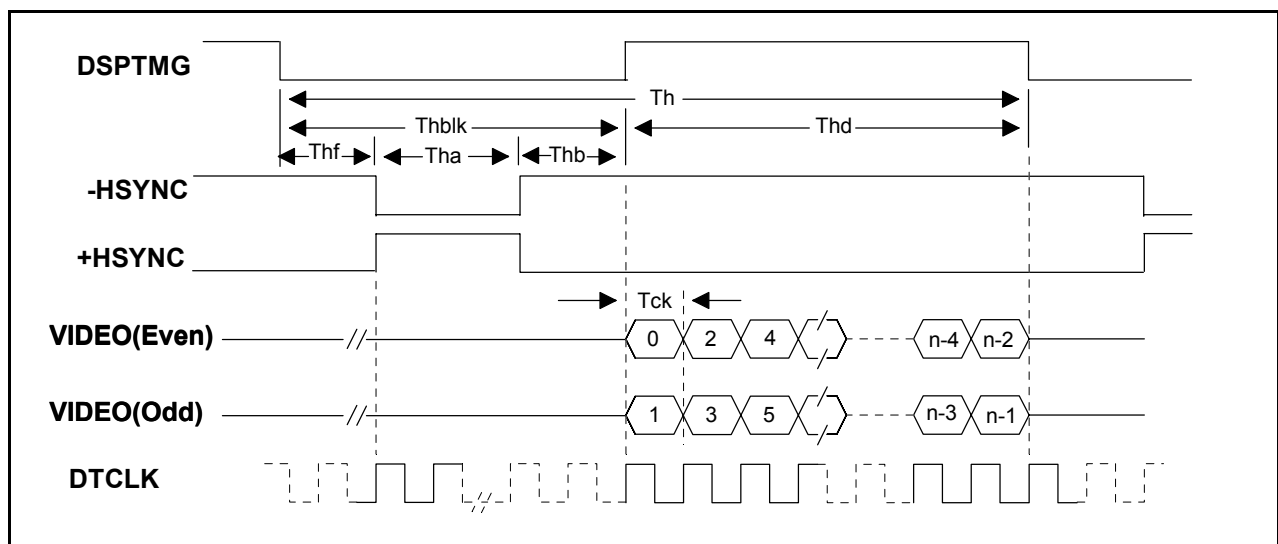
Vertical Timing

| Support mode | Tvblk Vertical Blanking | m Active Field | Tvf VSYNC Front Porch | Tv,Nv Frame Time | Tva VSYNC Width | Tvb VSYNC Back Porch |
|---|-------------------------------|---------------------------|--------------------------|---------------------------|-----------------------|----------------------------|
| 1400 x 1050 at 60Hz (H line rate : 15.63 us) | 0.250 ms (16 lines) | 16.411 ms (1050 lines) | 0.016 ms (1 line) | 16.661 ms (1066 lines) | 0.047 ms (3 lines) | 0.188 ms (12 lines) |



Horizontal Timing

| Support mode | Thblk Horizontal Blanking | Thd Active Field | Thf HSYNC Front Porch | Th,Nh H Line Time | Tha HSYNC Width | Thb HSYNC Back Porch |
|---|---------------------------------|--------------------------|--------------------------|--------------------------|------------------------|----------------------------|
| 1400 x 1050 Dotclock : 108.000 MHz (54.000MHz x2) | 2.667 us (288 dots) | 12.963 us (1400 dots) | 0.444 us (48 dots) | 15.630 us (1688 dots) | 1.037 us (112 dots) | 1.185 us (128 dots) |



9.0 Power Consumption

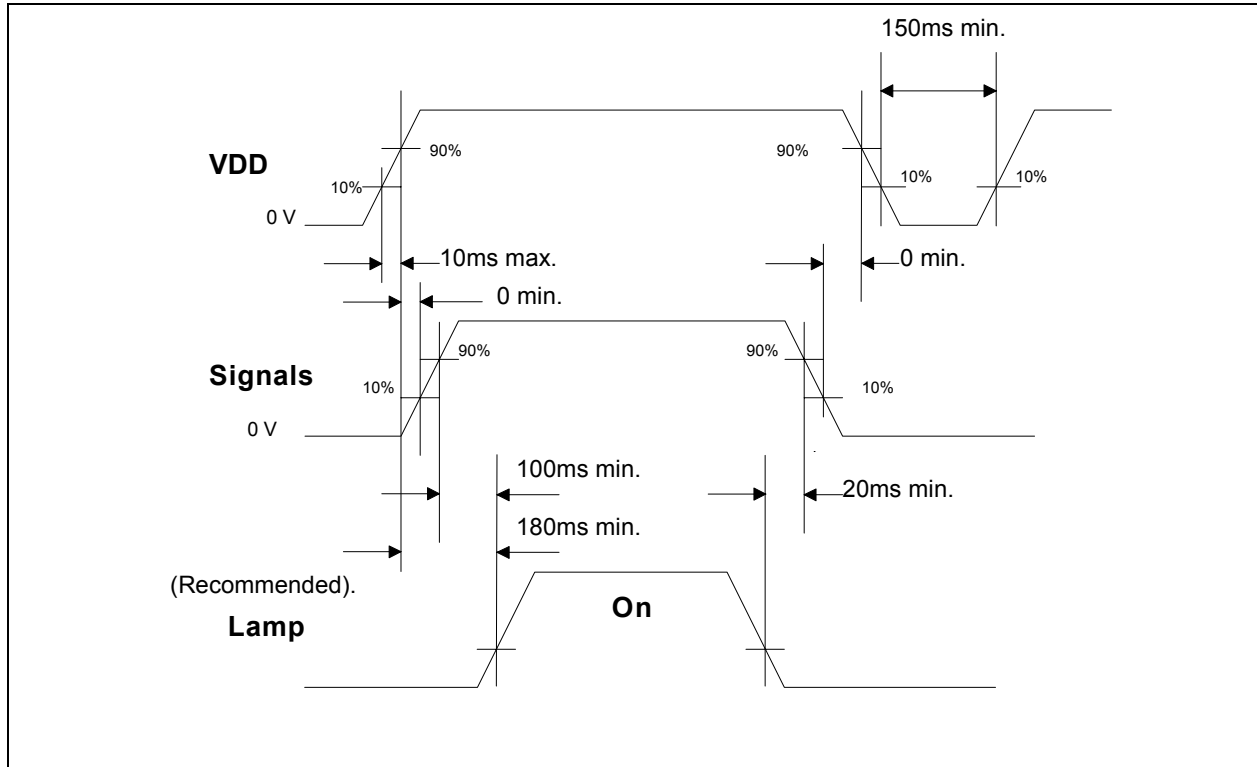
Input power specifications are as follows;

| SYMBOL | PARAMETER | Min | Typ | Max | UNITS | CONDITION |
|---------|--|-----|-----|-----|-------|--------------------------------------|
| VDD | Logic/LCD Drive Voltage | 3 | 3.3 | 3.6 | V | Load Capacitance 40uF |
| PDD | VDD Power Max | | | 3.2 | W | MAX Pattern VDD=3.6V |
| PDD | VDD Power | | 1.8 | | W | All Black Pattern VDD=3.3V |
| IDD Max | IDD Current Max | | | 890 | mA | MAX Pattern VDD=3.6V |
| IDD | IDD Current | | 545 | | mA | All Black Pattern VDD=3.3V |
| VDDrp | Allowable Logic/LCD Drive Ripple Voltage | | | 100 | mVp-p | |
| VDDns | Allowable Logic/LCD Drive Ripple Noise | | | 100 | mVp-p | |

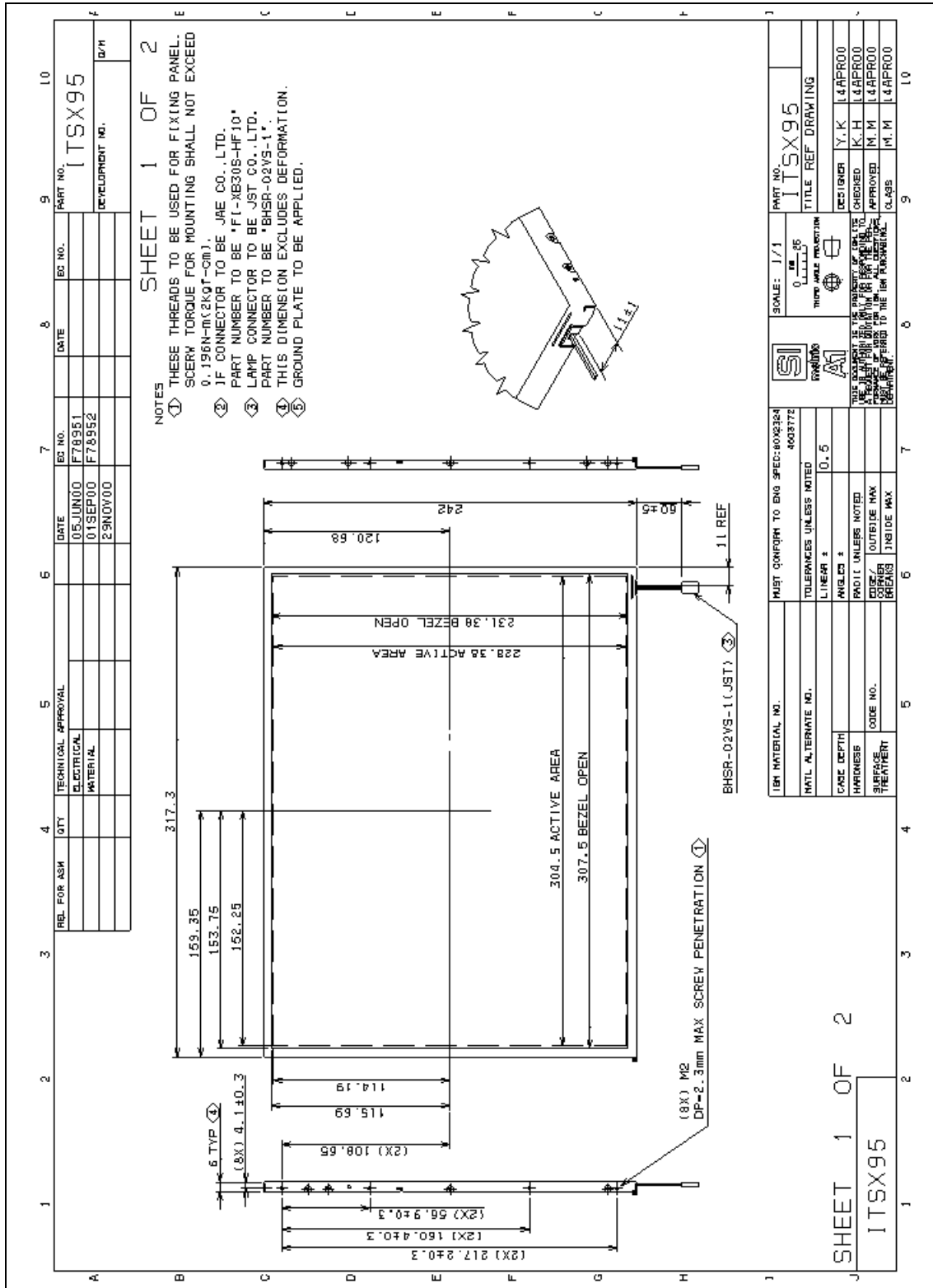
Note:Max Pattern:2 dot Vertical sub-pixel stripe.

10.0 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



11.0 Mechanical Characteristics



NOTES

SHEET 1 OF 2

① THESE THREADS TO BE USED FOR FIXING PANEL. SCREW TORQUE FOR MOUNTING SHALL NOT EXCEED 0.196N-M(2KGT-CM).

② IF CONNECTOR TO BE JAE CO., LTD. PART NUMBER TO BE *F(-)XB30S-HF10*

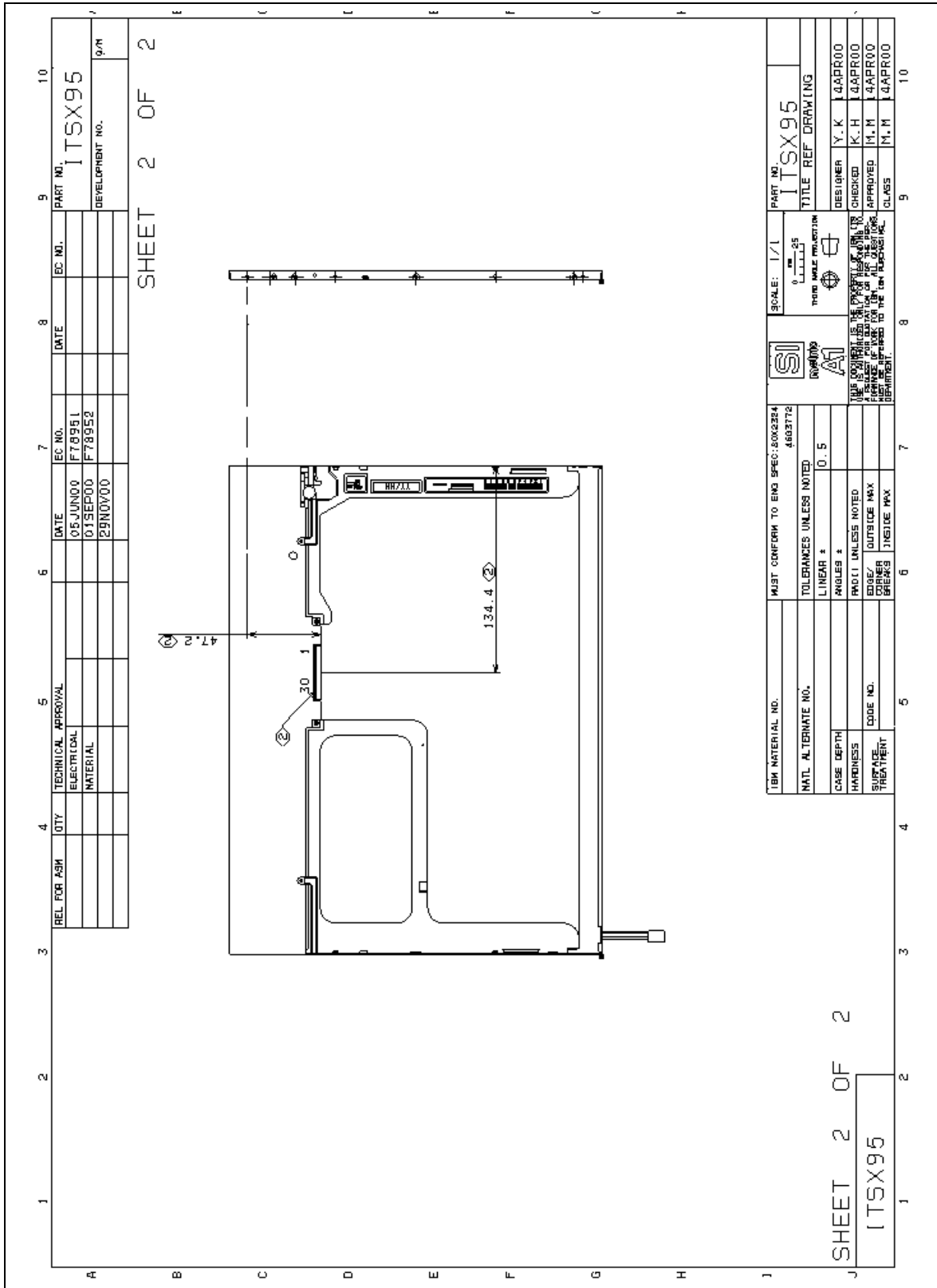
③ LAMP CONNECTOR TO BE JST CO., LTD. PART NUMBER TO BE *BHSR-02VS-1*

④ THIS DIMENSION EXCLUDES DEFORMATION.

⑤ GROUND PLATE TO BE APPLIED.

| | | | | | | | |
|-------------|-----|--------------------|-----------|--------|------|--------|-----------------|
| REL FOR ASM | QTY | TECHNICAL APPROVAL | DATE | EC NO. | DATE | EC NO. | PART NO. |
| | | ELECTRICAL | 05 JUN 00 | F78951 | | | ITSX95 |
| | | MATERIAL | 01 SEP 00 | F78952 | | | DEVELOPMENT NO. |
| | | | 29 NOV 00 | | | | D/M |

| | | | | | | | |
|-------------------------|--|----------------------------------|--|-----------------|--|--------------------------|--|
| MATERIAL NO. | | MUST CONFORM TO ENG SPEC: 002324 | | SCALE: 1/1 | | PART NO. ITSX95 | |
| MATERIAL ALTERNATE NO. | | 4003172 | | 0.5 | | TITLE REF DRAWING | |
| TOLERANCES UNLESS NOTED | | LINEAR ± | | TYPICAL SECTION | | DESIGNER Y.K. [4 APR 00] | |
| FACE DEPTH | | ANGLES ± | | FORMING | | CHECKED K.H. [4 APR 00] | |
| HARDNESS | | RADI I UNLESS NOTED | | FINISH | | APPROVED M.M. [4 APR 00] | |
| SURFACE TREATMENT | | OUTSIDE MAX | | DRAWING | | CLASS M.M. [4 APR 00] | |
| | | INSIDE MAX | | DATE | | | |



| REL FOR ASB | QTY | TECHNICAL APPROVAL | | DATE | EC NO. | DATE | EC NO. | PART NO. | |
|-------------|-----|--------------------|--|---------|--------|------|--------|-----------------|-----|
| | | ELECTRICAL | | 05JUN00 | F78951 | | | ITSX95 | |
| | | MATERIAL | | 01SEP00 | F78952 | | | | |
| | | | | 29NOV00 | | | | | |
| | | | | | | | | DEVELOPMENT NO. | 9/M |

SHEET 2 OF 2

| IBM MATERIAL NO. | | MUST CONFORM TO ENG SPEC: 8062284 | | SCALE: | 1/1 | PART NO. |
|---------------------|--|-----------------------------------|--|-----------------------|-----|----------|
| NATL. ALTERNATE NO. | | 4803772 | | 1/1 | | ITSX95 |
| CASE DEPTH | | 10.5 | | TITLE REF DRAWING | | |
| HARDNESS | | | | DESIGNER Y. K. QAPROO | | |
| SURFACE TREATMENT | | | | CHECKED K. H. QAPROO | | |
| | | | | APPROVED M. M. QAPROO | | |
| | | | | CLASS M. M. QAPROO | | |

SHEET 2 OF 2
ITSX95

12.0 National Test Lab Requirement

The display module is authorized to Apply the UL Recognized Mark.

Conditions of Acceptability

- This component has been judged on the basis of the required spacings in the Standard for Safety of Information Technology Equipment, Including Electrical Business Equipment, CAN/CSA C22.2 No.950-95 *UL 1950, Third Edition, including revisions through revision date March 1,1998, which are based on the Fourth Amendment to IEC 950, Second Edition, which would cover the component itself if submitted for Listing.
- CF Lamp circuit for this model should be supplied from Limited Current Circuit.
- The units are supplied by Limited Power Sources.
- The terminals and connectors are suitable for factory wiring only.
- The terminals and connectors have not been evaluated for field wiring.
- A suitable Electrical and Fire enclosure shall be provided.

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