Engineering Specification

Type 15.0 UXGA Color TFT/LCD Module
Model Name:ITUX97H

Document Control Number : OEM I-97H-03

Note:Specification is subject to change without notice. Consequently it is better to contact to International Display Technology before proceeding with the design of your product incorporating this module.

Sales Support
International Display Technology

i Contents

ii Record of Revision

Date	Document Revision	Page	Summary
October 30,2001	OEM I-97H-01	All	First Edition for customer. Based on Internal Specification EC F79204 as of September 7,2001. To adopt a "Burst mode Inverter".
December 10,2001	OEM I-97H-02	6 9 23 24	To update Backlight Power Consumption. To add Min. value of White Luminance. To update Electrical Specifications and Dimming. To update the Luminance versus the SMBUS Data.
February 1,2002	OEM I-97H-03	23 24	To update Inverter Signal Electrical Characteristics. To update Luminance versus SMBUS Data.

1.0 Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth; do not use solvents or abrasives.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) The fluorescent lamp in the liquid crystal display (LCD) contains mercury. Do not put it in trash that is disposed of in landfills. Dispose of it as required by local ordinances or regulations.
13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (2.11, IEC60950 or UL1950), or be applied exemption conditions of flammability requirements (4.4.3.3, IEC60950 or UL1950) in an end product.
14) Never apply detergent or other liquid directly to the screen.

- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by International Display Technology for any infringements of patents or other right of the third partied which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of International Display Technology or others.
- The information contained herein may be changed without prior notice. It is therefore advisable to contact International Display Technology before proceeding with the design of equipment incorporating this product.

2.0 General Description

This specification applies to the Type 15.0 Color TFT/LCD Module 'ITUX97H'.

This module is designed for a display unit of notebook style personal computer.

The screen format and electrical interface are intended to support the UXGA (1600(H) x 1200(V))screen.

Support color is native 262k colors (RGB 6-bit data driver).

All input signals are LVDS interface compatible.This module contains an inverter card for backlight.

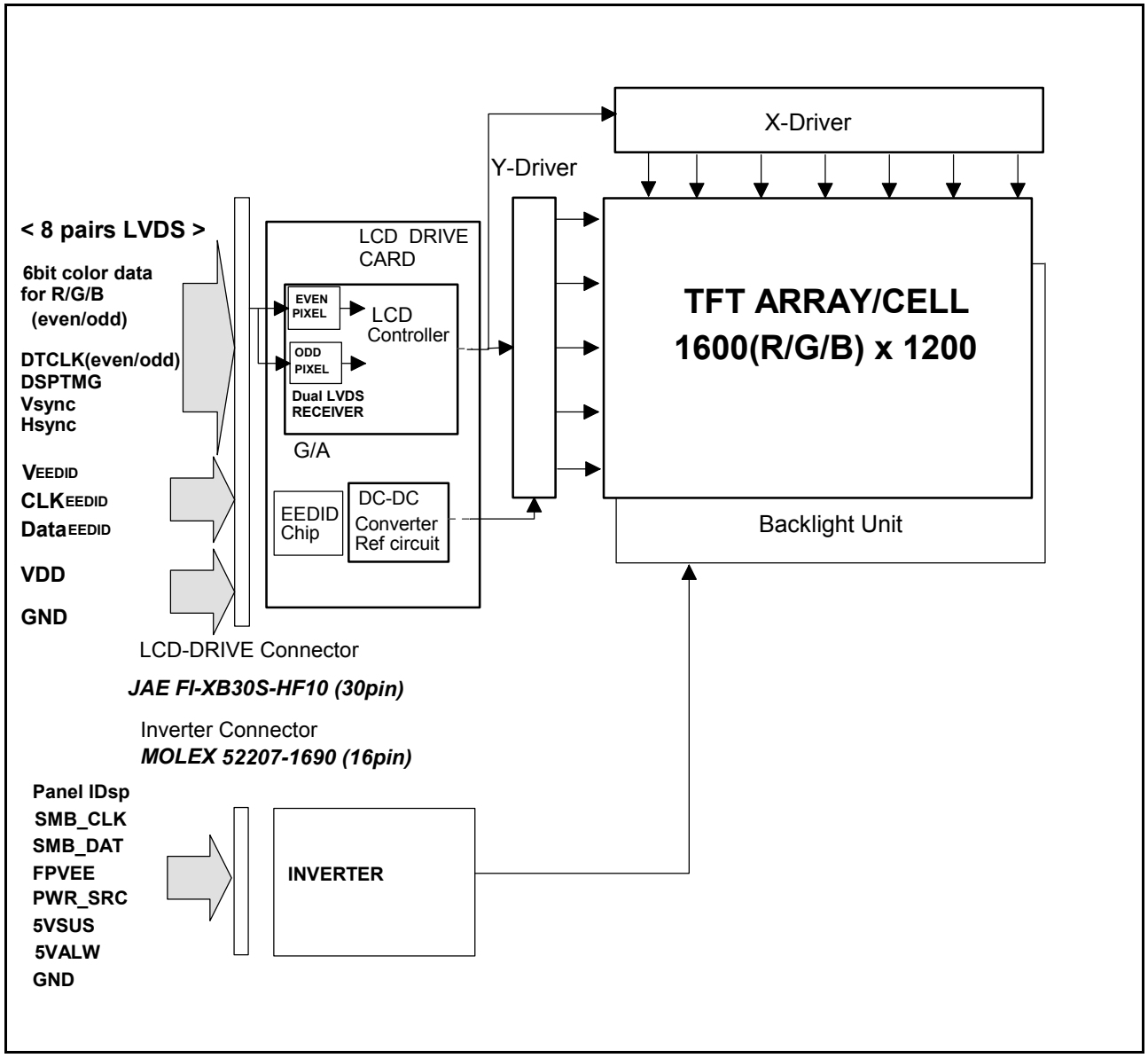
2.1 Characteristics

The following items are characteristics summary on the table under 25 degree C condition:

ITEMS	SPECIFICATIONS
Screen Diagonal [mm]	381
Active Area [mm]	304.8(H) x 228.6(V)
Pixels H x V	1600(x3) x 1200
Pixel Pitch [mm]	0.1905(per one triad) x 0.1905
Pixel Arrangement	R.G.B. Vertical Stripe
Display Mode	Normally White
Typical White Luminance [cd/m^2] SMData=00H:	150 Typ.(Center) 140 Typ.(5 Points average)
Contrast Ratio	200 : 1 Typ.
Optical Rise Time/Fall Time [msec]	30Typ., 50Max.(each)
Nominal Input Voltage [Volt] VDD 5VSUS,5VALW line PWR_SRC line	 +3.3 Typ. +5.0 Typ. +14.4 Typ.
Logic Power Consumption [watt]	2.4 Typ. 3.4 Max.
Backlight Power Consumption [watt] PWR_SRC=14.4V SMData=00H	5.6 Typ.
Weight [grams]	665 Typ. 700 Max.
Physical Size [mm]	317.3(W) x 242.0(H) x 11.2(D) Typ.11.5(D)Max.
Electrical Interface (Logic)	6-bit digital video for each color R/G/B, 3 sync, Clock (8 pairs LVDS)
Electrical Interface (Inverter)	Panel IDs,SMB_CLK,SMB_DAT,FPVEE
Support Color	Native 262K colors (RGB 6-bit data driver)
Temperature Range (degree C) Operating Storage (Shipping)	 0 to +50 -20 to +60

2.2 Functional Block Diagram

The following diagram shows the functional block of the Type 15.0 Color TFT/LCD Module.



The first LVDS port transmits even pixels while the second LVDS port transmits odd pixels.

3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

Item	Symbol	Min	Max	Unit	Conditions
Supply Voltage	VDD	-0.3	+4.0	V	
	5VSUS, 5VALW	-0.3	+5.5	V	
	PWR_SRC	-0.3	+25	V	
Input Voltage of Signal	Vin	-0.3	+VDD+0.3	V	
	FPVEE	-0.3	+5.5	V	
	SMB_CLK SMB_DAT	-1	+7	V	
Operating Temperature	TOP	0	+50	deg.C	Note 1
Operating Humidity	HOP	8	95	%RH	Note 1
Storage Temperature	TST	-20	+60	deg.C	Note 1
Storage Humidity	HST	5	95	%RH	Note 1
Vibration			1.5 10-200	G Hz	
Shock			50 18	G ms	Rectangle wave

Note 1 : Maximum Wet-Bulb should be 39 degree C and No condensation.

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

Item	Conditions	Specifiation	
		Typ.	Note
Viewing Angle (Degrees) K:Contrast Ratio	Horizontal (Right) K≧10 (Left) Vertical (Upper) K≧10 (Lower)	40 40 15 30	- - - -
Contrast ratio		200	100 Min.
Response Time (ms)	Rising	30	50 Max.
	Falling	30	50 Max.
Color Chromaticity (CIE)	Red x	0.569	-
	Red y	0.332	-
	Green x	0.312	-
	Green y	0.544	-
	Blue x	0.149	-
	Blue y	0.132	-
	White x	0.313	-
	White y	0.329	-
White Luminance (cd/m^2) SMData=00H		150 (Center) 140 (5 Points Average)	120 Min. (Center) 112 Min. (5 Points Average)

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	FI-XB30S-HF10
Mating Type / Part Number	FI-X30M

Connector Name / Designation	For Inverter Connector
Manufacturer	Molex
Type / Part Number	52207-1690
Mating Type / Part Number	(FPC)

5.2 Interface Signal Connector

Pin #	Signal Name
1	FG (GND)
2	GND
3	VDD
4	VDD
5	V_{EEDID} (Note 2,3)
6	NC (Reserved, Note 1)
7	CLK_{EEDID} (Note 2,4)
8	$Data_{EEDID}$ (Note 2,4)
9	ReIN0-
10	ReIN0+
11	GND
12	ReIN1-
13	ReIN1+
14	GND
15	ReIN2-
16	ReIN2+

Pin #	Signal Name
17	GND
18	ReCLKIN-
19	ReCLKIN+
20	GND
21	RoIN0-
22	RoIN0+
23	GND
24	RoIN1-
25	RoIN1+
26	GND
27	RoIN2-
28	RoIN2+
29	GND
30	RoCLKIN-
31	RoCLKIN+
32	FG (GND)

Note:
1. 'Reserved' pins are not allowed to connect any other line.
2. This LCD Module complies with "VESA ENHANCED EXTENDED DISPLAY IDENTIFICATION DATA STANDARD Release A, Revision 1" and supports "EEDID version 1.3".
   This module uses Serial EEPROM BR24C02FV (ROHM) or compatible as a EEDID function.
3. V_{EEDID} power source shall be the current limited circuit which has not exceeding 1A. (Reference Document : "Enhanced Display Data Channel (E-DDC™) Proposed Standard", VESA)
4. Both CLK_{EEDID} line and $Data_{EEDID}$ line are pulled-up with 10K ohm resistor to V_{EEDID} power source line at LCD panel, respectively.

Voltage levels of all input signals are LVDS compatible (except VDD,EEDID). Refer to "Signal Electrical Characteristics for LVDS(*)", for voltage levels of all input signals.

5.3 Interface Signal Description

PIN #	SIGNAL NAME	Description
1	FG	Frame Ground
2	GND	Ground
3	VDD	+3.3V Power Supply
4	VDD	+3.3V Power Supply
5	V_{EEDID}	EEDID 3.3V Power Supply
6	Reserved	Reserved
7	CLK_{EEDID}	EEDID Clock
8	$Data_{EEDID}$	EEDID Data
9	ReIN0-	Negative LVDS differential data input (Even R0-R5, G0)
10	ReIN0+	Positive LVDS differential data input (Even R0-R5, G0)
11	GND	Ground
12	ReIN1-	Negative LVDS differential data input (Even G1-G5, B0-B1)
13	ReIN1+	Positive LVDS differential data input (Even G1-G5, B0-B1)
14	GND	Ground
15	ReIN2-	Negative LVDS differential data input (Even B2-B5, HSYNC, VSYNC, DSPTMG)
16	ReIN2+	Positive LVDS differential data input (Even B2-B5, HSYNC, VSYNC, DSPTMG)
17	GND	Ground
18	ReCLKIN-	Negative LVDS differential clock input (Even)
19	ReCLKIN+	Positive LVDS differential clock input (Even)
20	GND	Ground
21	RoIN0-	Negative LVDS differential data input (Odd R0-R5, G0)
22	RoIN0+	Positive LVDS differential data input (Odd R0-R5, G0)
23	GND	Ground
24	RoIN1-	Negative LVDS differential data input (Odd G1-G5, B0-B1)
25	RoIN1+	Positive LVDS differential data input (Odd G1-G5, B0-B1)
26	GND	Ground
27	RoIN2-	Negative LVDS differential data input (Odd B2-B5)
28	RoIN2+	Positive LVDS differential data input (Odd B2-B5)
29	GND	Ground
30	RoCLKIN-	Negative LVDS differential clock input (Odd)
31	RoCLKIN+	Positive LVDS differential clock input (Odd)
32	FG	Frame Ground

Note:
1. Input signals of odd and even clock shall be the same timing.
2. The module uses a 100ohm resistor between positive and negative data lines of each receiver input.
3. Even: First Pixel , Odd: Second Pixel

SIGNAL NAME	Description
+RED 5 (ER5/OR5) +RED 4 (ER4/OR4) +RED 3 (ER3/OR3) +RED 2 (ER2/OR2) +RED 1 (ER1/OR1) +RED 0 (ER0/OR0) (EVEN/ODD)	RED Data 5 (MSB) RED Data 4 RED Data 3 RED Data 2 RED Data 1 RED Data 0 (LSB) Red-pixel Data: Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN 5 (EG5/OG5) +GREEN 4 (EG4/OG4) +GREEN 3 (EG3/OG3) +GREEN 2 (EG2/OG2) +GREEN 1 (EG1/OG1) +GREEN 0 (EG0/OG0) (EVEN/ODD)	GREEN Data 5 (MSB) GREEN Data 4 GREEN Data 3 GREEN Data 2 GREEN Data 1 GREEN Data 0 (LSB) Green-pixel Data: Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 (EB5/OB5) +BLUE 4 (EB4/OB4) +BLUE 3 (EB3/OB3) +BLUE 2 (EB2/OB2) +BLUE 1 (EB1/OB1) +BLUE 0 (EB0/OB0) (EVEN/ODD)	BLUE Data 5 (MSB) BLUE Data 4 BLUE Data 3 BLUE Data 2 BLUE Data 1 BLUE Data 0 (LSB) Blue-pixel Data: Each blue pixel's brightness data consists of these 6 bits pixel data.
DTCLK (EVEN/ODD)	Data Clock: The typical frequency is 81MHz. The signal is used to strobe the pixel +data and the +DSPTMG
+DSPTMG (DSP)	When the signal is high, the pixel data shall be valid to be displayed.
VSYNC (V-S)	Vertical Sync: This signal is synchronized with DTCLK. Both active high/low signals are acceptable.
HSYNC (H-S)	Horizontal Sync: This signal is synchronized with DTCLK. Both active high/low signals are acceptable.
VDD	Power Supply
GND	Ground
V_{EEDID}	EEDID 3.3V Power Supply
CLK_{EEDID}	EEDID Clock
$Data_{EEDID}$	EEDID Data

Note: Output signals except V_{EEDID} ,CLK_{EEDID} and $Data_{EEDID}$ from any system shall be Hi-Z state when VDD is off.

5.4 Interface Signal Electrical Characteristics

5.4.1 Signal Electrical Characteristics for LVDS Receiver

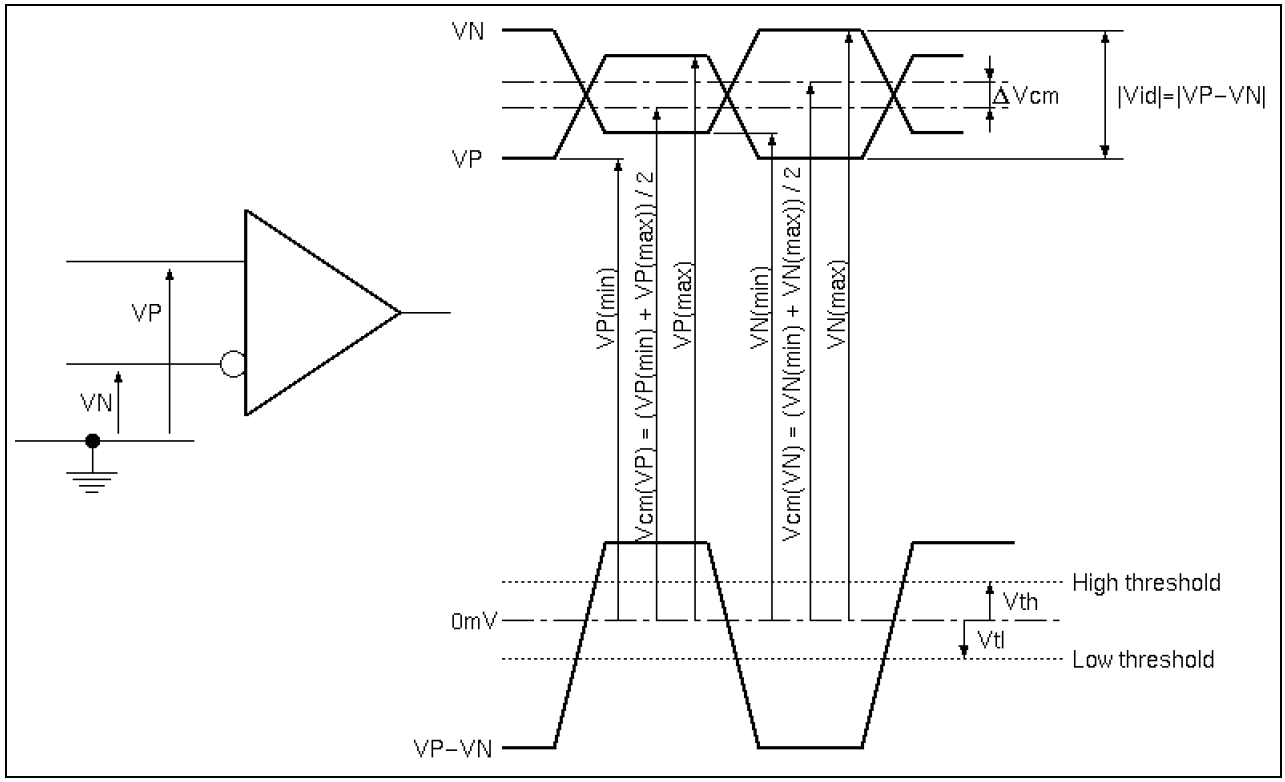
The LVDS receiver equipped in this LCD module is compatible with ANSI/TIA/TIA-644 standard.

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Differential Input High Threshold	Vth			+100	mV	Vcm=+1.2V
Differential Input Low Threshold	Vtl	-100			mV	Vcm=+1.2V
Magnitude Differential Input Voltage	|Vid|	100		600	mV	
Common Mode Voltage	Vcm	$0.825+\frac{\lvert Vid \rvert}{2}$		$2.4-\frac{\lvert Vid \rvert}{2}$	V	Vth - Vtl = 200mV
Common Mode Voltage Offset	△Vcm	-50		+50	mV	Vth - Vtl = 200mV

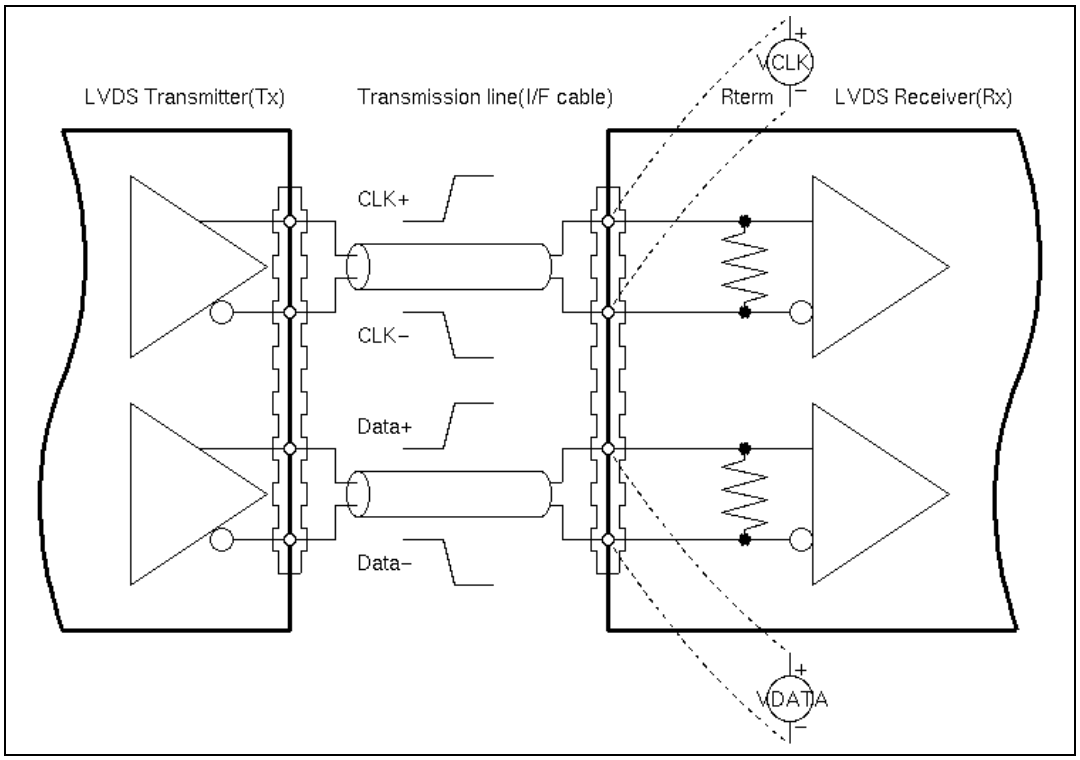
Note:

- Input signals shall be low or Hi-Z state when VDD is off.
- All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD (see "**Measurement system**").



Voltage Definitions

Measurement system

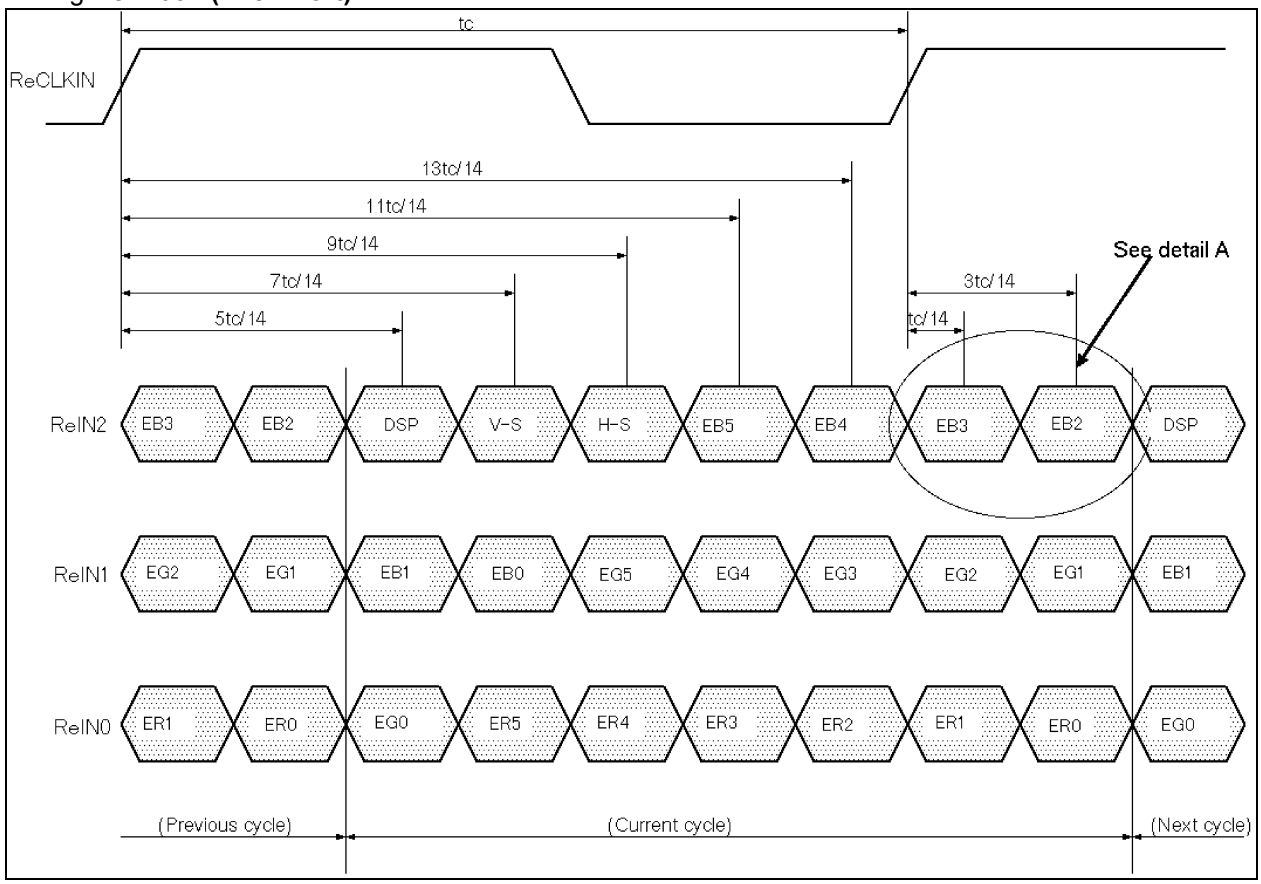


Switching Characteristics

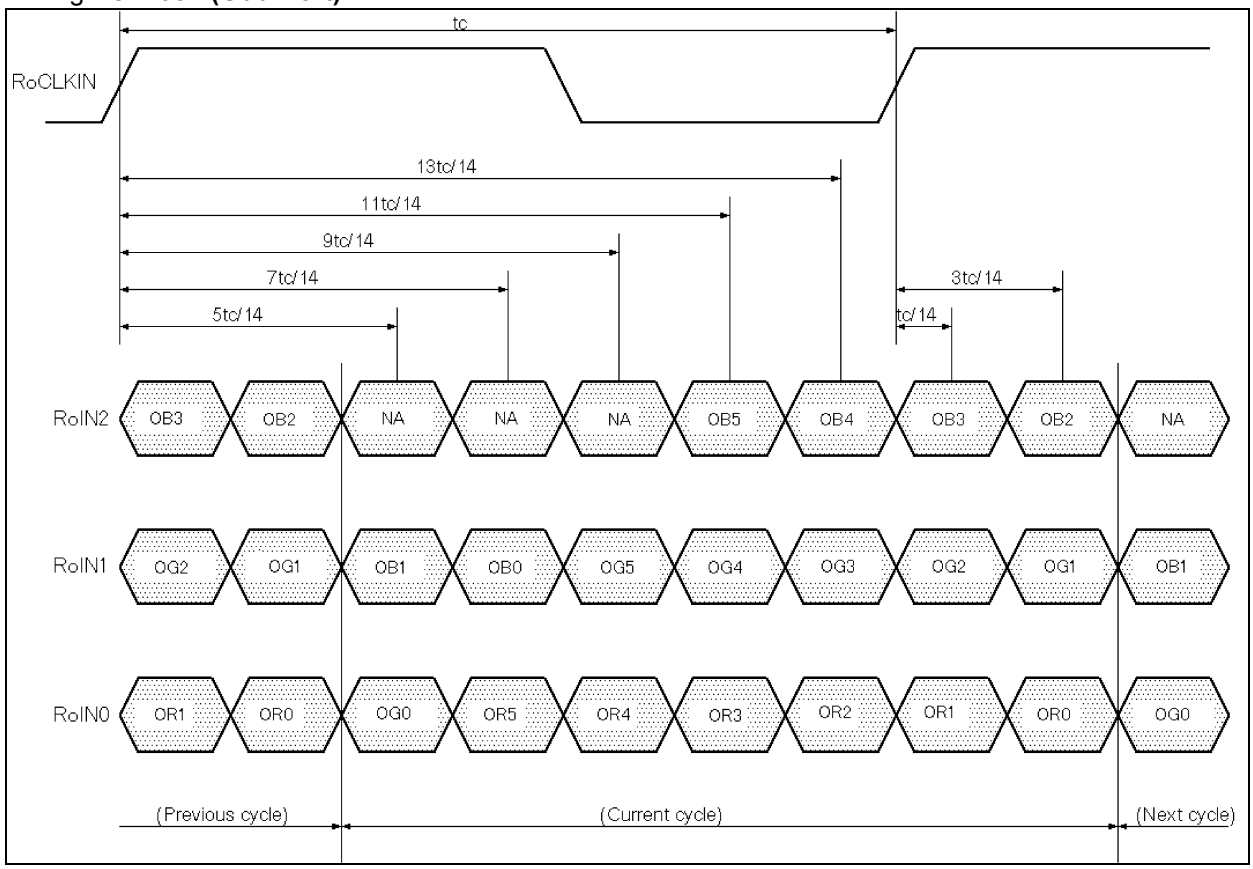
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Clock Frequency	fc	75.0	81.0	83.0	MHz	
Clock Frequency (FPT Mode)	fc	61.0	66.4	69.0	MHz	
Cycle Time	tc	12.0	12.3	13.3	ns	
Cycle Time (FPT Mode)	tc	14.5	15.1	16.4	ns	
Data Setup Time **(Note 2)**	Tsu	500			ps	fc = 81MHz, tCCJ < 50ps, Vth-Vtl = 200mV, Vcm = 1.2V, △Vcm = 0
Data Hold Time **(Note 2)**	Thd	500			ps	
Data Setup Time (FPT Mode) **(Note 2)**	Thd	600			ps	fc = 66.4MHz, tCCJ < 50ps, Vth-Vtl = 200mV, Vcm = 1.2V, △Vcm = 0
Data Hold Time (FPT Mode) **(Note 2)**	Thd	600			ps	
Cycle-to-cycle jitter **(Note 3)**	tCCJ	-150		+150	ps	fc = 81MHz, Tsu=Thd=720ps
Cycle-to-cycle jitter (FPT Mode) **(Note 3)**	tCCJ	-150		+150	ps	fc = 66.4MHz, Tsu=Thd=880ps
Cycle Modulation Rate **(Note 4)**	tCJavg			20	ps/clk	

Note 1: All values are at VDD=3.3V, Ta=25 degree C.
Note 2: See "**Timing Definition**" and "**Timing Definition(detail A)**" for definition.
Note 3: Jitter is the magnitude of the change in input clock period.
Note 4: This specification defines maximum average cycle modulation rate in peak-to-peak transition within any 100 clock cycles.
This specification is applied only if input clock peak jitter within any 100 clock cycles is greater than 300ps.

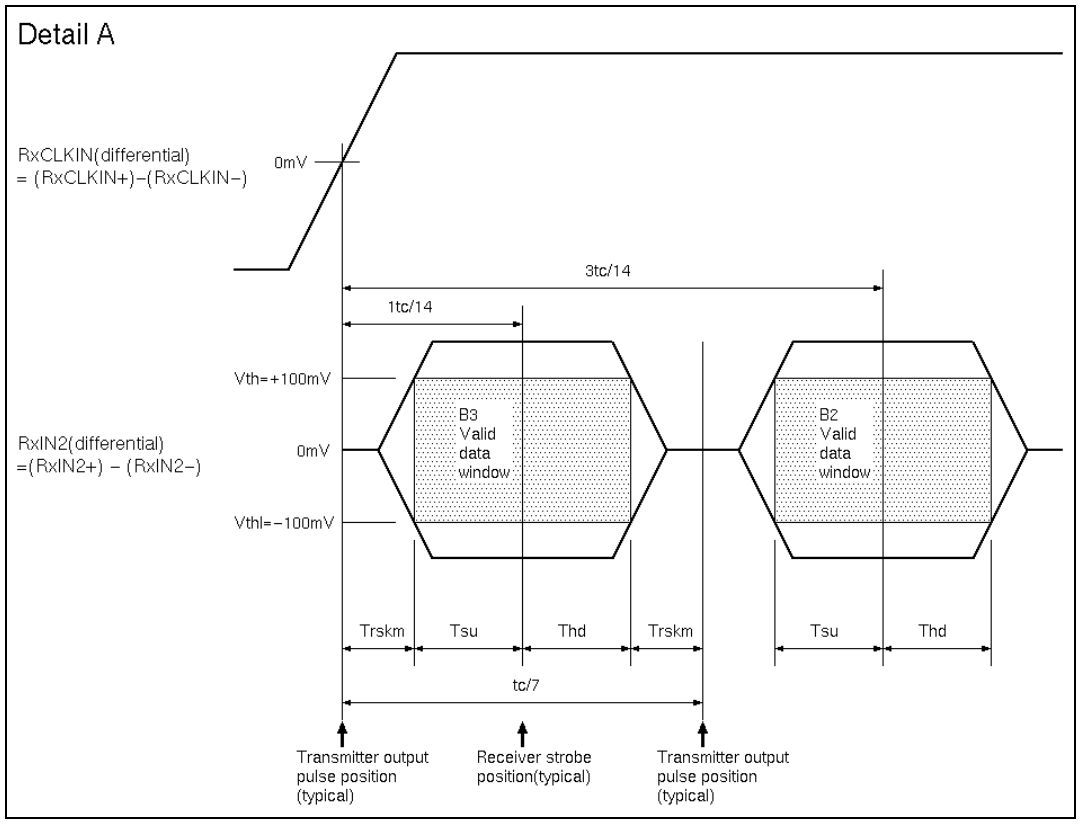
Timing Definition **(Even Port)**



Timing Definition **(Odd Port)**



Timing Definition(detail A)

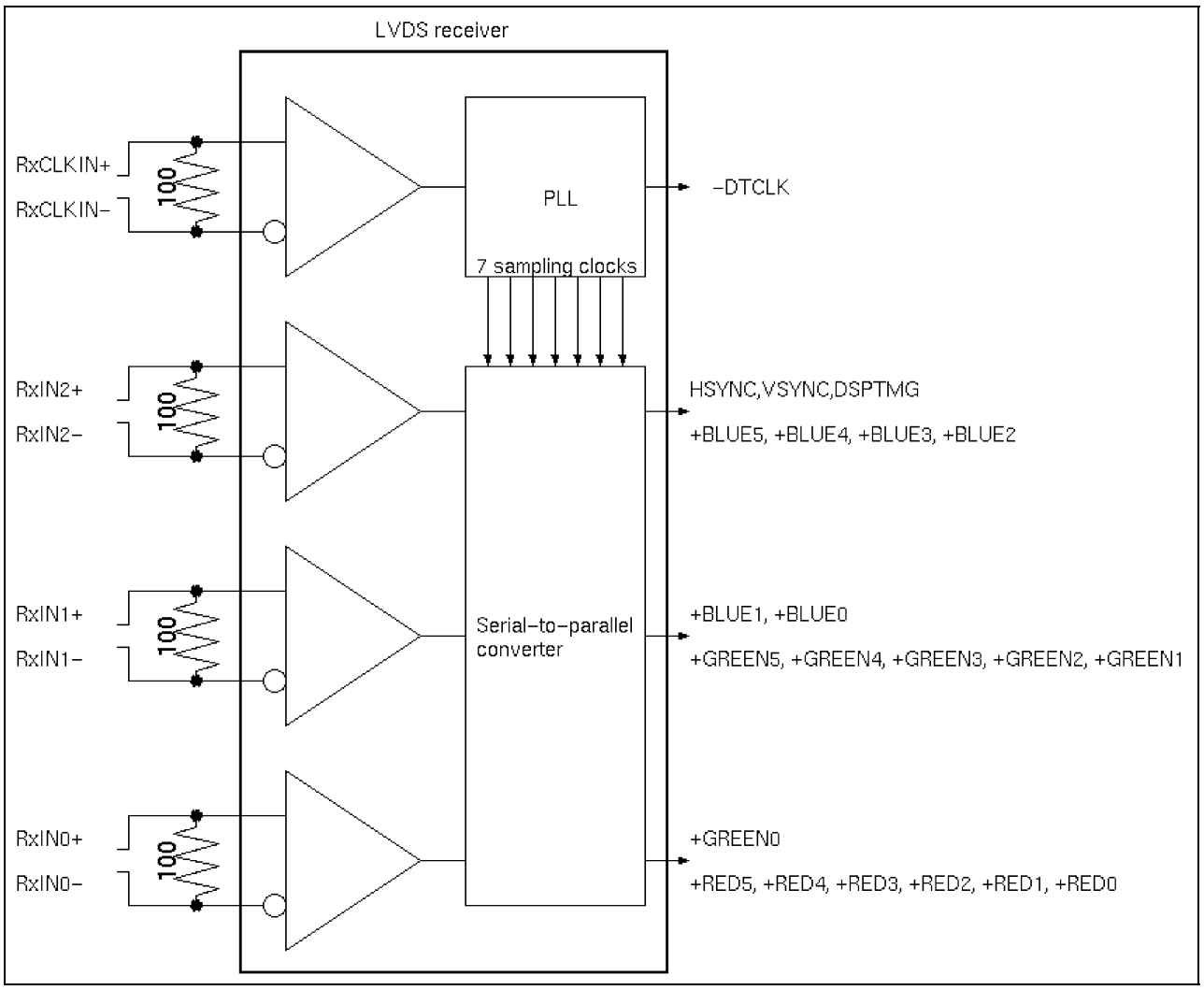


Note: Tsu and Thd are internal data sampling window of receiver. Trskm is the system skew margin; i.e., the sum of cable skew, source clock jitter, and other inter-symbol interference, shall be less than Trskm.

5.4.2 LVDS Receiver Internal Circuit

Below figure shows the internal block diagram of the LVDS receiver. This LCD module equips termination resistors for LVDS link.

Cycle Modulation Rate



5.4.3 Recommended Guidelines for Motherboard PCB Design and Cable Selection

Following the suggestions below will help to achieve optimal results.

- Use controlled impedance media for LVDS signals. They should have a matched differential impedance of 100ohm.
- Match electrical lengths between traces to minimize signal skew.
- Isolate TTL signals from LVDS signals.
- For cables, twisted pair, twinax, or flex circuit with close coupled differential traces are recommended.

5.5 Inverter Signal connector

Pin #	Signal Name	Pin #	Signal Name
1 **(Note*)**	PANEL-ID0	9	5VALW
2	PANEL-ID1	10	5VSUS
3	PANEL-ID2	11	GND
4	PANEL-ID3	12	GND
5	NC	13	GND
6	FPVEE	14	PWR_SRC
7	SMB_CLK	15	PWR_SRC
8	SMB_DAT	16	PWR_SRC

(Note*) Molex Connector No.1 Mark

5.6 Inverter Signal Description

Input connector		Typical(typ) Voltage levels	Description
Molex	52207-1690 (FFC/FPC)		
Pin	**Function**		
1*	PANEL_ID0		"1" Open
2	PANEL_ID1		"1" Open
3	PANEL_ID2		"0" Connect to GND
4	PANEL_ID3		"1" Open
5	NC		
6	FPVEE	(0,3.3V)typ	Control signal input into the inverter to turn the backlight ON & OFF (3.3V-ON,0V-OFF)
7	SMB_CLK	(0V,5V)typ	SMBus interface for sending brightness & contrast information to the inverter/panel
8	SMB_DAT	(0V,5V)typ	SMBus interface for sending brightness & contrast information to the inverter/panel
9	5VALW	5V typ	This should be used as power source that stores the brightness/contrast values & the circuit that interfaces with SMB_CLK & SMB_DAT
10	5VSUS	4.85V to 5.2V	This should be used as power source for the control circuitry on the inverter.
11	GND		
12	GND		
13	GND		
14	PWR_SRC	(9V to 21V) typ	This power rail should be used as a power rail to drive the backlight DC-AC converter
15	PWR_SRC	(9V to 21V) typ	This power rail should be used as a power rail to drive the backlight DC-AC converter
16	PWR_SRC	(9V to 21V) typ	This power rail should be used as a power rail to drive the backlight DC-AC converter

Note(*) : Molex Connector No.1 Mark

5.7 Inverter Signal Electrical Characteristics

Electrical Specifications

Item	Symbol	Min.	Typ.	Max.	UNITS	CONDITION
Input Voltage	PWR_SRC	9.0	14.4	21	[V]	Ta=25[deg. C]
	5VSUS, 5VALW	4.85	5.0	5.2	[V]	
Input Power	P(PWR_SRC)		5.6	6.2	[W]	SMData=00H PWR_SRC=14.4[V]
			1.0	1.4	[W]	SMData=0FFH PWR_SRC=14.4[V]
	P(5VSUS)		15	25	[mW]	
	P(5VALW)		5	25	[mW]	
ON/OFF	FPVEE	2.0			[V]	ON
	FPVEE			0.8	[V]	OFF
Lamp Frequency	F	52	59	66	[KHz]	
Burst Frequency	FB	156	160	164	[Hz]	

Dimming

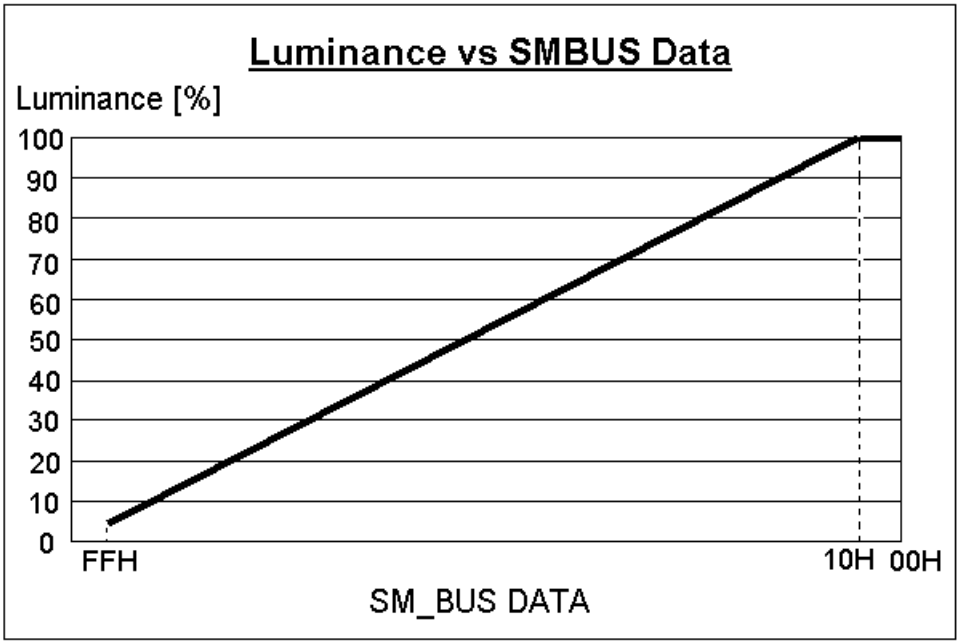
SMData	Brightness [%]			Brightness (center) [cd/m^2]	Lamp Current (Return side)[mA]
	Min.	Typ.	Max.		
00H	-	100	-	150 (*1)	6.5 (*1)
FFH	2	5	9	7.5 (*1)	1.7 (*1)

*1 : Reference Only

SMBUS Data

SMBUS	Device Identifier	Device Address
	0101	100

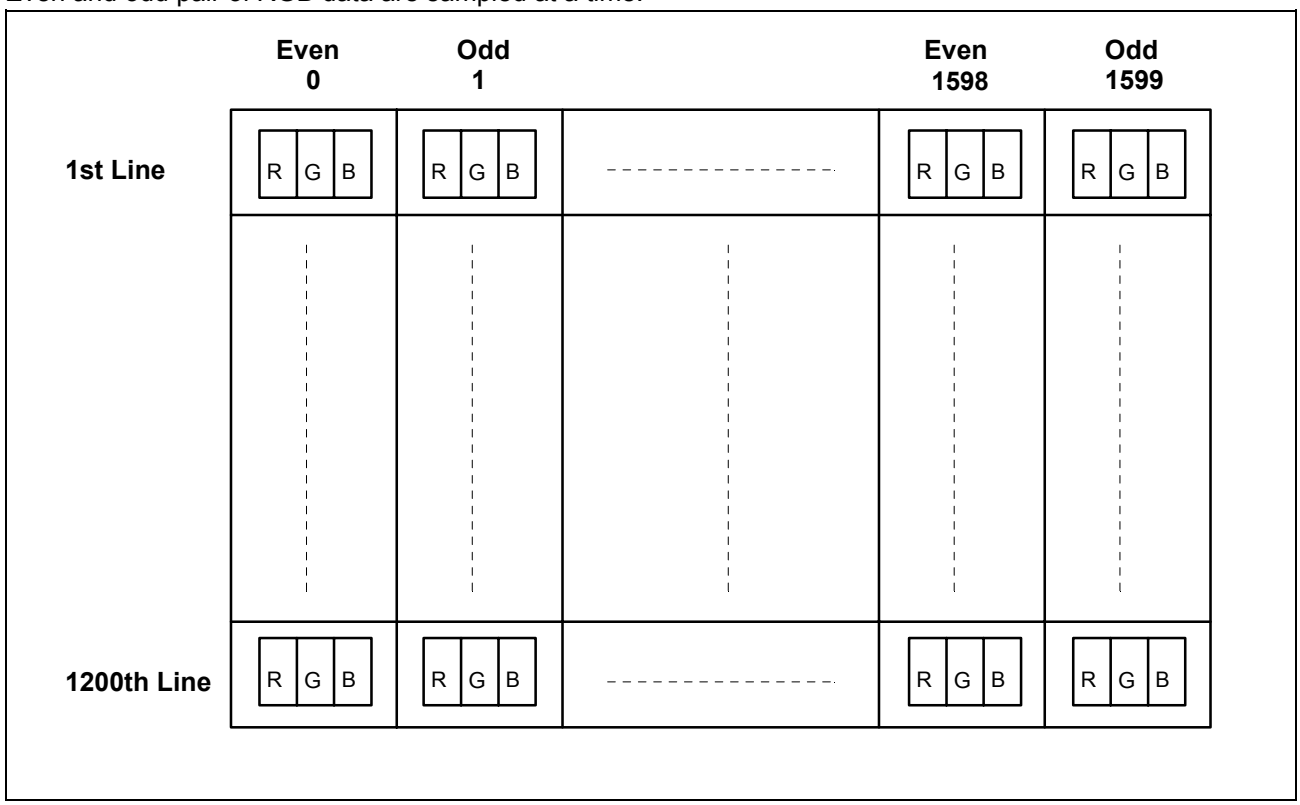
The following chart is the Luminance versus the SMBUS Data for your reference.



6.0 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format image.

Even and odd pair of RGB data are sampled at a time.



7.0 Interface Timings

7.1 Timing Characteristics

(VESA UXGA Mode)

Signal	Item	Symbol	MIN.	TYP.	MAX.	Unit
DTCLK	Freqency	Fdck	75.0	81.0	83.0	[MHz]
		Tck	12.0	12.3	13.3	[ns]
+V-Sync	Frame Rate	Fv		60.0		[Hz]
		Tv		16.67		[ms]
		Nv	1208	1250	2046	[lines]
	V-Active Level	Tva	13.33	40.0	839.8	[us]
		Nva	1	3	63	[lines]
	V-Back Porch	Nvb	6	46	125	[lines]
	V-Front Porch	Nvf	1	1	125	[lines]
+DSPTMG	V-Line	m		1200		[lines]
+H-Sync	Scan Rate	Fh		75.0		[KHz]
		Th		13.33		[usec]
		Nh	1024	1080	2047	[Tck]
	H-Active Level	Tha		1.185		[usec]
		Tha	8	96	255	[Tck]
	H-Back Porch	Thb	8	152	511	[Tck]
	H-Front Porch	Thf	8	32		[Tck]
+DSPTMG	Display	Thd		9.877		[usec]
+DATA	Data Even/Odd	n		1600		[dots]

Note1 : Both positive Hsync and positive Vsync polarity is recommended.

Note2 : When there are invalid timing, Display appears black pattern.
Synchronous Signal Defects and enter Auto Refresh for LCD Module Protection Mode.

(VESA UXGA FPT Mode)

Signal	Item	Symbol	MIN.	TYP.	MAX.	Unit
DTCLK	Freqency	Fdck	61.0	66.4	69.0	[MHz]
		Tck	14.5	15.1	16.4	[ns]
+V-Sync	Frame Rate	Fv		60.0		[Hz]
		Tv		16.67		[ms]
		Nv	1208	1214	2046	[lines]
	V-Active Level	Tva	13.7	13.7		[us]
		Nva	1	1	63	[lines]
	V-Back Porch	Nvb	1	1	125	[lines]
	V-Front Porch	Nvf	3	12	125	[lines]
+DSPTMG	V-Line	m		1200		[lines]
+H-Sync	Scan Rate	Fh		73.0		[KHz]
		Th		13.74		[usec]
		Nh	873	912	1023	[Tck]
	H-Active Level	Tha		0.121		[usec]
		Tha	8	8	255	[Tck]
	H-Back Porch	Thb	8	56	511	[Tck]
	H-Front Porch	Thf	8	48		[Tck]
+DSPTMG	Display	Thd		12.053		[usec]
+DATA	Data Even/Odd	n		1600		[dots]

Note1 : Both positive Hsync and positive Vsync polarity is recommended.

Note2 : When there are invalid timing, Display appears black pattern.
Synchronous Signal Defects and enter Auto Refresh for LCD Module Protection Mode.

(VESA UXGA Mode)

Typical Vertical Timing Table

Support mode	Tvblk Vertical Blanking	m Active Field	Tvf VSYNC Front Porch	Tv,Nv Frame Time	Tva VSYNC Width	Tvb VSYNC Back Porch
1600 x 1200 at 60Hz (H line rate : 13.3 us)	0.667 ms (50 lines)	16.000 ms (1200 lines)	0.013 ms (1 line)	16.667 ms (1250 lines)	0.040 ms (3 lines)	0.613 ms (46 lines)

Typical Horizontal Timing Table

Support mode	Thblk Horizontal Blanking	Thd Active Field	Thf HSYNC Front Porch	Th,Nh H Line Time	Tha HSYNC Width	Thb HSYNC Back Porch
1600 x 1200 Dotclock : 162.000 MHz (81.000MHz x2)	3.457 us (560 dots)	9.877 us (1600 dots)	0.395 us (64 dots)	13.333 us (2160 dots)	1.185 us (192 dots)	1.877 us (304 dots)

(VESA UXGA FPT Mode)

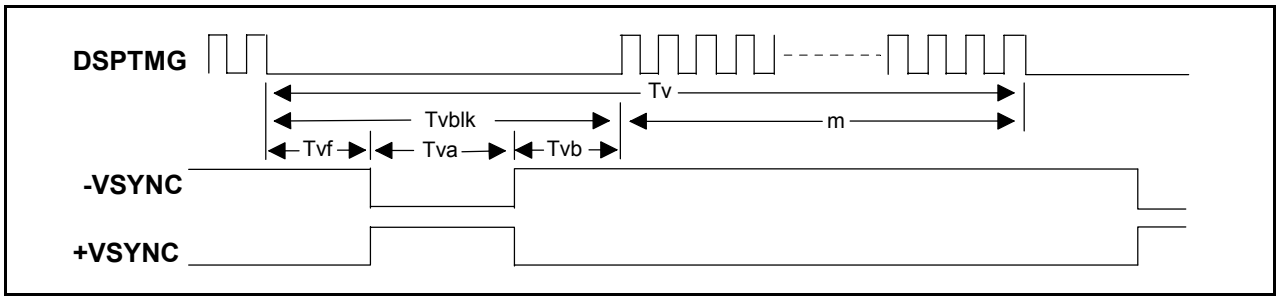
Typical Vertical Timing Table

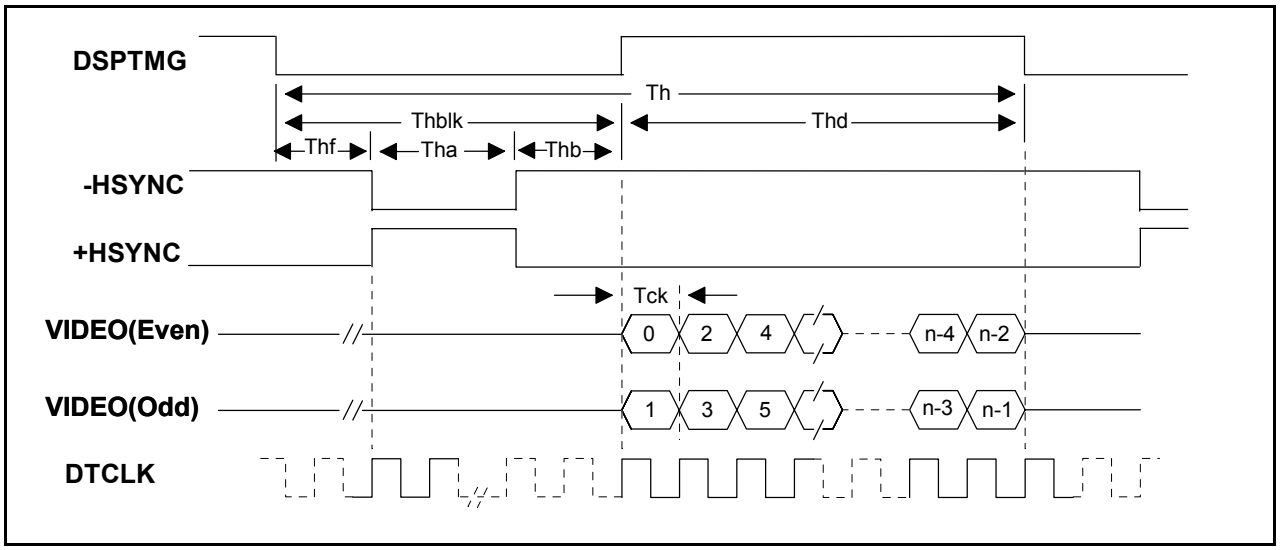
Support mode	Tvblk Vertical Blanking	m Active Field	Tvf VSYNC Front Porch	Tv,Nv Frame Time	Tva VSYNC Width	Tvb VSYNC Back Porch
1600 x 1200 at 60Hz (H line rate : 13.7 us)	0.192 ms (14 lines)	16.440 ms (1200 lines)	0.164 ms (12 line)	16.632 ms (1214 lines)	0.014 ms (1 line)	0.014 ms (1 line)

Typical Horizontal Timing Table

Support mode	Thblk Horizontal Blanking	Thd Active Field	Thf HSYNC Front Porch	Th,Nh H Line Time	Tha HSYNC Width	Thb HSYNC Back Porch
1600 x 1200 Dotclock : 132.75 MHz (66.375MHz x2)	1.687 us (224 dots)	12.053 us (1600 dots)	0.723 us (96 dots)	13.740 us (1824 dots)	0.121 us (16 dots)	0.844 us (112 dots)

7.2 Timing Definition





8.0 Power Consumption

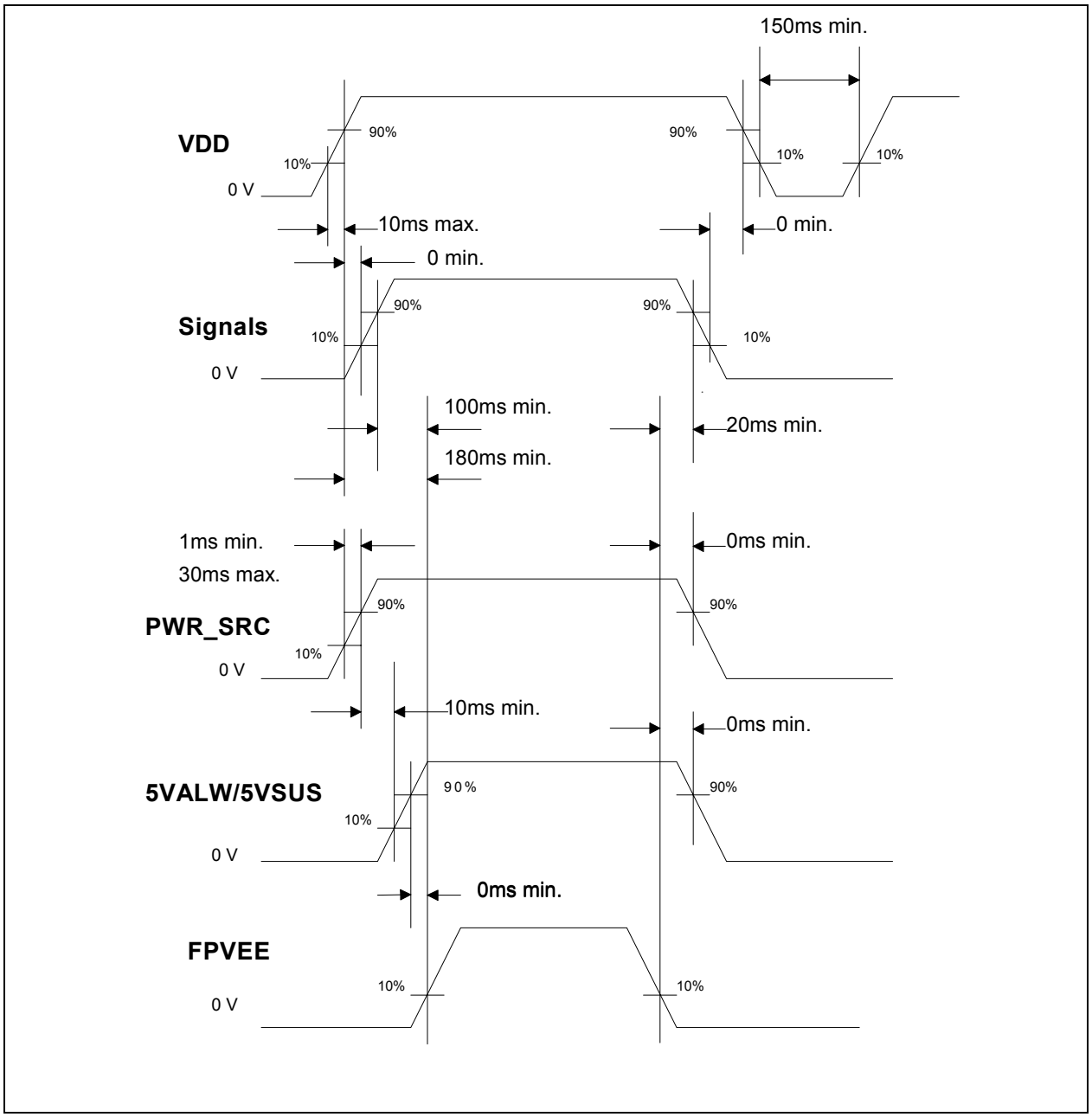
Input power specifications are as follows;

SYMBOL	PARAMETER	Min	Typ	Max	UNITS	CONDITION
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[V]	Load Capacitance 68uF
PDD	VDD Power			3.4	[W]	MAX. Pattern, VDD=3.6[V]
PDD	VDD Power		2.4		[W]	All Black Pattern, VDD=3.3[V]
IDD	VDD Current			940	[mA]	MAX Pattern, VDD=3.0[V]
IDD	VDD Current		730		[mA]	All Black Pattern, VDD=3.3[V]
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mVp-p]	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	[mVp-p]	

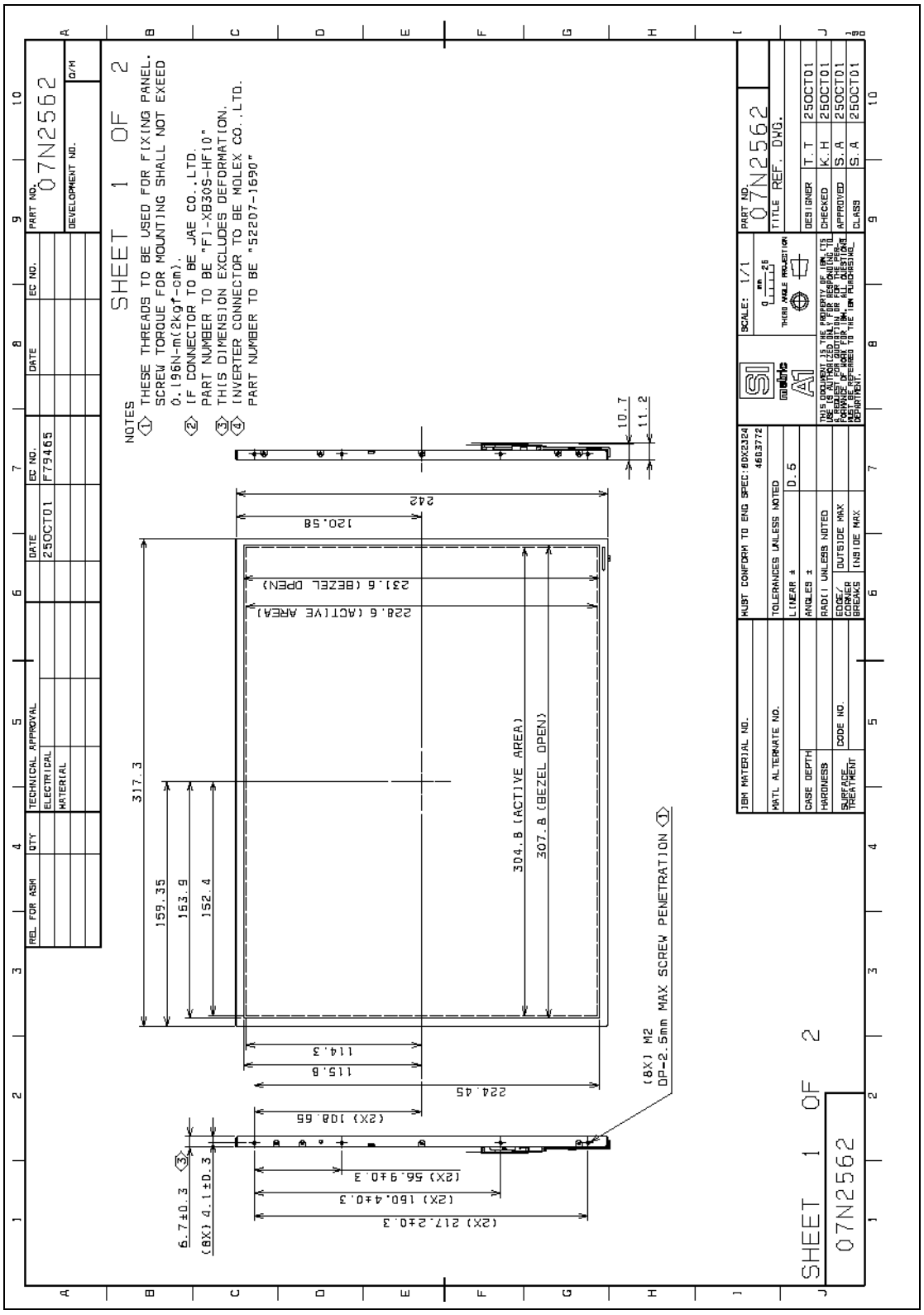
MAX. Pattern : 2dot Vertical sub-pixel Stripe.

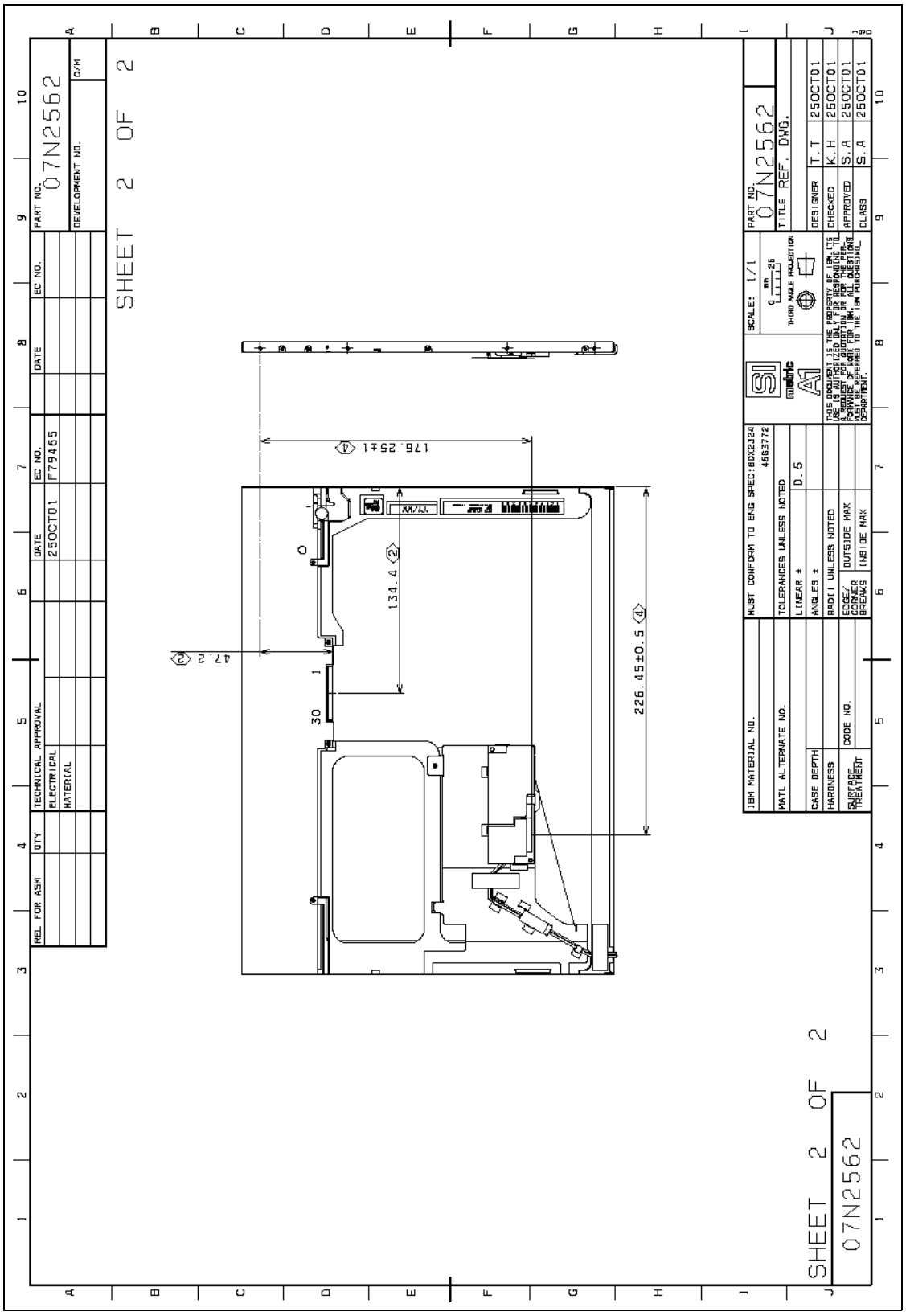
9.0 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



10.0 Mechanical Characteristics





11.0 National Test Lab Requirement

The display module is authorized to Apply the UL Recognized Mark.

Conditions of Acceptability

- This component has been judged on the basis of the required spacings in the Standard for Safety of Information Technology Equipment, Including Electrical Business Equipment, CAN/CSA C22.2 No.950-95 *UL 1950, Third Edition, including revisions through revision date March 1,1998, which are based on the Fourth Amendment to IEC 950, Second Edition, which would cover the component itself if submitted for Listing.
- The inverter output circuit supplied with this model is a Limited Current Circuit.
- The units are supplied by Limited Power Sources.
- The terminals and connectors are suitable for factory wiring only.
- The terminals and connectors have not been evaluated for field wiring.
- A suitable Electrical and Fire enclosure shall be provided.

****** End Of Page ******