□ Tentative Specification
■ Preliminary Specification
□ Approval Specification

# MODEL NO.: V390DK1
# SUFFIX: LS1

Customer:

APPROVED BY SIGNATURE

Name / Title _____ _____

Note

Please return 1 copy for your confirmation with your signature and comments.

| Approved By | Checked By | Prepared By |
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## REVISION HISTORY

| Version | Date | Page (New) | Section | Description |
|---|---|---|---|---|
| Ver. 0.0 | 12/14, 2012 | All | All | The tentative specification was first issued. |
| Ver. 1.0 | 1/24, 2013 | All | All | The preliminary specification was first issued. |

# 1. GENERAL DESCRIPTION

## 1.1 OVERVIEW

V390DK1-LS1 is a 39" TFT Liquid Crystal Display module with LED Backlight unit and 4ch-LVDS interface. This module supports 3840 x 2160 Quad Full HDTV format and can display true 1.07G colors (8-bit+FRC). The driving board module for backlight is built-in.

## 1.2 FEATURES

- High brightness (350 nits)
- High contrast ratio (5000:1)
- Fast response time (Gray to Gray typical : 6.5 ms)
- High color saturation (NTSC 72%)
- Quad Full HDTV (3840 x 2160 pixels) resolution, true HDTV format
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 100Hz/120Hz frame rate
- Viewing Angle : 176(H)/176(V) (CR>20) VA Technology
- Ultra wide viewing angle: Super MVA technology
- RoHs compliance
- T-con input frame rate : FHD 50/60Hz, FHD 100/120Hz or QFHD 24/30Hz
  Output frame rate: QFHD 50/60Hz, QFHD 100/120Hz or QFHD 48/60Hz

## 1.3 APPLICATION

- Standard Living Room TVs
- Public Display Application
- Home Theater Application
- MFM Application

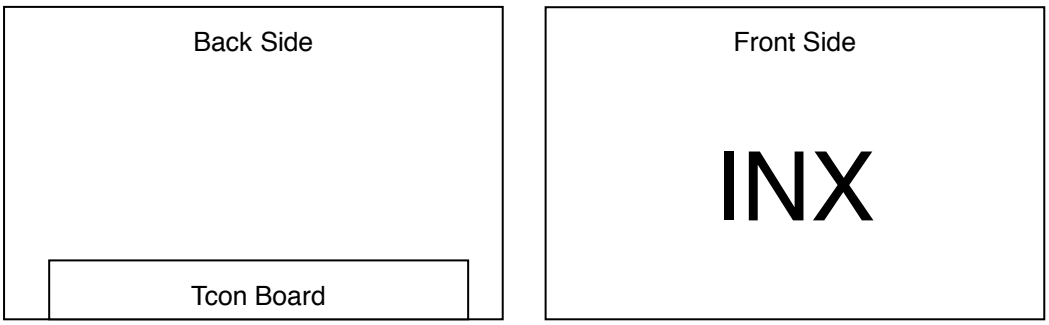
## 1.4 GENERAL SPECIFICATI0NS

| Item | Specification | Unit | Note |
|---|---|---|---|
| Active Area | 853.92 (H) x 480.33 (V) (39" diagonal) | mm | (1) |
| Bezel Opening Area | 861.32 (H) x 485.63 (V) | mm | |
| Driver Element | a-si TFT active matrix | - | - |
| Pixel Number | 3840 x R.G.B. x 2160 | pixel | - |
| Pixel Pitch(Sub Pixel) | 0.074125 (H) x 0.222375 (V) | mm | - |
| Pixel Arrangement | RGB vertical stripe | - | - |
| Display Colors | 1.07G colors (8-bit+FRC) | color | - |
| Display Operation Mode | Transmissive mode / Normally black | - | - |
| Surface Treatment | Anti-Glare coating (Haze 1%) | - | (2) |
| Rotation Function | Achievable | | (3) |
| Display Orientation | Signal input with "INX" | | (3) |

Note (1) Please refer to the attached drawings in chapter 11 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporarily for this phase. INX reserves the rights to change this feature.

Note (3)



## 1.5 MECHANICAL SPECIFICATIONS

| Item | | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Module Size | Horizontal (H) | 872.32 | 873.32 | 874.32 | mm | (1),(2) |
| | Vertical (V) | 500.63 | 501.63 | 502.63 | mm | (1),(2) |
| | Depth (D) | 17.4 | 18.4 | 19.4 | mm | To Rear |
| | | 24.6 | 25.6 | 26.6 | mm | To converter cover |
| Weight | | | (7110) | | g | |

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

## 2. ABSOLUTE MAXIMUM RATINGS

### 2.1 ABSOLUTE RATINGS OF ENVIRONMENT

| Item | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Storage Temperature | $T_{ST}$ | -20 | +60 | ºC | (1) |
| Operating Ambient Temperature | $T_{OP}$ | 0 | 50 | ºC | (1), (2) |
| Shock (Non-Operating) | $S_{NOP}$ | - | 50 | G | (3), (5) |
| Vibration (Non-Operating) | $V_{NOP}$ | - | 1.0 | G | (4), (5) |

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

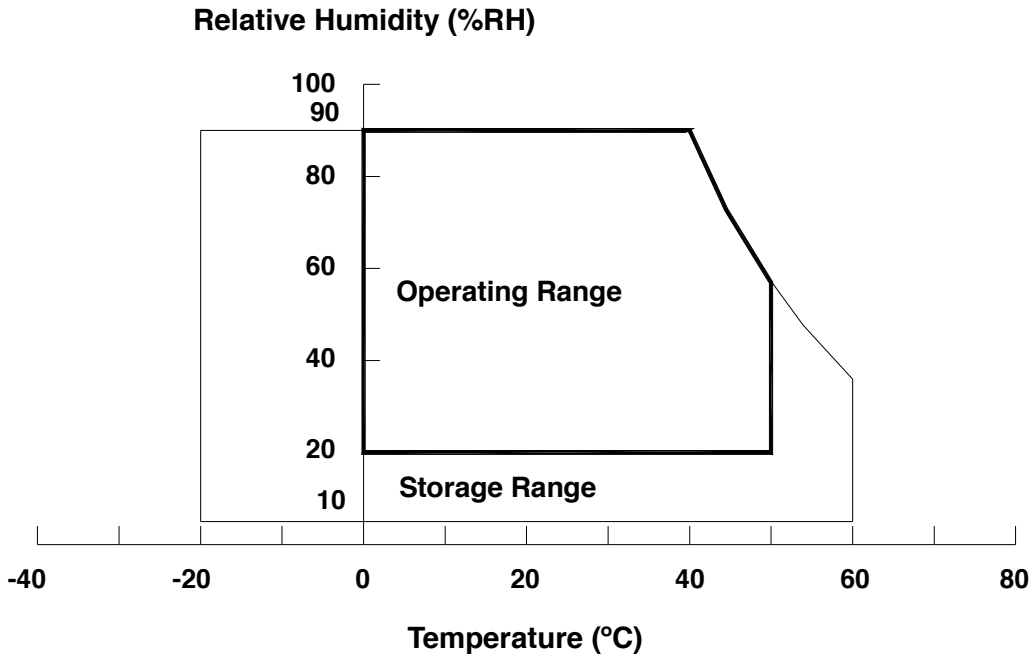
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



## 2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 ℃ at normal humidity without condensation.

(b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

## 2.3 ELECTRICAL ABSOLUTE RATINGS

### 2.3.1 TFT LCD MODULE

| Item | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Power Supply Voltage | $V_{CC}$ | -0.3 | 13.5 | V | (1) |
| Logic Input Voltage | $V_{IN}$ | -0.3 | 3.6 | V | |

### 2.3.2 BACKLIGHT CONVERTER UNIT

| Item | Symbol | Test Condition | Min. | Type | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| Light Bar Voltage | $V_W$ | Ta = 25 ℃ | - | - | 60 | $V_{RMS}$ | 3D Mode |
| Converter Input Voltage | $V_{BL}$ | - | 0 | - | 30 | V | |
| Control Signal Level | - | - | -0.3 | - | 6 | V | |

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and External PWM Control.

## 3. ELECTRICAL CHARACTERISTICS

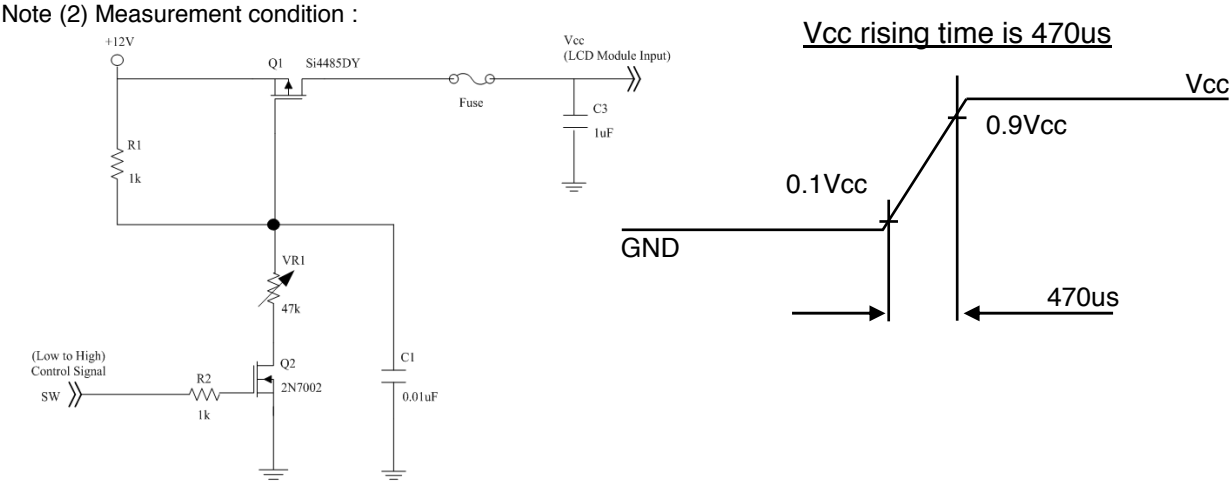
### 3.1 TFT LCD MODULE

(Ta = 25 ± 2 °C)

| Parameter | | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Power Supply Voltage | | $V_{CC}$ | 10.8 | 12 | 13.2 | V | (1) |
| Rush Current | | $I_{RUSH}$ | — | — | 1.65 | A | (2) |
| QFHD 120Hz Output Power Consumption | White Pattern | $P_T$ | — | (8.88) | (10.8) | W | (3) |
| | Horizontal Stripe | $P_T$ | — | (20.16) | (24.36) | W | |
| | Black Pattern | $P_T$ | — | (9.48) | (11.4) | W | |
| QFHD 120Hz Output Power Supply Current | White Pattern | — | — | (0.74) | (0.90) | A | |
| | Horizontal Stripe | — | — | (1.68) | (2.03) | A | |
| | Black Pattern | — | — | (0.79) | (0.95) | A | |
| QFHD 60Hz Output Power Consumption | White Pattern | $P_T$ | — | (8.76) | (10.8) | W | |
| | Horizontal Stripe | $P_T$ | — | (19.68) | (23.76) | W | |
| | Black Pattern | $P_T$ | — | (9.24) | (11.04) | W | |
| QFHD 60Hz Output Power Supply Current | White Pattern | — | — | (0.73) | (0.90) | A | |
| | Horizontal Stripe | — | — | (1.64) | (1.98) | A | |
| | Black Pattern | — | — | (0.77) | (0.92) | A | |
| LVDS interface | Differential Input High Threshold Voltage | $V_{LVTH}$ | +100 | — | +300 | mV | (4) |
| | Differential Input Low Threshold Voltage | $V_{LVTL}$ | -300 | — | -100 | mV | |
| | Common Input Voltage | $V_{CM}$ | 1.0 | 1.2 | 1.4 | V | |
| | Differential input voltage (single-end) | $\|V_{ID}\|$ | 200 | — | 600 | mV | |
| | Terminating Resistor | $R_T$ | — | 100 | — | ohm | |
| CMOS interface | Input High Threshold Voltage | $V_{IH}$ | 2.7 | — | 3.3 | V | |
| | Input Low Threshold Voltage | $V_{IL}$ | 0 | — | 0.7 | V | |

Note (1) The module should be always operated within the above ranges. The ripple voltage should be controlled under 10% of Vcc (Typ.)

Note (2) Measurement condition :




Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 °C, fv = 60 Hz, whereas a power dissipation check pattern below is displayed.

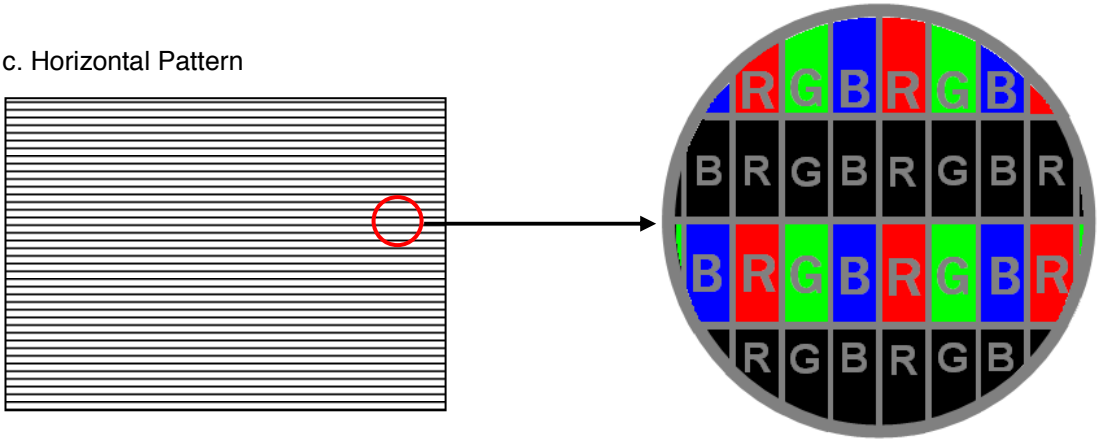
a. White Pattern

Active Area

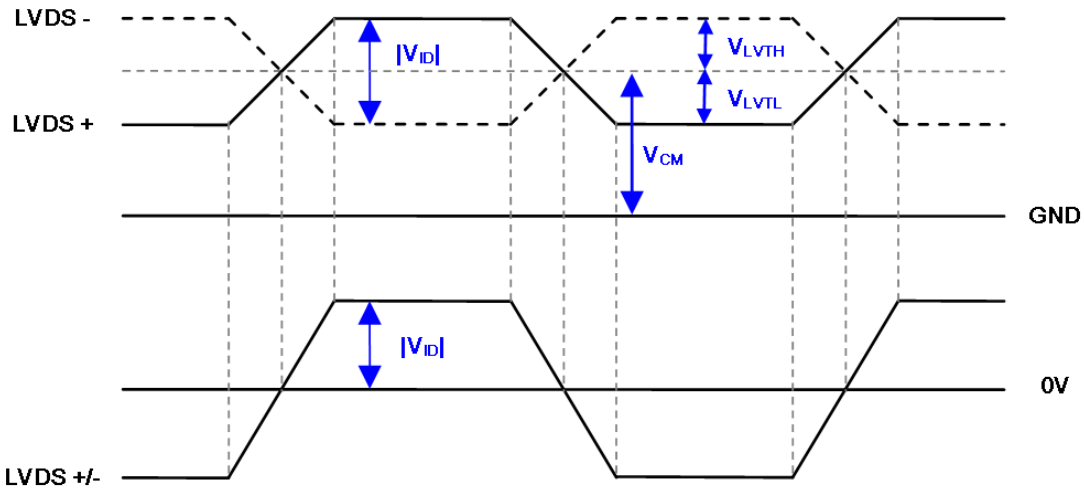
b. Black Pattern

Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics is shown as below :



## 3.2 BACKLIGHT UNIT

### 3.2.1 CONVERTER CHARACTERISTICS

| Parameter | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Power Consumption | $P_{BL(2D)}$ | — | (48.1) | (55.3) | W | (1), (2) |
| | $P_{BL(3D)}$ | — | (36.3) | (40.2) | W | (1), (2) |
| Converter Input Voltage | VBL | 22.8 | 24.0 | 25.2 | VDC | |
| Converter Input Current | $I_{BL(2D)}$ | — | (2.1) | (2.4) | A | Non Dimming |
| | $I_{BL(3D)}$ | — | (1.63) | (1.73) | A | |
| Input Inrush Current | $I_{R(2D)}$ | — | — | (3.27) | mApeak | $V_{BL}$=22.8V, (IL=typ.) (3), (6) |
| | $I_{R(3D)}$ | — | — | (5.4) | mApeak | $V_{BL}$=22.8V,(IL= 360 mA.) (3), (6) |
| Dimming Frequency | FB | 170 | 180 | 190 | Hz | (5) |
| Dimming Duty Ratio | DDR | 5 | - | 100 | % | (4), (5) |
| Life Time | - | 30,000 | - | - | Hrs | (7) |

Note (1) The power supply capacity should be higher than the total converter power consumption $P_{BL}$. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when converter dimming.

Note (2) The measurement condition of Max. value is based on 39" backlight unit under input voltage 24V, at 2D/3D Mode and lighting 1 hour later.

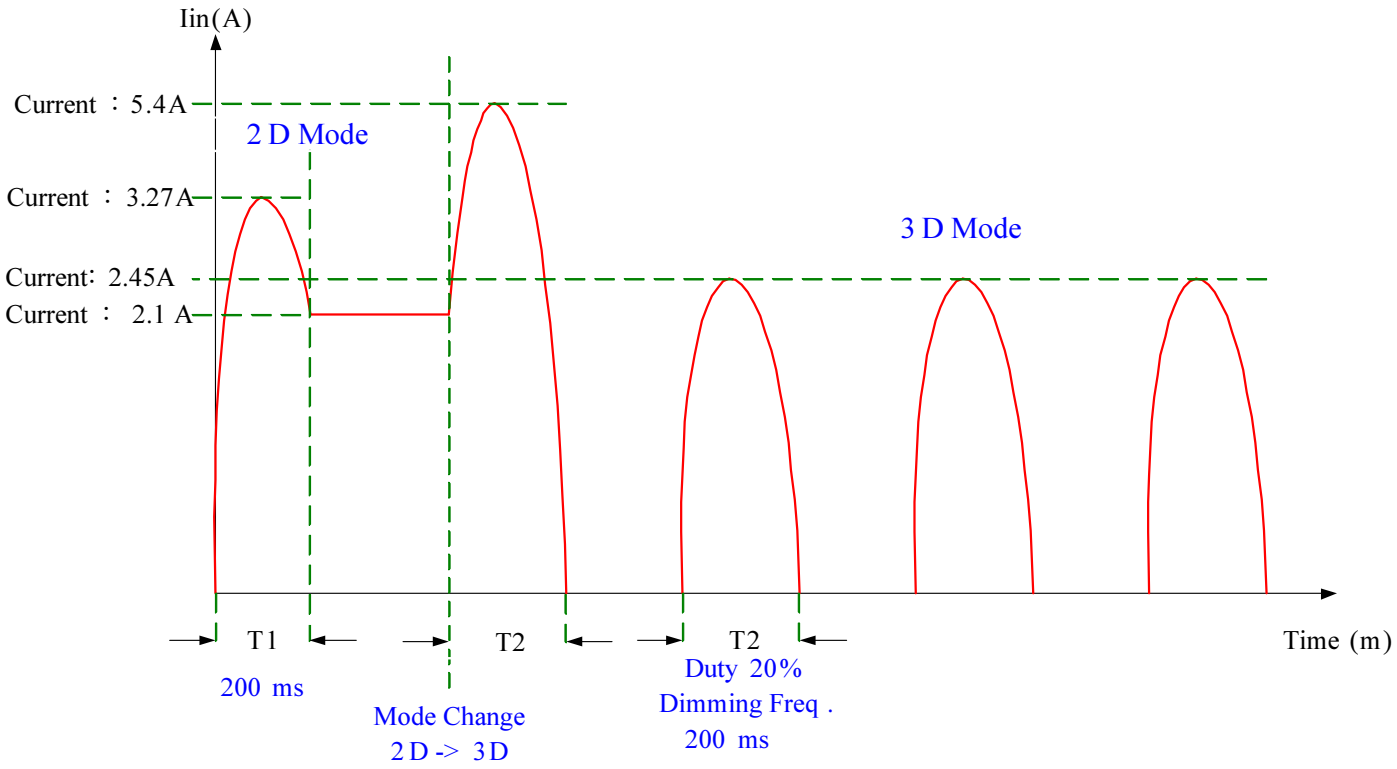
Note (3) For input inrush current measure, the VBL rising time from 10% to 90% is about 20ms.

Note (4) EPWM signal have to input available duty range. Between 97% and 100% duty (DDR) have to be avoided. (97% < DDR < 100%) But 100% duty(DDR) is possible. 5% duty (DDR) is only valid for electrical operation.

Note (5) FB and DDR are available only at 2D Mode.

Note (6) Below diagram is only for power supply design reference.

**Test Condition：$V_{BL}$=22.8V, IL=145 mA at 2 D Mode / IL=(450) mApeak at 3 D Mode**




Note (7) The lifetime is defined as the time which luminance of the LED decays to 50% compared to the initial value,

Operating condition: Continuous operating at Ta = 25±2℃

### 3.2.2 CONVERTER INTERFACE CHARACTERISTICS

| Parameter | | Symbol | Test Condition | Value | | | Unit | Note | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | | |
| On/Off Control Voltage | ON | VBLON | — | 2.0 | — | 5.0 | V | | |
| | OFF | | — | 0 | — | 0.8 | V | | |
| External PWM Control Voltage | HI | VEPWM | — | 2.0 | — | 5.25 | V | Duty on | (5), (6) |
| | LO | | — | 0 | — | 0.8 | V | Duty off | |
| External PWM Frequency | | $F_{EPWM}$ | — | 150 | 160 | 170 | Hz | Normal mode (7) | |
| Error Signal | | ERR | — | — | — | — | — | Abnormal: Open | |
| VBL Rising Time | | Tr1 | — | 20 | — | — | ms | 10%-90%$V_{BL}$ | |
| Control Signal Rising Time | | Tr | — | — | — | 100 | ms | | |
| Control Signal Falling Time | | Tf | — | — | — | 100 | ms | | |
| PWM Signal Rising Time | | TPWMR | — | — | — | 50 | us | (6) | |
| PWM Signal Falling Time | | TPWMF | — | — | — | 50 | us | | |
| Input Impedance | | Rin | — | 1 | — | — | MΩ | EPWM, BLON | |
| PWM Delay Time | | TPWM | — | 100 | — | — | ms | (6) | |
| BLON Delay Time | | $T_{on}$ | — | 300 | — | — | ms | | |
| | | $T_{on1}$ | — | 300 | — | — | ms | | |
| BLON Off Time | | Toff | — | 300 | — | — | ms | | |

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the Fig.1. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) When converter protective function is triggered, ERR will output open collector status. Please refers to Fig.2.

Note (5) The EPWM interface that inserts a pull up resistor to 5V in Max Duty (100%), please refers to Fig.3.

Note (6) EPWM is available only at 2D Mode.

Note (7) EPWM signal have to input available frequency range.

Note (8) [Recommend] EPWM duty ratio is set at 100%(Max. Brightness) in 3D Mode.

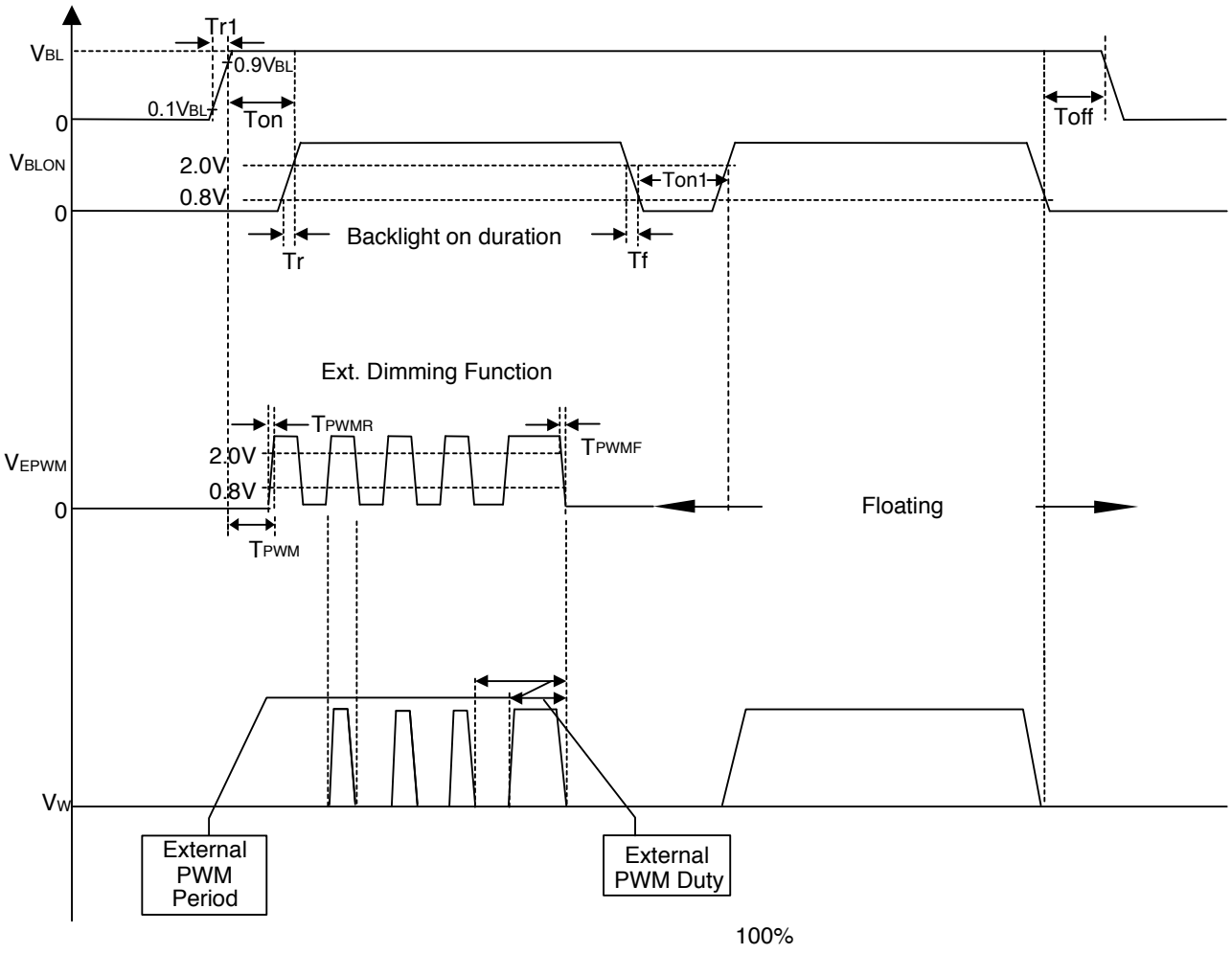



Fig. 1

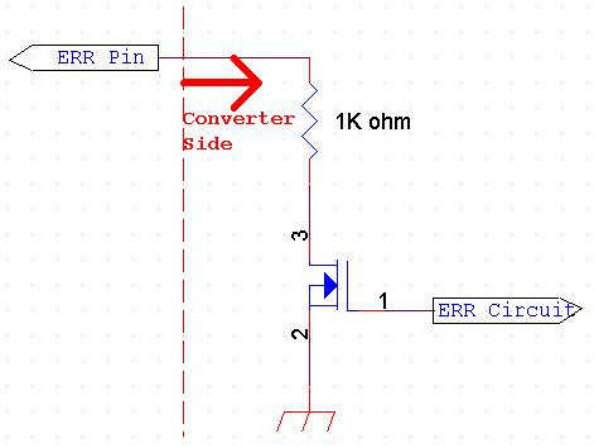



Fig. 2

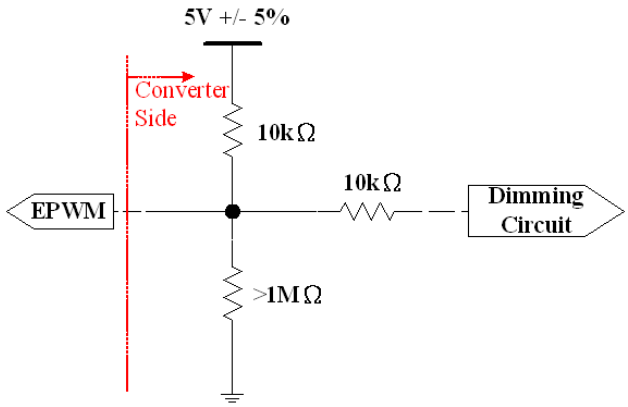
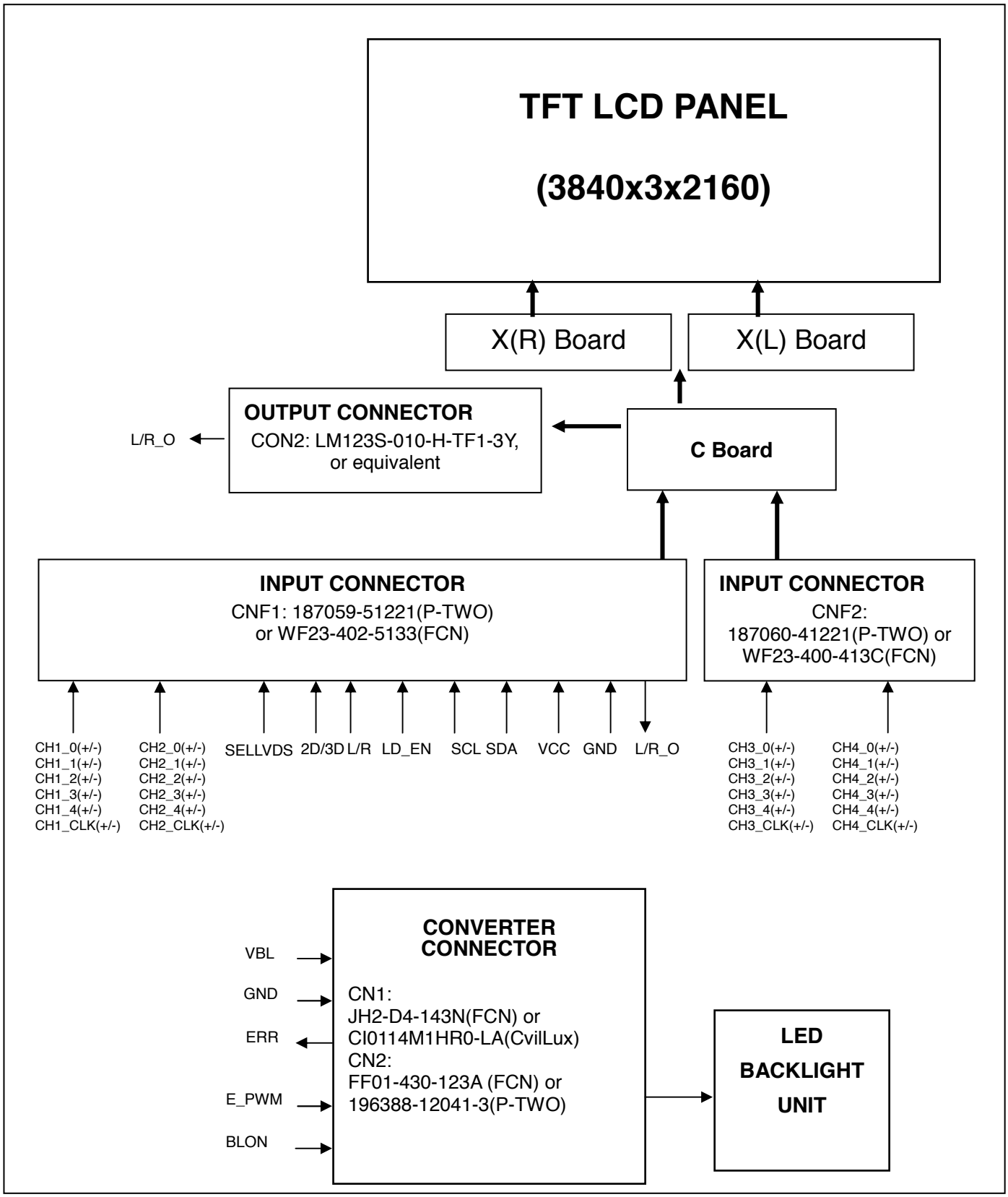



Fig. 3

## 4. BLOCK DIAGRAM OF INTERFACE

### 4.1 TFT LCD MODULE



## 5 .INPUT TERMINAL PIN ASSIGNMENT

### 5.1 TFT LCD MODULE

CNF1 Connector Pin Assignment (187059-51221(P-TWO) or WF23-402-5133 (FCN))

Matting connector: FI-RE51HL (JAE)

| Pin | Name | Description | Note |
|---|---|---|---|
| 1 | N.C. | No Connection | (1) |
| 2 | SCL | I2C Clock (for mode selection & function setting) | |
| 3 | SDA | I2C Data (for mode selection & function setting) | |
| 4 | N.C. | No Connection | (1) |
| 5 | L/R_O | Output signal for Left Right Glasses control | (2) |
| 6 | N.C. | No Connection | (1) |
| 7 | SELLVDS | Input signal for LVDS Data Format Selection | (3)(9) |
| 8 | N.C. | No Connection | |
| 9 | N.C. | No Connection | (1) |
| 10 | N.C. | No Connection | |
| 11 | GND | Ground | |
| 12 | CH1[0]- | First pixel Negative LVDS differential data input. Pair 0 | |
| 13 | CH1[0]+ | First pixel Positive LVDS differential data input. Pair 0 | |
| 14 | CH1[1]- | First pixel Negative LVDS differential data input. Pair 1 | (4) |
| 15 | CH1[1]+ | First pixel Positive LVDS differential data input. Pair 1 | |
| 16 | CH1[2]- | First pixel Negative LVDS differential data input. Pair 2 | |
| 17 | CH1[2]+ | First pixel Positive LVDS differential data input. Pair 2 | |
| 18 | GND | Ground | |
| 19 | CH1CLK- | First pixel Negative LVDS differential clock input. | (4) |
| 20 | CH1CLK+ | First pixel Positive LVDS differential clock input. | |
| 21 | GND | Ground | |
| 22 | CH1[3]- | First pixel Negative LVDS differential data input. Pair 3 | |
| 23 | CH1[3]+ | First pixel Positive LVDS differential data input. Pair 3 | (4) |
| 24 | CH1[4]- | First pixel Negative LVDS differential data input. Pair 4 | |
| 25 | CH1[4]+ | First pixel Positive LVDS differential data input. Pair 4 | |
| 26 | 2D/3D | Input signal for 2D/3D Mode Selection | (5)(10) |
| 27 | L/R | Input signal for Left Right eye frame synchronous | (6) |
| 28 | CH2[0]- | Second pixel Negative LVDS differential data input. Pair 0 | (4) |

| | | | |
|---|---|---|---|
| 29 | CH2[0]+ | Second pixel Positive LVDS differential data input. Pair 0 | |
| 30 | CH2[1]- | Second pixel Negative LVDS differential data input. Pair 1 | |
| 31 | CH2[1]+ | Second pixel Positive LVDS differential data input. Pair 1 | |
| 32 | CH2[2]- | Second pixel Negative LVDS differential data input. Pair 2 | |
| 33 | CH2[2]+ | Second pixel Positive LVDS differential data input. Pair 2 | |
| 34 | GND | Ground | |
| 35 | CH2CLK- | Second pixel Negative LVDS differential clock input. | (4) |
| 36 | CH2CLK+ | Second pixel Positive LVDS differential clock input. | |
| 37 | GND | Ground | |
| 38 | CH2[3]- | Second pixel Negative LVDS differential data input. Pair 3 | (4) |
| 39 | CH2[3]+ | Second pixel Positive LVDS differential data input. Pair 3 | |
| 40 | CH2[4]- | Second pixel Negative LVDS differential data input. Pair 4 | |
| 41 | CH2[4]+ | Second pixel Positive LVDS differential data input. Pair 4 | |
| 42 | LD_EN | Input signal for Local Dimming Enable | (7)(9) |
| 43 | N.C. | No Connection | (8) |
| 44 | GND | Ground | |
| 45 | GND | Ground | |
| 46 | GND | Ground | |
| 47 | N.C. | No Connection | (1) |
| 48 | VCC | +12V power supply | |
| 49 | VCC | +12V power supply | |
| 50 | VCC | +12V power supply | |
| 51 | VCC | +12V power supply | |

CNF2 Connector pin assignment (187060-41221 (P-TWO) or WF23-400-413C (FCN))

Matting connector: FI-RE41HL (JAE)

| Pin | Name | Description | Note |
|---|---|---|---|
| 1 | N.C. | No Connection | (1) |
| 2 | N.C. | No Connection | |
| 3 | N.C. | No Connection | |
| 4 | N.C. | No Connection | |
| 5 | N.C. | No Connection | |
| 6 | N.C. | No Connection | |

| | | | |
|---|---|---|---|
| 7 | N.C. | No Connection | |
| 8 | N.C. | No Connection | |
| 9 | GND | Ground | |
| 10 | CH3[0]- | Third pixel Negative LVDS differential data input. Pair 0 | (4) |
| 11 | CH3[0]+ | Third pixel Positive LVDS differential data input. Pair 0 | |
| 12 | CH3[1]- | Third pixel Negative LVDS differential data input. Pair 1 | |
| 13 | CH3[1]+ | Third pixel Positive LVDS differential data input. Pair 1 | |
| 14 | CH3[2]- | Third pixel Negative LVDS differential data input. Pair 2 | |
| 15 | CH3[2]+ | Third pixel Positive LVDS differential data input. Pair 2 | |
| 16 | GND | Ground | |
| 17 | CH3CLK- | Third pixel Negative LVDS differential clock input. | (4) |
| 18 | CH3CLK+ | Third pixel Positive LVDS differential clock input. | |
| 19 | GND | Ground | |
| 20 | CH3[3]- | Third pixel Negative LVDS differential data input. Pair 3 | (4) |
| 21 | CH3[3]+ | Third pixel Positive LVDS differential data input. Pair 3 | |
| 22 | CH3[4]- | Third pixel Negative LVDS differential data input. Pair 4 | |
| 23 | CH3[4]+ | Third pixel Positive LVDS differential data input. Pair 4 | |
| 24 | GND | Ground | |
| 25 | GND | Ground | |
| 26 | CH4[0]- | Fourth pixel Negative LVDS differential data input. Pair 0 | (4) |
| 27 | CH4[0]+ | Fourth pixel Positive LVDS differential data input. Pair 0 | |
| 28 | CH4[1]- | Fourth pixel Negative LVDS differential data input. Pair 1 | |
| 29 | CH4[1]+ | Fourth pixel Positive LVDS differential data input. Pair 1 | |
| 30 | CH4[2]- | Fourth pixel Negative LVDS differential data input. Pair 2 | |
| 31 | CH4[2]+ | Fourth pixel Positive LVDS differential data input. Pair 2 | |
| 32 | GND | Ground | |
| 33 | CH4CLK- | Fourth pixel Negative LVDS differential clock input. | (4) |
| 34 | CH4CLK+ | Fourth pixel Positive LVDS differential clock input. | |
| 35 | GND | Ground | |
| 36 | CH4[3]- | Fourth pixel Negative LVDS differential data input. Pair 3 | (4) |
| 37 | CH4[3]+ | Fourth pixel Positive LVDS differential data input. Pair 3 | |
| 38 | CH4[4]- | Fourth pixel Negative LVDS differential data input. Pair 4 | |

| | | | |
|---|---|---|---|
| 39 | CH4[4]+ | Fourth pixel Positive LVDS differential data input. Pair 4 | |
| 40 | GND | Ground | |
| 41 | GND | Ground | |

CON2 Connector Pin Assignment (LM123S010HTF13Y or equivalent)

| | | | |
|---|---|---|---|
| 1 | N.C. | No Connection | (1) |
| 2 | N.C. | No Connection | |
| 3 | N.C. | No Connection | |
| 4 | GND | Ground | – |
| 5 | N.C. | No Connection | (1) |
| 6 | L/R_O | Output signal for Left Right Glasses control | (2) |
| 7 | N.C. | No Connection | (1) |
| 8 | N.C. | No Connection | |
| 9 | N.C. | No Connection | |
| 10 | N.C. | No Connection | |

Note (1) Reserved for internal use. Please leave it open.

Note (2) The definition of L/R_O signal as follows

L= 0V, H=+3.3V

| L/R_O | Note |
|---|---|
| L | Right glass turn on |
| H | Left glass turn on |

Note (3) LVDS format selection.

L= Connect to GND, H=Connect to +3.3V or Open

| SELLVDS | Note |
|---|---|
| L | JEIDA Format |
| H or Open | VESA Format |

Note (4) LVDS Data Mapping

LVDS 4-port FHD 100/120Hz Input

| Port | Channel of LVDS | Data Stream |
|---|---|---|
| 1st Port | First Pixel | 1, 5, 9, ……1913, 1917 |
| 2nd Port | Second Pixel | 2, 6, 10, ….1914, 1918 |
| 3rd Port | Third Pixel | 3, 7, 11, ….1915, 1919 |
| 4th Port | Fourth Pixel | 4, 8, 12, ….1916, 1920 |

LVDS 2port FHD 50/60Hz Input

| Port | Channel of LVDS | Data Stream |
|---|---|---|
| 1st Port | First Pixel | 1, 3, 5, ……1917, 1919 |
| 2nd Port | Second Pixel | 2, 4, 6, ….1918, 1920 |

LVDS 4-port QFHD 24/30Hz Input

| Port | Channel of LVDS | Data Stream |
|---|---|---|
| 1st Port | First Pixel | 1, 5, 9, ……3833, 3837 |
| 2nd Port | Second Pixel | 2, 6, 10, ….3834, 3838 |
| 3rd Port | Third Pixel | 3, 7, 11, ….3835, 3839 |
| 4th Port | Fourth Pixel | 4, 8, 12, ….3836, 3840 |

Note (5) 2D/3D mode selection.

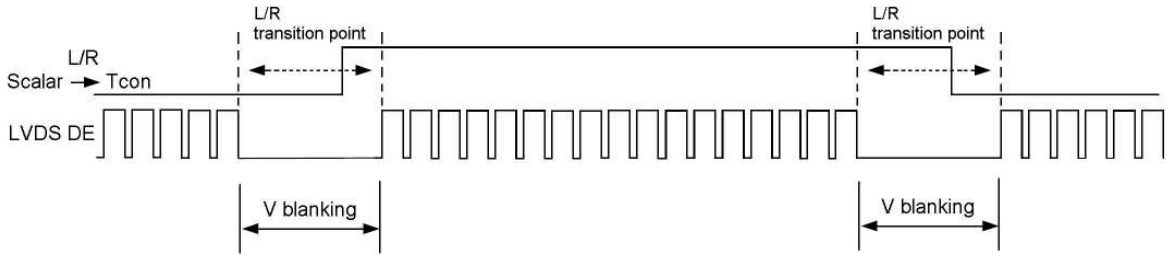
L= Connect to GND or Open, H=Connect to +3.3V

| 2D/3D | Note |
|---|---|
| L or Open | 2D Mode |
| H | 3D Mode |

Note (6) Input signal for left and right eye frame synchronous

$V_{IL}$=0~0.7 V, $V_{IH}$=2.7~3.3 V

| L/R | Note |
|---|---|
| L | Right synchronous signal |
| H | Left synchronous signal |



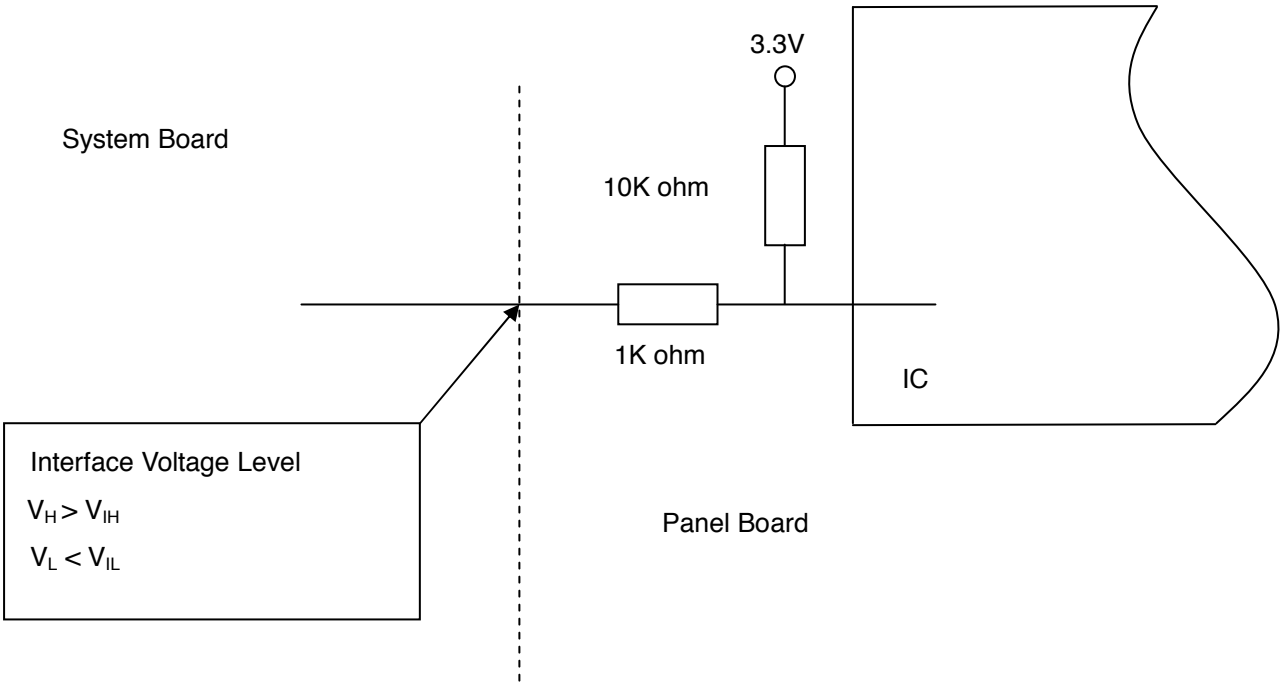

Note (7) Local dimming enable selection.

L= Connect to GND，H=Connect to +3.3V or Open

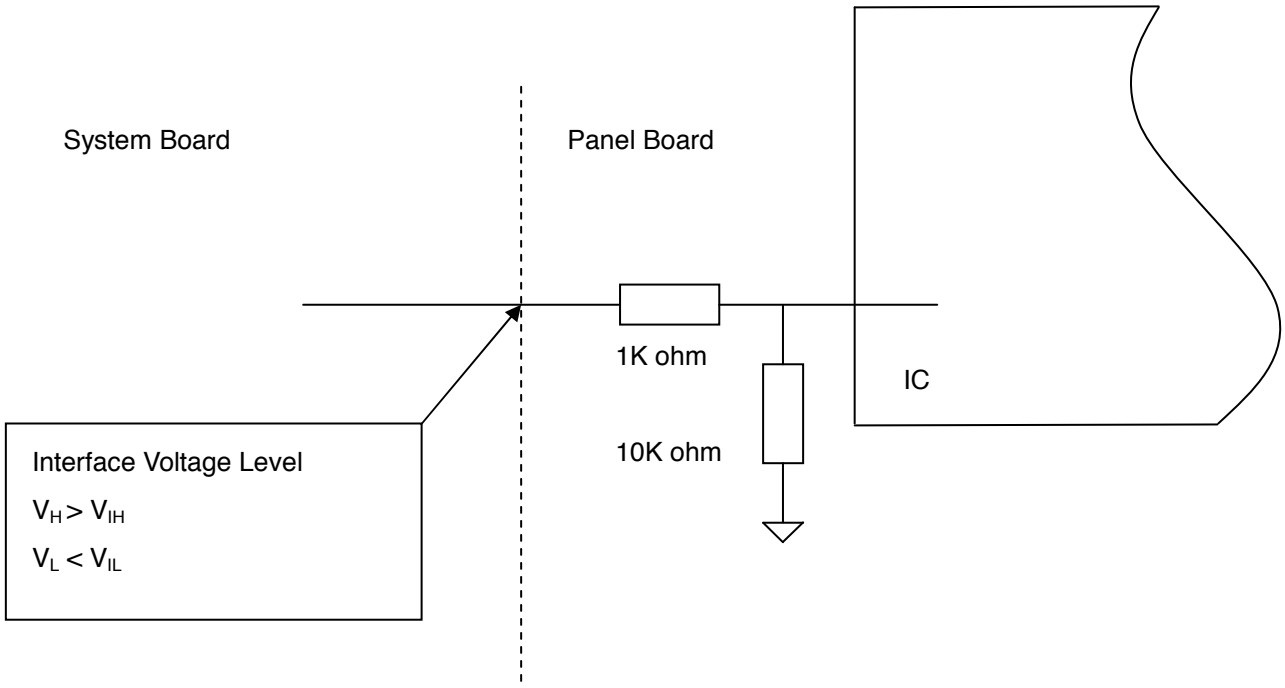
| LD_EN | Note |
|---|---|
| L | Local Dimming Disable |
| H or Open | Local Dimming Enable |

Note (8) Reserved for internal use. Open is preferred. However, it is also acceptable to reserve the wire connecting with specific High/Low voltage level.

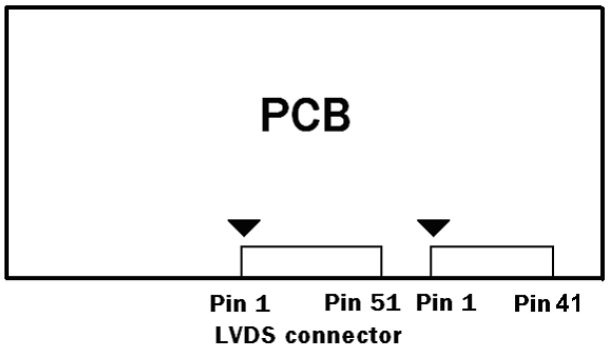
Note (9) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement which including panel board loading as below.



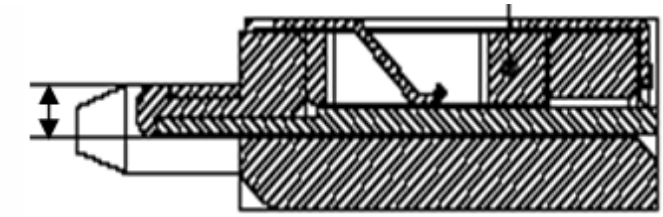

Note (10) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement which including panel board loading as below.



Note (11) LVDS connector pin order defined as follows




Note (12) LVDS connector mating dimension range request is 0.93mm~1.0mm as below



## 5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN2: FF01-430-123A(FCN) or 196388-12041-3(P-TWO).

| Pin № | Symbol | Feature |
|---|---|---|
| 1 | VLED+ | Positive of LED String |
| 2 | VLED+ | |
| 3 | VLED+ | |
| 4 | NC | NC |
| 5 | VLED- | Negative of LED String |
| 6 | VLED- | |
| 7 | VLED- | |
| 8 | VLED- | |
| 9 | VLED- | |
| 10 | VLED- | |
| 11 | VLED- | |
| 12 | VLED- | |

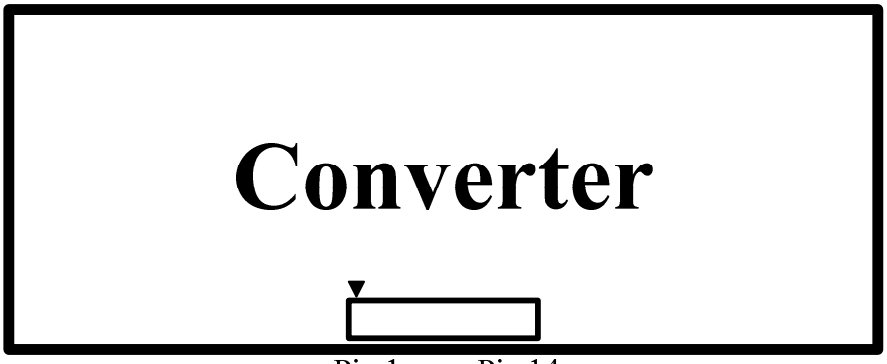
### 5.3 CONVERTER UNIT

CN1 (Header) : JH2-D4-143N(FCN) or CI0114M1HR0-LA (CvilLux)

| Pin No. | Symbol | Feature |
|---|---|---|
| 1 | VBL | +24V |
| 2 | | |
| 3 | | |
| 4 | | |
| 5 | | |
| 6 | GND | GND |
| 7 | | |
| 8 | | |
| 9 | | |
| 10 | | |
| 11 | ERR | Normal (GND) ; Abnormal (Open collector) |
| 12 | BLON | BL ON/OFF |
| 13 | NC | NC |
| 14 | E_PWM | External PWM Control |

Note (1) If Pin14 is open, E_PWM is 100% duty.

Note (2) Input connector pin order defined as follows

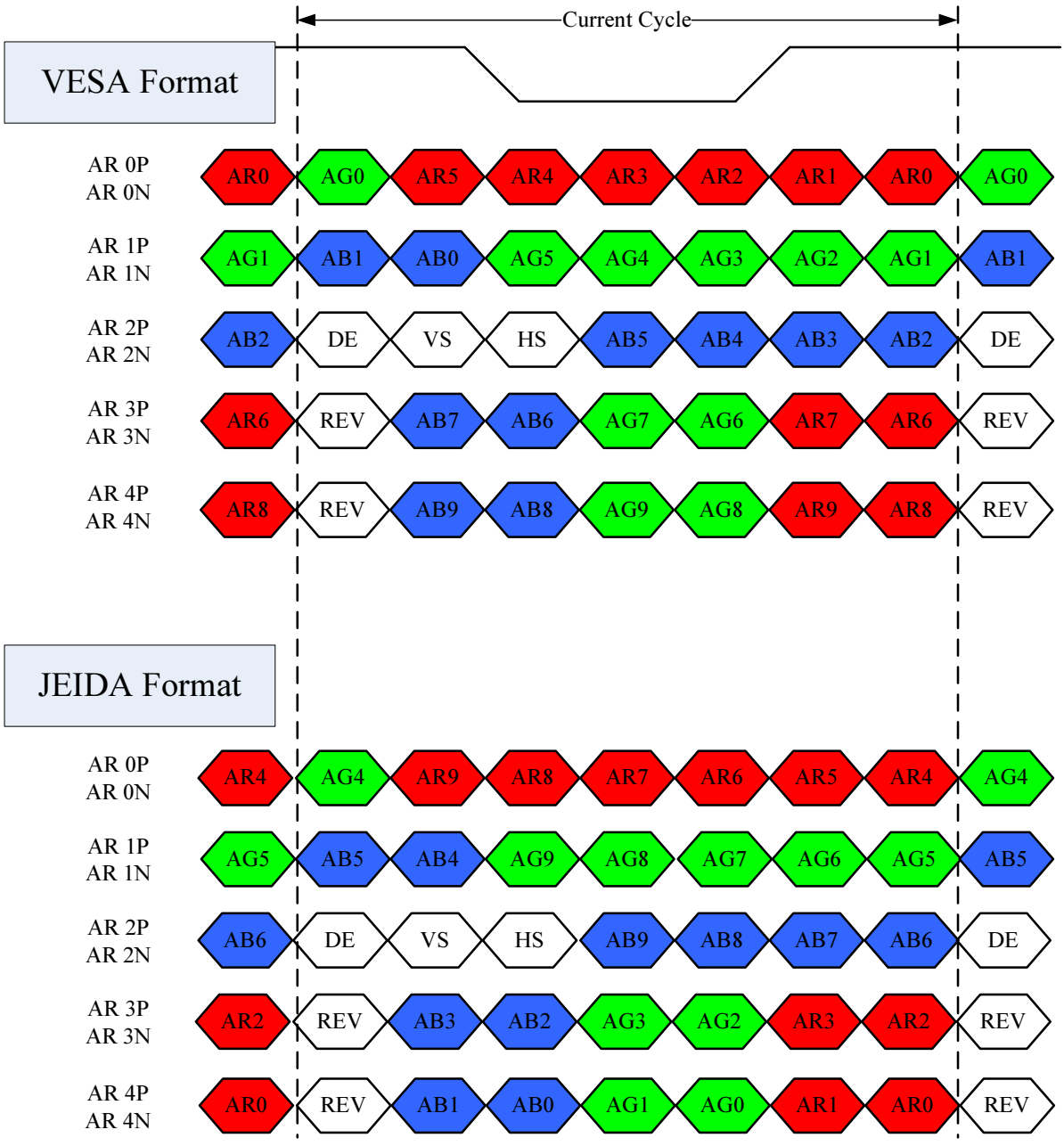



**Input Connector**

## 5.4 LVDS INTERFACE

JEIDA Format : SELLVDS = L

VESA Format : SELLVDS = H or Open




R0~R9: Pixel R Data (9; MSB, 0; LSB)

G0~G9: Pixel G Data (9; MSB, 0; LSB)

B0~B9: Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be “H” or “L”.

## 5.5 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

| Color | | Data Signal | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Red | | | | | | | | | | Green | | | | | | | | | | Blue | | | | | | | | | |
| | | R9 | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | G9 | G8 | G7 | G6 | G5 | G4 | G3 | G2 | G1 | G0 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Basic Colors | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Cyan | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Magenta | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Yellow | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | White | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Gray Scale Of Red | Red (0) / Dark | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red (1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red (2) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | : | | | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | : | | | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | Red (1021) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red (1022) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red (1023) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Gray Scale Of Green | Green (0) / Dark | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green (1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green (2) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | Green (1021) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green (1022) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green (1023) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Gray Scale Of Blue | Blue (0) / Dark | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | Blue (1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | Blue (2) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | Blue (1021) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| | Blue (1022) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| | Blue (1023) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Note (1) 0: Low Level Voltage，1: High Level Voltage

# 6. INTERFACE TIMING

## 6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram. (Ta = 25 ± 2 °C)

| Signal | Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| LVDS Receiver Clock | Input cycle to cycle jitter | $T_{rcl}$ | - | - | 200 | ps | (1) |
| | Spread spectrum modulation range | $F_{clkin\_mod}$ | $F_{clkin}$-1.5% | - | $F_{clkin}$+1.5% | MHz | (2) |
| | Spread spectrum modulation frequency | $F_{SSM}$ | - | - | 66 | KHz | |
| LVDS Receiver Data | Receiver skew margin | $T_{RSKM}$ | -400 | - | 400 | ps | (3) |

### 6.1.1 Input Timing Spec for FHD, Frame Rate = 50Hz

| Signal | Item | | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| LVDS Clock | Frequency | | $F_{clkin}$ (=1/TC) | 60 | 74.25 | 79 | MHz | (4) |
| Frame Rate | 2D Mode | | $F_r$ | 47 | 50 | 53 | Hz | (5) |
| Vertical Active Display Term | 2D Mode | Total | Tv | 1104 | 1350 | 1395 | Th | Tv=Tvd+Tvb |
| | | Display | Tvd | 1080 | | | Th | |
| | | Blank | Tvb | 24 | 270 | 315 | Th | |
| | | Front porch | Tvfp | 10 | — | — | Th | (6) |
| | | Back porch | Tvbp | 10 | — | — | Th | |
| | | Vsync | Tvswid | 4 | — | — | Th | |
| Horizontal Active Display Term | | Total | Th | 1060 | 1100 | 1340 | Tc | Th=Thd+Thb |
| | | Display | Thd | 960 | | | Tc | |
| | | Blank | Thb | 100 | 140 | 380 | Tc | |
| | | Front porch | Thfp | 5 | — | — | Tc | (6) |
| | | Back porch | Thbp | 5 | — | — | Tc | |
| | | Hsync | Thswid | 2 | — | — | Tc | |

### 6.1.2 Input Timing Spec for FHD, Frame Rate = 60Hz

| Signal | Item | | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| LVDS Clock | Frequency | | $F_{clkin}$ (=1/TC) | 60 | 74.25 | 79 | MHz | (4) |
| Frame Rate | 2D Mode | | $F_r$ | 57 | 60 | 63 | Hz | (5) |
| Vertical Active Display Term | 2D Mode | Total | Tv | 1104 | 1125 | 1395 | Th | Tv=Tvd+Tvb |
| | | Display | Tvd | 1080 | | | Th | |
| | | Blank | Tvb | 24 | 45 | 315 | Th | |
| | | Front porch | Tvfp | 10 | — | — | Th | (6) |
| | | Back porch | Tvbp | 10 | — | — | Th | |
| | | Vsync | Tvswid | 4 | — | — | Th | |
| Horizontal Active Display Term | | Total | Th | 1060 | 1100 | 1340 | Tc | Th=Thd+Thb |
| | | Display | Thd | 960 | | | Tc | |
| | | Blank | Thb | 100 | 140 | 380 | Tc | |
| | | Front porch | Thfp | 5 | — | — | Tc | (6) |
| | | Back porch | Thbp | 5 | — | — | Tc | |
| | | Hsync | Thswid | 2 | — | — | Tc | |

### 6.1.3 Input Timing Spec for FHD, Frame Rate = 100Hz

| Signal | Item | | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| LVDS Clock | Frequency | | $F_{clkin}$ (=1/TC) | 60 | 74.25 | 79 | MHz | (4) |
| Frame Rate | 2D Mode | | $F_r$ | 97 | 100 | 103 | Hz | (5) |
| Vertical Active Display Term | 2D Mode | Total | Tv | 1104 | 1350 | 1395 | Th | Tv=Tvd+Tvb |
| | | Display | Tvd | 1080 | | | Th | |
| | | Blank | Tvb | 24 | 270 | 315 | Th | |
| | | Front porch | Tvfp | 10 | — | — | Th | (6) |
| | | Back porch | Tvbp | 10 | — | — | Th | |
| | | Vsync | Tvswid | 4 | — | — | Th | |
| Horizontal Active | | Total | Th | 530 | 550 | 670 | Tc | Th=Thd+Thb |
| | | Display | Thd | 480 | | | Tc | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Display Term | | Blank | Thb | 50 | 70 | 190 | Tc | |
| | | Front porch | Thfp | 5 | — | — | Tc | (6) |
| | | Back porch | Thbp | 5 | — | — | Tc | |
| | | Hsync | Thswid | 2 | — | — | Tc | |

### 6.1.4 Input Timing Spec for FHD, Frame Rate = 120Hz

| Signal | Item | | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| LVDS Clock | 2D Mode | | $F_{clkin}$ (=1/TC) | 60 | 74.25 | 79 | MHz | (4) |
| | 3D Mode | | | 74.25 | | | MHz | |
| Frame Rate | 2D Mode | | $F_r$ | 117 | 120 | 123 | Hz | (5) |
| | 3D Mode | | | 120 | | | Hz | |
| Vertical Active Display Term | 2D Mode | Total | Tv | 1104 | 1125 | 1395 | Th | Tv=Tvd+Tvb |
| | | Display | Tvd | 1080 | | | Th | |
| | | Blank | Tvb | 24 | 45 | 315 | Th | |
| | | Front porch | Tvfp | 10 | — | — | Th | (6) |
| | | Back porch | Tvbp | 10 | — | — | Th | |
| | | Vsync | Tvswid | 4 | — | — | Th | |
| | 3D Mode | Total | Tv | 1125 | | | Th | |
| | | Display | Tvd | 1080 | | | Th | |
| | | Blank | Tvb | 45 | | | Th | |
| | | Front porch | Tvfp | 10 | — | — | — | (6) |
| | | Back porch | Tvbp | 10 | — | — | — | |
| | | Vsync | Tvswid | 4 | — | — | — | |
| Horizontal Active Display Term | 2D Mode | Total | Th | 530 | 550 | 670 | Tc | Th=Thd+Thb |
| | | Display | Thd | 480 | | | Tc | |
| | | Blank | Thb | 50 | 70 | 190 | Tc | |
| | | Front porch | Thfp | 5 | — | — | Tc | (6) |
| | | Back porch | Thbp | 5 | — | — | Tc | |
| | | Hsync | Thswid | 2 | — | — | Tc | |
| | 3D Mode | Total | Th | 530 | 550 | 670 | Tc | Th=Thd+Thb |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | Display | Thd | 480 | | | Tc | |
| | | Blank | Thb | 50 | 70 | 190 | Tc | |
| | | Front porch | Thfp | 5 | — | — | Tc | (6) |
| | | Back porch | Thbp | 5 | — | — | Tc | |
| | | Hsync | Thswid | 2 | — | — | Tc | |

### 6.1.5 Input Timing spec for QFHD, Frame Rate = 24Hz

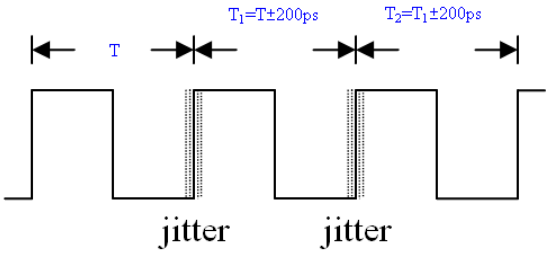
| Signal | Item | | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| LVDS Clock | Frequency | | $F_{clkin}$ (=1/TC) | 60 | 74.25 | 79 | MHz | (4) |
| Frame Rate | 2D Mode | | $F_r$ | 23 | 24 | 25 | Hz | (5) |
| Vertical Active Display Term | 2D Mode | Total | Tv | 2208 | 2250 | 2450 | Th | Tv=Tvd+Tvb |
| | | Display | Tvd | 2160 | | | Th | |
| | | Blank | Tvb | 48 | 90 | 290 | Th | |
| | | Front porch | Tvfp | 20 | — | — | Th | (6) |
| | | Back porch | Tvbp | 20 | — | — | Th | |
| | | Vsync | Tvswid | 8 | — | — | Th | |
| Horizontal Active Display Term | | Total | Th | 992 | 1375 | 1440 | Tc | Th=Thd+Thb |
| | | Display | Thd | 960 | | | Tc | |
| | | Blank | Thb | 32 | 415 | 480 | Tc | |
| | | Front porch | Thfp | 12 | — | — | Tc | (6) |
| | | Back porch | Thbp | 10 | — | — | Tc | |
| | | Hsync | Thswid | 4 | — | — | Tc | |

### 6.1.6 Input Timing spec for QFHD, Frame Rate = 30Hz

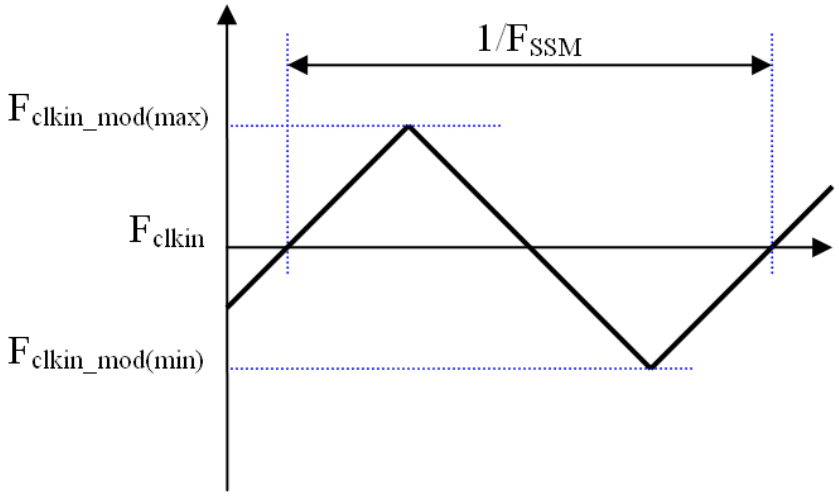
| Signal | Item | | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| LVDS Clock | Frequency | | $F_{clkin}$ (=1/TC) | 60 | 74.25 | 79 | MHz | (4) |
| Frame Rate | 2D Mode | | $F_r$ | 29 | 30 | 31 | Hz | (5) |
| Vertical Active | 2D Mode | Total | Tv | 2208 | 2250 | 2450 | Th | Tv=Tvd+Tvb |
| | | Display | Tvd | 2160 | | | Th | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Display Term | | Blank | Tvb | 48 | 90 | 290 | Th | |
| | | Front porch | Tvfp | 20 | — | — | Th | (6) |
| | | Back porch | Tvbp | 20 | — | — | Th | |
| | | Vsync | Tvswid | 8 | — | — | Th | |
| Horizontal Active Display Term | | Total | Th | 992 | 1100 | 1340 | Tc | Th=Thd+Thb |
| | | Display | Thd | 960 | | | Tc | |
| | | Blank | Thb | 32 | 140 | 380 | Tc | |
| | | Front porch | Thfp | 12 | — | — | Tc | (6) |
| | | Back porch | Thbp | 10 | — | — | Tc | |
| | | Hsync | Thswid | 4 | — | — | Tc | |

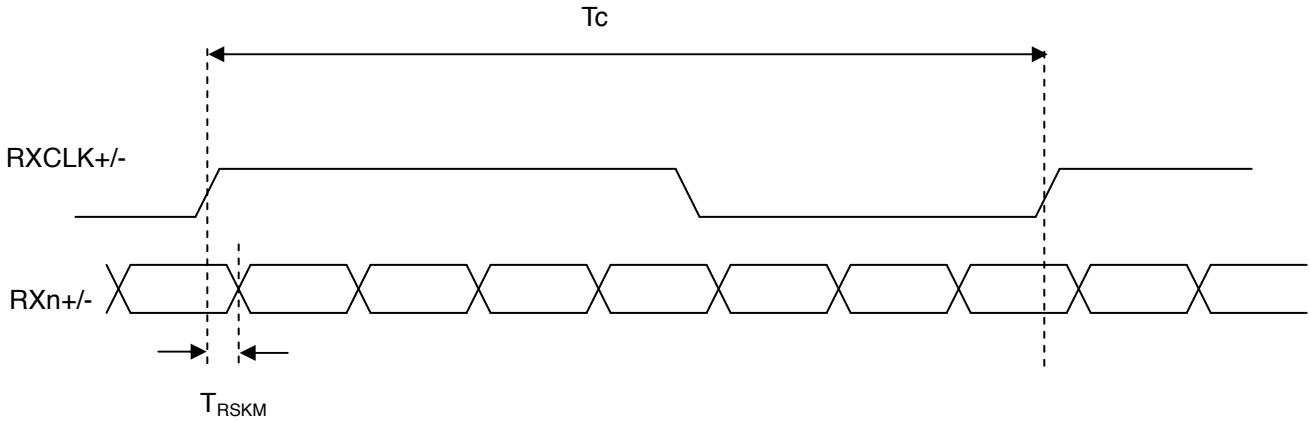
Note (1) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = | $T_1 - T$ |




Note (2) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (3) The LVDS timing diagram and the receiver skew margin is defined and shown in following figure.



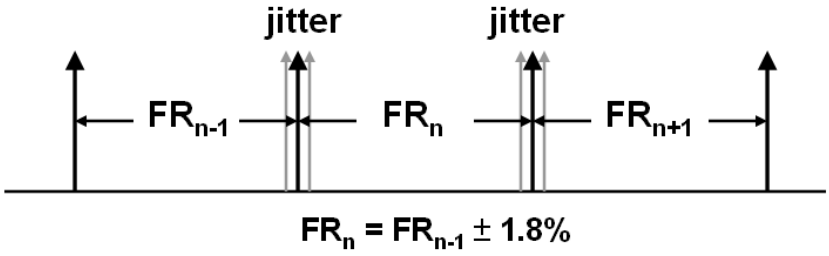

Note (4) Please make sure the range of pixel clock has follow the below equations.

Fclkin (max) ≧ (Fr × Tv × Th) ≧ Fclkin(min)

Note (5)

a. The frame-to-frame jitter of the input frame rate is defined as the following figure.

b. FRn = FRn-1 ± 1.8%.

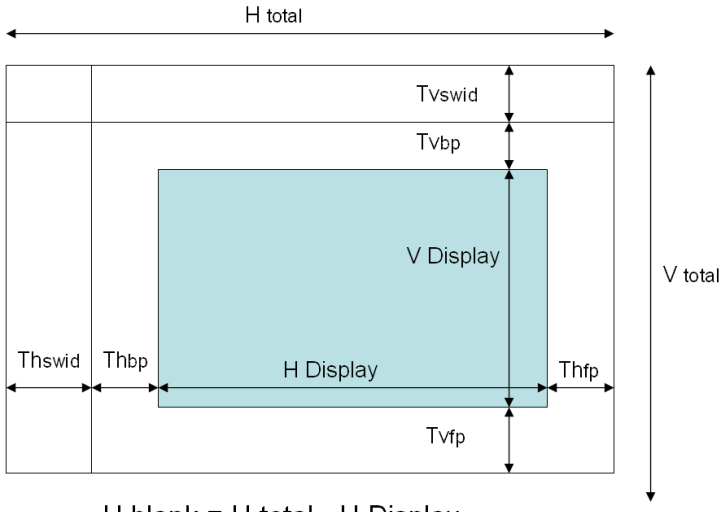



Note (6)

c. Hsync and Vsync signals are necessary for this module.

d. The polarity of Hsync & Vsync should be positive.

e. Please follow the input signal timing diagram as below :



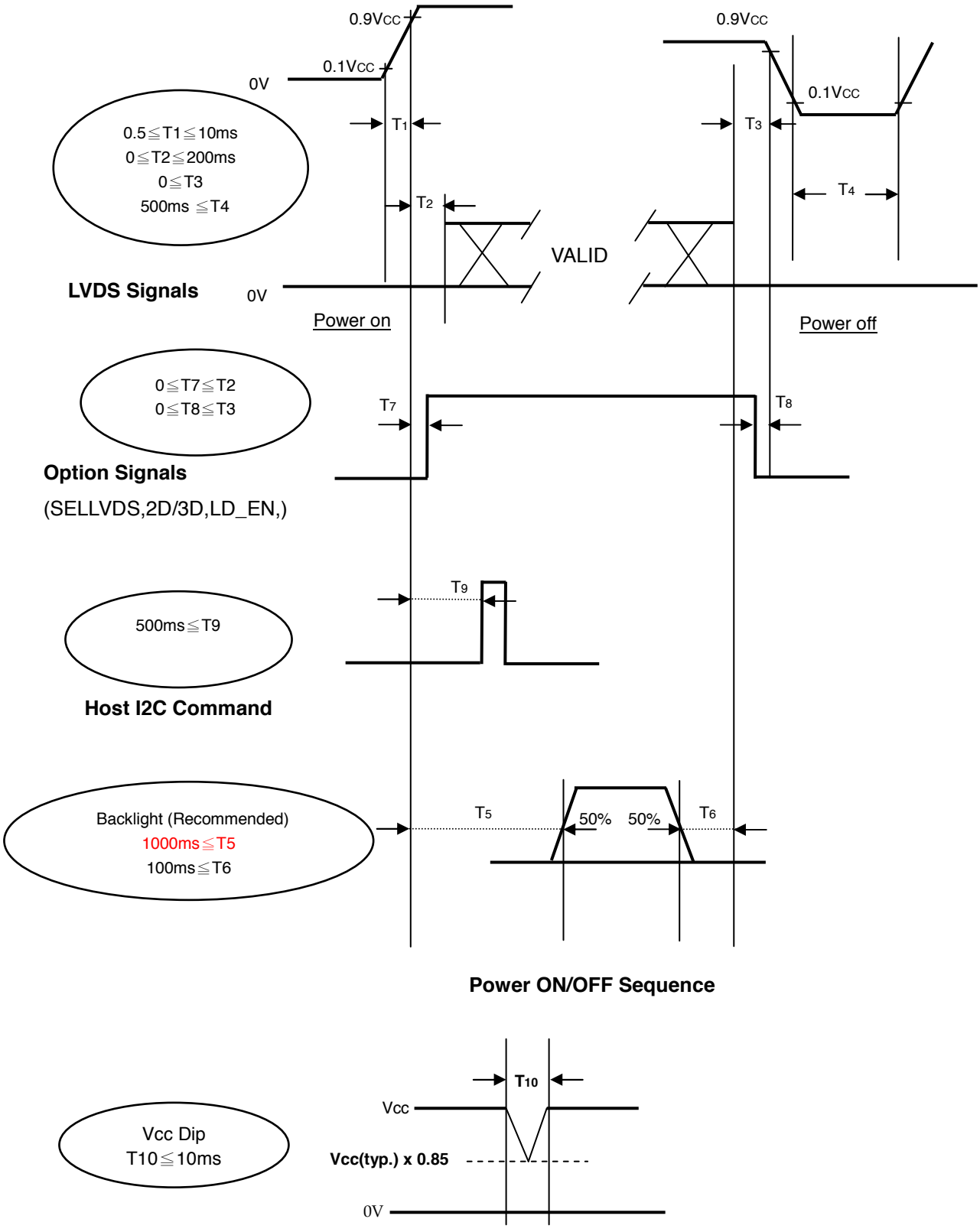

H blank = H total - H Display

V blank = V total - V Display

## 6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 °C)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Note (1) The supply voltage of external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of VCC=off, please keep the level of input signals on the low or high impedance.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

Note (6) Vcc must decay smoothly when power-off.

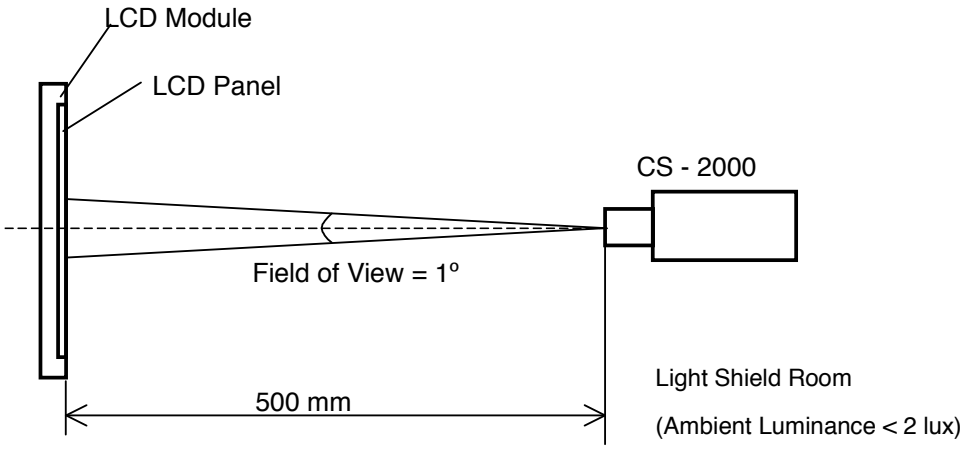
## 7. OPTICAL CHARACTERISTICS

### 7.1 TEST CONDITIONS

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Ambient Temperature | Ta | 25±2 | °C |
| Ambient Humidity | Ha | 50±10 | %RH |
| Supply Voltage | $V_{CC}$ | 12±1.2 | V |
| Input Signal | According to typical value in "3. ELECTRICAL CHARACTERISTICS" | | |
| Vertical Frame Rate | Fr | 120 | Hz |

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.

Local Dimming Function should be Disable before testing to get the steady optical characteristics (According to 5.1 CNF1 Connector Pin Assignment, Pin no. “42”)



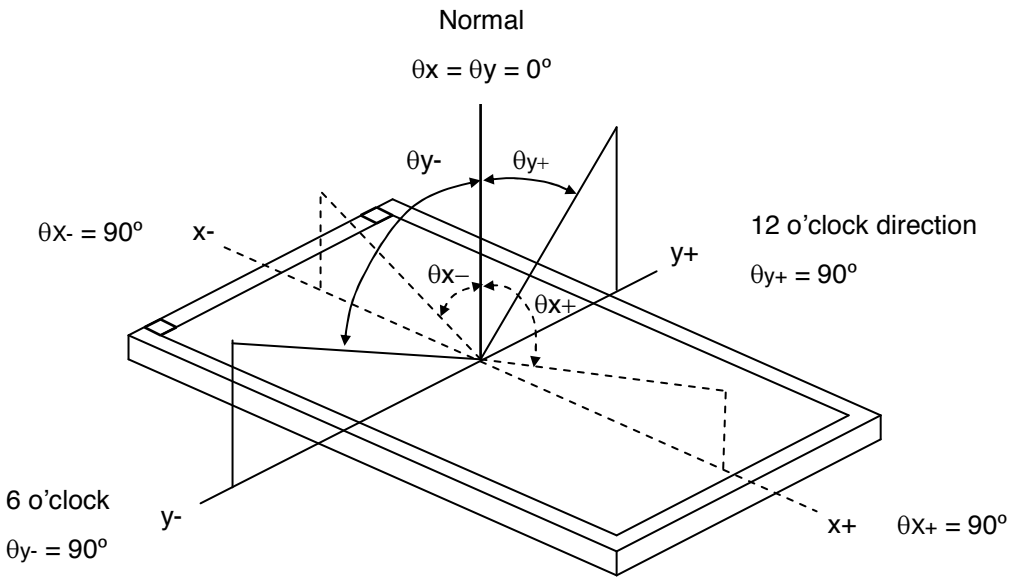
## 7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

| Item | | Symbol | | Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| Contrast Ratio | | CR | | $\theta_x$=0°, $\theta_Y$ =0° Viewing angle at normal direction | (3500) | (5000) | - | - | Note (2) |
| Response Time | | Gray to gray | | | | (6.5) | (13) | ms | Note (3) |
| Center Luminance of White | | $L_C$ | 2D | | (280) | (350) | - | cd/m$^2$ | Note (4) |
| | | | 3D | | | (60) | - | cd/m$^2$ | Note (8) |
| White Variation | | $\delta$W | | | | | 1.3 | - | Note (6) |
| Cross Talk | | CT | 2D | | - | | 4 | % | Note (5) |
| | | | 3D-W | | | 4 | - | % | Note (8) |
| | | | 3D-D | | | 11 | - | % | Note (8) |
| Color Chromaticity | Red | Rx | | | Typ.-0.03 | (0.645) | Typ.+0.03 | - | |
| | | Ry | | | | (0.335) | | - | |
| | Green | Gx | | | | (0.306) | | - | |
| | | Gy | | | | (0.617) | | - | |
| | Blue | Bx | | | | (0.149) | | - | |
| | | By | | | | (0.058) | | - | |
| | White | Wx | | | | (0.280) | | - | |
| | | Wy | | | | (0.290) | | - | |
| | Correlated color temperature | | | | | (9800) | | K | |
| | Color Gamut | C.G. | | | - | (72) | - | % | NTSC |
| Viewing Angle | Horizontal | $\theta_x$+ | | CR≥20 | 80 | 88 | - | Deg. | (1) |
| | | $\theta_x$- | | | 80 | 88 | - | | |
| | Vertical | $\theta_Y$+ | | | 80 | 88 | - | | |
| | | $\theta_Y$- | | | 80 | 88 | - | | |
| Transmission direction of the up polarizer | | $\Phi_{up}$ | | - | - | 90 | - | Deg. | (7) |

Note (1) Definition of Viewing Angle (θx, θy) :

Viewing angles are measured by Autronic Conoscope Cono-80 (or Eldim EZ-Contrast 160R).




Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

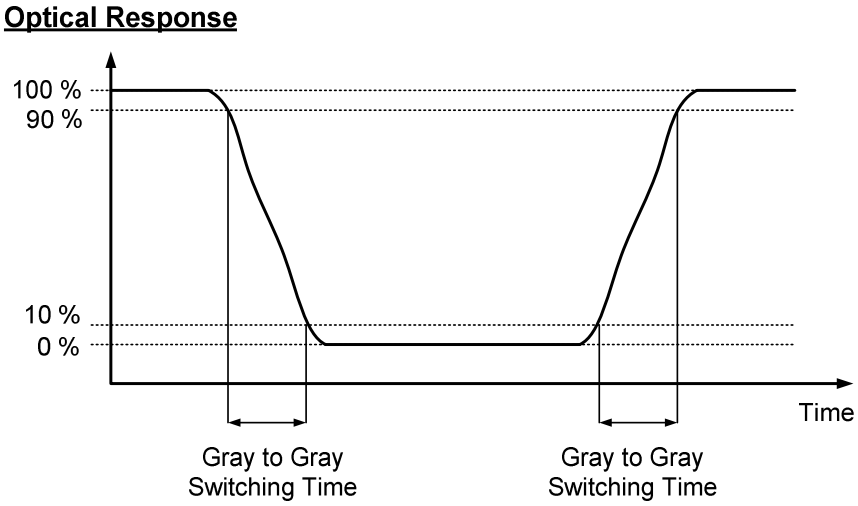
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L1023}}{\text{Surface Luminance of L0}}$$

L1023: Luminance of gray level 1023

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time :




The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

Note (4) Definition of Luminance of White ($L_C$) :

Measure the luminance of gray level 1023 at center point.

$L_C$ = L (5), where L (x) is corresponding to the luminance of the point X at the figure in Note (6).

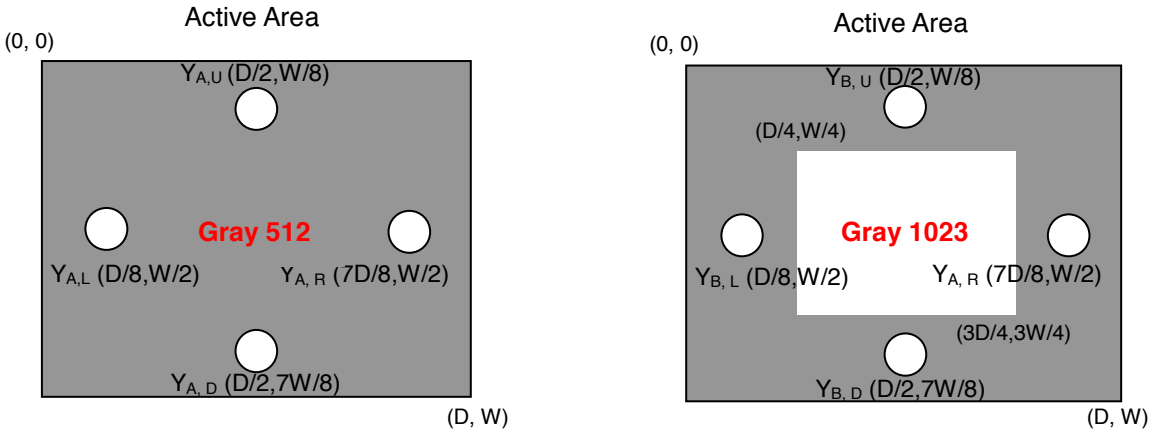
Note (5) Definition of Cross Talk (CT) :

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where :

YA = Luminance of measured location without gray level 1023 pattern (cd/m2)

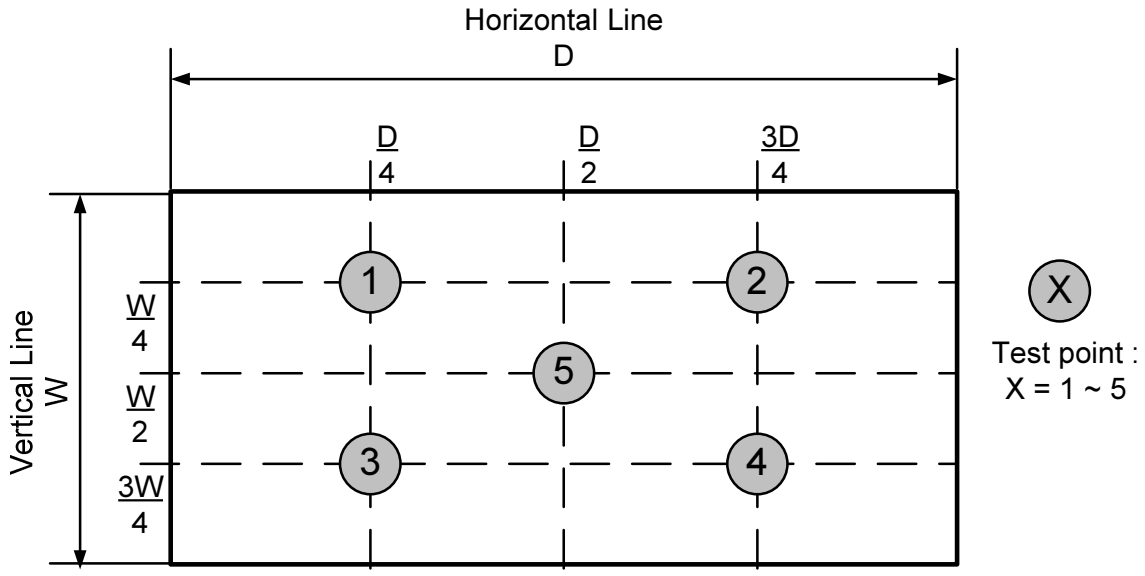
YB = Luminance of measured location with gray level 1023 pattern (cd/m2)



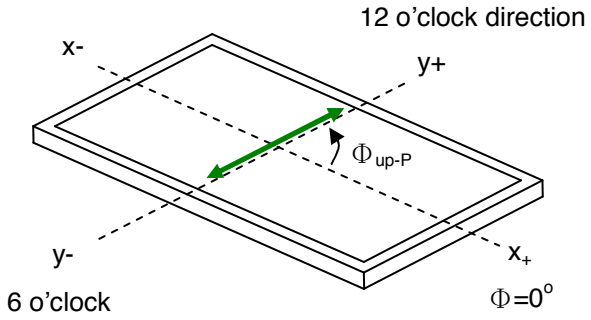

Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 1023 at 5 points

$$\delta W = \frac{\text{Maximum}[L(1), L(2), L(3), L(4), L(5)]}{\text{Minimum}[L(1), L(2), L(3), L(4), L(5)]}$$

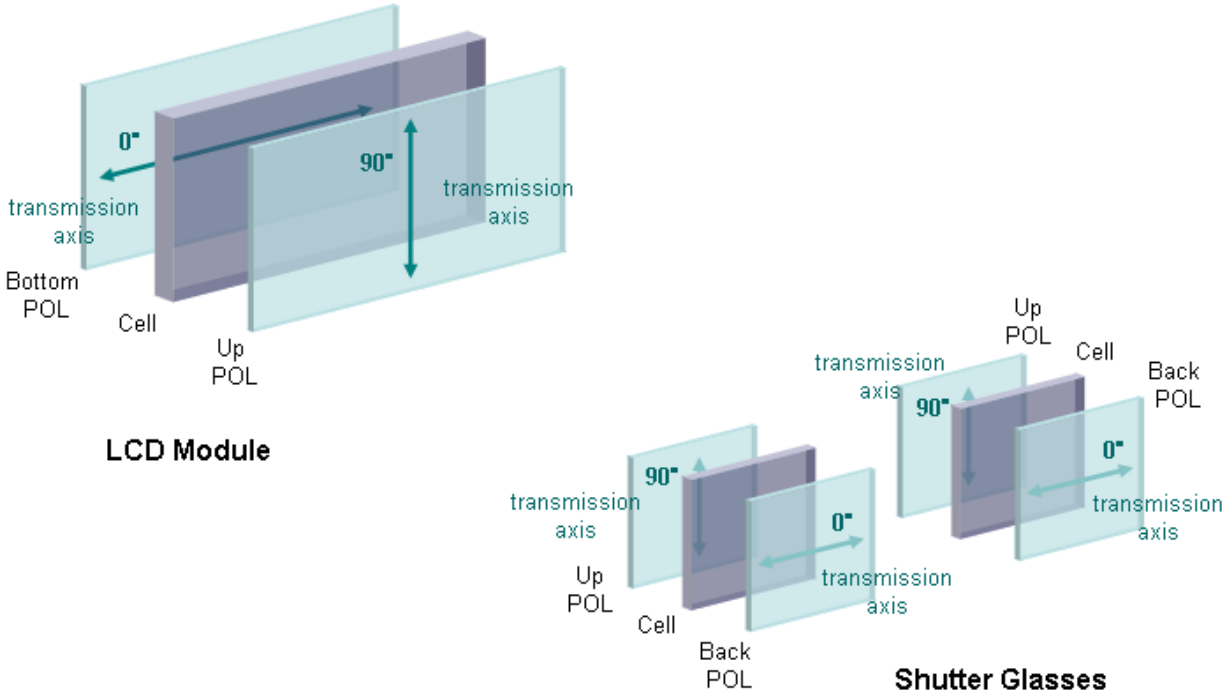


Note (7) This is a reference for designing the shutter glasses of 3D application. Definition of the transmission direction of the up polarizer ($\Phi_{up-P}$) on LCD Module :




Up Polarizer

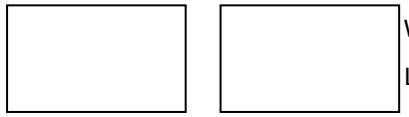
The transmission axis of the front polarizer of the shutter glasses should be parallel to this panel transmission direction to get a maximum 3D mode luminance.



Note (8) Definition of the 3D mode performance (measured under 3D mode, use INX's shutter glass) :

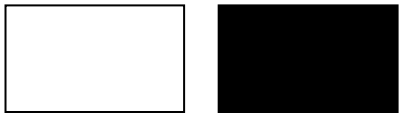
a. Test pattern

Left eye image and right eye image are displayed alternated



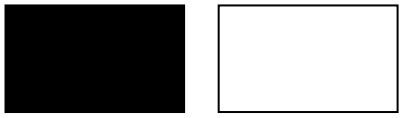
WW

Left eye image: W1023; Right eye image: W1023



WB

Left eye image: W1023; Right eye image: W0



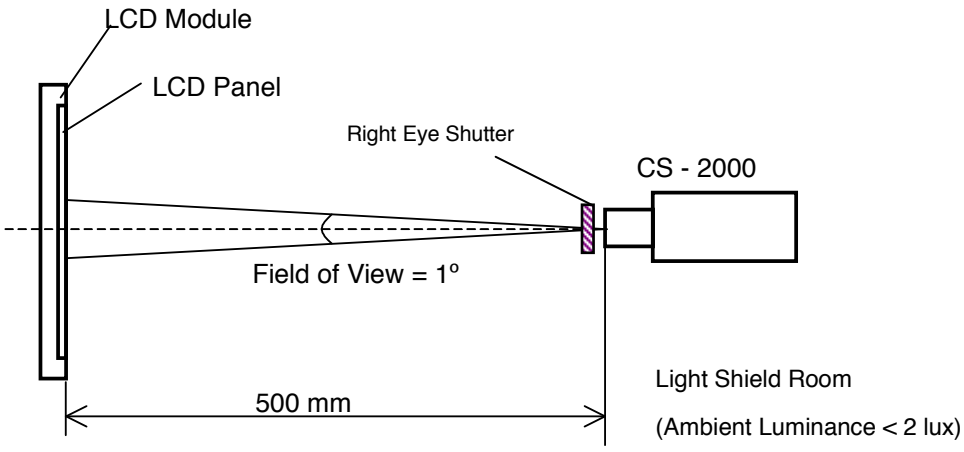
BW

Left eye image: W0; Right eye image: W1023

BB

Left eye image: W0; Right eye image: W0

b. Measurement setup




Shutter glasses are well controlled under suitable timing, and measure the luminance of the center point of the panel through the right eye glass. The transmittance of the glass should be larger than 40.0% under 3D mode operation. The luminance of the test pattern "WW", denoted L(WW); the luminance of the test pattern "WB", denoted L(WB) ; the luminance of the test pattern "BW", denoted L(BW); the luminance of the test pattern "BB", denoted "L(BB)

c. Definition of the Center Luminance of White, Lc (3D) : L(WW)

d. Definition of the 3D mode white crosstalk, CT (3D-W) : $CT(3D-W) \equiv \left| \frac{L(WB) - L(BB)}{L(WW) - L(BB)} \right|$

e. Definition of the 3D mode dark crosstalk, CT (3D-D) : $CT(3D-D) \equiv \left| \frac{L(WW) - L(BW)}{L(WW) - L(BB)} \right|$

# 8. PRECAUTIONS

## 8.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of LED will be higher than that of room temperature.

## 8.2 SAFETY PRECAUTIONS

(1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

## 8.3 SAFETY STANDARDS

The LCD module should be certified with safety regulations as follows:

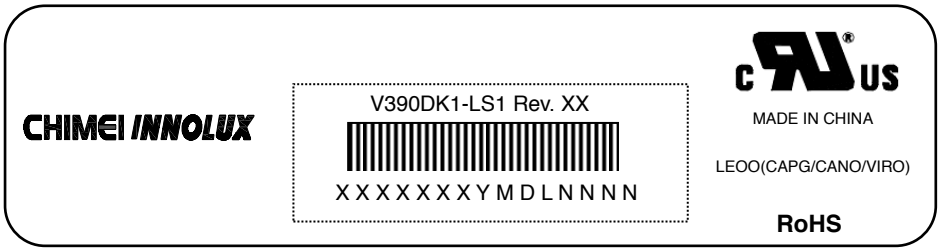
| Regulatory | Item | Standard |
|---|---|---|
| Information Technology equipment | UL | UL60950-1:2006 or Ed.2:2007 |
| | cUL | CAN/CSA C22.2 No.60950-1-03 or 60950-1-07 |
| | CB | IEC60950-1:2005 / EN60950-1:2006+ A11:2009 |
| Audio/Video Apparatus | UL | UL60065 Ed.7:2007 |
| | cUL | CAN/CSA C22.2 No.60065-03:2006 + A1:2006 |
| | CB | IEC60065:2001+ A1:2005 / EN60065:2002 + A1:2006+ A11:2008 |

If the module displays the same pattern for a long period of time, the phenomenon of image sticking may be occurred.

## 9. DEFINITION OF LABELS

### 9.1 INX MODULE LABEL

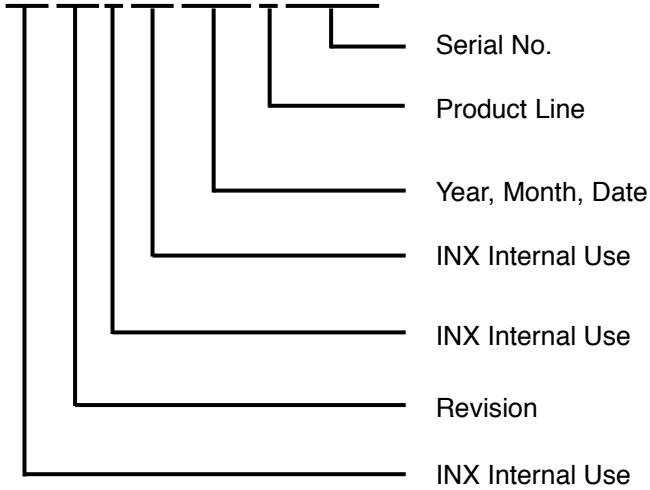
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.




Model Name : V390DK1-LS1

Revision : Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID : X X X X X X X Y M D L N N N N




Serial ID includes the information as below:

Manufactured Date:

Year : 2001=1, 2002=2, 2003=3, 2004=4…2010=0, 2011=1, 2012=2…

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code : Cover all the change

Serial No. : Manufacturing sequence of product

Product Line : 1→Line1, 2→Line 2, …etc.

## 9.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation.

P.O. NO._____

Parts ID._____

Model Name V390DK1-LS1

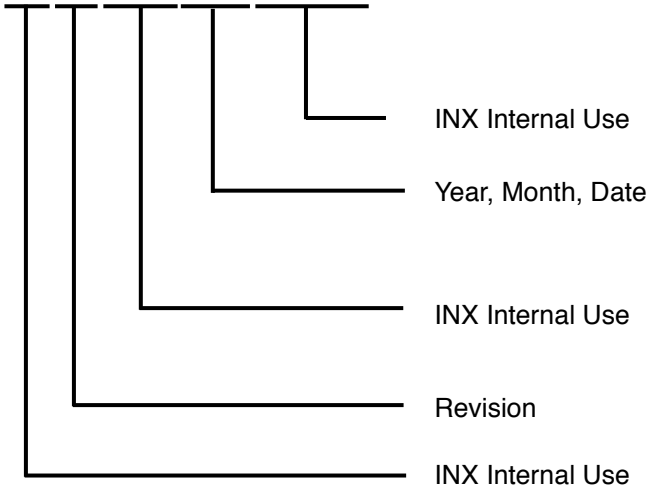
Carton ID._____ Quantities ___

XXXXXXXXXXXXX

Made In Taiwan (Made In China)

Model Name: V390DK1– LS1

Carton ID: X X X X X X X Y M D X X X X




Serial ID includes the information as below :

Manufactured Date:

Year: 2010=0, 2011=1, 2012=2…etc.

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

# 10. PACKAGING

## 10.1 PACKAGING SPECIFICATIONS

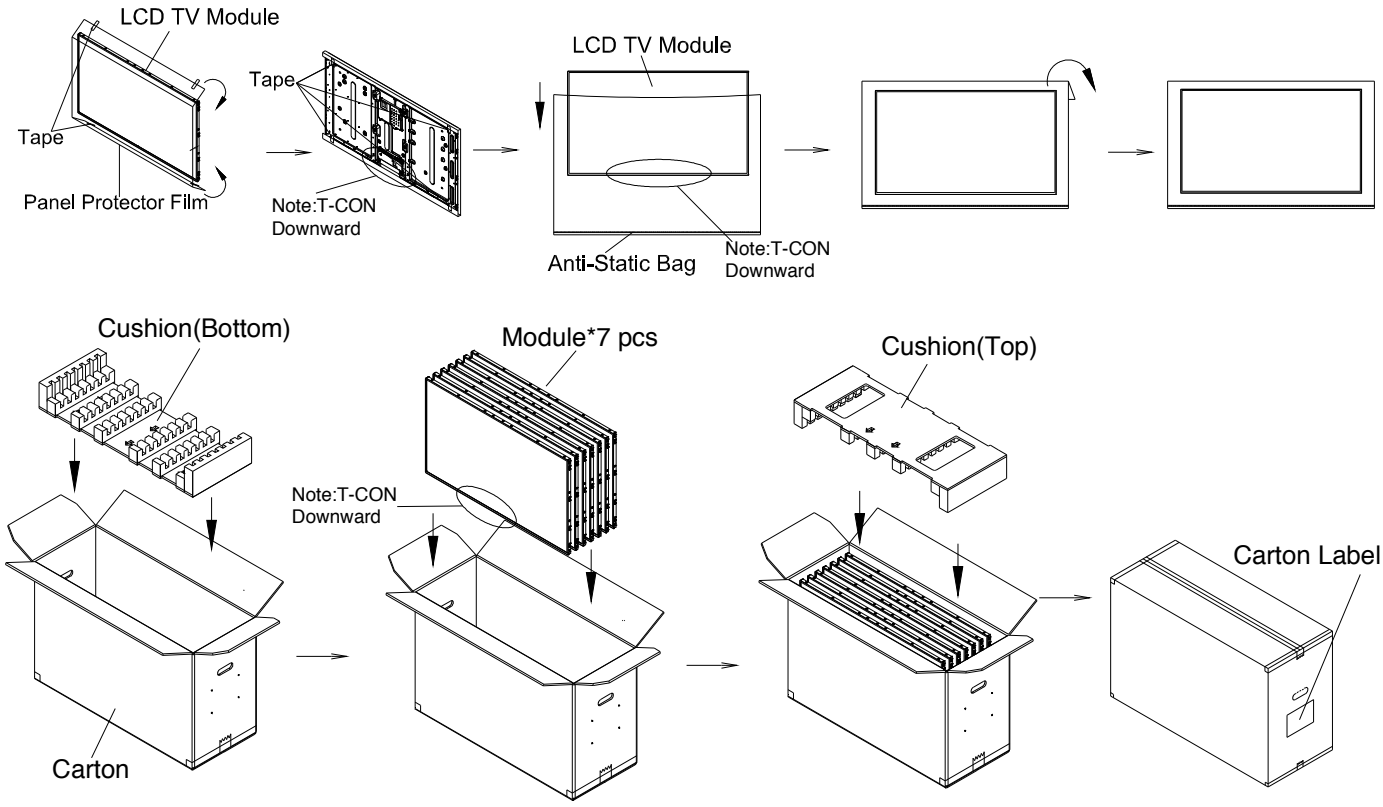
(1) 7 LCD TV modules / 1 Box

(2) Box dimensions : 954(L) X 378 (W) X 602 (H)

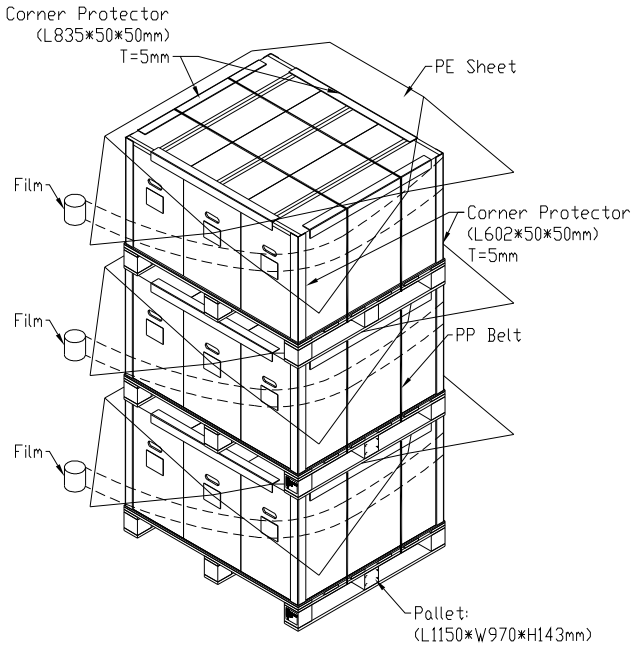
(3) Weight: approximately 54 Kg (7 modules per box)

## 10.2 PACKAGING METHOD

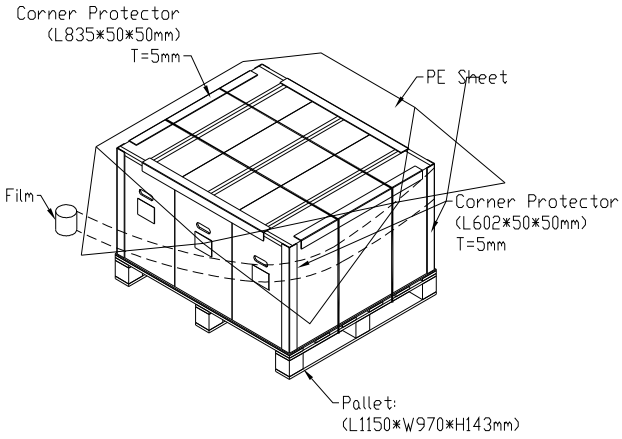
Packaging method is shown in following figures.



Sea / Land Transportation
(40ft HQ / 40ft Container)




Air Transportation



## 11. MECHANICAL CHARACTERISTIC