

Kaohsiung Opto-Electronics Inc.

FOR MESSRS:

DATE : May 30th ,2012

CUSTOMER'S ACCEPTANCE SPECIFICATIONS

TX43D50VM0BAA

Contents

No.	ITEM	SHEET No.	PAGE
1	COVER	7B64PS 2701-TX43D50VM0BAA-1	1-1/1
2	RECORD OF REVISION	7B64PS 2702-TX43D50VM0BAA-1	2-1/1
3	GENERAL DATA	7B64PS 2703-TX43D50VM0BAA-1	3-1/2~2/2
4	ABSOLUTE MAXIMUM RATINGS	7B64PS 2704-TX43D50VM0BAA-1	4-1/1
5	ELECTRICAL CHARACTERISTICS	7B64PS 2705-TX43D50VM0BAA-1	5-1/2~2/2
6	OPTICAL CHARACTERISTICS	7B64PS 2706-TX43D50VM0BAA-1	6-1/2~2/2
7	BLOCK DIAGRAM	7B64PS 2707-TX43D50VM0BAA-1	7-1/1
8	INTERFACE PIN ASSIGNMENT	7B64PS 2708-TX43D50VM0BAA-1	8-1/5~5/5
9	TIMING CHART	7B64PS 2709-TX43D50VM0BAA-1	9-1/4~4/4
10	OUTLINE DIMENSIONS	7B64PS 2710-TX43D50VM0BAA-1	10-1/2~2/2
11	APPEARANCE STANDARD	7B64PS 2711-TX43D50VM0BAA-1	11-1/3~3/3
12	PRECAUTIONS	7B64PS 2712-TX43D50VM0BAA-1	12-1/1~2/2
13	DESIGNATION OF LOT MARK	7B64PS 2713-TX43D50VM0BAA-1	13-1/1

ACCEPTED BY:_____

PROPOSED BY: Elton Lin

2. RECO	2. RECORD OF REVISION						
DATE	SHEET No.		SUMMARY				
DATE	SHEET No.		SUMMARY				
KAOHSIUNG O	PTO-ELECTRONICS INC.	SHEET NO.	7B64PS 2702-TX43D50VM0BAA-1	PAGE	2-1/1		

3. GENERAL DATA

3.1 DISPLAY FEATURES

This module is a 17" WXGA amorphous silicon TFT. The pixel format is vertical stripe and sub pixels are arranged as R (red), G (green), B (blue) sequentially. This display is RoHS compliant, COF (chip on film) technology and LED backlight are applied on this display.

Part Name	TX43D50VM0BAA
Module Dimensions	400.0(W) mm x 258.0(H) mm x 20.0 (D) mm typ.
LCD Active Area	369.6(W) mm x 221.76(H) mm
Pixel Pitch	0.28875(W) mm x 0.28875 (H) mm
Resolution	1280 x 3(RGB)(W) x 768(H) dots
Color Pixel Arrangement	R, G, B Vertical stripe
LCD Type	Transmissive Color Mode; Normally Black Mode
Display Type	Active Matrix
Number of Colors	16.7M Colors
Backlight	Edge Light Type with White LED
Weight	1700 typ. (g)
Interface	1-channel LVDS (LVDS:Low Voltage Differential Signaling)
Power Supply Voltage	5V for LCD; 12V for Backlight
Viewing Direction	Super Wide Version (In-Plane Switching)

KAOHSIUNG OPTO-ELECTRONICS INC.	SHEET NO.	7B64PS 2703-TX48D50VM0BAA-1	PAGE	3-1/2
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3.2 APPLICATION AND OTHERS

- (1) This LCD module was designed and manufactured to be used in an air-conditioned room away from direct sunlight.
- (2) This LCD module cannot be applied to an instrument which requires extremely high reliability and safety from its functions and precision. These instruments include medical equipment which affects life- and/or wealth-support apparatus.
- (3) Any problems caused by a use with deviation from the conditions mentioned in this specification are not included in the warranty.
- (4) Maintenance

This LCD module and the aforementioned data may be changed without notice. When you demand maintenance parts, please inquire about the changes in advance.

(5) Repair

We will replace or repair all defective modules if the relevant defect is caused by KOE. However, we will not take any responsibilities for defective modules after the expiration of warranty period. Also, if you access the modules for repairs, we will not warrant them either even if it is within the warranty period.

- (6) Items in this specification may be changed for improvement without prior notice. Please consult our sales division before engineering an instrument with this LCD module.
- (7) When a question arises concerning the specification, please contact our sales division.

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	VDD	0	6	V	-
Input Voltage of Logic	VI	-0.3	3.4	V	Note 1
Operating Temperature	Тор	0	50	°C	Note 2
Storage Temperature	Tst	-20	60	°C	Note 2
Backlight Input Voltage	VLED	-	(18)	V	-

Note 1: It is applied to LVDS signal.

Note 2: Temperature and Humidity should be applied to the center glass surface of TFT module, not to the system installed with a module. The temperature at the center of rear surface should be less than 60°C on the condition of operating. Function of module is guaranteed in above operating temperature range, but optical characteristics is specified for only 25°C operating condition.

KAOHSIUNG OPTO-ELECTRONICS INC.	SHEET NO.	7B64PS 2704-TX43D50VM0BAA-1	PAGE	4-1/ ⁻
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5. ELECTRICAL CHARACTERISTICS

5.1 LCD CHARACTERISTICS

 $T_a = 25 \ ^{\circ}C, \ \text{VSS} = 0\text{V}$

Item	Symbol	Min.	Тур.	Max.	Unit	Remarks
Power Supply Voltage	VDD	4.5	5	5.5	V	-
Input Voltage of Logic	VI	-0.3	-	3.4	V	-
Power Supply Current	IDD	-	430	520	mA	Note 2
Vsync Frequency	f_v	50	60	65	Hz	Note 3
Hsync Frequency	$f_{\scriptscriptstyle H}$	44.8	47.1	52.3	KHz	Note 3
CLK Frequency	f_{CLK}	65	66	73	MHz	Note 3

Note 1: It is applied to except LVDS signal.

Note 2: Temperature and Humidity should be applied to the center glass surface of TFT module, not to the system installed with a module. The temperature at the center of rear surface should be less than 60°C on the condition of operating. Function of module is guaranteed in above operating temperature range, but optical characteristics is specified for only 25°C operating condition.

- Note 3: As this module contains fuse (1.0A), prepare current source that is enough for cutting current fuse (larger than 2.5A) or set a protection circuit when a trouble happens.
- Note 4: The picture on typcal current is white picture.
- Note 5: When at low frequency drive, flicker may appear on screen. Please verify the flicker level before system design.

KAOHSIUNG OPTO-ELECTRONICS INC.	SHEET NO.	7B64PS 2705-TX43D50VM0BAA-1	PAGE	5-1/2
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5.2 BACKLIGHT CHARACTERISTICS

5.2 BACKLIGHT CHARACTERISTICS $T_a =$								
Item		Sym	ıbol	Min.	Тур.	Max.	Unit	Remarks
Input Voltage		Vin		10.8	12.0	13.2	V	-
Input Current		lin		-	(1.36)	1.9	А	Note 1
ON/OFF	ON			2.5	-	5.0	V	B/L=ON
Control Voltage	OFF		JFF	0	-	0.8	V	B/L=OFF
Brightness Control	Voltage	Vbc		1.0	-	3.6	V	Note 2
PWM dimming sigr	nal	High		2.9	-	5.0	V	Note 3
Input Voltage		Low		0	-	0.9	V	-
PWM Frequency		PW	′Mf	140	150	160	Hz	_

Note 1: VIN=12.0V, VBC=3.3V or PWMf=150Hz and display pattern is a full White (Gray scale = 255 level).

Note 2: A protection fuse is built into this module. As this module contains fuse (1.0A), prepare current source that is enough for cutting current fuse (larger than 2.5A) or set a protection circuit when a trouble happens.

Note 3: The picture on typcal current is white picture.

V _{BC} (Typ.)	Brightness
1.0V	20%
1.3V	30%
1.5V	40%
1.8V	50%
2.0V	60%
2.3V	70%
2.5V	80%
2.8V	90%
Above 3.0V	100%

Note 4: Brightness Control (Reference value)

PWM (Typ.)	Brightness
5%	5%
10%	10%
20%	20%
30%	30%
40%	40%
50%	50%
60%	60%
70%	70%
80%	80%
90%	90%
100%	100%

SHEET NO.

6. OPTICAL CHARACTERISTICS

The following optical characteristics are measured when the LCD is set alone (apart from driving circuits and monitor cabinets) and under stable conditions. It takes about 30 minutes to reach stable conditions. The measuring point is the center of display area unless otherwise noted. The optical characteristics should be measured in a dark room or equivalent state.

Measuring equipment : KONICA MINOLTA: CS-2000 or equivalent. Ambient Temperature=25±3°C, VDD=5.0V, fV=60Hz, VIN=12.0V, and VBC=3.3V or PWM=100% (PWMf=150Hz)

Item		Symbol	Condition	Min.	Тур.	Max.	Unit	Remarks
Brightness of White		Bwh		420	500	-	cd/m ²	Note 1,2
Brightness Uniform	ity	Buni	$\theta = 0^{\circ}$	75	-	-	%	Note 3
Contrast Ratio		CR		700	1000	-	-	Note 4
	Rise	ton	ton	-	12	20		Niete E
Response Time	Fall	toff	toff	-	10	18	ms	Notes
	Ded	Х		0.621	0.651	0.681		
	Rea	Y	$\theta = 0^{\circ}$	0.298	0.328	0.358	- - - -	Note 6
	Green	Х		0.280	0.310	0.340		
Color		Y		0.588	0.618	0.648		
	Dhia	Х		0.118	0.148	0.178		
	Blue	Y		0.025	0.055	0.085		
	\A/b:4a	Х		0.283	0.313	0.343		
	vvnite	Y		0.299	0.329	0.359		
Contrast Ratio at 85° CF			$\theta = 85^{\circ}$					
		CR 85 $^{\circ}$	$\phi=0^\circ, 90^\circ,$	10	-	-	-	-
			180° , 270°					
NTSC Ratio			$\theta = 0^{\circ}$	-	72	-	%	-

Note 1: The brightness is measured from the panel center point, P5 in Fig. 6.2, for the typical value. Note 2: Brightness of white is measured by LCM is light up after 30 minutes .

KAOHSIUNG OPTO-ELECTRONICS INC.	SHEET NO.	7B64PS 2706-TX43D50VM0BAA-1	PAGE	6-1/2
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Note 3: The brightness uniformity is calculated by the equation as below:

Brightness uniformity = $\frac{\text{Min. Brightness}}{\text{Max. Brightness}} \times 100\%$

, which is based on the brightness values of the 9 points measured by CS-1000A as shown in Fig. 6.2.



Note 4: The Contrast Ratio is measured from the center point of the panel, P5, and defined as the following equation:

$$CR = \frac{Brightness of White}{Brightness of Black}$$

Note 5: The definition of response time is shown in Fig. 6.3. The rising time is the period from 10% brightness to 90% brightness when the data is from black to white. Oppositely, Falling time is the period from 90% brightness rising to 10% brightness.





Note 6: The color chromaticity is measured from the center point of the panel, P5, as shown in Fig. 6.2.

KAOHSIUNG OPTO-ELECTRONICS INC.	SHEET NO.	7B64PS 2706-TX43D50VM0BAA-1	PAGE	6-2/2
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7. BLOCK DIAGRAM

7.1 TFT Module



8. INTERFACE PIN ASSIGNMENT

8.1 TFT-LCD MODULE

CN1: JAE: FI-X30SSLA-HF or Equivalent (Matching connector: JAE: FI-X30HL or FI-X30C2L-NPB or Equivalent)

Pin No.	Symbol	Function	Note
1	VDD		
2	VDD		
3	VDD	Power Supply (+5.0V)	4
4	VDD		
5	VSS		
6	VSS		
7	VSS	GND (0V)	1)
8	VSS		
9	TEST1	Test Pin (OPEN)	3)
10	TEST2	Test Pin (OPEN)	3)
11	VSS	GND (0V)	1)
12	RX0-	Divel Date	0)
13	RX0+	Pixel Data	2)
14	VSS	GND (0V)	1)
15	RX1-	Divel Date	0)
16	RX1+	Pixel Data	2)
17	VSS	GND (0V)	1)
18	RX2-	Divel Date	0)
19	RX2+	Pixel Data	2)
20	VSS	GND (0V)	1)
21	CLK-	Divel Cleak	2)
22	CLK+	Pixel Clock	2)
23	VSS	GND (0V)	1)
24	RX3-		2)
25	RX3+		۷)
26	VSS	GND (0V)	1)
27	AMODE	LVDS Mode Select	5)
28	TEST3	Test Pin (OPEN)	3)
29	TEST4	Test Pin (OPEN)	3)
30	VSS	GND (0V)	1)

Notes 1) All Vss pins should be grounded.

2) RXn- and RXn+ (n=0,1,2,3), CLK- and CLK+ should be wired by twist-pairs

or side-by-side FPC patterns, respectively.

3) Please keep open.

4) All VDD pins should be connected to +50 V (typ.).

5) Please refer to page 8-4/5 "LVDS interface" for LVDS data mapping.

8.2 BACK-LIGHT UNIT

CN2 : TARNG YU Enterprise: TU2001WNR-12S (Matching connector : JST PHR-12 or TARNG YU Enterprise TU2001HNO-12)

Pin No.	Symbol	Description	Note
1	V _{IN}		
2	V _{IN}		1)
3	V _{IN}	Power Supply (typ. 12.0V)	1)
4	V _{IN}		
5	ON/OFF	High : Backlight ON, Low : Backlight OFF	4)
6	V _{SS}		2)
7	V _{SS}	GND (0V)	2)
8	V _{BC}	Brightness Control Signal	5),6)
9	PWM	PWM Dimming Signal	3),6)
10	NC	NC	-
11	V _{SS}		2)
12	V _{SS}		2)

Notes

1) All V_{IN} pins should be connected to +12.0V (Typ.).

2) All V_{SS} pins should be grounded. The metal bezel is internally connected to GND.

3) High level:2.5~5.0V, Low level:0~0.9

4) High level:2.5 ~ 5.0V DC, Low level:0 ~ 0.5V DC

5) Input Voltage : 1.0 ~ 3.6V DC

6) These signals can't input at the same time.

KAOHSIUNG OPTO-ELECTRONICS INC.	SHEET NO.	7B64PS 2708-TX43D50VM0BAA-1	PAGE	8-2/5
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8.3 BLOCK DIAGRAM OF INTERFACE



Receiver: Equivalent of THC63LVDF84B by THine

- R0~7 : R data
- G0~7 : G data
- B0~7 : B data
- DTMG : Display timing data

Notes 1) The system must have a LVDS transmitter to drive a module.

2) The impedance of LVDS cable shall be about 100 ohms per twist-pair line when it is used differentially.

KAOHSIUNG OPTO-ELECTRONICS INC.	SHEET NO.	7B64PS 2708-TX43D50VM0BAA-1	PAGE	8-3/5
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8.4 LVDS INTERFACE

LVDS INTERFACE

2 · junt Signal Intermete connector Reserver 171 Control AMODE R0 (L&B) 51 TNN0 27 Rx0UT0 R0 (L&B) R1 52 TNN1 Tx OUT0+ Rx IN0 + 30 RxOUT2 R2 R4 56 TNN4 Tx OUT0+ Rx IN0 + 30 RxOUT3 R3 R4 56 TNN4 Tx OUT0+ Rx IN0 + 30 RxOUT3 R4 G0 L&B TNN5 Tx OUT0+ Rx IN0 + 30 RxOUT4 R4 G0 L&B TNN13 Tx OUT1+ Rx IN1+ 43 RxOUT3 G1 G1 G TNN13 Tx OUT1+ Rx IN1+ 45 RxOUT3 G0 L&B G0 LSB 15 TNN13 Tx OUT1+ Rx IN1+ 47 RxOUT3 B0 LSB GND B3 22 TNN54 Tx OUT2+ Rx IN2+ 5 RxOUT3 B3 RxOUT4 B0 LSB GND 127	07.1		-		Incontras C			Dessions	TTT C
AMODE	27pin	Signal	T	ransmitter	Interface Co	nnector		Receiver	TFT Control
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	AMODE	Signar	Pin	Input	System Device	TFT Module	Pin	Output	Input
1.1. 1.2. TRNYI 1.2. TROUTO+ RAUTO+		R0 (LSB)	51	TxIN0			27	RxO11T0	R0 (LSR)
Ris 022 Ris IALLS INNS S5 TANNS S5 T		D1	50	THINK			- ão	D.OUTI	D1
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		RI	52	IXINI			29	RXUUTI	RI
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		R2	54	TxIN2	Tx OUT0+	Rx IN0+	30	RxOUT2	R2
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		R3	55	TxIN3			32	RxOUT3	R.3
A* 50 1ALVA TXING Tx OUTO Rx INO 53 RXUL14 R4 R5 R4 R5 G1 6 TXING G2 7 TXING TXING Tx OUTO Rx INO 35 RXUL14 R4 R5 R4 R5 RXUTT G0 (LBB) G1 (LB) G3 11 TXIN12 G4 TXIN12 TXIN13 Tx OUT1+ Rx IN1- R5 37 RXUT16 G1 (LB) G3 RXUT12 G3 G4 12 TXIN15 TXIN15 Tx OUT1- Rx IN1- R5 RXUT12 G3 RXUT14 G5 B0 LSB 15 TXIN15 TXIN15 Tx OUT1- Rx IN1- R5 RXUT18 B1 B1 19 TXIN16 TXIN10 Tx OUT2+ Rx IN2- R5 RXUT18 B1 B2 4 TXIN26 R50 TXIN26 RXUT2 RXUT21 B3 R50 TXIN26 TX TX OUT2+ Rx IN2- S RAOUT2 B3 R50 TXIN26 TX TX OUT2+ Rx IN2- S RAOUT2 TX R6		D 4	EC	T-TAL			22	D-OLITA	D 4
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		R4	90	TXIN4			- 33	RXOUT4	R4
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		R5	- 3	TxIN6	Tx OUT0-	Rx IN0 ⁻	35	RxOUT6	R5
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		G0 (LSB)	4	T _v IN7			37	RvOUT7	G0 (LSB)
OI 0 INING G3 TAING TINN12 38 RXOUT3 RAUT13 OI G2 G3 11 TAIN12 TX OUT1+ RX IN1+ 39 RXOUT3 G4 G4 12 TAIN13 TX OUT1+ RX IN1+ 43 RXOUT3 G4 G5 14 TXIN15 TX OUT1+ RX IN1+ 45 RXOUT3 G4 B1 19 TXIN15 TX OUT1+ RX IN1+ 47 RXOUT3 B0 LSB B1 19 TXIN20 TX OUT2+ RX IN2+ 53 RXOUT3 B1 B2 B5 24 TXIN25 TX OUT2+ RX IN2+ 55 RXOUT3 Not use B7 R6 50 TXIN25 TX OUT3+ RX IN3+ 41 RXOUT3 B7 MA RXOUT3 R7 MA RXOUT3 R7 MA RXOUT3 B7 MA RXOUT3 B7 MA RXOUT3 TXOUT3+ RX IN3+ 41 RXOUT1 R7 MA RXOUT3 MA RXOUT3 MA RXOUT3			-	T 1210				D OUTO	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		G1	6	TXIN8			38	RXO UT8	G1
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		G2	7	TxIN9			39	RxOUT9	G2
Constraint Constraint <thconstraint< th=""> Constraint Constrai</thconstraint<>		G3	11	TwIN119	$T_{T} OIIT1 +$	P ₂ IN1⊥	43	PrOLIT19	G-3
64 12 181.13 43 RX0UT14 65 B1 19 TXN15 Tx OUT1- Rx IN1- 47 Rx0UT14 65 B1 19 TXN19 53 Rx0UT14 65 B1 B2 20 TXN19 53 Rx0UT12 B1 B2 B4 23 TXN21 Tx OUT2+ Rx IN2+ 54 Rx0UT20 B3 B5 24 TXN24 7 Rx0UT23 D4 8 Rx0UT26 D1 B5 7XN24 7 Rx0UT26 D1 8 Rx0UT26 D1 6 R50 TXN27 7 Rx0UT26 D1 6 Rx0UT16 6 Rx0UT16 6 6 10 Rx0UT3 7 Rx0UT16 6 10 6 7 Rx0UT26 D1 6 7 Rx0UT16 6 7 Rx0UT16 7 7 7 7 7 7 7 7 7 <th></th> <td>0.0</td> <td>11</td> <td>TAIN12</td> <td>1x 0011</td> <td>IXX IIVI +</td> <td>- 40</td> <td>D OUT12</td> <td>0.5</td>		0.0	11	TAIN12	1x 0011	IXX IIVI +	- 40	D OUT12	0.5
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		G4	12	TXIN15	I		45	RXOUT15	G4
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		G5	14	TxIN14			46	RxOUT14	G5
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		BO (LSB)	15	TvIN15	TY OUT1.	Ry IN1-	47	R _v OUT15	BO (LSB)
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		BU (LOB)	10	TAINIO	120011	IX INI	11	RX00115	DU (LOD)
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	_	B1	19	TxIN18			51	RxOUT18	B1
(GND) B3 22 TXIN20 S4 RXOUT20 B3 B4 23 TXIN21 Tx OUT2+ Rx IN2+ 54 RxOUT20 B4 B5 1 TXIN22 Tx OUT2+ Rx IN2+ 55 RxOUT21 B4 B5 1 TXIN24 Tx OUT2+ Rx IN2+ 56 RxOUT24 Not use B5 12 TXIN25 Tx OUT2- Rx IN2+ 5 RxOUT24 Not use B6 TXIN26 Tx OUT3+ Tx OUT3+ Rx IN3+ 41 RxOUT16 66 G6 S TXIN10 Tx OUT3+ Rx IN3+ 41 RxOUT16 67 (MSB) B6 16 TXIN16 Tx OUT3+ Rx IN3+ 41 RxOUT17 B7 0.00 16 67 (MSB) 10 TxIN23 Not use B6 16 TXIN11 Tx OUT3+ Rx IN3+ 41 RxOUT23 Not use 27pin Rsigan Trin11 TxOUT3+	=L	B2	20	TxIN19			53	RxOUT19	B2
	(CNID)	D2	00	T-1100			54	P-OUT00	D 2
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	(GIND)		44	TXIN20			04	KX00120	D0
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		B4	23	TxIN21	Tx OUT2+	Rx IN2+	55	RxOUT21	B4
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		B5	24	TxIN22			1	RxOUT22	B5
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	1	DEVID 1)	07	TyINI04			â	RyOUT204	Net ure
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	1	LOAD D	21	1 X11NZ4	_		0	RX00124	INOU USE
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		RSVD 1)	28	TxIN25	Tx OUT2-	Rx IN2 ⁻	5	RxOUT25	Not use
2000 200 <th>1</th> <td>DTMG</td> <td>30</td> <td>TxIN26</td> <td></td> <td></td> <td>6</td> <td>RxOUT26</td> <td>DTMG</td>	1	DTMG	30	TxIN26			6	RxOUT26	DTMG
Ro 300 1 KIN27 7 RX0U12/ 41 Rx0U15 RX0U15 R7 G6 R7 G6 R7 G7 G7 G7 MSB) R7 G7 G7 G7 MSB) R7 G7 G7 G7 MSB) R7 G7 G7 G7 MSB) R7 G7 G7 MSB) R7 G7 G7 MSB) R7 G7 G7 G7 MSB) R7 G7 G7 G7 MSB) R7 G7 G7 G7 MSB) R7 G7 G7 MSB) R7 G7 G7 MSB) R7 G7 G7 MSB) R7 G7 G7 MSB) R7 G7 G7 MSB) R7 G7 G7 MSB) R7 G7 G7 MSB) R7 G7 G7 MSB) R7 G7 G7 MSB) R7 G7 MSB) R7 MSD MD1	1	DIMO	50	T-12107			- <u>2</u>	D-OUT20	Dinic
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	1	Rb	90 0G	1 XIN27			1	KXOUT27	Rb
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	1	R7 (MSB)	2	TxIN5			34	RxOUT5	R7 (MSB)
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	1	G6	8	TyIN10	Tx OUT3+	Rx IN3+	41	RxOUT10	G6
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	1	an (aron)	10	Tuttit	14 00 10	In INO .	10	Dection	OT (MOT)
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		G7 (MSB)	10	TXINII			42	RXOUTII	G7 (MSB)
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		B6	16	TxIN16			49	RxOUT16	B6
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		B7 (MSB)	18	TwIN17	TY OTT3-	Ry INS-	50	R _v OUT17	B7 (MSB)
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		DOUD 1)	00	TAIN17	12 0 0 15	IX IND		D OUTO2	D7 (MIDD)
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		RSVD 1)	- 25	TXIN25			2	RXOUT23	Not use
Z7pin AMODE Signal Transmitter Input Interface Connector Receiver TFT Control Input R2 51 TxIN0 27 RxOUT0 R2 R3 52 TxIN1 27 RxOUT0 R2 R4 54 TxIN2 Tx OUT0+ Rx IN0+ 30 RxOUT1 R3 R6 55 TxIN3 Tx OUT0+ Rx IN0+ 30 RxOUT2 R4 R5 55 TxIN4 32 RxOUT3 R5 R6 56 TxIN4 33 RxOUT4 R6 G2 4 TxIN7 37 RxOUT5 G3 G4 7 TxIN9 39 RxOUT6 R7 (MSB) G4 7 TxIN12 Tx OUT1+ Rx IN1+ 43 RxOUT13 G6 G5 11 TxIN12 Tx OUT1+ Rx IN1+ 45 RxOUT13 G6 G7 (MSB) 14 TxIN14 S RxOUT13 G6 R3		DCLK	31	TxCLK IN	TxCLK OUT+	RxCLK IN+	26	RxCLK OUT	DCLK
27pin AMODE Signal Transmitter Interface Connector Receiver TFT Control Input R2 51 Tx1N0 27 RxOUT0 R2 R3 52 Tx1N1 29 RxOUT0 R2 R4 54 Tx1N2 Tx OUT0+ Rx IN0+ 30 RxOUT1 R3 R4 54 Tx1N2 Tx OUT0+ Rx IN0+ 30 RxOUT2 R4 R5 55 Tx1N4 Tx OUT0+ Rx IN0+ 30 RxOUT3 R5 R6 56 Tx1N4 Tx OUT0- Rx IN0+ 33 RxOUT6 R7 (M5B) G2 4 Tx1N9 Tx OUT0- Rx IN0+ 35 RxOUT7 G6 G4 7 Tx1N9 38 RxOUT12 G5 G7 (M5B) G6 G1 Tx1N15 Tx OUT1+ Rx IN1+ 43 RxOUT13 G6 G7 (M5B) 14 TxIN15 Tx OUT1+ Rx IN1+ 45 RxOUT13 G6 <t< td=""><th></th><td></td><td></td><td></td><td>TXCLK OUT:</td><td>RXCLK IN-</td><td></td><td></td><td></td></t<>					TXCLK OUT:	RXCLK IN-			
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	L				THOLM OUT	RACEN IN			
$\begin{array}{c c c c c c c c c c c c c c c c c c c $									
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	27pin	Signal	T	ransmitter	Interface C	onnector		Receiver	TFT Control
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	-					-			
$ = H \\ (3.3V) = $	AMODE	oignai	Din	Pin Input		TET Module	Din	Output	Imput
$ = H \\ (3.3V) = H \\ (3.3V) = H \\ (3.5V) = $	AMODE	Signal	Pin	Input	System Device	TFT Module	Pin	Output	Input
$ = H \\ (3.3V) = H \\ (3.3V) = H \\ (3.3V) = H \\ (3.1V) = $	AMODE	R2	Pin 51	Input TxIN0	System Device	TFT Module	Pin 27	Output RxOUT0	Imput R2
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	AMODE	R2 R3	Pin 51 52	Imput TxIN0 TxIN1	System Device	TFT Module	Pin 27 29	Output RxOUT0 RxOUT1	Imput R2 R3
= H = H = B4 = 20 - TxIN16 - Tx OUT1 - Tx OUT1 - Rx IN1 - 33 - RxOUT1 - R7 (MSB) - 33 - TxIN6 - Tx OUT1 + Rx IN1 + 43 - RxOUT1 - G2 - 33 - 7 - RxOUT7 - G2 - 33 - 7 - RxOUT1 - G2 - 33 - 7 - RxOUT7 - G2 - 33 - 7 - RxOUT7 - G2 - 33 - 8 - 7 - RxOUT1 - G2 - 33 - 8 - 7 - RxOUT1 - G2 - 33 - 8 - 7 - RxOUT1 - G2 - 33 - 8 - 7 - RxOUT1 - G2 - 33 - 8 - 7 - RxOUT1 - G2 - 33 - 8 - 7 - RxOUT1 - G3 - 7 - RxOUT1 - G3 - 7 - RxOUT1 - G3 - 7 - RxOUT2 - S - 7 - RxOUT2 - S - RxOUT2 - S - 8 - 7 - RxOUT2 - Rx IN2 - 5 - RxOUT2 - Rx IN2 - 5 - RxOUT2 - Rx IN2 - 5 - RxOUT2 - Rx IN2 - 7 - RxOUT2 - R1 - 2 - 7 - RxOUT2 - Rx IN3 - 34 - RxOUT1 - G1 - 10 - TxIN1 - 7 - 7 - RxOUT2 - R1 - 7 - RxOUT2 - R1 - 10 - TxIN1 - 7 - 7 - RxOUT2 - R1 - 7 - RxOUT2 - R1 - 10 - TxIN1 - 7 - 7 - RxOUT2 - R1 - 10 - TxIN1 - 7 - 7 - RxOUT2 - R1 - 10 - TxIN1 - 7 - 7 - RxOUT2 - R1 - 10 - TxIN1 - 7 - 7 - RxOUT2 - R1 - 10 - TxIN1 - 7 - 7 - RxOUT2 - R1 - 10 - 7 - 10 - 10 - 10 - 10 - 10 - 10	AMODE	R2 R3 R4	Pin 51 52 54	Input TxIN0 TxIN1 TxIN2	System Device	TFT Module	Pin 27 29 30	Output RxOUT0 RxOUT1 RxOUT2	Input R2 R3 R4
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	AMODE	R2 R3 R4	Pin 51 52 54	Imput TxIN0 TxIN1 TxIN2	System Device Tx OUT0+	TFT Module Rx IN0+	Pin 27 29 30	Output RxOUT0 RxOUT1 RxOUT2 RxOUT2	Imput R2 R3 R4
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	AMODE	R2 R3 R4 R5	Pin 51 52 54 55	Imput TxIN0 TxIN1 TxIN2 TxIN3	System Device Tx OUT0+	Rx IN0+	Pin 27 29 30 32	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3	Imput R2 R3 R4 R5
= H = H = B4 = 20 = TxIN20 = TxIN10	AMODE	R2 R3 R4 R5 R6	Pin 51 52 54 55 56	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4	System Device Tx OUT0+	Rx IN0+	Pin 27 29 30 32 33	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4	Imput R2 R3 R4 R5 R6
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	AMODE	R2 R3 R4 R5 R6 P7 (MSP)	Pin 51 52 54 55 56 3	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6	System Device Tx OUT0+	Rx IN0+	Pin 27 29 30 32 33 35	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 PxOUT6	Imput R2 R3 R4 R5 R6 P7 ()(SP)
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	AMODE	R2 R3 R4 R5 R6 R7 (MSB)	Pin 51 52 54 55 56 3	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6	System Device Tx OUT0+ Tx OUT0-	Rx IN0+ Rx IN0-	Pin 27 29 30 32 33 35	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT6 RxOUT6	Imput R2 R3 R4 R5 R6 R7 (MSB)
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	AMODE	R2 R3 R4 R5 R6 R7 (MSB) G2	Pin 51 52 54 55 56 3 4	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7	System Device Tx OUT0+ Tx OUT0-	Rx IN0+ Rx IN0-	Pin 27 29 30 32 33 35 37	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT6 RxOUT7	Imput R2 R3 R4 R5 R6 R7 (MSB) G2
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	AMODE	R2 R3 R4 R5 R6 R7 (MSB) G2 G3	Pin 51 52 54 55 56 3 4 6	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8	System Device Tx OUT0+ Tx OUT0-	TFT Module Rx IN0+ Rx IN0-	Pin 27 29 30 32 33 35 35 37 38	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT6 RxOUT7 RxOUT8	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	AMODE	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4	Pin 51 52 54 55 56 3 4 6 7	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9	System Device Tx OUT0+ Tx OUT0-	TFT Module Rx IN0+ Rx IN0-	Pin 27 29 30 32 33 35 37 38 30	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	AMODE	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4	Pin 51 52 54 55 56 3 4 6 7	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN6 TxIN7 TxIN8 TxIN9	System Device Tx OUT0+ Tx OUT0-	Rx IN0+ Rx IN0-	Pin 27 29 30 32 33 35 37 38 39	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	AMODE	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5	Pin 51 52 54 55 56 3 4 6 7 11	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN9 TxIN12	System Device Tx OUT0+ Tx OUT0- Tx OUT1+	TFT Module Rx IN0+ Rx IN0- Rx IN1+	Pin 27 29 30 32 33 35 37 38 39 43	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT92	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5
B2 15 TxIN15 Tx OUT1 Rx IN1 47 RxOUT15 B2 B3 19 TxIN18 Tx OUT1 Rx IN1 47 RxOUT15 B2 (3.3V) B5 22 TxIN19 53 RxOUT19 B4 (3.3V) B6 23 TxIN21 Tx OUT2+ Rx IN2+ 55 RxOUT20 B5 B7 (MSB) 24 TxIN21 Tx OUT2+ Rx IN2+ 55 RxOUT21 B6 B7 (MSB) 24 TxIN22 1 RxOUT2+ Rx IN2+ 55 RxOUT21 B6 B7 (MSB) 24 TxIN22 3 RxOUT20 B5 B3 RSVD 1) 27 TxIN24 3 RxOUT25 Not use B0 (LSB) 50 TxIN25 Tx OUT2+ Rx IN2+ 5 RxOUT26 DTMG R0 (LSB) 50 TxIN26 7 RxOUT27 R0 (LSB) G0 (LSB) G1 10 TxIN16 49 R	AMODE	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6	Pin 51 52 54 55 56 3 4 6 7 11 12	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN9 TxIN12 TxIN13	System Device Tx OUT0+ Tx OUT0- Tx OUT1+	TFT Module Rx IN0+ Rx IN0- Rx IN1+	Pin 27 29 30 32 33 35 37 38 39 43 45	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT12 RxOUT13	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	AMODE	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G6 (C7 (MSB)	Pin 51 52 54 55 56 3 4 6 7 11 12 14	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN9 TxIN12 TxIN13 TxIN14	System Device Tx OUT0+ Tx OUT0• Tx OUT1+	TFT Module Rx IN0+ Rx IN0- Rx IN1+	Pin 27 29 30 32 33 35 37 38 39 43 45 46	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT12 RxOUT13 RxOUT14	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB)
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	AMODE	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB)	Pin 51 52 54 55 56 3 4 6 7 11 12 14	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN9 TxIN12 TxIN13 TxIN14 TxIN15	System Device Tx OUT0+ Tx OUT0- Tx OUT1+	TFT Module Rx IN0+ Rx IN0- Rx IN1+	Pin 27 29 30 32 33 35 37 38 39 43 45 46	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT6 RxOUT7 RxOUT7 RxOUT9 RxOUT9 RxOUT12 RxOUT13 RxOUT14 RxOUT14	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB)
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	AMODE	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN9 TxIN9 TxIN12 TxIN13 TxIN14 TxIN15	System Device Tx OUT0+ Tx OUT0- Tx OUT1+ Tx OUT1-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+	Pin 27 29 30 32 33 35 37 38 39 43 45 46 47	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT9 RxOUT12 RxOUT13 RxOUT14 RxOUT15	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	AMODE	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN9 TxIN9 TxIN12 TxIN12 TxIN13 TxIN14 TxIN15 TxIN18	System Device Tx OUT0+ Tx OUT0- Tx OUT1+ Tx OUT1-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+	Pin 27 29 30 32 33 35 37 38 39 43 45 46 47 51	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT13 RxOUT14 RxOUT15 RxOUT18	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	AMODE	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 R4	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN7 TxIN8 TxIN9 TxIN12 TxIN13 TxIN14 TxIN15 TxIN18 TxIN19	System Device Tx OUT0+ Tx OUT0- Tx OUT1+ Tx OUT1-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+	Pin 27 29 30 32 35 35 37 38 39 43 45 46 47 51 53	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT12 RxOUT12 RxOUT13 RxOUT15 RxOUT18 RxOUT18 RxOUT19	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4
B6 23 TxIN21 Tx OUT2+ Rx IN2+ 55 RxOUT21 B6 B7 (MSB) 24 TxIN22 1 RxOUT22 B7 (MSB) 3 RxOUT22 B7 (MSB) RSVD 1) 27 TxIN24 3 RxOUT24 Not use RSVD 1) 28 TxIN25 Tx OUT2* Rx IN2* 5 RxOUT25 Not use DTMG 30 TxIN26 6 RxOUT26 DTMG Not use R0 (LSB) 50 TxIN27 7 RxOUT27 R0 (LSB) R1 2 TxIN10 G0 (LSB) 8 TxIN10 Tx OUT3* Rx IN3* 41 RxOUT10 G0 (LSB) G1 10 TxIN16 49 RxOUT10 G0 (LSB) B0 (LSB) 16 TxIN17 Tx OUT3* Rx IN3* 40 RxOUT16 B0 (LSB) B1 18 TxIN17 Tx OUT3* Rx IN3* 2 RxOUT17 B1 RSVD 1) 25 TxIN23 2	AMODE =H	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 P5	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN13 TxIN14 TxIN15 TxIN15 TxIN19 TxIN19 TxIN19 TxIN19 TxIN19	System Device Tx OUT0+ Tx OUT0- Tx OUT1+ Tx OUT1-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+	Pin 27 29 30 32 33 35 37 38 39 43 45 46 47 51 51	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT6 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT12 RxOUT13 RxOUT14 RxOUT15 RxOUT18 RxOUT18 RxOUT19 ProVUT02	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 D5
B7 (MSB) 24 TxIN22 1 RxOUT22 B7 (MSB) RSVD 1) 27 TxIN24 3 RxOUT24 Not use RSVD 1) 28 TxIN25 Tx OUT2* Rx IN2* 5 RxOUT25 Not use DTMG 30 TxIN26 6 RxOUT26 DTMG 0 TxIN27 R1 2 TxIN5 7 RxOUT27 R0 (LSB) 60 (LSB) 8 TxIN10 Tx OUT3* Rx IN3* 41 RxOUT10 G0 (LSB) G1 10 TxIN11 42 RxOUT10 G0 (LSB) G1 10 TxIN16 B1 18 TxIN17 Tx OUT3* Rx IN3* 41 RxOUT16 B0 (LSB) B1 18 TxIN17 Tx OUT3* Rx IN3* 41 RxOUT16 B0 (LSB) B1 18 TxIN17 Tx OUT3* Rx IN3* 50 RxOUT17 B1 RSVD 1) 25 TxIN23 2 RxOUT23 Not use	=H (3.33)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN9 TxIN12 TxIN13 TxIN14 TxIN15 TxIN18 TxIN18 TxIN19 TxIN20	System Device Tx OUT0+ Tx OUT0- Tx OUT1+ Tx OUT1-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+	Pin 27 29 30 32 33 35 37 38 39 43 45 46 47 51 53 54	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT13 RxOUT14 RxOUT15 RxOUT18 RxOUT19 RxOUT20	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5
RSVD 1) 27 TxIN24 3 RxOUT24 Not use RSVD 1) 28 TxIN25 Tx OUT2 Rx IN2 3 RxOUT24 Not use DTMG 30 TxIN26 6 RxOUT26 DTMG R0 (LSB) 50 TxIN27 7 RxOUT27 R0 (LSB) R1 2 TxIN5 7 RxOUT27 R0 (LSB) G0 (LSB) 8 TxIN10 Tx OUT3+ Rx IN3+ 41 RxOUT10 G0 (LSB) G1 10 TxIN16 42 RxOUT10 G0 (LSB) G1 10 G1	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN9 TxIN12 TxIN13 TxIN14 TxIN15 TxIN18 TxIN18 TxIN19 TxIN20 TxIN21	System Device Tx OUT0+ Tx OUT0- Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT1-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1- Rx IN2+	Pin 27 29 30 32 33 35 37 38 39 43 45 46 47 51 53 54 55	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT13 RxOUT14 RxOUT15 RxOUT15 RxOUT18 RxOUT19 RxOUT20 RxOUT21	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6
RSVD I) 27 TXIN24 3 RXOUT24 Not use RSVD I) 28 TxIN25 Tx OUT2 Rx IN2 5 RxOUT25 Not use DTMG 30 TxIN26 7 Rx IN2 6 RxOUT26 DTMG R0 (LSB) 50 TxIN27 7 RxOUT27 R0 (LSB) R1 2 TxIN5 7 RxOUT27 R0 (LSB) G0 (LSB) 8 TxIN10 Tx OUT3+ Rx IN3+ 41 RxOUT10 G0 (LSB) G1 10 TxIN11 42 RxOUT10 G0 (LSB) G0 (LSB) 16 TxIN16 B1 18 TxIN17 Tx OUT3* Rx IN3* 50 RxOUT16 B0 (LSB) B1 18 TxIN17 Tx OUT3* Rx IN3* 2 RxOUT17 B1 RSVD 1) 25 TxIN23 2 RxOUT23 Not use DCLK 31 TxCLK IN TxCLK OUT* RxCLK IN* 26 RxCLK OUT	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 R7 (MSP)	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23 24	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN7 TxIN8 TxIN9 TxIN12 TxIN13 TxIN14 TxIN15 TxIN15 TxIN18 TxIN19 TxIN20 TxIN20 TxIN21	System Device Tx OUT0+ Tx OUT0- Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT1-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+ Rx IN1- Rx IN2+	Pin 27 29 30 32 35 37 38 39 43 45 46 47 51 53 54 55	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT3 RxOUT4 RxOUT6 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT12 RxOUT13 RxOUT14 RxOUT15 RxOUT15 RxOUT19 RxOUT20 RxOUT21 RxOUT21 RxOUT21 RxOUT21	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSP)
RSVD 1) 28 TxIN25 Tx OUT2* Rx IN2* 5 RxOUT25 Not use DTMG 30 TxIN26 6 RxOUT26 0TMG 0TMG 0TMG R0 (LSB) 50 TxIN27 7 RxOUT26 0TMG 0CLSB 0TMG 0CLSB 0TMG 0CLSB 0CLK	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB)	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23 24	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN13 TxIN14 TxIN15 TxIN18 TxIN18 TxIN19 TxIN20 TxIN20 TxIN21 TxIN22	System Device Tx OUT0+ Tx OUT0- Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT2+	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+ Rx IN1- Rx IN2+	Pin 27 29 30 32 33 35 37 38 39 43 45 46 47 51 53 54 55 1	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT13 RxOUT14 RxOUT15 RxOUT18 RxOUT19 RxOUT20 RxOUT21 RxOUT22	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB)
DTMG 30 TxIN26 6 RxOUT26 DTMG R0 (LSB) 50 TxIN27 7 RxOUT27 R0 (LSB) R1 2 TxIN5 34 RxOUT5 R1 G0 (LSB) 8 TxIN10 Tx OUT3+ Rx IN3+ 41 RxOUT10 G0 (LSB) G1 10 TxIN10 Tx OUT3+ Rx IN3+ 41 RxOUT10 G0 (LSB) G1 10 TxIN16 49 RxOUT16 B0 (LSB) B1 18 TxIN17 Tx OUT3' Rx IN3' 50 RxOUT17 B1 RSVD 1) 25 TxIN23 2 RxOUT23 Not use DCLK 31 TxCLK IN TxCLK OUT' RxCLK IN' 26 RxCLK OUT DCLK	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) RSVD 1)	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23 24 27	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN13 TxIN14 TxIN15 TxIN14 TxIN15 TxIN18 TxIN19 TxIN20 TxIN20 TxIN21 TxIN22 TxIN24	System Device Tx OUT0+ Tx OUT0- Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT2+	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+ Rx IN1- Rx IN2+	Pin 27 29 30 32 33 35 37 38 39 43 45 46 47 51 53 54 55 1 3	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT13 RxOUT14 RxOUT15 RxOUT15 RxOUT18 RxOUT19 RxOUT19 RxOUT20 RxOUT21 RxOUT22 RxOUT24	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) Not use
Bind S0 TXIN20 C RXOU120 DIMG R0 (LSB) 50 TxIN27 7 RxOUT27 R0 (LSB) R1 2 TxIN5 34 RxOUT5 R1 G0 (LSB) 8 TxIN10 Tx OUT3+ Rx IN3+ 41 RxOUT10 G0 (LSB) G1 10 TxIN11 42 RxOUT10 G0 (LSB) G0 (LSB) B1 18 TxIN17 Tx OUT3+ Rx IN3+ 41 RxOUT16 B0 (LSB) B1 18 TxIN17 Tx OUT3+ Rx IN3- 50 RxOUT17 B1 RSVD 1) 25 TxIN23 2 RxOUT23 Not use DCLK 31 TxCLK IN TxCLK OUT+ RxCLK IN+ 26 RxCLK OUT DCLK	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) RSVD 1) RSVD 1)	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23 24 27 28	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN12 TxIN13 TxIN14 TxIN15 TxIN14 TxIN15 TxIN18 TxIN19 TxIN20 TxIN20 TxIN21 TxIN22 TxIN24 TxIN25	System Device Tx OUT0+ Tx OUT0- Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT1- Tx OUT2-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1- Rx IN2+ Rx IN2-	Pin 27 29 30 32 35 37 38 39 43 45 46 47 51 53 54 55 1 3 5	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT13 RxOUT14 RxOUT15 RxOUT14 RxOUT15 RxOUT15 RxOUT18 RxOUT19 RxOUT20 RxOUT21 RxOUT22 RxOUT24 RxOUT25	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) Not use Not use
R0 (LSB) 50 Tx1N27 7 RxOUT27 R0 (LSB) R1 2 Tx1N5 34 RxOUT5 R1 G0 (LSB) 8 Tx1N10 Tx OUT3+ Rx IN3+ 41 RxOUT10 G0 (LSB) G1 10 Tx1N11 42 RxOUT10 G0 (LSB) G1 G1 B0 (LSB) 16 Tx1N16 49 RxOUT16 B0 (LSB) B0 (LSB) B1 18 Tx1N17 Tx OUT3+ Rx IN3+ 50 RxOUT16 B0 (LSB) B1 18 Tx1N17 Tx OUT3+ Rx IN3- 50 RxOUT17 B1 RSVD 1) 25 Tx1N23 2 RxOUT23 Not use DCLK 31 TxCLK IN TxCLK OUT+ RxCLK IN+ 26 RxCLK OUT DCLK	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) RSVD 1) RSVD 1) DTMC	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23 24 27 28 30	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN12 TxIN13 TxIN14 TxIN15 TxIN18 TxIN18 TxIN19 TxIN20 TxIN20 TxIN21 TxIN22 TxIN24 TxIN25 TxIN26	System Device Tx OUT0+ Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT1- Tx OUT2+ Tx OUT2-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+ Rx IN1- Rx IN2+ Rx IN2-	Pin 27 29 30 32 35 37 38 39 43 45 46 47 51 53 54 55 1 3 5 6	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT3 RxOUT4 RxOUT6 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT12 RxOUT13 RxOUT14 RxOUT15 RxOUT15 RxOUT15 RxOUT19 RxOUT20 RxOUT21 RxOUT22 RxOUT24 RxOUT25 RxOUT25 RxOUT25 RxOUT25 RxOUT26	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) Not use Not use DTMG
R1 2 TxIN5 34 RxOUT5 R1 G0 (LSB) 8 TxIN10 Tx OUT3+ Rx IN3+ 41 RxOUT10 G0 (LSB) G1 10 TxIN11 42 RxOUT11 G1 B0 (LSB) 16 TxIN16 49 RxOUT16 B0 (LSB) B1 18 TxIN17 Tx OUT3+ Rx IN3+ 50 RxOUT16 B0 (LSB) RSVD 1) 25 TxIN23 7 2 RxOUT23 Not use DCLK 31 TxCLK IN TxCLK OUT+ RxCLK IN+ 26 RxCLK OUT DCLK	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) RSVD 1) RSVD 1) DTMG	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23 24 27 28 30	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN12 TxIN13 TxIN14 TxIN15 TxIN15 TxIN18 TxIN19 TxIN19 TxIN20 TxIN20 TxIN21 TxIN22 TxIN22 TxIN24 TxIN25 TxIN26	System Device Tx OUT0+ Tx OUT0- Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT1- Tx OUT2+ Tx OUT2-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+ Rx IN1- Rx IN2+ Rx IN2-	Pin 27 29 30 32 33 35 37 38 39 43 45 46 47 51 53 54 55 1 3 5 6	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT3 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT13 RxOUT14 RxOUT15 RxOUT15 RxOUT15 RxOUT18 RxOUT19 RxOUT20 RxOUT21 RxOUT22 RxOUT24 RxOUT25 RxOUT26	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) Not use Not use DTMG R7 (MSB)
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) RSVD 1) RSVD 1) RSVD 1) DTMG R0 (LSB)	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23 24 27 28 30 50	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN12 TxIN13 TxIN14 TxIN15 TxIN14 TxIN15 TxIN18 TxIN19 TxIN10 TxIN20 TxIN20 TxIN21 TxIN22 TxIN22 TxIN25 TxIN26 TxIN27	System Device Tx OUT0+ Tx OUT0- Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT2+ Tx OUT2-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1- Rx IN1- Rx IN2+ Rx IN2-	Pin 27 29 30 32 33 35 37 38 39 43 45 46 47 51 53 54 55 1 3 5 6 7	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT3 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT12 RxOUT14 RxOUT15 RxOUT14 RxOUT15 RxOUT15 RxOUT15 RxOUT18 RxOUT19 RxOUT20 RxOUT21 RxOUT21 RxOUT22 RxOUT22 RxOUT24 RxOUT25 RxOUT26 RxOUT27	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) Not use Not use DTMG R0 (LSB)
G1 10 TxIN10 Tx OUT3+ Rx IN3+ 41 RxOUT10 G0 (LSB) G1 10 TxIN11 42 RxOUT11 G1 B0 (LSB) 16 TxIN16 49 RxOUT16 B0 (LSB) B1 18 TxIN17 Tx OUT3+ Rx IN3+ 50 RxOUT17 B1 RSVD 1) 25 TxIN23 2 RxOUT23 Not use DCLK 31 TxCLK IN TxCLK OUT+ RxCLK IN+ 26 RxCLK OUT DCLK	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) RSVD 1) RSVD 1) DTMG R0 (LSB) R1	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23 24 27 28 30 50 2	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN12 TxIN13 TxIN14 TxIN15 TxIN14 TxIN15 TxIN18 TxIN19 TxIN20 TxIN20 TxIN21 TxIN22 TxIN22 TxIN22 TxIN24 TxIN25 TxIN26 TxIN27 TxIN5	System Device Tx OUT0+ Tx OUT0- Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT1- Tx OUT2+ Tx OUT2-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1- Rx IN1- Rx IN2+ Rx IN2-	Pin 27 29 30 32 35 37 38 39 43 45 46 47 51 53 54 55 1 3 5 6 7 34	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT13 RxOUT14 RxOUT15 RxOUT15 RxOUT19 RxOUT20 RxOUT21 RxOUT22 RxOUT22 RxOUT24 RxOUT25 RxOUT26 RxOUT27 RxOUT5	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) Not use Not use DTMG R0 (LSB) R1
G1 10 TxIN11 42 RxOUT11 G1 B0 (LSB) 16 TxIN16 49 RxOUT16 B0 (LSB) B1 18 TxIN17 Tx OUT3* Rx IN3* 50 RxOUT17 B1 RSVD 1) 25 TxIN23 7xCLK OUT+ RxCLK IN+ 26 RxCLK OUT Not use DCLK 31 TxCLK IN TxCLK OUT+ RxCLK IN+ 26 RxCLK OUT DCLK	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) RSVD 1) RSVD 1) DTMG R0 (LSB) R1 C0 (LSP)	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23 24 27 28 30 50 2 8 20 20 20 20 20 20 20 20 20 20	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN13 TxIN14 TxIN15 TxIN18 TxIN19 TxIN15 TxIN18 TxIN19 TxIN20 TxIN21 TxIN22 TxIN22 TxIN24 TxIN25 TxIN26 TxIN27 TxIN5 TxIN10	System Device Tx OUT0+ Tx OUT0- Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT2+ Tx OUT2-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+ Rx IN1- Rx IN2+ Rx IN2- Rx IN2-	Pin 27 29 30 32 33 35 37 38 39 43 45 46 47 51 53 54 55 1 3 5 6 7 34 41	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT3 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT13 RxOUT14 RxOUT15 RxOUT15 RxOUT10 RxOUT22 RxOUT24 RxOUT25 RxOUT27 RxOUT5 RxOUT5 RxOUT5 RxOUT10	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) Not use DTMG R0 (LSB) R1 G0 (LSP)
B0 (LSB) 16 TxIN16 49 RxOUT16 B0 (LSB) B1 18 TxIN17 Tx OUT3· Rx IN3· 50 RxOUT17 B1 RSVD 1) 25 TxIN23 7 7 Not use Not use DCLK 31 TxCLK IN TxCLK OUT+ RxCLK IN+ 26 RxCLK OUT DCLK 1 <th>=H (3.3V)</th> <td>R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) RSVD 1) RSVD 1) RSVD 1) RSVD 1) DTMG R0 (LSB) R1 G0 (LSB)</td> <td>Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23 24 27 28 30 50 2 8 </td> <td>Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN12 TxIN12 TxIN13 TxIN14 TxIN15 TxIN18 TxIN15 TxIN18 TxIN19 TxIN20 TxIN20 TxIN21 TxIN22 TxIN22 TxIN25 TxIN26 TxIN27 TxIN5 TxIN10</td> <td>System Device Tx OUT0+ Tx OUT0- Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT1- Tx OUT2+ Tx OUT2- Tx OUT3+</td> <td>TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+ Rx IN1- Rx IN2+ Rx IN2- Rx IN2-</td> <td>Pin 27 29 30 32 33 35 37 38 39 43 45 46 47 51 53 54 55 1 3 5 6 7 34 41</td> <td>Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT14 RxOUT15 RxOUT15 RxOUT20 RxOUT21 RxOUT22 RxOUT22 RxOUT22 RxOUT25 RxOUT27 RxOUT5 RxOUT10</td> <td>Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) Not use Not use DTMG R0 (LSB) R1 G0 (LSB)</td>	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) RSVD 1) RSVD 1) RSVD 1) RSVD 1) DTMG R0 (LSB) R1 G0 (LSB)	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23 24 27 28 30 50 2 8 	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN12 TxIN12 TxIN13 TxIN14 TxIN15 TxIN18 TxIN15 TxIN18 TxIN19 TxIN20 TxIN20 TxIN21 TxIN22 TxIN22 TxIN25 TxIN26 TxIN27 TxIN5 TxIN10	System Device Tx OUT0+ Tx OUT0- Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT1- Tx OUT2+ Tx OUT2- Tx OUT3+	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+ Rx IN1- Rx IN2+ Rx IN2- Rx IN2-	Pin 27 29 30 32 33 35 37 38 39 43 45 46 47 51 53 54 55 1 3 5 6 7 34 41	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT14 RxOUT15 RxOUT15 RxOUT20 RxOUT21 RxOUT22 RxOUT22 RxOUT22 RxOUT25 RxOUT27 RxOUT5 RxOUT10	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) Not use Not use DTMG R0 (LSB) R1 G0 (LSB)
B1 18 TxIN17 Tx OUT3· Rx IN3· 50 RxOUT17 B1 RSVD 1) 25 TxIN23 2 RxOUT23 Not use DCLK 31 TxCLK IN TxCLK OUT+ RxCLK IN+ 26 RxCLK OUT DCLK Image: Comparison of the text of the text of text	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) RSVD 1) RSVD 1) RSVD 1) DTMG R0 (LSB) R1 G0 (LSB) G1	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23 24 27 28 30 50 2 8 10	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN12 TxIN12 TxIN13 TxIN14 TxIN15 TxIN14 TxIN15 TxIN18 TxIN19 TxIN20 TxIN20 TxIN21 TxIN22 TxIN22 TxIN25 TxIN26 TxIN27 TxIN5 TxIN10 TxIN11	System Device Tx OUT0+ Tx OUT0- Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT1- Tx OUT2+ Tx OUT2- Tx OUT2-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+ Rx IN1- Rx IN2+ Rx IN2- Rx IN2- Rx IN3+	Pin 27 29 30 32 33 35 37 38 39 43 45 46 47 51 53 54 55 1 3 5 6 7 34 41 42	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT14 RxOUT15 RxOUT14 RxOUT15 RxOUT15 RxOUT20 RxOUT21 RxOUT22 RxOUT22 RxOUT22 RxOUT24 RxOUT25 RxOUT26 RxOUT27 RxOUT5 RxOUT10 RxOUT11	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) Not use Not use DTMG R0 (LSB) R1 G0 (LSB) G1
B1 B1 B1 B1 RSVD 1) 25 TxIN23 1x 0015* 1x 1N5* 50 Rx00117 B1 DCLK 31 TxCLK IN TxCLK OUT+ RxCLK IN+ 26 RxCLK OUT DCLK Image: Distribution of the state o	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) RSVD 1) RSVD 1) DTMG R0 (LSB) R1 G0 (LSB) G1 B0 (LSB)	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23 24 27 28 30 50 2 8 10 16	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN12 TxIN13 TxIN14 TxIN15 TxIN15 TxIN18 TxIN19 TxIN20 TxIN20 TxIN21 TxIN22 TxIN22 TxIN25 TxIN25 TxIN26 TxIN27 TxIN5 TxIN10 TxIN11 TxIN16	System Device Tx OUT0+ Tx OUT0- Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT1- Tx OUT2+ Tx OUT2- Tx OUT2-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+ Rx IN1- Rx IN2+ Rx IN2- Rx IN2- Rx IN3+	Pin 27 29 30 32 35 37 38 39 43 45 46 47 51 53 54 55 1 3 5 6 7 34 41 42 49	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT13 RxOUT14 RxOUT15 RxOUT15 RxOUT10 RxOUT27 RxOUT26 RxOUT27 RxOUT5 RxOUT10 RxOUT11 RxOUT16	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) Not use Not use DTMG R0 (LSB) R1 G0 (LSB) G1 B0 (LSB)
RSVD 1) 25 TxIN23 2 RxOUT23 Not use DCLK 31 TxCLK IN TxCLK OUT+ RxCLK IN+ 26 RxCLK OUT DCLK Image: Comparison of the second	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) RSVD 1) RSVD 1) RSVD 1) RSVD 1) DTMG R0 (LSB) R1 G0 (LSB) G1 B0 (LSB)	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23 24 27 28 30 2 8 10 10 10 10 10 10 10 10 10 10	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN12 TxIN13 TxIN14 TxIN15 TxIN14 TxIN15 TxIN18 TxIN19 TxIN20 TxIN20 TxIN21 TxIN22 TxIN22 TxIN22 TxIN25 TxIN25 TxIN26 TxIN27 TxIN5 TxIN10 TxIN10 TxIN11 TxIN16 TxIN17	System Device Tx OUT0+ Tx OUT0- Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT1- Tx OUT2+ Tx OUT2- Tx OUT2+	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+ Rx IN1- Rx IN2+ Rx IN2+ Rx IN2- Rx IN3+	Pin 27 29 30 32 33 35 37 38 39 43 45 46 47 51 53 54 55 1 3 5 6 7 34 41 42 9 9 9 9 9 9 9 9 9 9 9 9 9	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT12 RxOUT14 RxOUT15 RxOUT15 RxOUT16 RxOUT22 RxOUT26 RxOUT27 RxOUT27 RxOUT27 RxOUT10 RxOUT16 RxOUT16 RxOUT16 RxOUT16	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) Not use DTMG R0 (LSB) R1 G0 (LSB) G1 B0 (LSB) P1
DCLK 31 TxCLK IN TxCLK OUT+ RxCLK IN+ 26 RxCLK OUT DCLK TxCLK OUT RxCLK IN· 26 RxCLK OUT DCLK	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) RSVD 1) RSVD 1) RSVD 1) RSVD 1) RSVD 1) DTMG R0 (LSB) R1 G0 (LSB) G1 B0 (LSB) B1	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23 24 27 28 30 50 2 8 10 16 18 10 10 10 10 10 10 10 10 10 10	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN12 TxIN12 TxIN13 TxIN14 TxIN15 TxIN15 TxIN18 TxIN19 TxIN20 TxIN20 TxIN21 TxIN22 TxIN22 TxIN25 TxIN26 TxIN25 TxIN26 TxIN27 TxIN5 TxIN10 TxIN11 TxIN16 TxIN17	System Device Tx OUT0+ Tx OUT0- Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT1- Tx OUT2+ Tx OUT2- Tx OUT3+ Tx OUT3-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+ Rx IN1- Rx IN2+ Rx IN2+ Rx IN2- Rx IN3+ Rx IN3-	$\begin{array}{c} \text{Pin} \\ 27 \\ 29 \\ 30 \\ 32 \\ 33 \\ 35 \\ 37 \\ 38 \\ 39 \\ 43 \\ 45 \\ 46 \\ 47 \\ 51 \\ 53 \\ 54 \\ 55 \\ 1 \\ 3 \\ 5 \\ 6 \\ 7 \\ 34 \\ 41 \\ 42 \\ 49 \\ 50 \end{array}$	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT12 RxOUT14 RxOUT15 RxOUT15 RxOUT10 RxOUT20 RxOUT21 RxOUT22 RxOUT22 RxOUT22 RxOUT22 RxOUT25 RxOUT26 RxOUT27 RxOUT5 RxOUT10 RxOUT11 RxOUT11 RxOUT11 RxOUT16 RxOUT17	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) Not use DTMG R0 (LSB) R1 G0 (LSB) G1 B0 (LSB) B1
TxCLK OUT RxCLK IN TXCLK OUT BELK	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) RSVD 1) RSVD 1) RSVD 1) DTMG R0 (LSB) R1 G0 (LSB) G1 B0 (LSB) B1 RSVD 1)	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23 24 27 28 30 50 2 8 10 16 18 25 50 28 10 10 10 10 10 10 10 10 10 10	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN12 TxIN13 TxIN14 TxIN15 TxIN14 TxIN15 TxIN18 TxIN19 TxIN20 TxIN20 TxIN21 TxIN20 TxIN21 TxIN22 TxIN24 TxIN25 TxIN26 TxIN25 TxIN26 TxIN27 TxIN5 TxIN10 TxIN11 TxIN16 TxIN17 TxIN23	System Device Tx OUT0+ Tx OUT0- Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT1- Tx OUT2+ Tx OUT2- Tx OUT3+ Tx OUT3-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+ Rx IN1- Rx IN2+ Rx IN2+ Rx IN2- Rx IN3+ Rx IN3-	Pin 27 29 30 32 33 35 37 38 39 43 45 46 47 51 53 54 55 1 3 5 6 7 34 41 42 49 50 2 2 3 5 5 5 2 5 5 2 5 5 2 5 5 5 5 5 5 5 5 5 5 5 5 5	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT12 RxOUT14 RxOUT15 RxOUT14 RxOUT15 RxOUT15 RxOUT10 RxOUT21 RxOUT22 RxOUT22 RxOUT24 RxOUT25 RxOUT26 RxOUT27 RxOUT5 RxOUT27 RxOUT5 RxOUT10 RxOUT11 RxOUT11 RxOUT11 RxOUT17 RxOUT17 RxOUT17 RxOUT23	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) Not use DTMG R0 (LSB) R1 G0 (LSB) G1 B0 (LSB) B1 Not use
TxCLK OUT RxCLK IN	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) RSVD 1) RSVD 1) DTMG R0 (LSB) R1 G0 (LSB) B1 RSVD 1) DCL K	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23 24 27 28 30 50 2 8 10 16 18 25 31 25 31 32 32 32 32 32 32 32 32 32 32	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN12 TxIN13 TxIN14 TxIN15 TxIN14 TxIN15 TxIN18 TxIN19 TxIN15 TxIN18 TxIN19 TxIN20 TxIN21 TxIN22 TxIN22 TxIN25 TxIN26 TxIN25 TxIN26 TxIN27 TxIN5 TxIN10 TxIN11 TxIN10 TxIN11 TxIN16 TxIN17 TxIN23 TxOLK UN	System Device Tx OUT0+ Tx OUT0- Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT1- Tx OUT2+ Tx OUT2- Tx OUT3+ Tx OUT3- Tx OUT3-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+ Rx IN1- Rx IN2+ Rx IN2- Rx IN2- Rx IN3+ Rx IN3- Rx IN3-	Pin 27 29 30 32 33 35 37 38 39 43 45 46 47 51 53 54 55 1 3 5 6 7 34 41 42 49 50 2 2 3 2 3 3 3 5 5 5 5 5 5 5 5 5 5 5 5 5	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT13 RxOUT14 RxOUT15 RxOUT14 RxOUT15 RxOUT14 RxOUT15 RxOUT15 RxOUT20 RxOUT21 RxOUT22 RxOUT22 RxOUT24 RxOUT25 RxOUT26 RxOUT27 RxOUT5 RxOUT10 RxOUT11 RxOUT16 RxOUT17 RxOUT17 RxOUT23 RxOUT23	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) Not use DTMG R0 (LSB) R1 G0 (LSB) G1 B0 (LSB) B1 Not use
	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) RSVD 1) RSVD 1) DTMG R0 (LSB) R1 G0 (LSB) B1 B1 RSVD 1) DCLK	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 22 23 24 27 28 30 50 2 8 10 16 18 25 31 10 20 22 23 24 25 30 20 20 20 21 20 21 21 20 22 23 24 25 30 20 20 20 20 20 20 20 20 20 2	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN12 TxIN13 TxIN14 TxIN15 TxIN13 TxIN14 TxIN15 TxIN18 TxIN19 TxIN20 TxIN20 TxIN20 TxIN21 TxIN22 TxIN22 TxIN22 TxIN24 TxIN25 TxIN26 TxIN27 TxIN5 TxIN10 TxIN11 TxIN10 TxIN11 TxIN16 TxIN17 TxIN23 TxCLK IN	System Device Tx OUT0+ Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT1- Tx OUT2+ Tx OUT2- Tx OUT3+ Tx OUT3- TxCLK OUT+	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+ Rx IN1- Rx IN2+ Rx IN2+ Rx IN2- Rx IN3+ Rx IN3- Rx CLK IN+	Pin 27 29 30 32 33 35 37 38 39 43 45 46 47 51 53 54 55 1 3 5 6 7 34 41 42 49 50 2 26	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT14 RxOUT15 RxOUT14 RxOUT15 RxOUT16 RxOUT16 RxOUT20 RxOUT21 RxOUT22 RxOUT22 RxOUT22 RxOUT24 RxOUT25 RxOUT25 RxOUT26 RxOUT27 RxOUT27 RxOUT27 RxOUT5 RxOUT10 RxOUT11 RxOUT11 RxOUT117 RxOUT27 RxOUT27 RxOUT27 RxOUT27 RxOUT27 RxOUT27 RXOUT17 RXO	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) Not use DTMG R0 (LSB) R1 G0 (LSB) G1 B0 (LSB) B1 Not use DCLK
	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) RSVD 1) RSVD 1) RSVD 1) DTMG R0 (LSB) R1 G0 (LSB) B1 RSVD 1) DCLK	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 20 22 23 24 27 28 30 50 2 8 10 18 25 31	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN12 TxIN12 TxIN13 TxIN14 TxIN15 TxIN13 TxIN14 TxIN15 TxIN18 TxIN19 TxIN20 TxIN20 TxIN21 TxIN22 TxIN22 TxIN22 TxIN24 TxIN25 TxIN26 TxIN25 TxIN26 TxIN27 TxIN5 TxIN10 TxIN11 TxIN16 TxIN17 TxIN23 TxCLK IN	System Device Tx OUT0+ Tx OUT0- Tx OUT1+ Tx OUT1+ Tx OUT1- Tx OUT2+ Tx OUT2+ Tx OUT2- Tx OUT3+ Tx OUT3- TxCLK OUT+ TxCLK OUT+	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+ Rx IN1- Rx IN2+ Rx IN2+ Rx IN2- Rx IN3+ Rx IN3- Rx CLK IN+ Rx CLK IN+	$\begin{array}{c} \text{Pin} \\ 27 \\ 29 \\ 30 \\ 32 \\ 33 \\ 35 \\ 37 \\ 38 \\ 39 \\ 43 \\ 45 \\ 46 \\ 47 \\ 51 \\ 53 \\ 54 \\ 55 \\ 1 \\ 3 \\ 56 \\ 7 \\ 34 \\ 41 \\ 42 \\ 49 \\ 50 \\ 2 \\ 26 \\ \end{array}$	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT13 RxOUT14 RxOUT15 RxOUT14 RxOUT15 RxOUT15 RxOUT20 RxOUT21 RxOUT22 RxOUT21 RxOUT22 RxOUT22 RxOUT24 RxOUT25 RxOUT25 RxOUT26 RxOUT27 RxOUT5 RxOUT10 RxOUT11 RxOUT11 RxOUT16 RxOUT17 RxOUT17 RxOUT23 RxCLK OUT	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) Not use DTMG R0 (LSB) R1 G0 (LSB) G1 B0 (LSB) B1 Not use DCLK
	=H (3.3V)	R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) RSVD 1) RSVD 1) RSVD 1) DTMG R0 (LSB) R1 G0 (LSB) G1 B0 (LSB) B1 RSVD 1) DCLK	Pin 51 52 54 55 56 3 4 6 7 11 12 14 15 19 20 23 24 27 28 30 50 2 8 10 18 25 31	Input TxIN0 TxIN1 TxIN2 TxIN3 TxIN4 TxIN6 TxIN7 TxIN8 TxIN9 TxIN12 TxIN12 TxIN13 TxIN14 TxIN15 TxIN14 TxIN15 TxIN18 TxIN19 TxIN20 TxIN10 TxIN21 TxIN22 TxIN24 TxIN25 TxIN26 TxIN25 TxIN26 TxIN27 TxIN5 TxIN10 TxIN11 TxIN10 TxIN11 TxIN16 TxIN17 TxIN23 TxCLK IN	System Device Tx OUT0+ Tx OUT0- Tx OUT1+ Tx OUT1- Tx OUT1- Tx OUT2+ Tx OUT2+ Tx OUT2- Tx OUT3+ Tx OUT3- TxCLK OUT+ TxCLK OUT-	TFT Module Rx IN0+ Rx IN0- Rx IN1+ Rx IN1+ Rx IN1- Rx IN2+ Rx IN2+ Rx IN2- Rx IN3+ Rx IN3- Rx CLK IN+ Rx CLK IN+	Pin 27 29 30 32 33 35 37 38 39 43 45 46 47 51 53 54 55 1 3 5 6 7 34 41 42 49 50 2 26 	Output RxOUT0 RxOUT1 RxOUT2 RxOUT3 RxOUT4 RxOUT4 RxOUT6 RxOUT7 RxOUT8 RxOUT9 RxOUT9 RxOUT9 RxOUT12 RxOUT12 RxOUT12 RxOUT14 RxOUT15 RxOUT14 RxOUT15 RxOUT15 RxOUT16 RxOUT27 RxOUT5 RxOUT26 RxOUT27 RxOUT27 RxOUT5 RxOUT27 RxOUT5 RxOUT10 RxOUT11 RxOUT17 RxOUT17 RxOUT17 RxOUT17 RxOUT23 RxCLK OUT	Imput R2 R3 R4 R5 R6 R7 (MSB) G2 G3 G4 G5 G6 G7 (MSB) B2 B3 B4 B5 B6 B7 (MSB) Not use DTMG R0 (LSB) R1 G0 (LSB) G1 B0 (LSB) B1 Not use DCLK

Note 1) RSVD (reserved) pins on the transmitter shall be "H" or "L".

KAOHSIUNG OPTO-ELECTRONICS INC. SHEET NO.

8.5 CORRESPONDENCE BETWEEN INPUT DATA AND DISPLAY IMAGE



R0~R7 : R data G0~G7 : G data B0~B7 : B data

1				
	1,1	1,2	1,3	 1,1280
	2,1	2,2	2,3	 2,1280
	3,1	3,2	3,3	 3,1280
	768,1	768,2	768,3	 768,1280



KAOHSIUNG OPTO-ELECTRONICS INC.SHEET NO.7B64PS 2708-TX43	(43D50VM0BAA-1 PAGE
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	Item		Min.	Тур.	Max.	Unit	Note
DCLK	Frequency	1/t _{CLK}	65	66	73	MHz	
	0 data position	t _{RP0}	1/7t _{CLK} -0.44	1/7t _{CLK}	1/7t _{CLK} +0.44		
	1st data position	t _{RP1}	-0.44	0	+0.44		
DiaV	2nd data position	t _{RP2}	6/7t _{CLK} -0.44	6/7t _{CLK}	6/7t _{CLK} +0.44		
RINX	3rd data position	t _{RP3}	5/7t _{CLK} -0.44	5/7t _{CLK}	5/7t _{CLK} +0.44	ns	
(\(\Lambda = 0, 1, 2)	4th data position	t _{RP4}	$4/7t_{CLK} - 0.44$	4/7t _{CLK}	$4/7t_{CLK} + 0.44$		
	5th data position	t _{RP5}	3/7t _{CLK} -0.44	3/7t _{CLK}	3/7t _{CLK} +0.44		
	6th data position	t _{RP6}	2/7t _{CLK} -0.44	2/7t _{CLK}	2/7t _{CLK} +0.44	1	



Item		Symbol	Min.	Тур.	Max.	Unit	Note
DOLK	Cycle time	t _{CLK}	13.7	15.1	15.4	ns	
DOLK	Duty	D	0.35	0.5	0.65	-	
	Horizontal period	Т _н	1396	1406	1450	t _{CLK}	
	Horizontal width-Active	T _{HD}	1280	1280	1280	t _{CLK}	
DTMG	Vertical period	Τv	773	783	825	Т _Н	
	Vertical width-Active	T _{VD}	768	768	768	Т _Н	
	Frame frequency	f _V	55	60	65	Hz	

9.3 TIMING BETWEEN INTERFACE SIGNALS AND POWER SUPPLY



NO.

9.4 DATA INPUT for DISPLAY COLOR

\sim	Input data		R data										Gd	lata				B data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Color		MSB	•						LSB	MSE	3						LSB	MSE	;						LSB
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Basic	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Color	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Red	:	÷	÷	:	÷	:	÷	:	:	:	:	÷	÷	÷	:	:	÷	1	:	÷	:	:	:	:	:
	÷	÷	÷	:	÷	÷	÷	:	÷	:	÷	÷	÷	÷	÷	÷	÷	÷	:	÷	:	÷	:	:	÷
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Green	:	:	:	:	:	:	:	:	÷	:	:	:	÷	:	:	:	÷	:	÷	÷	:	:	:	:	÷
		:	÷	:	:	:	:	:	÷	:	:	:	÷	:	:	:	÷	:	÷	÷	:	÷	:	:	÷
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Blue	÷	:	:	1	÷	:	:	:	:	:	:	÷	÷	:	:	:	÷	1	÷	÷	:	:	÷	:	:
	:	:	:	:	÷	:	:	:	:	:	:	÷	÷	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Notes 1) Definition of gray scale: Color (n) n indicates gray scale level. Higher n means brighter level.

2) Data signals: 1: High, 0: Low





11. APPEARANCE STANDARD

11.1 CONDITIONS FOR COSMETIC INSPECTION

(1) Viewing zone

a) The figure shows the correspondence between eyes (of inspector) and TFT-LCD module. $\theta < 45^{\circ}$: when non-operating inspection $\theta < 5^{\circ}$: when operating inspection b) Inspection should be executed only from front side and only A-zone. Cosmetic of B-zone and C-zone are ignore. (refer to 9.2 DEFINITION OF ZONE)



(2) Environmental

- a) Temperature : 25°C
- b) Ambient light : about 700 lx and non-directive when operating inspection.
 - : about 1000 lx and non-directive when non-operating inspection.
- c) Back-light : when non-operating inspection, back-light should be off.

11.2 DEFINITION OF ZONE



11.3 LCD APPEARANCE SPECIFICATION

The specification as below is defined as the amount of unexpected phenomenon or material in different zones of LCD panel. The definitions of length, width and average diameter using in the table are shown in Fig. 11.3 and Fig. 11.4.

Item	Criteria				Applied zone			
	Length (mm)	Widt	h (mm)	Maximum ni	umber	Minimum space		
	Ignored	W≦	≦0.02	Ignored		-		
	L≦40	W≦	≦0.04	10		-		
	L≦20	W≦	≦0.08	10 -				
Scratches	Round (Dot Shape)						A,B	
	Average diameter (mm) Ma		Maxim	num number Mi		nimum space		
	D≦0.2			Ignore		-		
	D≦0.6	D≦0.6		10		-		
Dent		Se	erious one	is not allowed			А	
Wrinkles in polarizer		Se	erious one	is not allowed			A	
	Average diar	neter (n	חm)	Max	kimum number			
	D	0≦0.3		Ignored				
Bubbles on polarizer	0.3 <d< td=""><td>≦0.5</td><td></td><td colspan="3">10</td><td>А</td></d<>	≦0.5		10			А	
	0.5 <d< td=""><td>≦1.0</td><td></td><td></td><td>5</td><td></td><td></td></d<>	≦1.0			5			
	1.0 <d< td=""><td></td><td></td><td></td><td>none</td><td></td><td></td></d<>				none			
	Filamentou			(Line shape)				
	Length (mm)		Width (mm)		Maximum number		A,B	
	-		W≦0.02		Ignored			
	L≦4.0		W≦0.04		8			
1) Stains	L≦2.0		W≦0.08		8			
2) Foreign Materials	-		W>0.08		Dot Shape			
3) Dark Spot	Round (Dot shape)							
	Average diameter (mm)		Maximum number		-			
	D≦0.22		Ignored		-		A,B	
	D≦0.5		8		-			
	D>0.5	;		None		-		
	Those wiped out easily are acceptable							
				Type Maximum number				
Dot-Defect (Note 1)			1 dot		lot 6			
	Bright dot-defect	et –	2 adjacent dot		ent dot 3			
	Bright dot-delete		3 adjacent dot or above		ot or above Not allowed			
			In total		otal 8		А	
	Dark dot-defect		1 dot		8 4 Not allowed			
			2 adjacent dot					
			3 adjacent dot or above					
			In	total	10		4	
	In total				14			

SHEET

NO.



Fig 11.3

Fig 11.4

Note 1: The definitions of dot defect are as below:

- The defect area of the dot must be bigger than half of a dot.
- For bright dot-defect, showing black pattern, the dot's brightness must be over 30% brighter than others.
- For dark dot-defect, showing white pattern, the dot's brightness must be under 70% darker than others.
- The definition of 1-dot-defect is the defect-dot, which is isolated and no adjacent defect-dot.
- The definition of adjacent dot is shown as Fig. 11.5.
- The Density of dot defect is defined in the area within diameter $_{\varphi}$ =20mm.

		1	
	A		

The dots colored gray are adjacent to defect-dot A.

Fig 11.5

Note 2: Polarizer area inside of B-Zone is not applied.

12. PRECAUTIONS

12.1 PRECAUTIONS of ESD

- 1) Before handling the display, please ensure your body has been connected to ground to avoid any damages by ESD. Also, do not touch display's interface directly when assembling.
- 2) Please remove the protection film very slowly before turning on the display to avoid generating ESD.

12.2 PRECAUTIONS of HANDLING

- 1) In order to keep the appearance of display in good condition, please do not rub any surfaces of the displays by sharp tools harder than 3H, especially touch panel, metal frame and polarizer.
- 2) Please do not pile the displays in order to avoid any scars leaving on the display. In order to avoid any injuries, please pay more attention for the edges of glasses and metal frame, and wear finger cots to protect yourself and the display before working on it.
- 3) Touching the display area or the terminal pins with bare hand is prohibited. This is because it will stain the display area and cause poor insulation between terminal pins, and might affect display's electrical characteristics furthermore.
- 4) Do not use any harmful chemicals such as acetone, toluene, and isopropyl alcohol to clean display's surfaces.
- 5) Please use soft cloth or absorbent cotton with ethanol to clean the display by gently wiping. Moreover, when wiping the display, please wipe it by horizontal or vertical direction instead of circling to prevent leaving scars on the display's surface, especially polarizer.
- 6) Please wipe any unknown liquids immediately such as saliva, water or dew on the display to avoid color fading or any permanently damages.
- 7) Maximum pressure to the surface of the display must be less than 1.96×10^4 Pa. If the area of adding pressure is less than 1 cm^2 , the maximum pressure must be less than 1.96N.

12.3 PRECAUTIONS OF OPERATING

- 1) Please input signals and voltages to the displays according to the values defined in the section of electrical characteristics to obtain the best performance. Any voltages over than absolute maximum rating will cause permanent damages to this display. Also, any timing of the signals out of this specification would cause unexpected performance.
- 2) When the display is operating at significant low temperature, the response time will be slower than it at 25 C°. In high temperature, the color will be slightly dark and blue compared to original pattern. However, these are temperature-related phenomenon of LCD and it will not cause permanent damages to the display when used within the operating temperature.
- 3) The use of screen saver or sleep mode is recommended when static images are likely for long periods of time. This is to avoid the possibility of image sticking.
- 4) Spike noise can cause malfunction of the circuit. The recommended limitation of spike noise is no bigger than ± 100 mV.

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12.4 PRECAUTIONS of STORAGE

If the displays are going to be stored for years, please be aware the following notices.

- 1) Please store the displays in a dark room to avoid any damages from sunlight and other sources of UV light.
- 2) The recommended long term storage temperature is between 10 C° ~35 C° and 55% ~75% humidity to avoid causing bubbles between polarizer and LCD glasses, and polarizer peeling from LCD glasses.
- 3) It would be better to keep the displays in the container, which is shipped from KOE, and do not unpack it.
- 4) Please do not stick any labels on the display surface for a long time, especially on the polarizer.

KAOHSIUNG OPTO-ELECTRONICS INC.	SHEET NO.	7B64PS 2712-TX43D50VM0BAA-1	PAGE	12-2/2

13. DESIGN ATION OF LOT MARK

1) The lot mark is showing in Fig.13.3. First 4 digits are used to represent production lot, T represented made in Taiwan, and the last 5 digits are the serial number.



2) The tables as below are showing what the first 4 digits of lot mark are shorted for.

Year	Mark
2012	2
2013	3
2014	4
2015	5
2016	6

Month	Mark	Month	Mark
1	01	7	07
2	02	8	08
3	03	9	09
4	04	10	10
5	05	11	11
6	06	12	12

Week (Days)	Mark
1~7	1
8~14	2
15~21	3
22~28	4
29~31	5

3) Except letters I and O, revision number will be shown on lot mark and following letters A to Z.

4) The location of the lot mark is on the back of the display shown in Fig. 13.3.



Fig 13.3

KAOHSIUNG OPTO-ELECTRONICS INC.	SHEET NO.	7B64PS 2713-TX43D50VM0BAA-1	PAGE	13-1/1
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