Principal Strategic Partner

In Plane Switching

19” IPS

Development Plan

Feb., 15th, 2013.

LG Display

Contents

LG Display

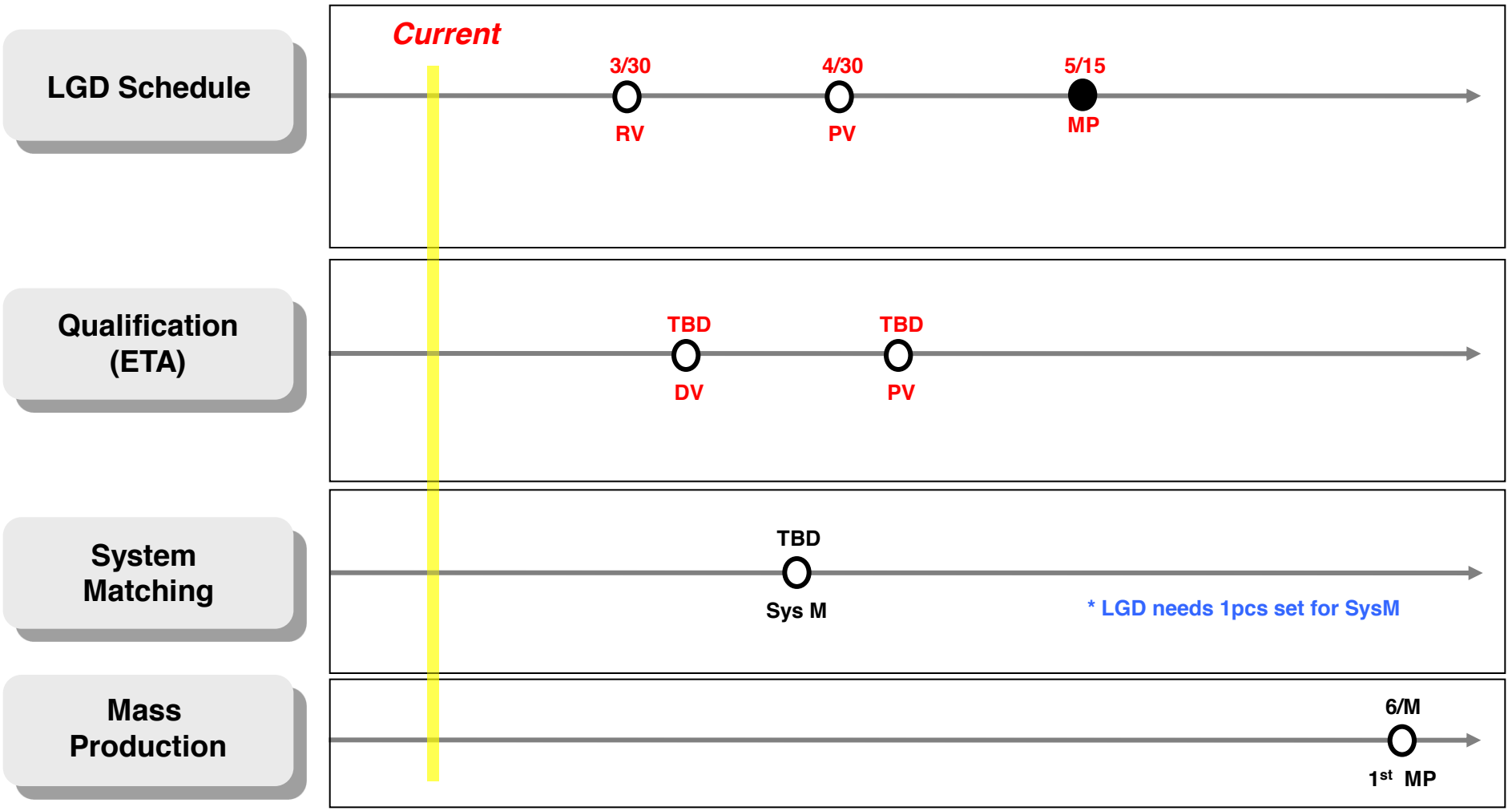
In Plane Switching

LGD will support LGE's Project as below spec.

Item		LM190E09-TLD1	LM190E0A-SLA1
General	Resolution	1280 x 1024	←
	LC Mode	TN	AH-IPS
	Panel Type	Forward	←
Optical	Brightness	250nit	←
	Contrast Ratio	1000:1	←
	Response time	Typ 5ms (B/W)	Typ 14ms (GTG)
	Color Gamut	72%	←
	Viewing Angle (V/H)	170 / 160	178/178
	Color Depth	16.7M (6-bit+A-FRC)	←
Electrical	Input voltage	5V	←
	Interface	LVDS 2port	←
	V freq.	60Hz (typ.)	←
Mech.	Outline Dimension	396(H) x 324(V) (typ)	←
	Thickness	9.9T	←
	Weight	1620g (Typ)	1705g
	No. of Lamp/LED or PKG	30ea	←
	Lamp/LED Current	60mA	100mA
ETC	Fab	P7	P8
	M-Site	GZ,China	←

Schedule

System Matching Test and real time event test result on each site are strongly necessary for safe project launching.



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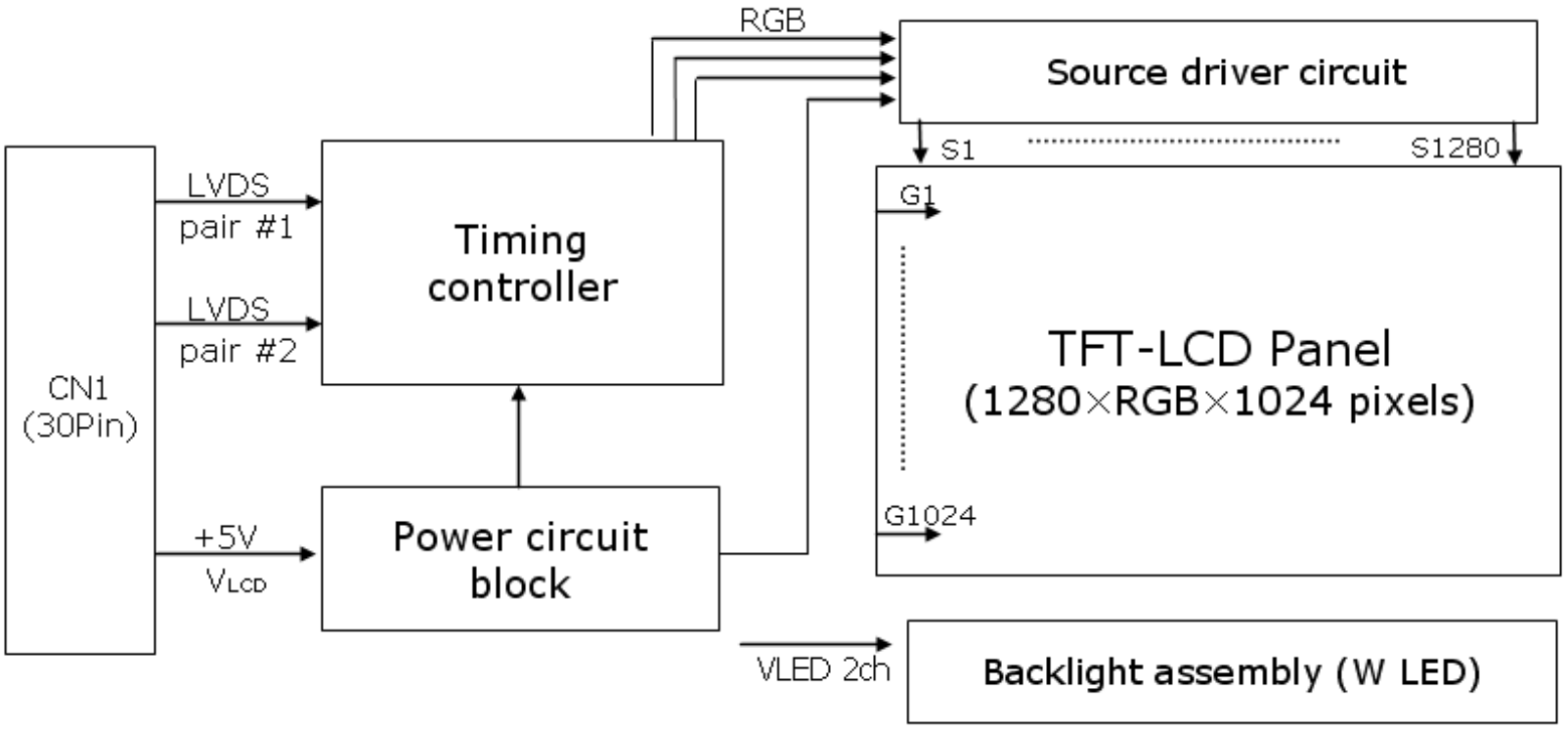
Circuit Block diagram

▣ Block Diagram



▣ LCD Connector(CN1) : IS100-L30O-C23(UJU),GT103-30S-H15(LSM)

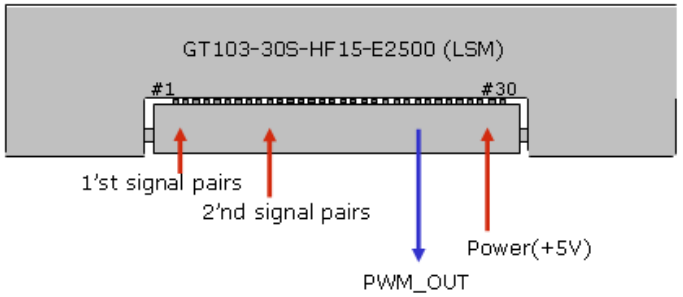
Mating connector : FI-X30H and FI-X30HL (JAE) or Equivalent

▣ Pin Description

Pin No	Symbol	Description	
1	RXO0-	Minus signal of 1st channel 0 (LVDS)	First Pixel data
2	RXO0+	Plus signal of 1st channel 0 (LVDS)	
3	RXO1-	Minus signal of 1st channel 1 (LVDS)	
4	RXO1+	Plus signal of 1st channel 1 (LVDS)	
5	RXO2-	Minus signal of 1st channel 2 (LVDS)	
6	RXO2+	Plus signal of 1st channel 2 (LVDS)	
7	GND	Ground	
8	RXOC-	Minus signal of 1st clock channel (LVDS)	
9	RXOC+	Plus signal of 1st clock channel (LVDS)	
10	RXO3-	Minus signal of 1st channel 3 (LVDS)	
11	RXO3+	Plus signal of 1st channel 3 (LVDS)	
12	RXE0-	Minus signal of 2nd channel 0 (LVDS)	Second Pixel data
13	RXE0+	Plus signal of 2nd channel 0 (LVDS)	
14	GND	Ground	
15	RXE1-	Minus signal of 2nd channel 1 (LVDS)	
16	RXE1+	Plus signal of 2nd channel 1 (LVDS)	
17	GND	Ground	
18	RXE2-	Minus signal of 2nd channel 2 (LVDS)	
19	RXE2+	Plus signal of 2nd channel 2 (LVDS)	
20	RXEC-	Minus signal of 2nd clock channel (LVDS)	
21	RXEC+	Plus signal of 2nd clock channel (LVDS)	
22	RXE3-	Minus signal of 2nd channel 3 (LVDS)	
23	RXE3+	Plus signal of 2nd channel 3 (LVDS)	
24	GND	Ground	
25	NC	No Connection (I2C Serial interface for LCM)	
26	NC	No Connection (I2C Serial interface for LCM)	
27	PWM_OUT	For Control Burst frequency of Inverter	
28	V_{LCD}	Power Supply (5.0V)	
29	V_{LCD}	Power Supply (5.0V)	
30	V_{LCD}	Power Supply (5.0V)	

Note:

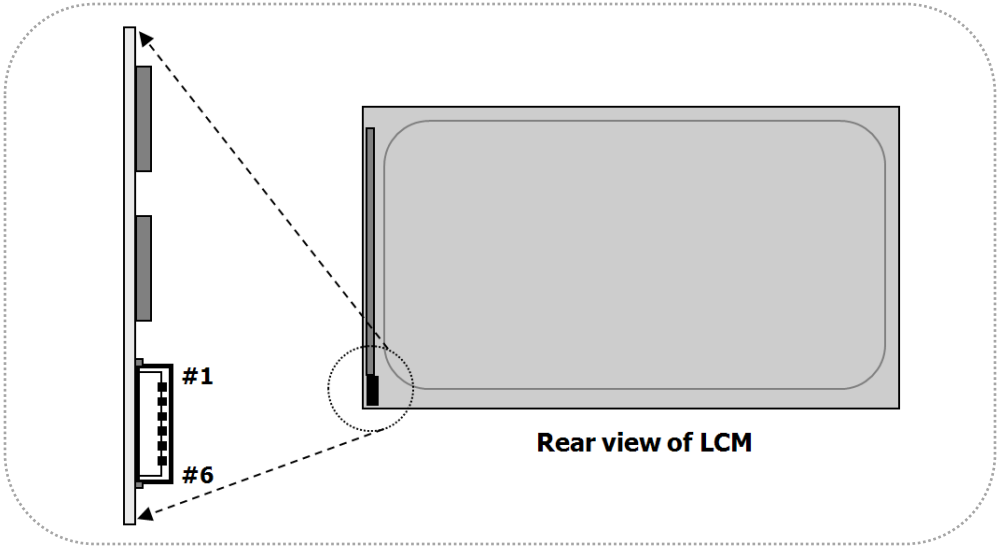
1. NC: No Connection.
2. All GND(ground) pins should be connected together and to Vss which should also be connected to the LCD's metal frame.
3. 3. All V_{LCD} (power input) pins should be connected together.
4. Input Level of LVDS signal is based on the IEA 664 Standard.
5. PWM_OUT is a reference signal for LED Driver control.
   This PWM signal is synchronized with vertical frequency.
   Its frequency is 6 times of vertical frequency, and its duty ratio is 50%.
   If the system don't use this pin, do not connect.



Connector Configuration – LED Connector

■ **LED connector pin configuration**

Pin	Symbol	Description	Notes
1	FB1	Channel1 Current Feedback	
2	NC	No Connection	
3	VLED	LED Power Supply	
4	VLED	LED Power Supply	
5	NC	No Connection	
6	FB2	Channel2 Current Feedback	



[Backlight connector view]

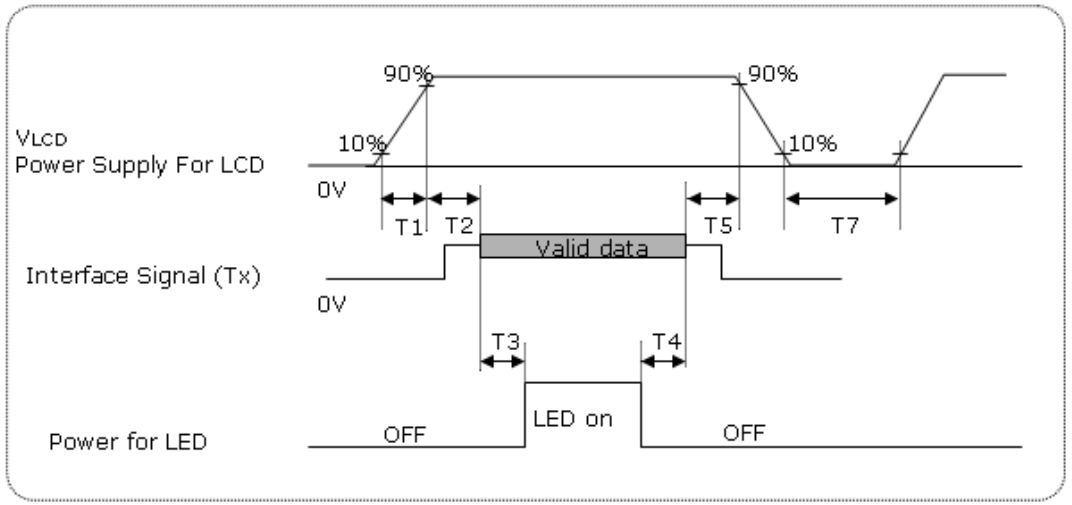
▣ Signal Timing

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
D_{CLK}	Period	t_{CLK}	14.8	18.5	22.2	ns	Pixel frequency : Typ.108MHz
	Frequency	f_{CLK}	45.0	54.0	67.5	MHz	
Horizontal	Horizontal Valid	t_{HV}	640	640	640	t_{CLK}	
	H Period Total	t_{HP}	704	844	960		
	Horizontal Blank	t_{HB}	64	204	320		
	Hsync Frequency	f_H	53.3	64.0	80.0	kHz	
	Width	t_{WH}	16	56	80	t_{CLK}	
	Horizontal Back Porch	t_{HBP}	32	124	200		
	Horizontal Front Porch	t_{HFP}	16	24	40		
Vertical	Vertical Valid	t_{VV}	1024	1024	1024	t_{HP}	
	V Period Total	t_{VP}	1032	1066	1536		
	Vertical Blank	t_{VB}	8	42	512		
	Vsync Frequency	f_V	50	60	75	Hz	
	Width	t_{VVV}	2	3	250	t_{HP}	
	Vertical Back Porch	t_{VBP}	5	38	250		
	Vertical Front Porch	t_{VFP}	1	1	12		

Note: Hsync period and Hsync width-active should be even number times of tCLK. If the value is odd number times of tCLK, display control signal can be asynchronous. In order to operate this LCM a Hsync, Vsyn, and DE(data enable) signals should be used.

1. The performance of the electro-optical characteristics may be influenced by variance of the vertical refresh rates.
2. Vsync and Hsync should be keep the above specification.
3. Hsync Period, Hsync Width, and Horizontal Back Porch should be any times of of character number(4).
4. The polarity of Hsync, Vsync is not restricted.
5. The Max frequency of 1280X1024 resolution is 67.5Mhz

▣ Input Signal/Power Sequence

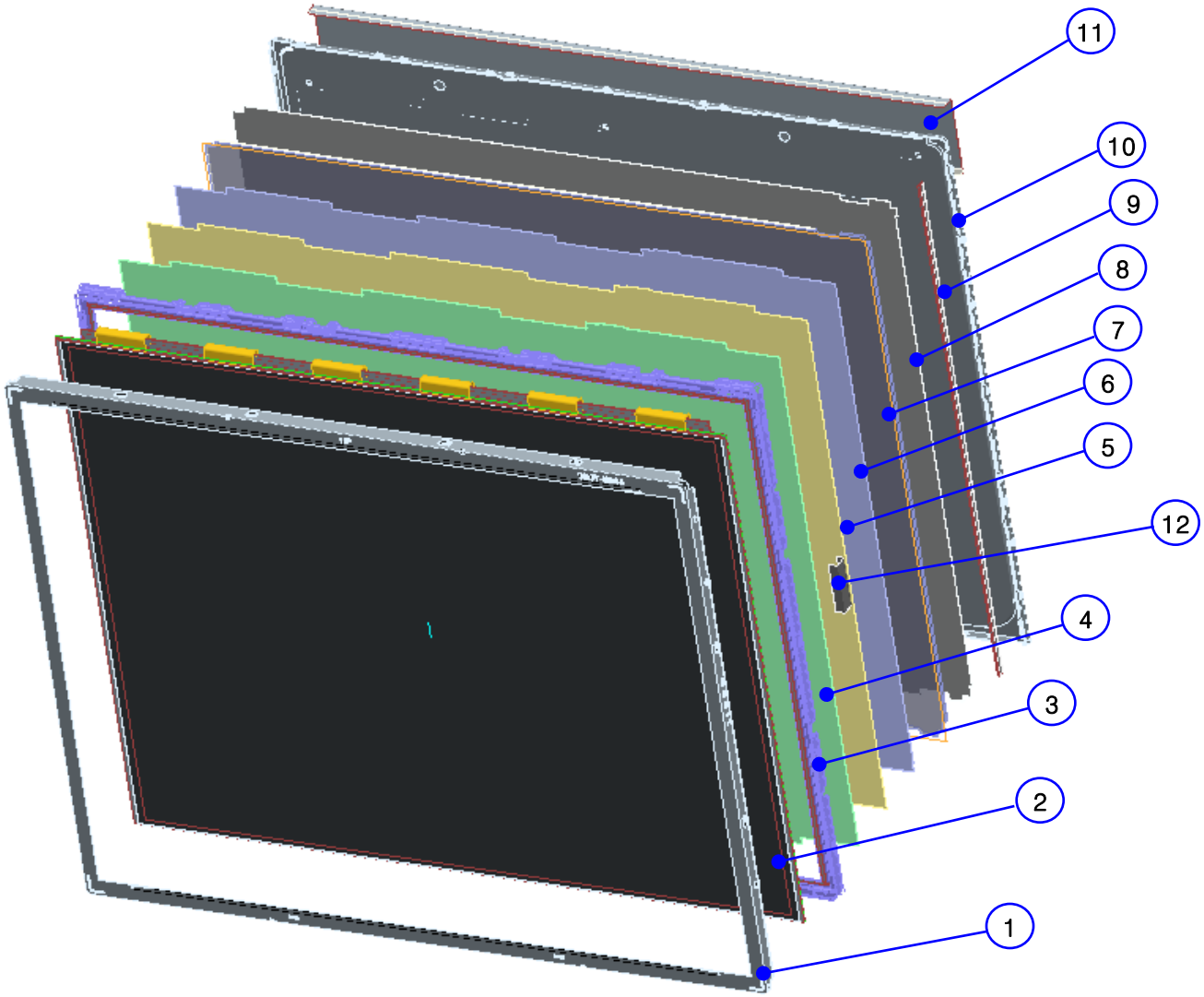


Parameter	Values			Units
	Min	Typ	Max	
T1	0.5	-	10	ms
T2	0.01	-	50	ms
T3	500	-	-	ms
T4	200	-	-	ms
T5	0.01	-	50	ms
T7	1	-	-	s

Notes :

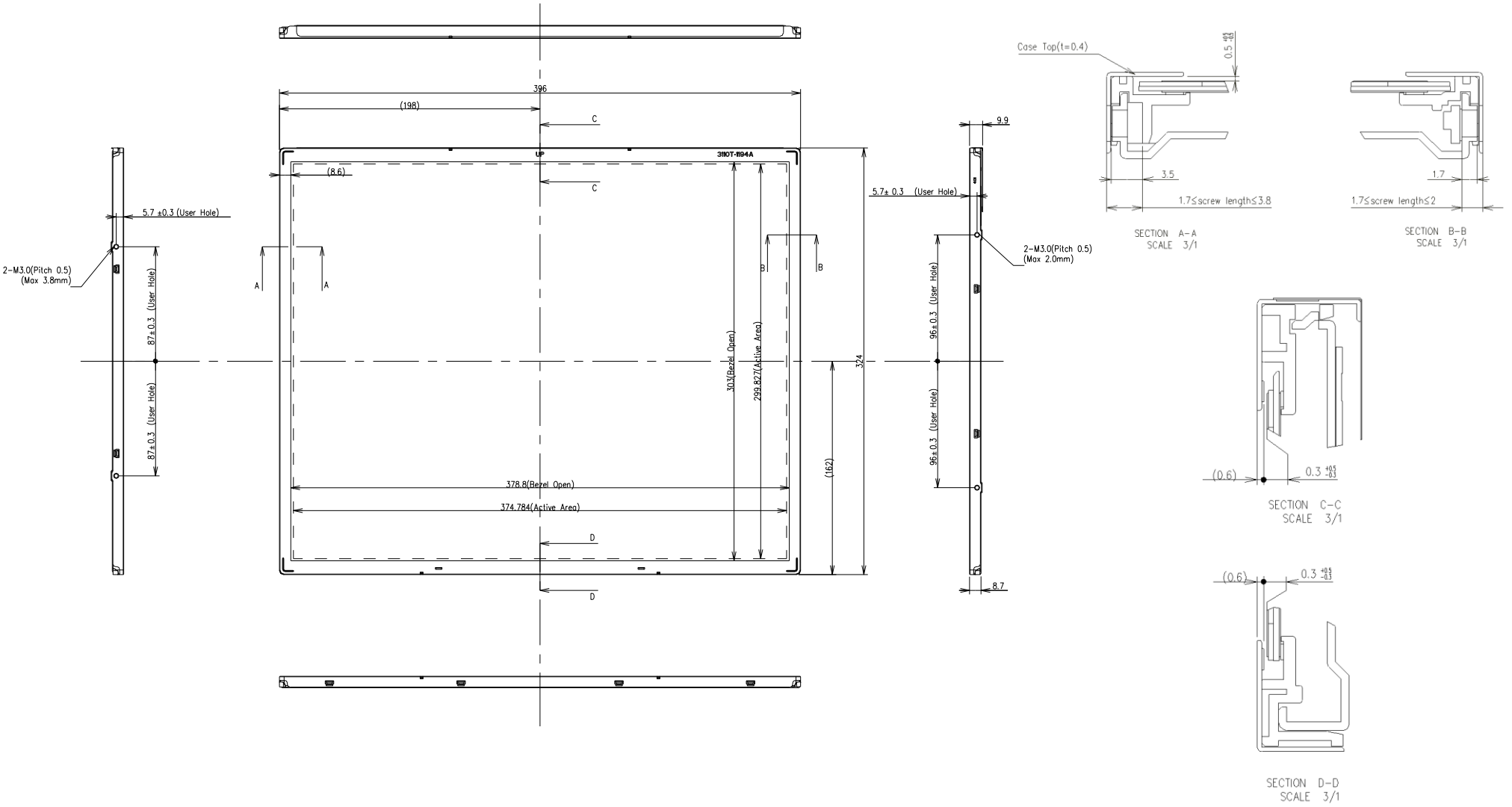
1. Please VLCD power on only after connecting interface cable to LCD.
2. Please avoid floating state of interface signal at invalid period.
3. When the interface signal is invalid, be sure to pull down the power supply for LCD VLCD to 0V.
4. LED power must be turn on after power supply for LCD an interface signal are valid.

Over view Mechanical structure

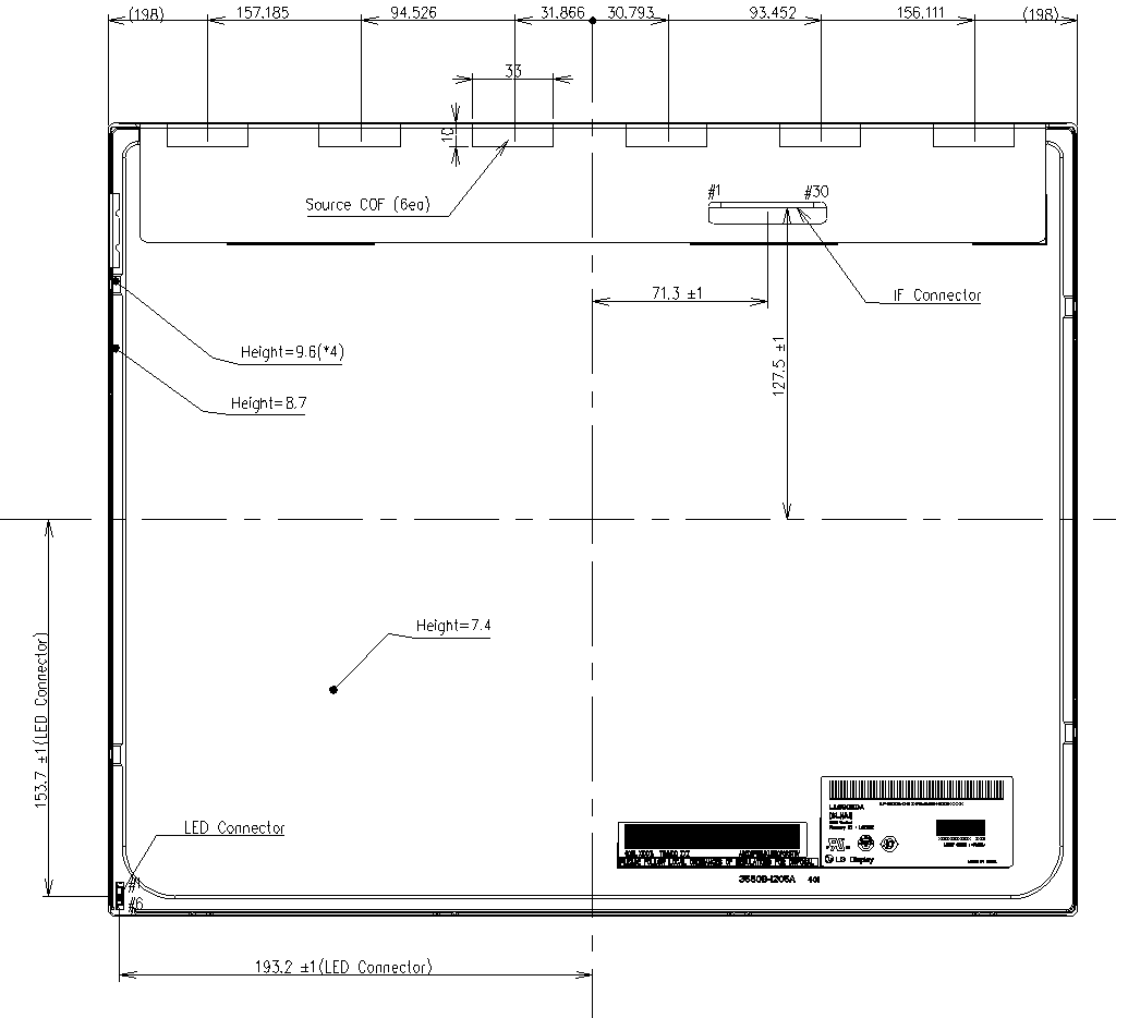


1) Case Top Assembly (EGI 0.4t)
2) Board Assembly
3) Guide Panel Assembly
4) Prism Sheet
5) Diffuser Sheet
6) Diffuser Sheet
7) LGP Assembly (PMMA 2.0t)
8) Reflector
9) LED PKG Assembly
10) Cover Bottom (EGI 0.8t)
11) Cover Shield (PET 0.1t)
12) Electronic Conductive Tape

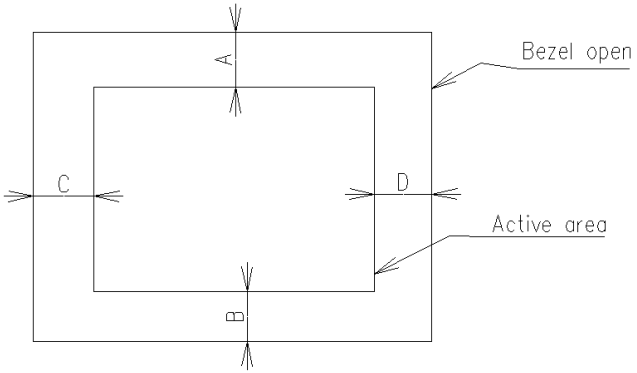
Front view



Rear view



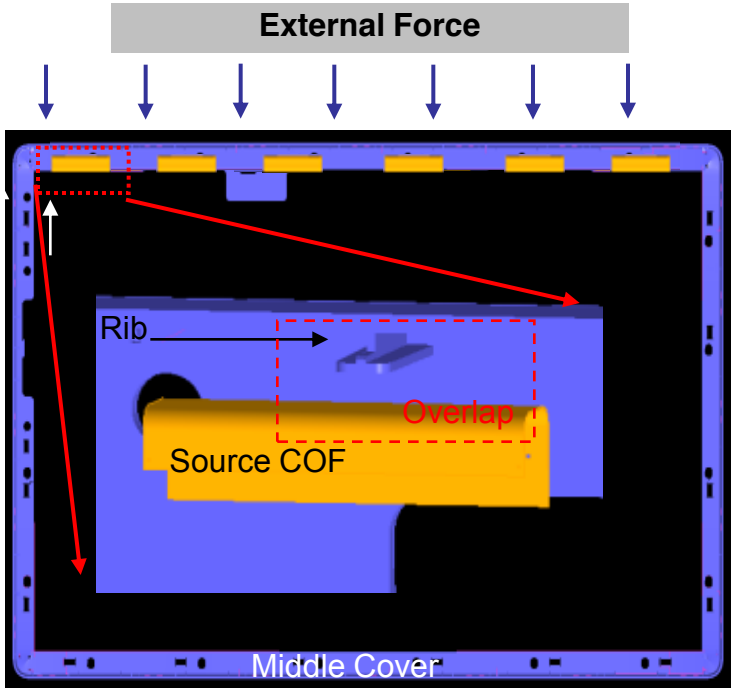
Notes
1. Backlight has 1 LED Array Ass'y
2. I/F Connector Specification : GT103-30S-HF15-E2500 (LGM).
3. LED Connector Specification : JST, SM06B-SHJH(HF).
4. Torque of user hole : 3.0~4.0kgf-cm
5. Tilt and partial disposition tolerance of display area as following
   (1) Y-Direction : IA-BI ? 1.0
   (2) X-Direction : IC-DI ? 1.0



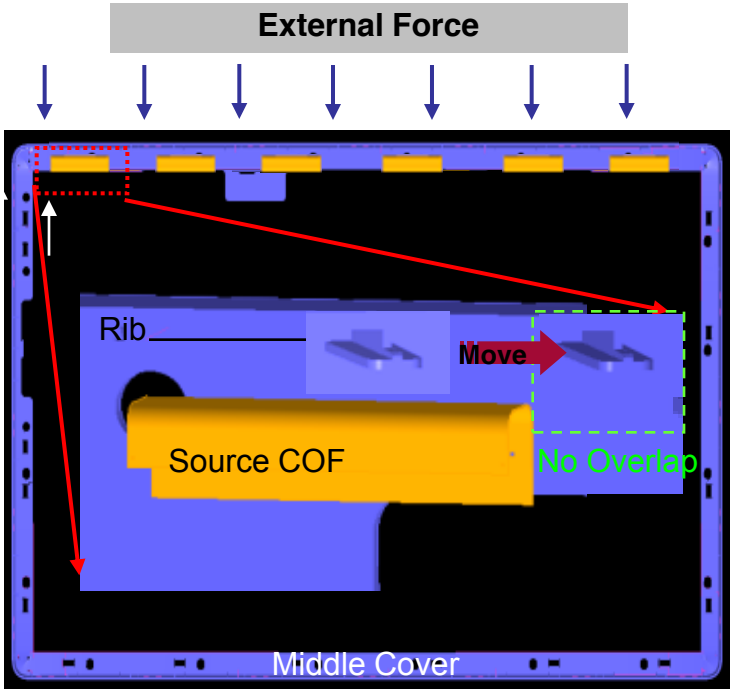
6. Unspecified tolerances to be ±0.5mm
7. The COF area is weak & sensitive, So, please don't press the COF area.

LGD would like you to design Position of rib which is not much projected on the Middle cover not to push Source COF Area

Disadvantageous condition for LCM

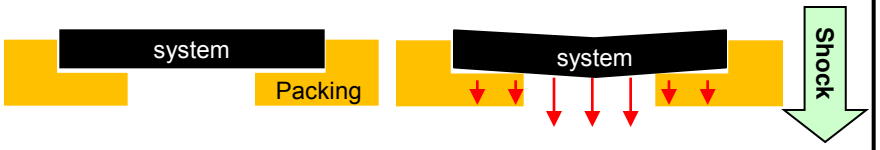


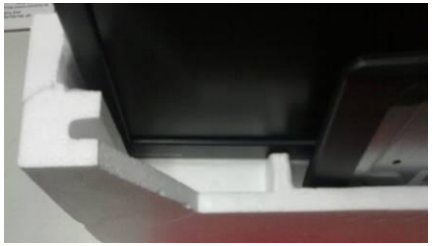
Advantageous condition for LCM

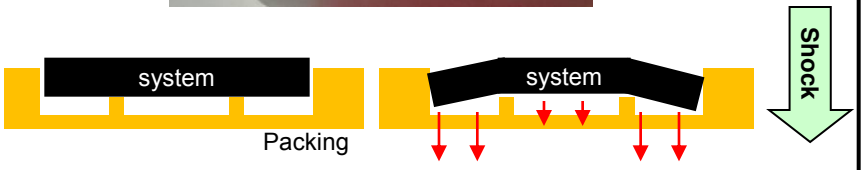


LGD would like you to design packing to support LCM sufficiently.

Disadvantageous condition for LCM

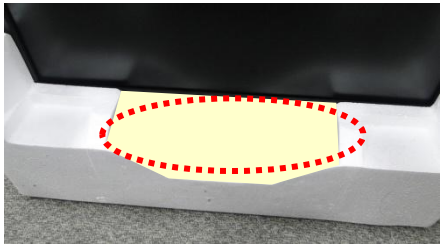


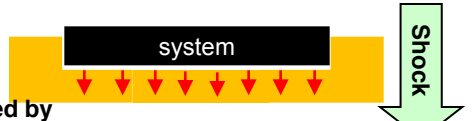


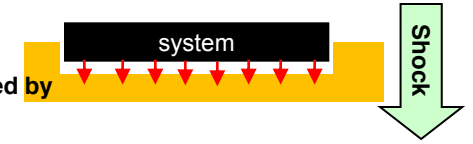


System center or bottom area is not supported by packing

Advantageous condition for LCM



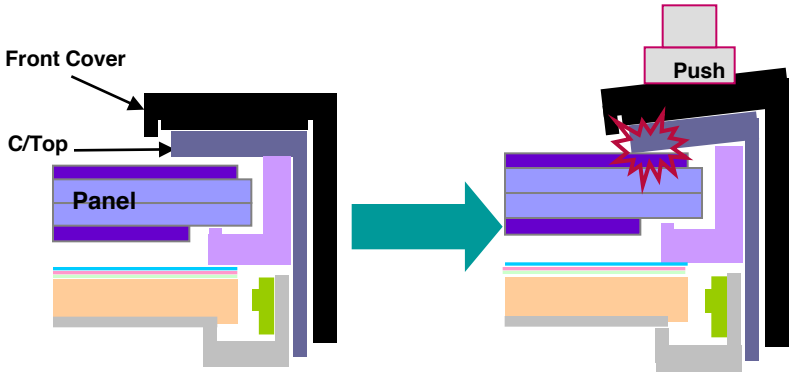




System center & bottom area is supported by packing

LGD would like you to design add the front cover rib to improve ripple.

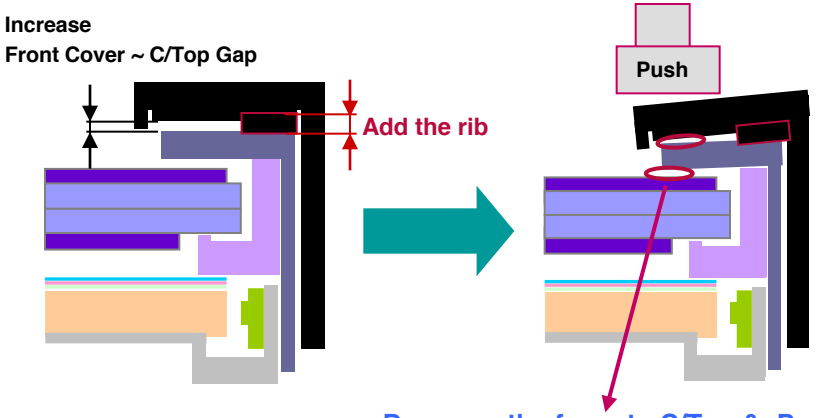
Disadvantageous condition for LCM



Push System Front Cover Rib → C/Top → Panel

Occur Ripple

Advantageous condition for LCM



Decrease the force to C/Top & Panel → Improve ripple

LG Display Measured data

	ES 6.0 Draft 3.0 UPDATE				Remark
	Logic	BLU	Total	LCM Portion (70%)	
19(SXGA, IPS)	2.4W	8.63W	11.03	69.0%	

LED information

	Type	Inch	LCM Model name	LED vendor	Luminous Flux (lm)	Package size	Total no. of LEDs	LED String	No. of chip/pakage	LED string (Voltage/Current)	LED bar structure
IPS	Plus13	19SX	LM190E0A-SLA1	WEL	42	8520	30	2	2	45.8V/100mA	Vertical 1bar